CRYSTAL
Semiconductor Corporation

CS6158

PCM Line Interface

T-75-11-29

Features

- Provides Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Internal generation of transmitted T1 pulse width and pulse shape. Pulses meet template requirements over full power supply and temperature range.
- Fully Monolithic Clock Recovery
- Minimum External Components (no external crystal required)

General Description

The CS6158 combines the analog transmit and receive line interface functions for a T1 or PCM-30 interface in a 28 pin device. The line interface operates from a single 5 volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse* ™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for line lengths ranging from 0 to 655 feet from a DSX-1 cross connect. This device offers pin compatibility with the higher functionality CS61534 and CS61574.

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Applications

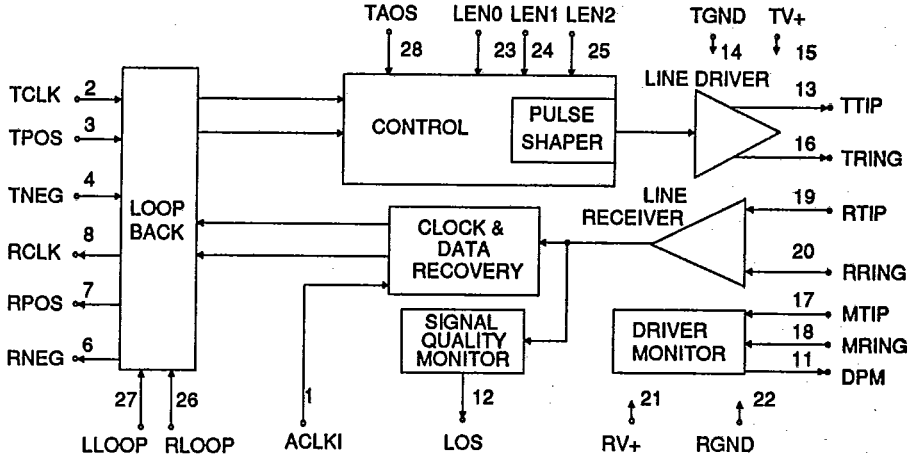
Synchronous communication systems which employ frame buffers, including:

- Central Office Exchanges
- Digital Access and Cross Connect Systems
- Large PABX's

ORDERING INFORMATION

CS6158-IP	-	28 Pin Plastic DIPT1 only
CS6158-IP1	-	28 Pin Plastic DIPT1 & PCM-30
CS6158-IL	-	28 Pin PLCCT1 only
CS6158-IL1	-	28 Pin PLCCT1 & PCM-30

Block Diagram



Preliminary Product Information | This document contains information on a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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JAN '89
DS34PP3
2-91

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+, TV+	-	6.0	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	RV+ + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, which must stay within -6V to RV + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total Power Dissipation (Note 4) 100% ones density & max. line length @ 5.25V	P_D	-	620	-	mW
Normal Power Dissipation (Note 4) 50% ones density & 300 ft. line length @ 5.0V	P_D	-	400	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 25 Ω load over operating temperature range. Includes CS6158 and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 5) PINS 1-4, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 5) PINS 1-4, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 5) I_{OUT}=-40 uA PINS 6-8, 11, 12	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 5) I_{OUT}= 1.6 mA PINS 6-8, 11, 12	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA

Notes: 5. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V)

Parameter		Min	Typ	Max	Units
TRANSMITTER					
AMI Output Pulse Amplitudes **Line Length Selections LEN2/1/0 = 0/0/0 & 0/1/0** (Measured at xfmr output; for 0/0/0 see Figure 5) **All line length settings except, LEN2/1/0 = 0/0/0, 0/1/0 & 0/0/1** (Measured at the DSX; Normalization factor for Figure 4)		2.7 2.4	3.0 3.0	3.3 3.6	V V
Load Presented To Transmitter Output		-	25	-	Ohms
Jitter Added by the Transmitter (Note 6)	10Hz - 8kHz 8kHz - 40kHz 10Hz - 40kHz Broad Band	- - - -	0.005 0.008 0.010 0.015	- - - -	UI UI UI UI
Power in 2kHz band about 772kHz (note 7)		12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (note 7) (referenced to power at 772kHz)		-29	-38	-	dB
Positive to Negative Pulse Imbalance (note 7)		-	0.2	0.5	dB
RECEIVER					
Sensitivity Below DSX (0dB = 2.4V)		-10	-	-	dB
Loss of Signal Threshold		-	0.3	-	V
Data Decision Threshold	T1 pulse settings CCITT LEN2/1/0 = 000	- -	65 50	- -	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance (Note 8)	10kHz - 100kHz 10Hz and below	0.4 300	- -	- -	UI

Notes: 6. Input signal to TCLK is jitter free.
7. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.
8. See Figure 7.

T1 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
TCLK Frequency	f_{in}	-	1.544	-	MHz
ACLKI Frequency (Note 9)	f_{out}	-	1.544	-	MHz
RCLK Cycle Width	t_{pw1}	348	648	948	ns
	t_{pwh1}	-	508	-	ns
(Notes 11, 12, 14)	t_{pwl}	100	140	-	ns
RCLK Duty Cycle (Notes 11, 12, 14)	t_{pwh1}/t_{pw1}	48	78	89	%
Rise Time, All Digital Outputs (Note 13)	t_r	-	-	85	ns
Fall Time, All Digital Outputs (Note 13)	t_f	-	-	85	ns
RPOS/RNEG to RCLK Rising Setup Time (Note 14)	t_{su1}	50	140	-	ns
RCLK Rising to RPOS/RNEG Hold Time (Note 14)	t_{h1}	50	508	-	ns
TPOS/TNEG to TCLK Falling Setup Time	t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time	t_{h2}	25	-	-	ns

CCITT SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
TCLK Frequency	f_{in}	-	2.048	-	MHz
TCLK Duty Cycle for LEN2/1/0 = 0/0/0 (Note 10)	t_{pwh2}/t_{pw2}	44	50	53	%
ACLKI Frequency (Note 9)	f_{out}	-	2.048	-	MHz
RCLK Cycle Width	t_{pw1}	260	488	714	ns
	t_{pwh1}	-	348	-	ns
(Notes 11, 12, 14)	t_{pwl}	100	140	-	ns
RCLK Duty Cycle (Notes 11, 12, 14)	t_{pwh1}/t_{pw1}	49	71	82	%
Rise Time, All Digital Outputs (Note 13)	t_r	-	-	85	ns
Fall Time, All Digital Outputs (Note 13)	t_f	-	-	85	ns
RPOS/RNEG to RCLK Rising Setup Time (Note 14)	t_{su1}	50	140	-	ns
RCLK Rising to RPOS/RNEG Hold Time (Note 14)	t_{h1}	50	348	-	ns
TPOS/TNEG to TCLK Falling Setup Time	t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time	t_{h2}	25	-	-	ns

Notes:
9. ACLKI provided by an external source or TCLK.
10. The transmitted pulse width for LEN2/1/0 = 0/0/0 is tied to the high cycle of TCLK.
11. RCLK cycle width will vary with extent by which received pulses are displaced by jitter.
12. Max & Min RCLK duty cycles and pulse widths are for worst case jitter conditions: i.e. 0.4 UI AMI data displacement for T1 or 0.2 UI AMI data displacement for CCITT 2.048 MHz. See text section on *Jitter and Recovered Clock*.
13. At max load of 50 pF.
14. Not production tested. Guaranteed by design and/or characterization.

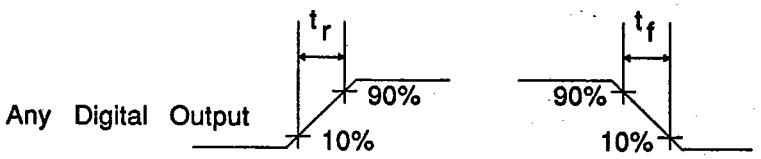

Figure 1. - Signal Rise and Fall Characteristics

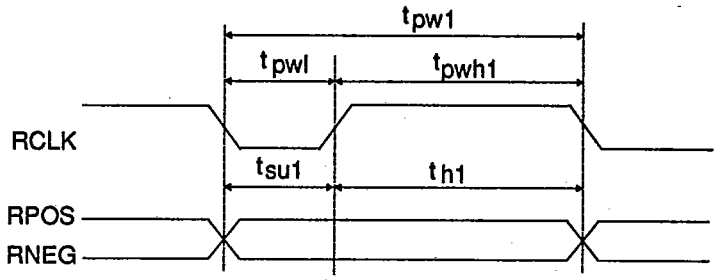

Figure 2. - Recovered Clock and Data Switching Characteristics

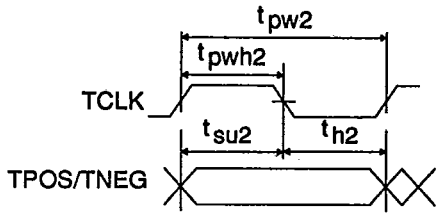

Figure 3. - Transmit Clock and Data Switching Characteristics

THEORY OF OPERATION

Transmitter

The transmitter takes binary (dual unipolar) data from a T1 terminal and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Either T1 or CCITT G.703 pulse shapes may be selected. For T1 application, line lengths from 0 to 655 feet (as measured from the CS6158 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a two-to-one, step-up transformer is required. The line driver is designed to drive a 25 Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), the TPOS and TNEG should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit Line Length Selection

The transmitter has a 13-phase delay line which divides each TCLK cycle into 13 phases. For T1 applications, these phases are then used to trigger different portions of the output wave form. The line length selection offers a five partition arrangement for ABAM and PIC cable as shown in Table 1. For each line length selected, the CS6158 modifies the output pulse to meet the requirements of Compatibility Bulletin 119. The exact pulse shape achieved at the DSX-1 can be effected by details of the board layout, transformer selection, and other factors. For cable types other than ABAM, it is recommended that the line length settings be evaluated. It is possible that an alternative interpretation of the LEN2/1/0 distance ranges is more appropriate. A typical output pulse is shown in Figure 4.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	APPLICATION
0	1	1	0-133	DSX-1 ABAM
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	
0	0	1		Reserved
0	0	0	G.703	2.048 MHz CCITT
0	1	0	Part 68, Option A	CSU
0	1	1	T1C1.2	

Table 1 - Line Length Selection

The T1 CSU pulse shapes meet FCC Part 68 for 0dB line build out and future ECSA T1C1.2 pulse shapes as shown in Table 1.

The CCITT G.703 pulse shape is also supported with line length selection LEN2/1/0 = 000. In this

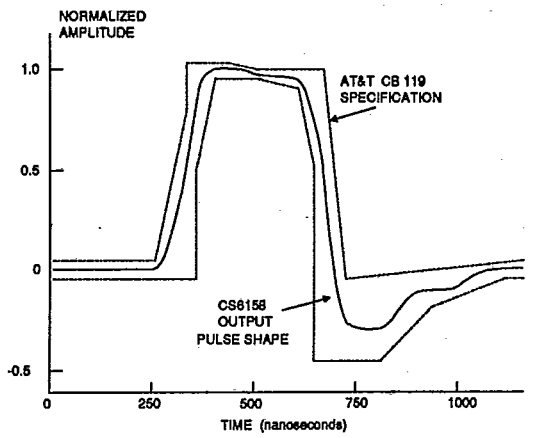

Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

	For coaxial cable, 75 ohm load and transformer specified in Table A1.	For shielded twisted pair, 120 ohm load and transformer specified in Table A1.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05 *	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

* When configured with a 0.47 uF nonpolarized capacitor in series with the Tx transformer primary as shown in Figures A1 and A2.

Table 2 - CCITT G.703 Pulse Specifications

case only, the width of this pulse is determined by the high cycle of TCLK. The pulse will meet the CCITT pulse shape template shown in Figure 5, and specified in Table 2, assuming the transmitter is terminated correctly and the TCLK duty cycle and frequency are appropriate. The rising and falling edge of TCLK control the time at which the rising and falling edges of the output pulse occur. Transmitter termination information is provided in the applications section which ap-

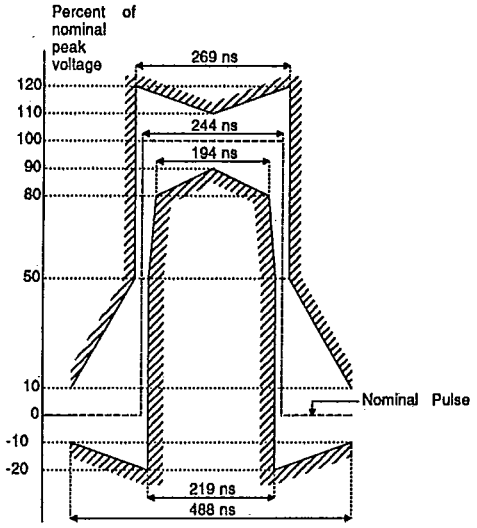

Figure 5 - Mask of the Pulse at the 2048 kbps Interface

pends this data sheet. Note that the pulse shape LEN2/1/0 = 010 generates the same amplitudes as the G.703 pulse (LEN2/1/0 = 000), but the pulse width is determined by the transmit delay line and will be approximately 263 ns when TCLK is 2.048 MHz.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals down to approximately 300 mV in amplitude and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS6158 side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

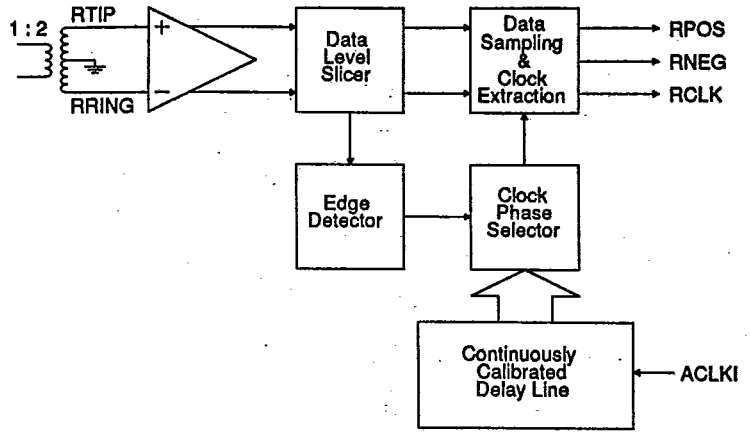

Figure 6. - Receiver Block Diagram

A block diagram of the receiver is shown in Figure 6. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. For all cases except where CCITT pulse shape (LEN2/1/0 = 000) are selected, the comparator thresholds are dynamically established by peak detectors to be at least 65% of peak level. When CCITT pulse shape is selected, the comparator threshold is 50% of peak level to improve signal to noise performance for long cable lengths.

The receiver uses an edge detector and a continuously calibrated delay line to generate the recovered clock. The delay line divides its reference clock, ACLKI, into 13 equal divisions of phases. Continuous calibration ensures timing accuracy, even if temperature or power supply voltage fluctuate.

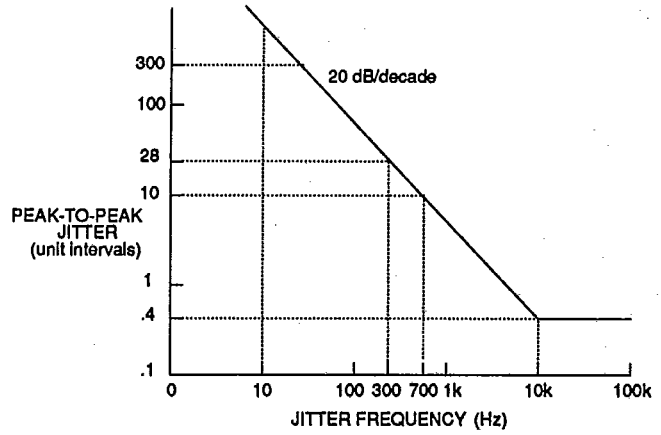

Figure 7. - Input Jitter Tolerance of Receiver

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data. The jitter tolerance of the CS6158 meets or exceeds the plot shown in Figure 7.

The initial production CS6158 devices will not output clock at RCLK until a signal is input to RTIP/RRING. The clock recovery circuit is calibrated, and the device will lock onto the AMI data input immediately. If loss of signal occurs, the RCLK frequency will equal the ACLKI frequency. In future versions of the CS6158, RCLK will be output and locked onto the ACLKI calibration clock any time no signal is present at the receiver, including initial power up.

Data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock.

Jitter and Recovered Clock

The CS6158 is designed for error free clock and data recovery from an AMI encoded data stream in the presence of more than 0.4 unit intervals of jitter at high frequency. This clock recovery circuit is also tolerant of long strings of zeros. The edge of an incoming data bit causes the circuitry to choose a phase from the delay line which most closely corresponds with the arrival time of the data edge, and that clock phase triggers a one shot which is typically 140 ns in duration. This phase of the delay line will continue to be selected until data bit arrives which is closer to another of the 13 phases, causing a new phase to be selected. The largest jump allowed along the delay line is six phases.

When an input signal is jitter free, the phase selection will occasionally jump between two adjacent phases resulting in RCLK jitter with an amplitude of 1/13 UI. These single phase jumps are due to differences in frequency of the incoming data and the calibration clock input to ACLKI. For T1 operation of the CS6158, the instantaneous period can be 14/13 * 648 ns = 698 ns (1,662,769 Hz) or 12/13 * 648 ns = 598 ns (1,425,231 Hz) when adjacent clock phases are chosen. As long as the same phase is chosen, the period will be 648 ns. Similiar calculations hold for PCM-30 rates.

The clock recovery circuit is designed to accept at least 0.4 UI of jitter at the receiver. Since the data stream only contains information when ones are transmitted, a clock/data recovery circuit must assume a zero when no signal is measured during a bit period. Likewise, when zeros are received, no information is present to update the clock recovery circuit regarding the trend of a signal which is jittered. The result is that two ones that are separated by a string of zeros can exhibit maximum deviation in pulse arrival time. For example; one half of a period of jitter at 100 kHz occurs in 5 µs, which is 7.7 T1 bit periods. If the jitter amplitude is 0.4 UI, then a one preceded by seven zeros can have maximum displacement in arrival time, i.e. either 0.4 UI too early or 0.4 UI too late. For the CS6158, the data recovery circuit correctly assigns a received bit to its proper clock period if it is displaced by less than 6/13 of a bit period from its optimal location. Theoretically, this would give a jitter tolerance of 0.46 UI. The actual jitter tolerance of the CS6158 is only slightly less than the ideal.

In the event of a maximum jitter hit, the RCLK clock period immediately adjusts to align itself with the incoming data and prepare to accurately place the next one, whether it arrives one period later, or after another string of zeros and is displaced by jitter. For a maximum early jitter hit, RCLK will have a period of 7/13 * 648 ns = 349 ns (2,865,961 Hz). For a maximum late jitter hit, RCLK will have a period of 19/13 * 648 ns = 947 ns (1,055,880 Hz).

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.3 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. Since the receiver is being calibrated by ACLKI, the RCLK output will equal the ACLKI frequency upon loss of signal. On initial production CS6158 devices, LOS returns to a logic 0 upon receipt of the first bit at the RTIP/RRING inputs. For future versions, LOS returns to logic zero when the received signal returns to 12.5% ones density (based on 4 ones out of 32 bit periods). Received data is output on RPOS/RNEG regardless of LOS status.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG, and outputs it at RCLK, RPOS and RNEG. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 27, high.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent back out on the line via TTIP and TRING. The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In remote loopback, the recovered clock is used to calibrate the transmitter delay line. Because RCLK cycle times vary, selecting RLOOP will result in adding jitter to the transmitted data. *Therefore selection of the RLOOP function on a functioning link is not recommended.* Rather, it is recommended that remote loopbacks be implimented external to the CS6158, for example, by using a frame buffer in the data path between the CS6158 receiver and transmitter.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS6158 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors the transmitted signal on input pins, MTIP and MRING. If no signal is present on MTIP and MRING for 63 clock cycles, the DPM pin goes high.

Whenever more than one CS6158 reside on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each CS6158 monitor performance of a neighboring CS6158 device, rather than having it monitor its own performance. Note that in the host mode, DPM is available from both the register and pin 11.

Power On Reset / Reset

Upon power-up, the CS6158 is held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can only be calibrated if a reference clock is present. The reference clock for the receiver is provided by ACLKI. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function foregoes any requirement to reset a CS6158 when in operation. However, a reset function is available which will clear the internal logic.

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A reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP or LLOOP).

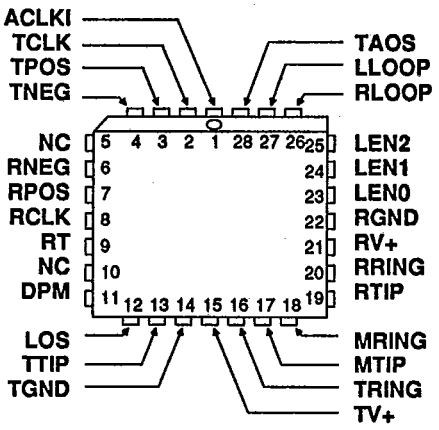
Power Supply

The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for proper operation of the analog circuits in both the transmit and receive paths. The best way to configure the power supplies is to tie TV+ to RV+ at the chip. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as close as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire wrap bread-boarding of the CS6158 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

ALT. EXTERNAL CLOCK INPUT	ACLKI	1	28	TAOS	TRANSMIT ALL ONES SELECT
TRANSMIT CLOCK	TCLK	2	27	LLOOP	LOCAL LOOP BACK
TRANSMIT POSITIVE PULSE	TPOS	3	26	RLOOP	REMOTE LOOP BACK
TRANSMIT NEGATIVE PULSE	TNEG	4	25	LEN2	BIT 2 OF LINE LENGTH SELECT
NO CONNECT	NC	5	24	LEN1	BIT 1 OF LINE LENGTH SELECT
RECEIVED NEGATIVE PULSE	RNEG	6	23	LEN0	BIT 0 OF LINE LENGTH SELECT
RECEIVED POSITIVE PULSE	RPOS	7	22	RGND	RECEIVE GROUND
RECOVERED CLOCK	RCLK	8	21	RV+	RECEIVE V+ (+5VDC)
RESISTOR TERMINATION	RT	9	20	RRING	RECEIVE RING
NO CONNECT	NC	10	19	RTIP	RECEIVE TIP
DRIVER PERFOMANCE MONITOR	DPM	11	18	MRING	MONITORED RING
LOSS OF SIGNAL	LOS	12	17	MTIP	MONITORED TIP
TRANSMIT TIP	TTIP	13	16	TRING	TRANSMIT RING
TRANSMIT GROUND	TGND	14	15	TV+	TRANSMIT V+ (+5VDC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.
Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.
Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.
Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.
Power supply ground for the device, except transmit drivers; typically 0 volts.

Control

LLOOP - Local Loopback, Pin 27.

Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins. TCLK and TPOS/TNEG are still transmitted. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

TAOS - Transmit All Ones select, Pin 28.

Setting TAOS to logic 1 causes continuous ones to be transmitted at the frequency selected by TCLK.

Inputs

ACLKI - Alternate External Clock Input, Pin 1.

Either a 1.544 MHz (or 2.048 MHz for CCITT) clock must be input to ACLKI, which is used to calibrate the receiver delay line. Since ACLKI is used to calibrate the receiver, RCLK will equal ACLKI upon loss of signal.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RPOS/RNEG and RCLK.

RT - Resistor Termination, Pin 9.

This pin should be connected to a supply rail. Power consumption will be minimized by connecting pin to RV+ through a 1kΩ resistor.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a CS6158. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

CRYSTAL

Data Book Errata

Please mark your Crystal Semiconductor Data Book with the following corrections.

Page	Part #	Description of corrections
2-73	CS61574	Line 13, column 1 should be " $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of ... ".
2-104	CS6158	Pin 5, NC, must be grounded.
4-28	CS80600	Second paragraph, delete "four times". Also Figure A7 should show SLAVE CS80600 pin 6 pulled high to V+ through a 10 kΩ resistor.
4-29	CS80600	Last sentence should read " which uses an external divide by 128,".
6-32	CS8126	NC pins must be left floating.
7-31	CS8870	The end of the 2nd paragraph should be " a t_{REC} of 40 ms is achieved by using a 380 kΩ resistor."
8-5	CS5012	12 kHz Peak Harmonic for -7 is 80 dB typical, 75 dB minimum.
8-8	CS5012	t_{ca} and t_{ra} is 90 ns typ., 120 ns max. for K, B.
8-38	CS5014	t_{ca} and t_{ra} is 115 ns typ., 150 ns max. for T.
8-68	CS5016	t_{fd} is 90 ns typ., 110 ns max. for K,B. t_{fd} is 90 ns typ., 140 ns max. for T.
8-18	CS5012	Figure 9, SCLK and SDATA should be shifted 2 CLKIN cycles to the right.
8-48	CS5014	
8-78	CS5016	
8-98	CS5101	Delete -10 Master Clock Period options. CLKIN duty cycle is 30% to 70%.
8-98	CS5101	Note 13. SSH only works correctly if $\overline{HOLD}$ falling edge is within ±30 ns of CH1/2 edge OR if CH1/2 edge occurs between 120 ns after $\overline{HOLD}$ falls to 64 t_{CLK} after $\overline{HOLD}$ falls.
8-103	CS5101	In coarse charge the CS5101 will slew at 13 V/µs in unipolar mode and 26 V/µs in bipolar mode. In fine charge, the slew rate is 1.3 V/µs in unipolar mode and 2.6 V/µs in bipolar mode.
8-148	CS5317	CLKIN pulse width, low and high, in CLKG1 and CLKG2 modes is 200 ns min.
8-164	CS5317	Delete the "Z" from the Ordering Guide Model Number.
8-174	CS5326	VREF capacitor is 10 µF in parallel with a 0.1 µF.
9-16	CS3112	Analog characteristics table changes. Contact the factory or your local sales representative for the latest information.
9-26	CS31412	
9-20	CS3112	Pin 1 must be grounded.
13-26	CS5014B	t_{FD} max. is 250 ns, t_{ss} is 2/f_{CLK} - 50 ns, t_{SH} is 2/f_{CLK} - 100 ns.
13-42	CS5016B	
14-25	CDB5317	Figure 2 should show the REFBUF 0.1 µF capacitor going to AGND NOT VA-.
14-35	CDB5412	Figure 5. Pin 29 is CLKIN, Pin 28 is XIN.
14-54	CDB615Xx	R_3 = 220 kΩ.
14-58	CDB61544	The "new and improved reset circuit" should have R_3 = 220 kΩ and show 1 kΩ pull down resistors from RLOOP and LLOOP to ground.
15-22		Figure 12. The +4.5 V output should not be connected to ground!

2-104a

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Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when 175 consecutive zeros have been detected. In initial production devices, LOS returns to logic 0 on the first bit received. In future versions, LOS returns to a logic 0 when a 12.5% ones density signal returns (determined by receipt of 4 ones within 32 bit periods). When in loss of signal state, received ones are still output at RPOS/RNEG.

DPM - Driver Performance Monitor, Pin 11.

If no signal is present on MTIP and MRING for 63 clock cycles, DPM goes to a logic 1 until the first detected signal.

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.

Data and clock are recovered from the RTIP and RRING inputs and are output at these pins. A signal on RPOS corresponds to a positive pulse received on RTIP and RRING, while a signal on RNEG corresponds to the receipt of a negative pulse. RPOS and RNEG are NRZ. RPOS and RNEG are stable and valid on the rising edge of RCLK.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. This output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, approximately 4.4 ohms of resistance should be added in series with the transformer primary. The transmitter will drive twisted-shielded pair cable, terminated with 120 Ω, without additional components.

Miscellaneous

NC - No Connects, Pins 5 and 10

These pins are not connected to the die, and may be left floating.

APPLICATIONS

Line Interface

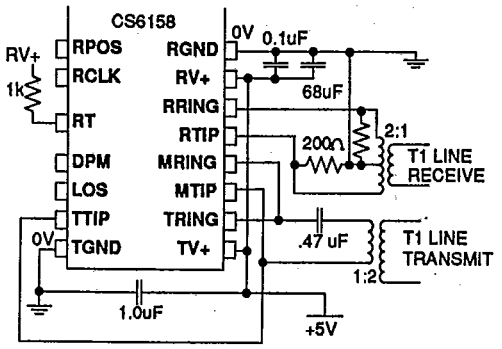


Figure A1. - Typical Configuration Showing Line Interface

Figure A1 shows the typical configuration for interfacing the CS6158 to a T1 line through transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200 Ω resistors between the center tap and each leg on the CS6158 side. These resistors provide the 100 Ω termination for the T1 line. When terminating twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load.

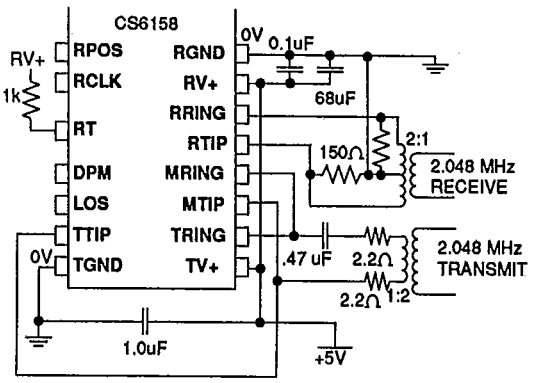


Figure A2. - Configuration for Transmitting onto 75 Ω Coax

Figure A2 shows the configuration needed for transmitting data at 2.048 MHz onto a 75 Ω coax cable. The 2.2 Ω resistors serve two functions. First, they provide the appropriate 25 Ω load to TTIP and TRING. Second, the resistors attenuate the signal slightly to meet the CCITT pulse amplitude requirements. Note that these 2.2 Ω resistors should not be used when interfacing to CCITT 120 Ω cable. For the receiver, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

To save on power consumption under normal operating conditions, the output drivers are powered down during the transmission of a space (zero) on to the line. Approximately one quarter cycle prior to transmitting a mark (one), the drivers are enabled. The transformer interacting with the driver can cause a slight voltage difference (< 200 mV) between the driven zero and the non-driven zero. We recommend that this effect be eliminated by inserting a 0.47 µF, non-polarized capacitor in series with the primary transformer.

Transformers

Transformers listed in Table A1 have been found to be suitable for use with the CS6158. Figure A3 shows the connections for some of the recom-

Manufacturer	Part #
Pulse Engineering	PE-64931 (FAL 1.0)
Pulse Engineering	PE-64951 (FAL 4.1)
Schott Corp.	67112060
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-0001
Midcom	671-5832

Note: The Pulse Eng. 1682x and 5764 are still acceptable, but the other Pulse Engineering transformers are preferred.

Table A1. - Suitable Transformers

mended transformers for the transmitter. Key transmit transformer specifications are:

Turns ratio: 1:2 (or 1:1:1) ± 5%,

Primary inductance: 600 µH min measured at 10kHz and 0.005 VRMS.

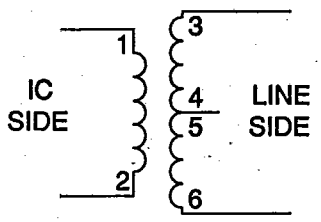
Leakage inductance: 1.3 µH max with secondary shorted.

Interwinding capacitance: 23 pF max, primary to secondary.

Receive transformer specifications are not critical.

Interfacing the CS6158 with T1 Digital Transceiver

This section gives general guidance on how to interface the CS6158 with digital T1 framing and signaling transceivers such as the CS2180A. Design attention must be given to insure that the devices are properly interfaced. To interface with the CS2180A, connect the devices as shown in Figure A4.



Pulse Engineering 5764 & PE-64931
Bell Fuse 0553-5006-16
Schott 67112060

Figure A3.- Some Recommended Transmitter Transformer Configurations

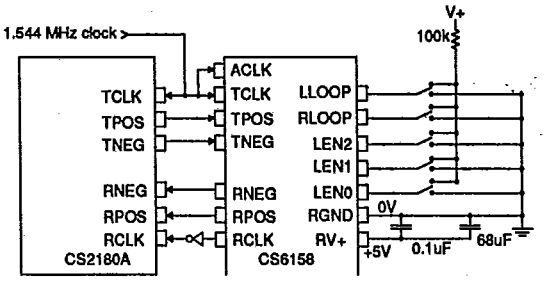


Figure A4. - Interfacing the CS6158 with and CS2180A