Semiconductor Corporation

CS61574

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, Jitter Attenuator and Clock Recovery Functions
- Diagnostic Features
- Microprocessor Controllable
- Has the same pin-out and uses the same external components as the CS61577. The CS61577 has performance advantanges over the CS61574.

General Description

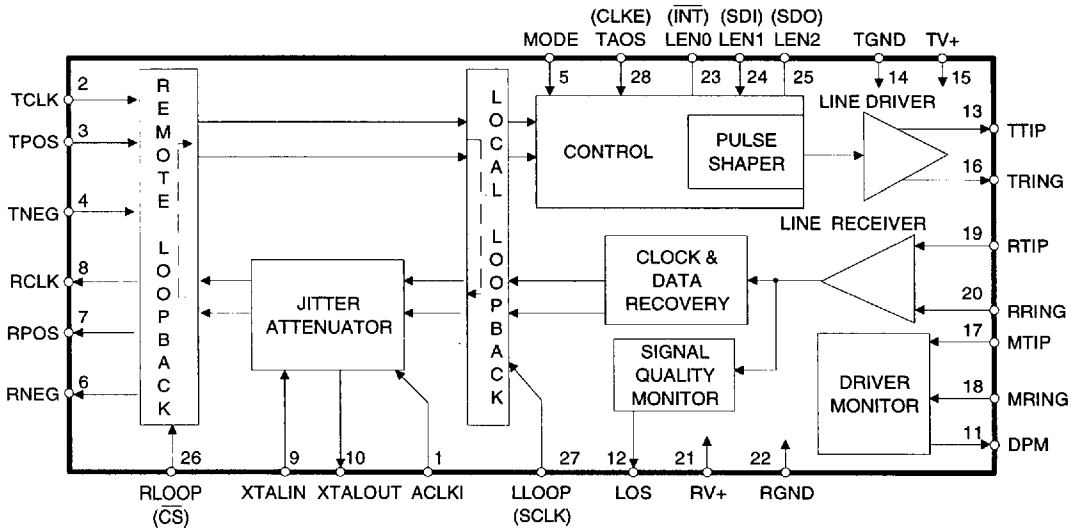
The CS61574 combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device. The CS61574 supports processor-based or stand-alone operation and interfaces with industry standard T1 and E1 framers.

The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance. The transmitter internally shapes output pulses according T1 DSX-1 and E1 template specifications.

Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

ORDERING INFORMATION - See page 3-217.



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ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply	(referenced to GND	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin	(Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply	(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
Power Consumption	(Notes 4,5)	P_C	-	620	760	mW
Power Consumption	(Notes 4,6)	P_C	-	400	-	mW

Notes:
3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (T_A = -40° to 85°C; TV+, RV+ = 5.0V ± 5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage PINS 1-5, 23-28	(Note 7)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage PINS 1-5, 23-28	(Note 7)	V_{IL}	-	-	0.8	V
High-Level Output Voltage I_{OUT} = -40 µA PINS 6-8, 11, 12, 23, 25	(Note 8)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA PINS 6-8, 11, 12, 23, 25	(Note 8)	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)			-	-	±10	µA

Notes:
7. Functionality of pins 23 and 25 depends on the mode. See Operating Modes description.
8. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (T_A = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 9)				
E1, 75 Ω	(Note 10)	2.14	2.37	2.6	V
T1, Part 68; E1, 120 Ω	(Note 11)	2.7	3.0	3.3	V
T1, DSX-1	(Note 12)	2.4	3.0	3.6	V
Recommended Output Load at TTIP and TRING		-	25	-	Ω
Jitter Added During Remote Loopback	(Note 13)				
10Hz - 8kHz		-	0.005	-	UI
8kHz - 40kHz		-	0.008	-	UI
10Hz - 40kHz		-	0.010	-	UI
Broad Band		-	0.015	-	UI
Power in 2kHz band about 772kHz	(Notes 14, 15)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Note 14, 15)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Note 14, 15)	-	0.2	0.5	dB
Receiver					
Sensitivity Below DSX (0dB = 2.4V)		-10	-	-	dB
Loss of Signal Threshold		-	0.3	-	V
Data Decision Threshold T1 pulse settings		-	65	-	% of peak
E1, LEN2/1/0 = 000 or 010		-	50	-	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance	(Note 16)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Jitter Attenuator					
Jitter Attenuation Curve Corner Frequency	(Notes 15, 17)	-	6	-	Hz
Attenuation at 10kHz Jitter Frequency	(Notes 15, 17)	-	50	-	dB
Attenuator Input Jitter Tolerance (Before Onset of FIFO Overflow or Underflow Protection)	(Notes 15, 17)	12	23	-	UI

Notes:
9. Using transformer recommended in the Application Section.
10. This amplitude is measured at the output of the transformer for line length setting LEN2/1/0 = 000 (see Figure 8) with a 4.4 Ω resistor in series with TTIP.
11. These amplitudes, measured at the output of the transformer for line length setting LEN2/1/0 = 000 or LEN210 = 010.
12. These amplitudes, measured at the DSX-1 Cross-Connect, are for all line length settings from LEN2/1/0 = 011 to LEN2/1/0 = 111 (see Figure 7).
13. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
14. Typical performance with a 0.47µF capacitor in series with primary of transmitter output transformer.
15. Not production tested. Parameters guaranteed by design and characterization.
16. Jitter tolerance increases at lower frequencies. See Figure 10.
17. Attenuation measured with input jitter equal to 3/4 of measured jitter tolerance. Circuit attenuates jitter at 20 dB/decade above the corner frequency. See Figure 11.
Output jitter can increase significantly when more than 12 UI's are input to the attenuator.
See discussion in Wander and Jitter Attenuator section.

T1 SWITCHING CHARACTERISTICS (T_A = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 18)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
ACLKI Frequency	(Note 19)	f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle	(Note 20)	t_{pwh1}/t_{pw1}	-	50	-	%
Rise Time, All Digital Outputs	(Note 21)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 21)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su1}	-	274	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_{h1}	-	274	-	ns

PCM-30 SWITCHING CHARACTERISTICS (T_A = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 18)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
TCLK Duty Cycle for LEN2/1/0 = 0/0/0	(Note 22)	t_{pwh2}/t_{pw2}	44	50	53	%
ACLKI Frequency	(Note 19)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	(Note 20)	t_{pwh1}/t_{pw1}	-	50	-	%
Rise Time, All Digital Outputs	(Note 21)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 21)	t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su1}	-	194	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_{h1}	-	194	-	ns

Notes: 18. Crystal must meet specifications described in CXT6176/CXT8192 data sheet.
19. ACLKI provided by an external source or TCLK.
20. RCLK duty cycle will be 62.5% or 37.5% when jitter attenuator limits are reached.
21. At max load of 1.6 mA and 50 pF.
22. The transmitted pulse width for LEN2/1/0 = 0/0/0 is tied to the high cycle of TCLK.

SWITCHING CHARACTERISTICS (T_A = -40° to 85°C; TV+, RV+ = ±5%;
Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	240	-	-	ns
SCLK High Time	t_{ch}	240	-	-	ns
SCLK Rise and Fall Time	t_r, t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 23)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns

Notes: 23. Output load capacitance = 50pF.

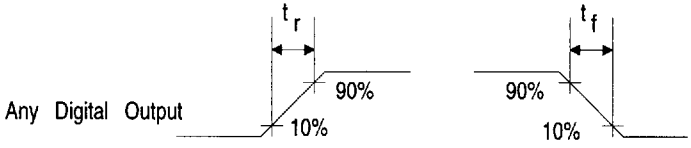


Figure 1. Signal Rise and Fall Characteristics

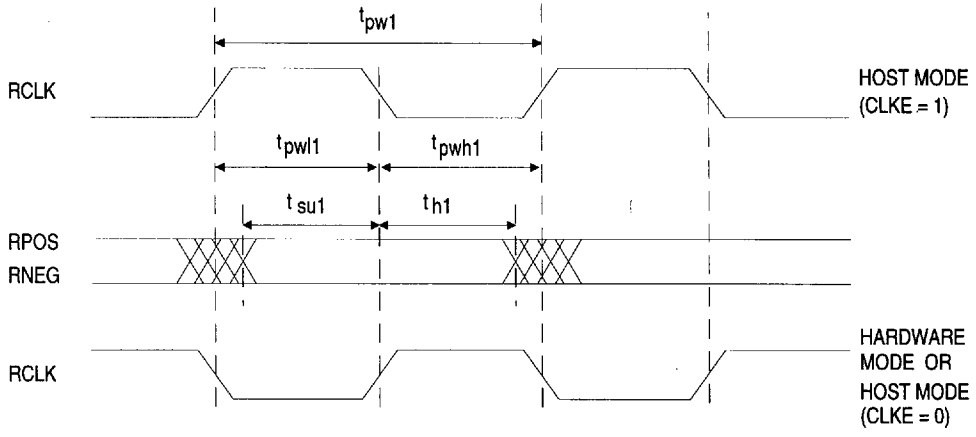


Figure 2. Recovered Clock and Data Switching Characteristics

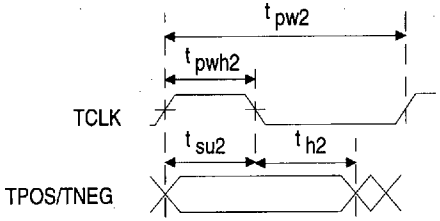


Figure 3. Transmit Clock and Data Switching Characteristics

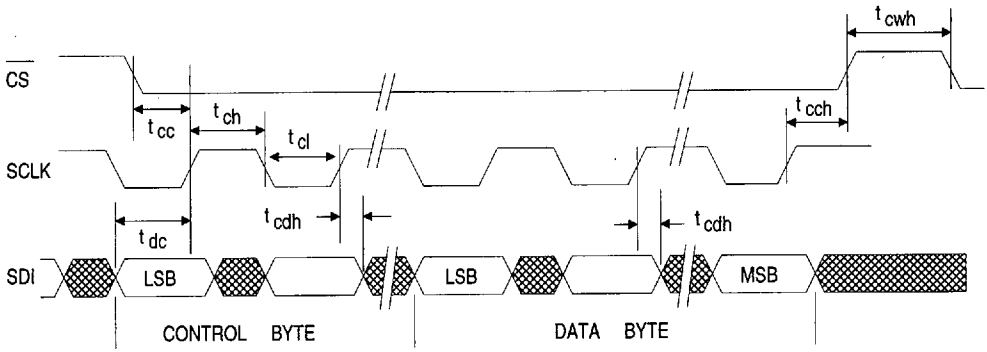


Figure 4. Serial Port Write Timing Diagram

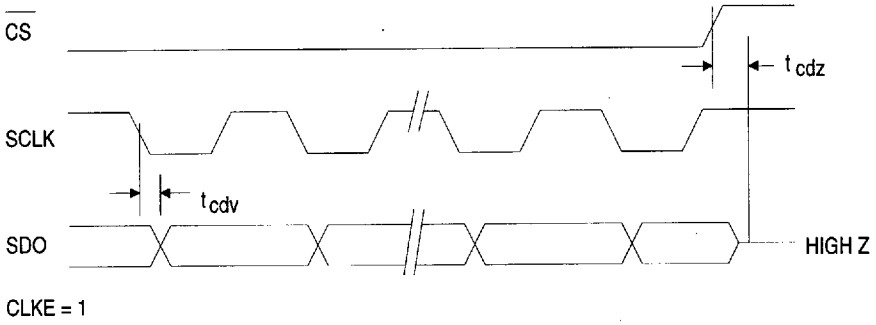


Figure 5. Serial Port Read Timing Diagram

THEORY OF OPERATION

Introduction to Operating Modes

The CS61574 supports two operating modes (as selected by pin MODE) as shown in Figure 6, and Figures A1 and A2 of the applications section.

The modes are Hardware Mode, and Host Mode. In Hardware Mode, discrete pins are used to interface the device's control functions and status information. In the Host Mode, the line interface is connected to a host processor and a serial data bus is used for input and output of control and status information

Transmitter

The transmitter takes data from a T1 (or E1) terminal, and produces pulses of appropriate shape. The transmit clock (TCLK) and transmit data (TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

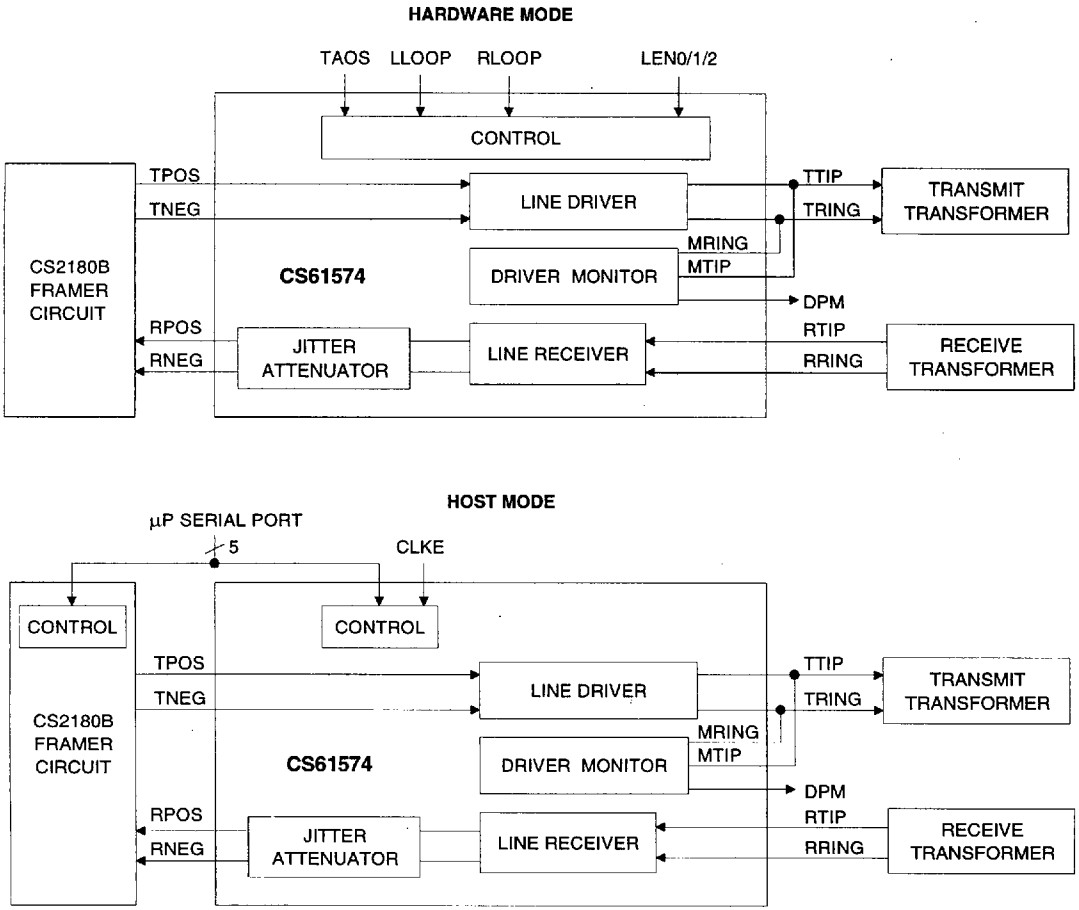


Figure 6. Overview of Operating Modes

LEN2	LEN1	LEN0	Option Selected	Application
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	0	75Ω (with 4.4Ω resistor) & 120 Ω	E1 CCITT G.703
0	0	1		RESERVED
0	1	0	FCC PART 68, OPT. A	NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 1. Line Length Selection

Either T1 (DSX-1 or Network Interface) or E1 CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs as shown in Table 1. The CS61574 drives a 25 Ω load.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) are selectable. The five partition arrangement meets CB-119 requirements when using ABAM cable. A typical output pulse is shown in Figure 7. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

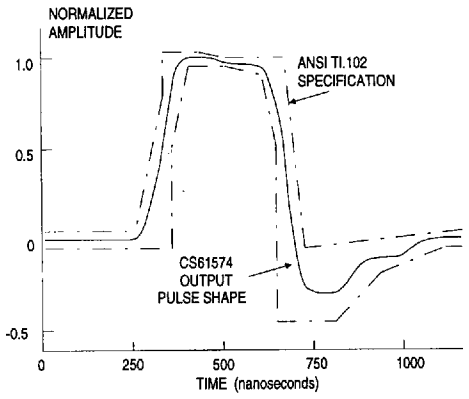


Figure 7. Typical Pulse Shape at DSX-1 Cross Connect

For T1 Network Interface applications, additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns).

The CCITT G.703 E1 output pulse shapes supported with line length selection LEN2/1/0=0/0/0. For 75Ω E1 applications a 4.4Ω resistor is required in series with the TTIP or TRING pins as shown in Figure A1.

Note that for LEN2/1/0=000, the transmitter pulse width is determined by the high time of TCLK. The pulse will meet the CCITT pulse shape template shown in Figure 8, and specified in Table 2, assuming the TCLK duty cycle and frequency are appropriate.

If the clock signal is removed from TCLK on the CS61574, TPOS and TNEG should both be low during the last falling edge of TCLK.

To place the device in a low power dissipation mode (i.e., to disable the drive), TPOS and TNEG should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter

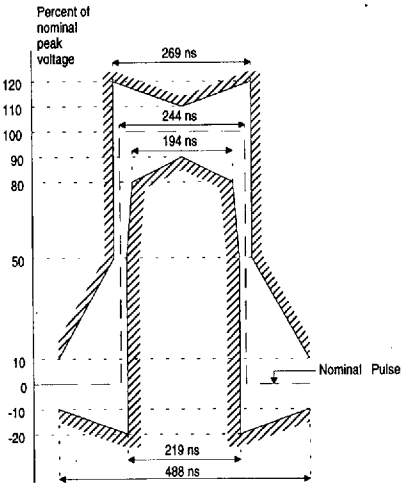


Figure 8. Mask of the Pulse at the 2048 kbps Interface

outputs may not meet all data sheet specifications for 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of ABAM cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411-1990, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 9. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for PCM-30, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data.

Data sampling will continue at the periods selected by the phase selector until an incoming pulse deviates enough to cause a new phase to be selected for data sampling. The phases of the delay line are selected and updated to allow as much as 0.4 UI of jitter from 10 kHz to 100 kHz, without error. The jitter tolerance of the receiver exceeds that shown in Figure 10. Additionally, this method of clock and data recovery is tolerant of long strings of consecutive zeros. The data sampler will continuously sample data based on

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transfromer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figures A1, and A2

Table 2. CCITT G.703 Specifications

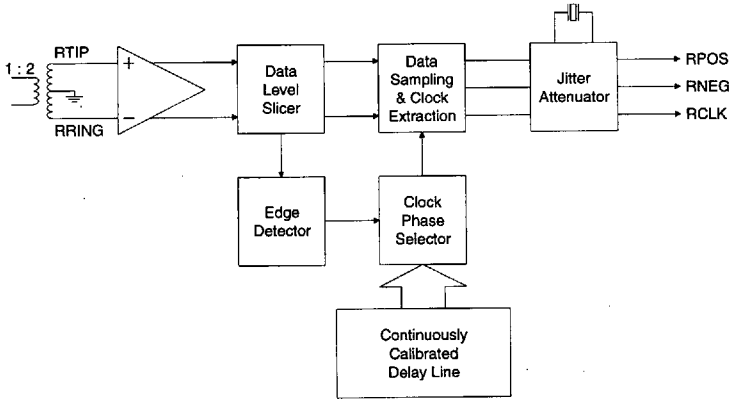


Figure 9. Receiver Block Diagram

its last input until a new pulse arrives to update the clock phase selector.

The delay line is continuously calibrated relative to a reference clock, which is provided by the crystal oscillator. The delay line produces 13 phases for each cycle of the reference clock. In effect, the 13 phases are analogous to a 20 MHz clock when the reference clock is 1.544 MHz. This implementation utilizes the benefits of a 20 MHz clock for clock recovery without actually having the clock present to impede analog circuit performance.

In the Hardware Mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the Host mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 3.

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2V)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+) - 0.2V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+) - 0.2V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

Table 3. Data Output/Clock Relationship

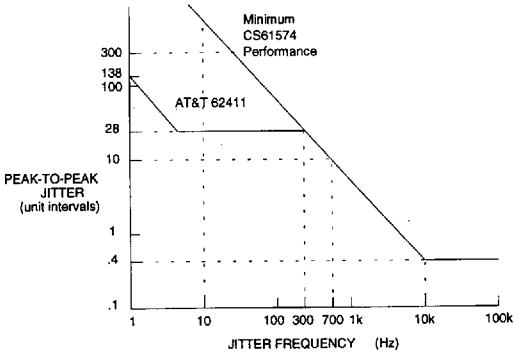


Figure 10. Minimum Input Jitter Tolerance of Receiver (Clock Recovery Circuit and Jitter Attenuator)

Loss of Signal

The receiver will indicate loss of signal upon receiving 175 consecutive zeros. A digital counter counts received zeros, based on RCLK cycles. The zero input level is determined either when zeros are received, or when the received signal amplitude degrades below a $0.3V_{peak}$ threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt will be issued on $\overline{INT}$. LOS will go low (and flag the $\overline{INT}$ pin again if the serial I/O is used) when a valid signal is detected. Note that in the host mode, LOS is simultaneously available from both the register and pin 12. Table 4 shows

the status of RCLK upon LOS. Received data is output on RPOS/RNEG regardless of LOS status.

LOS returns to logic zero when the first one is received. ACLKI serves no significant purpose and should be grounded.

Crystal Present?	ACLKI Present?	Source of RCLK
No	Yes	ACLKI
Yes	No	Centered Crystal
Yes	Yes	RTIP/RRING via Jitter Attenuator

Table 4. RCLK Status at LOS

Jitter Attenuator

The jitter attenuator reduces wander and jitter in the recovered clock signal. It consists of a 32-bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 11. The CS61574 will have a discontinuity in the jitter transfer function when the incoming jitter amplitude exceeds approximately 23 UIs.

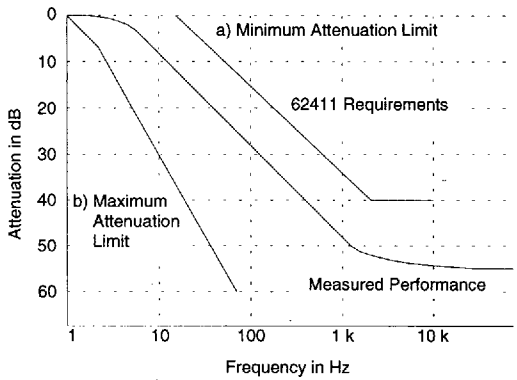


Figure 11. Typical Jitter Transfer Function

The jitter attenuator works in the following manner. The recovered clock and data are input to the FIFO with the recovered clock controlling the FIFO's write pointer. The crystal oscillator controls the FIFO's read pointer which reads data out of the FIFO and presents it at RPOS and RNEG. The update rate of the read pointer is analogous to RCLK. By changing the load capacitance that the IC presents to the crystal, the oscillation frequency is adjusted to the average frequency of the recovered signal. Logic determines the phase relationship between the read and write pointers and decides how to adjust the load capacitance of the crystal. Thus the jitter attenuator behaves as a first-order phase lock loop. Signal jitter is absorbed in the FIFO.

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should they attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. During this activity, data will never be lost.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG sends it through the jitter attenuator and outputs it at RCLK, RPOS and RNEG. If the jitter attenuator is disabled, it is bypassed. Inputs to the transmitter are still transmitted on the line, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted to the line at the rate determined by TCLK. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 27, high or LLOOP may be commanded via the serial interface.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the

jitter attenuator to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 5). The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset). A remote loopback bypasses the line code encoder/decoder, insuring that the transmitted signal matches the received signal, even in the presence of received bipolar violations.

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	TCLK
1	X	RTIP & RRING	RTIP & RRING (RCLK)

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 5. Interaction of RLOOP with TAOS

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the IC is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if (MTIP-MRING) does not transition above or below a threshold level of approximately 500 mV at least once within 64±2 cycles. In the Host Mode, DPM is available from both the register and pin 11. The driver performance monitor is not designed to detect broken printed ciruit board traces between TTIP/TRING and the line termination or between MTIP/MRING and TTIP/TRING.

DPM should be averaged externally in hardware or software for approximately 500 ms to filter short assertions caused by very low ones density before action is taken to respond to the driver failure.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance. Note that a CS61574 cannot be used to monitor the TTIP/TRING pins of a CS61574A, CS61535A, CS6158A or CS61575.

Power On Reset / Reset

Upon power-up, the IC is held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by the crystal oscillator, or ACLKI if the oscillator is disabled. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset the line interface

when in operation. However, a reset function is available which will clear all registers.

In the Hardware Mode, a reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0 and force the oscillator to its center frequency before initiating calibration.

Serial Interface

In the Host mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to via the SDI pin or read from via the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 3. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 12 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 1, data bit D7 is held until the falling edge of the 16th clock cycle.When CLKE = 0, data bit D7 is held until the rising edge of the 17th clock cycle. SDO goes High-Z after $\overline{CS}$ goes high *or* at the end of the hold period of data bit D7.

An address/command byte, shown in Table 6, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The line interface responds to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 6. Address/Command Byte

The data register, shown in Table 7, can be written to the serial port. Data is input on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver.

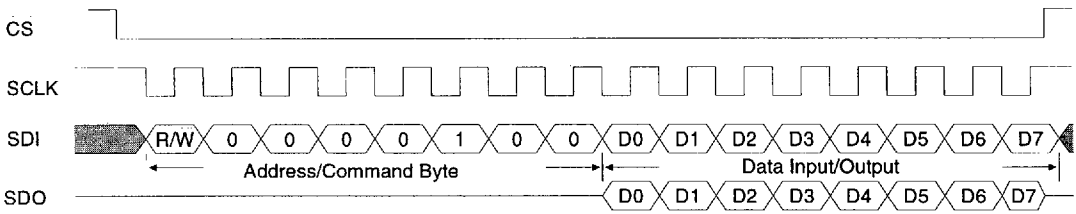


Figure 12. Input/Output Timing

LSB: first bit in	0	clr LOS	Clear Loss Of Signal
	1	clr DPM	Clear Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in	7	TAOS	Transmit All Ones Select

NOTE: Setting bits 5,6 & 7 to 101 or 111 puts the CS61574 into a factory test mode.

Table 7. Input Data Register

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) The current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt).
2) Output data bits 5, 6 and 7 will be reset as appropriate.
3) Future interrupts for the corresponding LOS or DPM will be suppressed (i.e., prevented from occurring).

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Input bits 5/6/7=111 and 5/6/7=101 are the same request, and cause the line interface to enter into the factory test mode. In other words, when RLOOP=1 (Bit 5) and TAOS=1 (Bit 7), LOOP (Bit 6) is a don't care. For normal operation, RLOOP and TAOS should not be simultaneously selected via the serial interface.

Output data from the serial interface is presented as shown in Tables 8 and 9. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (Bits 5, 6 and 7) indicate intermitent losses of signal and/or driver problems.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

LSB: first bit in	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select

Table 8. Output Data Bits 0 - 4

Bits 5	6	7	Status
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS in effect.
0	1	0	LLOOP in effect.
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect.
1	0	1	DPM changed state since last "clear DPM" occurred.
1	1	0	LOS changed state since last "clear LOS" occurred.
1	1	1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 9. Coding for Serial Output bits 5,6,7

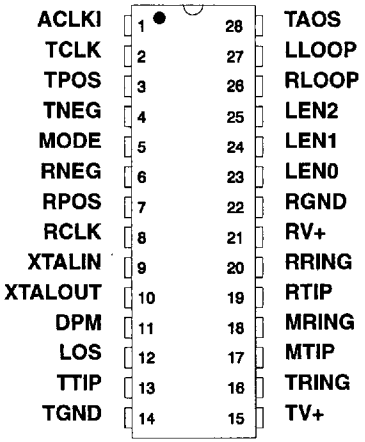
Power Supply

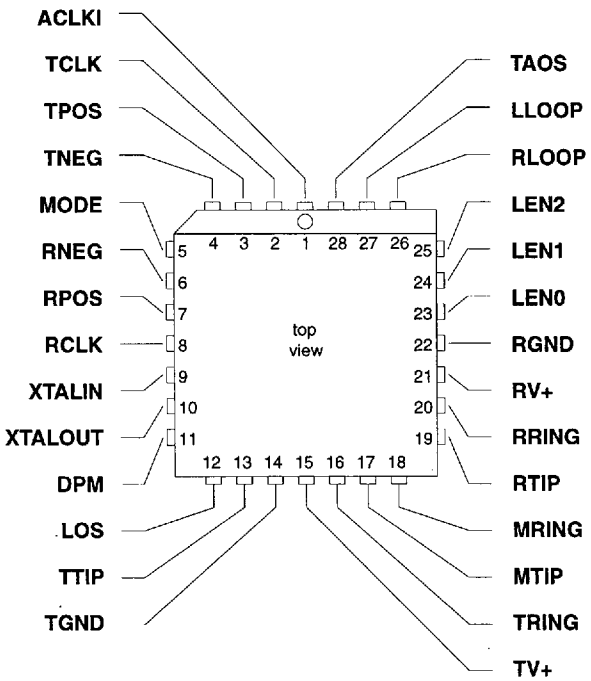
The device operates from a single 5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

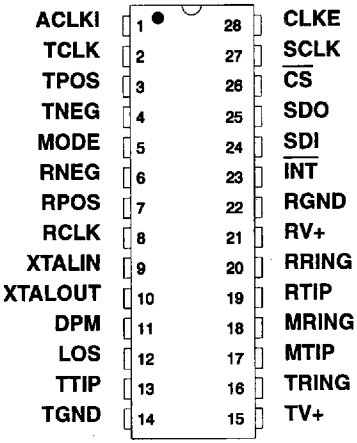
PIN DESCRIPTIONS

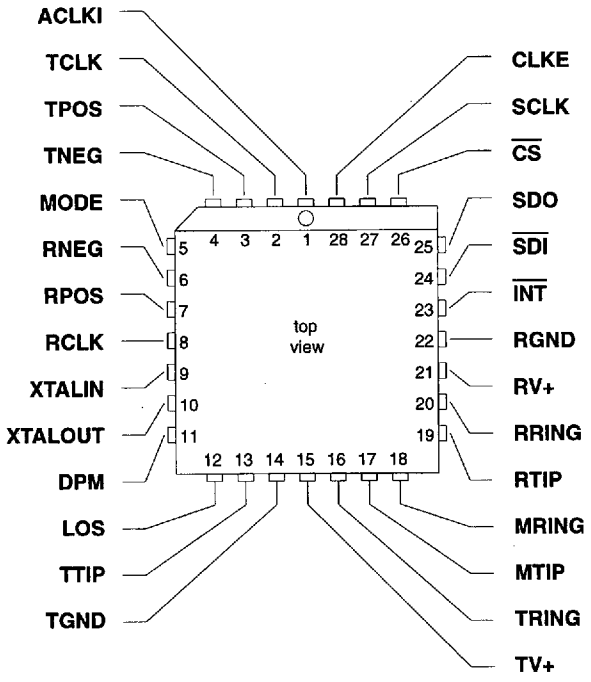
Hardware Mode





Host Mode





Power Supplies

TV+ - Power Supply, Transmit Driver, Pin 15.
Power supply for the transmit driver; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3 V.

TGND - Ground, Transmit Driver, Pin 14.
Power supply ground for the transmit driver; typically 0 Volts.

RV+ - Power Supply, Pin 21.
Power supply for all subcircuits except the transmit driver; typically +5 Volts.

RGND - Ground, Pin 22.
Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.
A 6.176 MHz (or 8.192 MHz) crystal should be connected across these pins. If a 1.544 MHz (or 2.048 MHz) clock is provided on ACLKI (pin 1), the jitter attenuator may be disabled by tying XTALIN, Pin 9 to RV+ through a 1 kΩ resistor, and floating XTALOUT, Pin 10.
Note: Overdriving the oscillator with an external clock is not supported.

Control

MODE - Mode Select, Pin 5.
Driving the MODE pin high puts the line interface in the Host Mode. In the Host mode, a serial control port is used to control the line interface and determine its status. Grounding the MODE pin puts the line interface in the Hardware Mode, where configuration and status are controlled by discrete pins.

TAOS - Transmit All Ones Select, Pin 28 (Hardware Mode).
Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK. In the host mode, simultaneous selection of RLOOP & TAOS enables a factory test mode.

LLOOP - Local Loopback, Pin 27 (Hardware Mode).
Setting LLOOP to a logic 1 routes the transmit clock and data through the jitter attenuator to the receive clock and data pins. TCLK and TPOS/TNEG are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 26. (Hardware Mode)
Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG. Any TAOS request is ignored in the hardware mode. In the Host mode, simultaneous selection of RLOOP & TAOS enables a factory test mode. Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25. (Hardware Mode)

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection. Also controls the receiver slicing level.

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23. (Host Mode)

Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by writing "clear LOS" or "clear DPM" to the register. $\overline{\text{INT}}$ is an open drain output and should be tied to the positive supply through a resistor.

SDI - Serial Data Input, Pin 24. (Host Mode)

Data for the on-chip register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25. (Host Mode)

Status and control information from the on-chip register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

CLKE - Clock Edge, Pin 28. (Host Mode)

Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

SCLK - Serial Clock, Pin 27. (Host Mode)

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

$\overline{\text{CS}}$ - Chip Select, Pin 26. (Host Mode)

Pin must transition from high to low to read or write the serial port.

ACLKI - Alternate External Clock Input, Pin 1.

A 1.544 MHz (or 2.048 MHz) clock may be input to ACLKI, or this pin must be tied to ground.

Data

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RCLK and RPOS/RNEG.

RCLK - Recovered Clock, Pin 8.

The receiver recovered clock generated by the jitter attenuator is output on this pin. When in the loss of signal state RPOS/RNEG are forced low. If ACLKI is grounded, RCLK is forced to the center frequency of the crystal oscillator during loss of signal.

RPOS, RNEG - Receive Positive Data, Receive Negative Data, Pins 6 and 7 (Hardware and Host Modes).

The receiver recovered digital data is output on these pins. In the Hardware mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the Host mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 3. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. The transmitter output is designed to drive a 25 Ω load between TTIP and TRING.

TCLK - Transmit Clock, Pin 2.

The1.544 MHz (or 2.048 MHz) transmit clock is input on this pin. TPOS/TNEG are sampled on the falling edge of TCLK.

TPOS, TNEG - Transmit Positive Data, Transmit Negative Data, Pins 3 and 4 (Hardware and Host Modes).

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

Status

LOS - Loss of Signal, Pin 12.

LOS goes high when 175 consecutive zeros have been received. LOS returns low after the next pulse is received. When in the loss of signal state RPOS/RNEG are forced low. If ACLKI is grounded, RCLK is forced to the center frequency of the crystal oscillator during loss of signal.

MTIP, MRING - Monitor Tip, Monitor Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a line interface IC. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly. If the $\overline{\text{INT}}$ pin in the host mode is used, and the monitor is not used, writing "clear DPM" to the serial interface will prevent an interrupt from the driver performance monitor.

DPM - Driver Performance Monitor, Pin 11.

DPM goes high if no activity is detected on MTIP and MRING for 64±2 bit periods. DPM returns low when the first transition is detected on MTIP and MRING.

Ordering Guide

Model	Frequency	Package
CS61574-IP	T1 only	28-pin Plastic DIP
CS61574-IP1	T1 & E1	28-pin Plastic DIP
CS61574-IL	T1 only	28-pin PLCC
CS61574-IL1	T1 & E1	28-pin PLCC

APPLICATIONS

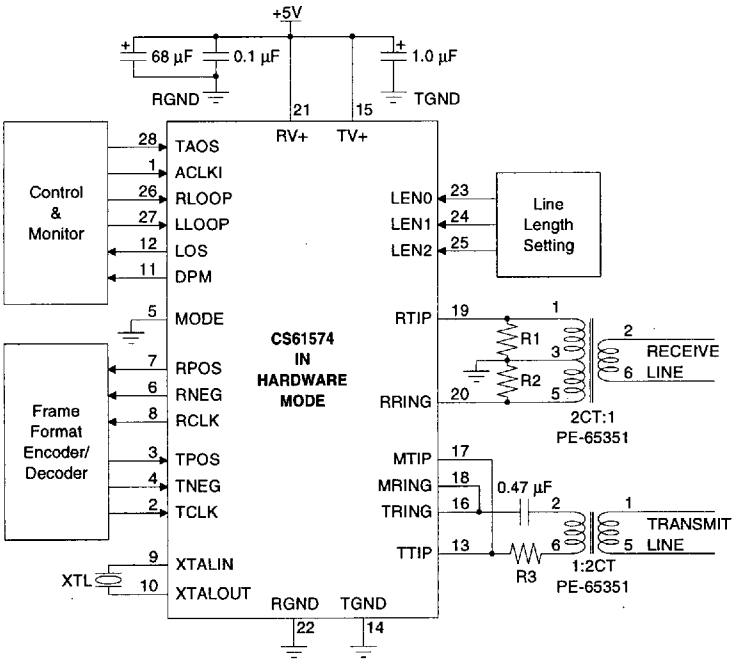


Figure A1. E1 Hardware Mode Configuration

Frequency MHz	Crystal XTL	Cable Ω	LEN2/1/0	R3 Ω	R1 and R2 Ω
1.544 (T1)	CXT6176	100	0/1/1 - 1/1/1	not used	200
2.048 (E1)	CXT8192	120	0/0/0	not used	240
		75	0/0/0	4.4	150

Table A1. External Component Values

Line Interface

Figures A1-A2 show typical T1 and E1 line interface application circuits. Table A1 shows the external components which are specific to each application. Figure A1 illustrates an E1 interface in the Host Mode. Figure A2 illustrates a T1 interface in the Hardware Mode.

The 1:2 receiver transformer has a grounded center tap on the IC side. Resistors R1 and R2 between the RTIP and RRING pins to ground provide the termination for the receive line. The transmitter also uses a 1:2 transformer. A 0.47 µF capacitor is required in series with the transmit transformer primary. This capacitor is needed to prevent any output stage imbalance from resulting in a DC current through the transformer primary. This current might saturate the transformer producing an output offset level shift.

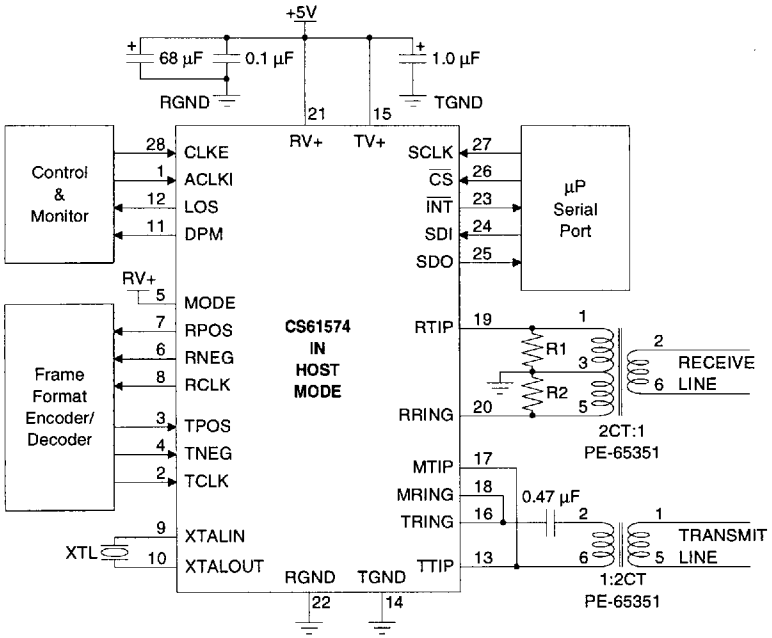


Figure A2. T1 Host Mode Configuration

Transformers

Recommended transmitter and receiver transformer specifications are shown in Table A2. The transformers in Table A3 have been tested and recommended for use with the CS61574. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

Turns Ratio	1:2 CT ± 5%
Primary Inductance	600 µH min. @ 772 kHz
Primary Leakage Inductance	1.3 µH max. @ 772 kHz
Secondary Leakage Inductance	0.4 µH max. @ 772 kHz
Interwinding Capacitance	23 pF max.
ET-constant	16 V-µs min. for T1 12 V-µs min. for E1

Table A2. Transformer Specifications

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the jitter attenuator. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for E1 applications.

Turns Ratio(s)	Manufacturer	Part Number	Package Type
1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
	Schott	67129300	
	Bel Fuse	0553-0013-HC	
dual 1:2CT	Pulse Engineering	PE-64951	1.5 kV through-hole, dual
	Bel Fuse	0553-0013-1J	
dual 1:2CT	Pulse Engineering	PE-65761	1.5 kVsurface-mount, dual
	Bel Fuse	S553-0013-03	
1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved

Table A3. Recommended Transformers

Transmit Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the signal to be transmitted. A CS61574 in local loopback mode can be used as a jitter attenuator. The inputs to the jitter attenuator are TPOS, TNEG, TCLK. The outputs from the jitter attenuator are RPOS, RNEG and RCLK.

Line Protection

Secondary protection components can be added to provide lightning surge and AC power-cross immunity. Refer to the application note "Secondary Line Protection for T1 and E1 Line Cards" for detailed information on the different electrical safety standards and specific application circuit recommendations.

Interfacing The CS61574 With the CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A3. In this case, the line interface and CS2180B are in host mode controlled by a microprocessor serial interface. If the line interface is used in Hardware Mode, then the line interface RCLK output must be inverted before being input to the CS2180B.

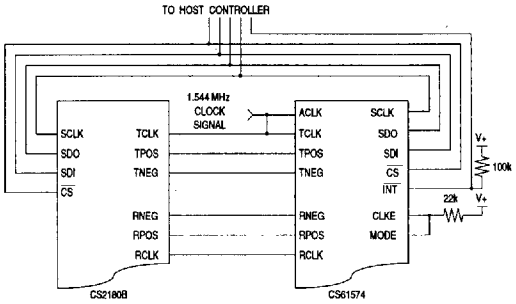


Figure A3. Interfacing the CS61574 with a CS2180B (Host Mode)