

CS6100

Motion JPEG Encoder



The CS6100 Motion JPEG (M-JPEG) Encoder is a highly integrated virtual component solution for leading-edge image compression and transmission applications. Its high performance is capable of sustaining data rates of over 180 mega-samples/sec¹ – delivering full motion, full color video images up to 4 megapixels². Equally suited to low-power, battery-operated consumer electronics as it is to high-end professional video equipment and office automation solutions, the CS6100 delivers the optimal performance and low power consumption that only an application specific virtual component (ASVC) can provide. The CS6100 is available in both ASIC and programmable logic versions that have been handcrafted by Amphion to deliver high performance with low-power and minimal silicon area.

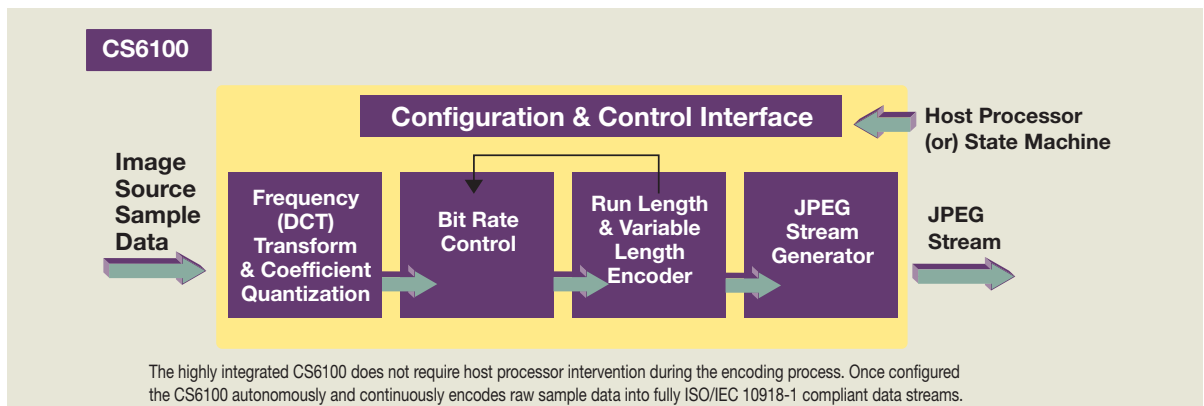


Figure 1: CS6100 Overview Diagram

FEATURES

- ◆ **High Performance >180 Msamples/s Encoding Capability¹**
 - Single sample per clock cycle processing
- ◆ **Low Power**
 - Fully synchronous operation
 - Zero-power standby mode³
- ◆ **Fully Compliant with Baseline JPEG Standard ISO/IEC 10918-1/2**
- ◆ **Autonomous Operation**
 - Sample data in, JPEG stream out
 - No host processor intervention required
- ◆ **Dual Mode Operation**
 - AutoMode™ continuous streaming mode
 - Variable image mode
- ◆ **Ease of Integration**
 - Tapeout-Ready™ Firm-IP targeted netlist
 - No code memory required
 - TestReady™ netlist configuration
- ◆ **Advanced Image Coding Features**
 - Four programmable quantization tables
 - Four programmable Huffman Coding Tables
 - Bit-rate control for dynamic output rate stabilization (patent pending)⁴
 - On-board configuration data memory

◆ Ease of Configuration

- State machine: synchronous handshake interface
- Host Processor: memory mapped interface capability
- Support for standard and abbreviated JPEG configuration formats
- AutoMode™ configure-once encode-many operation

◆ Flexible Image Source Input

- Image Size up to 65,535 by 65,535 (4.3 Gigapixel)
- All color formats including: RGB, YUV, YCbCr, CMYK and Grayscale
- Horizontal and vertical sub-sampled input supported
- Interleaved and non-interleaved scans supported

KEY METRICS

- ◆ **Logic:** 72K gates (std cell)
- ◆ **Memory:** 21.6K bits RAM (5 blocks)
- ◆ **Area:** < 1.6mm die area

APPLICATIONS

- ◆ **Digital Still Cameras:**
- ◆ **Remote Digital Video:**
- ◆ **Video Production:**
- ◆ **Office Automation Equipment:**
- ◆ **Handheld Scanners:**

1) Performance is dependent on the silicon process and libraries selected. 180MHz operation is representative of 0.18 micron silicon using standard cell libraries.
 2) 30 frame/sec, 24-bit color images with three components in 4:2:0 format.
 3) When implemented with fully static SRAM blocks w/power-down.
 4) US Patent Application No. 09/588,266

CS6100 FUNCTIONAL DESCRIPTION

The CS6100 ASVC is a highly integrated JPEG encoder suitable for a wide range of imaging applications. Designed for continuous data flow – one image sample per clock cycle – without host microprocessor intervention, the CS6100 can address the most demanding frame-based video compression applications. In addition, it is ideal for low power applications where – once configured – it can be stopped and restarted instantaneously. The fully synchronous, highly autonomous design requires no software overhead. A rich feature set includes an adaptive-feedback bit rate control (BRC) mechanism (patent pending), multiple real-time selectable coding tables, manual and automatic configuration modes and on-board configuration memory. The CS6100 is a powerful and flexible JPEG encoding solution.

FUNCTIONAL BLOCK OVERVIEW

Image source data in any color space format is input to the CS6100 in block data format. The CS6100 can process up to 255 color components in an unlimited number of scans per image (each scan can contain between one and four color components). The image samples are compressed according to user-definable quantization and Huffman coding parameters. Built-in bit rate control circuitry is selectively employed for bandwidth constrained applications. The CS6100 outputs an ISO/IEC 10918-1 compliant data stream. Separate configuration, parameter extraction and test access ports provide high visibility and flexible control for ease of integration of the CS6100 into the complete system-level ASIC design.

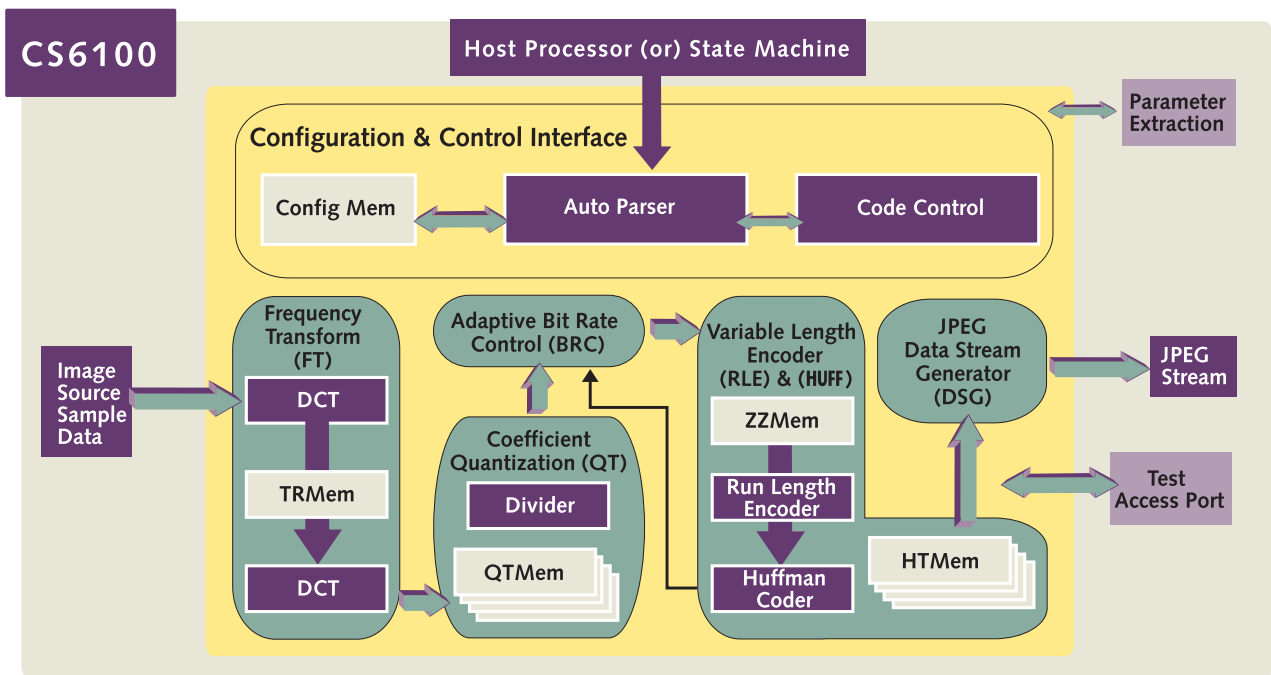


Figure 2: CS6100 JPEG Encoder block diagram

FREQUENCY TRANSFORM

The frequency transform (FT) unit accepts 64-byte (8 x 8) blocks of image sample data (raster order within the block) and converts these to 8 x 8 blocks of frequency coefficients using a 2D discrete cosine transform (DCT) architecture. This is implemented as two, 1D DCT operations, with the intermediate results being stored in the dual-port transpose memory (TRMem) buffer. The architecture of the FT unit allows for continuous one-sample per cycle operation with a latency between first sample in and first coefficient out of 72 clock cycles. The 11-bit coefficient data is streamed out from the FT unit for direct input to the quantization unit.

COEFFICIENT QUANTIZATION

The coefficient quantization unit (QT) divides each of the 64 DCT coefficients in an image sample block by the values specified in one of the four quantization tables stored in QTMem (each table contains 64 entries, one per coefficient). The purpose of the quantization process is to reduce the amplitude of the coefficients and to increase the number of zero value coefficients in preparation for the latter stages of the JPEG encoding process. The 11-bit DCT data is loaded into QT directly from the FT in column major order. The QT unit quantizes one sample per clock cycle with a latency between the first sample in and the first sample out of three clock cycles.

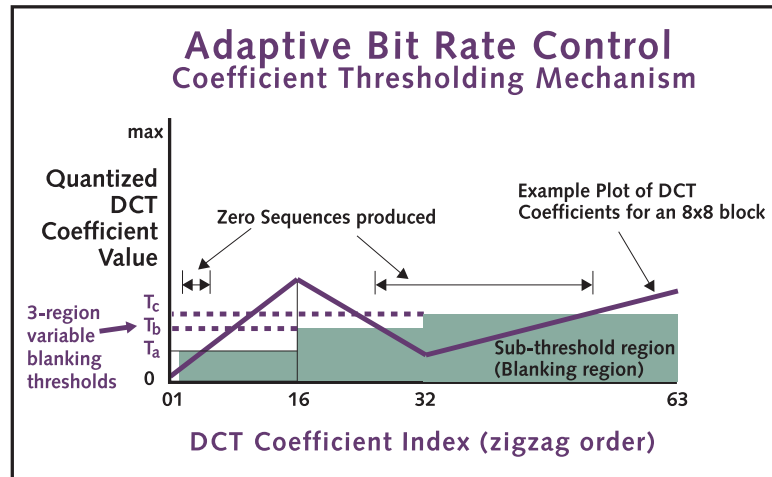


Figure 3: Bit Rate Control Illustration

ADAPTIVE BIT RATE CONTROL

The adaptive bit rate control unit (BRC) applies a coefficient thresholding technique for ensuring that the compressed image size does not exceed a user defined bandwidth budget. This particular feature of the CS6100 is essential for applications where the JPEG stream output from the CS6100 is to be transmitted over a bandwidth-constrained data channel. The BRC tracks the byte-count growth during the compression of an image via feedback from the Huffman encoder in the VLE block. The BRC adapts dynamically as the total image is processed, applying different rules to selectively remove (zero-out) coefficients in order to converge the actual compressed image size and the ideal size. Further details on the BRC mechanism are provided in the CS6100 Databook. The CS6100 BRC features are a significant advancement over the requirements set forth in the JPEG standard, yet the resultant output stream is 100% compliant with the standard and can be decoded by any standard-compliant JPEG decoder.

VARIABLE LENGTH CODER

The variable length encoding unit (VLE) consists of both the run length encoding unit (RLE) and the Huffman encoder (HUFF). Data output by the BRC is buffered in the ZigZag Memory (ZZMem) then loaded into the run length encoder (RLE) unit. The RLE compresses the data stream by converting the data to Run-Size pair data bytes. Huffman encoding techniques are then applied to the stream of Run-Size pairs to replace them with a corresponding code read from a look-up table stored in the Huffman Table memory (HTMem). Huffman codes are designed to be uniquely identifiable yet minimize the number of bits required to store all the Run-Size codes for an image. The CS6100 can store four user-defined Huffman Tables, two for DC coefficients and two for AC coefficients, the DC and AC coefficients being Huffman encoded separately. The compression produced by the VLE is data dependent thus latency can vary from one block to the next.

DATA STREAM GENERATOR

The data stream generator unit (DSG) accepts the Huffman encoded data stream from the VLE and packs the variable length words into double-byte words. The double-byte words are output over the JPEG output bus (JpgOut) when requested by the external system. Additionally, the DSG outputs JPEG file header information according to the parameters set during configuration and under control of the JPEG mask control port (JpgMask). The DSG also provides feedback to the BRC to enable the dynamic control of the compression should this feature be selected by the system. The latency of the DSG is variable and depends on the data received from the VLE. When the last data for a frame is received from the VLE, the double-byte word is padded out and is immediately available for output.

CONFIGURATION & CONTROL INTERFACE

The configuration and control interface unit (CCI) includes an AutoParser that interprets configuration data, a configuration memory (ConfigMem) for storing the full configuration stream for later use as part of the JPEG output stream, and a code control state machine (CodCtrl) that manages the operation of the CS6100.

SIGNAL	I/O	DESCRIPTION
CLK	Input	Clock-rising edge active
RSTn	Input	Asynchronous reset (power-on reset)
CLR	Input	Synchronous reset
CONFIGURATION PORT		
CfgIn[7:0]	Input	Configuration input port
CfgRdy	Output	Indicates that the CS6100 is ready to accept configuration data
CfgStrb	Input	Configuration input strobe
STATUS & CONTROL		
AutoAvail	Output	Indicates that AutoMode™ may be used
AutoStart	Input	Causes the CS6100 to enter AutoEncode state
InitProg	Output	Indicates that the CS6100 is currently initializing its internal memories
TblDef[7:0]	Output	Indicates number of tables defined. Bits[7:4] indicate Huffman Tables. Bits [3:0] indicate quantization tables, 1 bit/table
PValue[15:0]	Output	Encoding parameter bus
PType[3:0]	Input	Signal specifying parameters to be placed on port PValue
PValid	Output	Indicates valid coding parameters
SigSOS	Output	Indicates that a SOS segment has been input via CfgIn or has been read from the configuration memory and the CS6100 is about to start encoding a scan
EncFlags[7:0]	Output	CS6100 internal status and error flag status register
JPEG STREAM PORT		
JpgMask[4:0]	Input	JpgOut stream configuration port
JpgOut[15:0]	Output	JPEG output stream
JpgAvail	Output	Indicates that valid data is available on JpgOut
JpgNext	Input	Informs core to place next 16-bit word of output data onto JpgOut. Data held if JpgNext not asserted
JpgLast	Output	Indicates that the data on port JpgOut is the last one of an encoded JPEG data stream
JpgEnd	Output	Indicates that the last data of the encoded JPEG data stream has been output on port JpgOut
DATA SAMPLE INPUT PORT		
PixIn[7:0]	Input	Sample data input port
PixStrb	Input	Indicates the first pixel of an 8x8 block
PixRdy	Output	Indicates that the CS6100 is ready to accept data
ScanEnd	Input	Indicates that the current MCU row is the last one of the scan
TEST PORT		
TType	Input	Test type selector
TSOS	Output	Marks the first value in the first 8x8-output block of test data
TSOB	Output	Marks the first value in each 8x8-output block of test data
TData [10:0]	Output	11-bit output test data port – displays DCT coefficients or quantized coefficients
TValid	Output	Indicates valid test data output
TestEn	Input	Causes memories to be bypassed for test purposes

Table 1: I/O Signal Description.

MEMORY ELEMENTS

MEMORY BLOCK	CONFIGURATION (WORDS X BITS)	PORTS
Huffman Tables (HTMem)	384x20	Single Port, synchronous
Transpose Memory (TRMem)	64 x 15	Dual Port, synchronous
ZigZag Memory (ZZMem)	192 x 11	Dual Port, synchronous
Quantization Tables (QTMem)	512 x 8	Single Port, synchronous
Configuration Memory (CFMem)	840 x 8	Single port, synchronous

Table 2: Memory Block Size Information

CS6100 SYMBOL & PIN DESCRIPTION

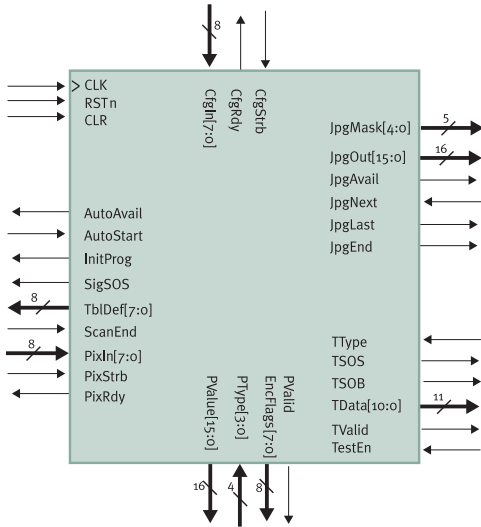


Figure 4: CS6100 Symbol

CS6100 OPERATION

The major operating modes and states of the CS6100 are shown in Figure 5.

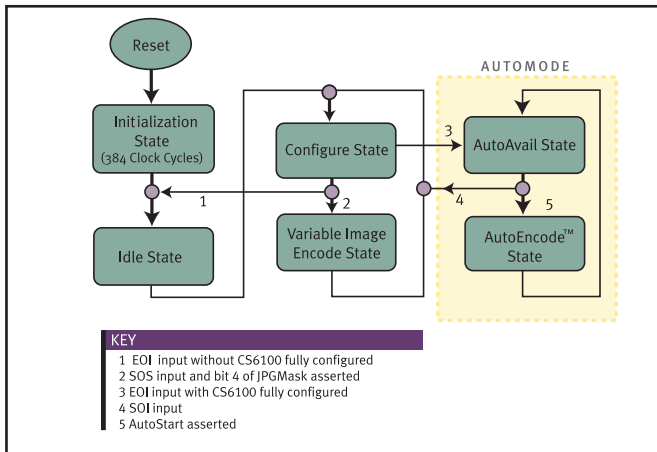


Figure 5: CS6100 Operation

MARKER	JPEG MARKER NAME	DESCRIPTION
SOI	Start of Image	Start of image marker 0xFFD8 indicates the start of a configuration stream
COM	Comment	Reserved for text fields
APPn	Application segment, n=0-F	Reserved for application use
DQT	Define quantization table(s)	Marker for input of quantization tables. Up to 4 tables may be defined.
DHT	Define Huffman Table(s)	Marker for definition of the Huffman Tables. Up to 4 tables may be defined
DRI	Define restart interval	Set to zero by default, this allows the image to be broken up into independently decodable segments
SOF0	Baseline frame definition	Defines frame parameters that apply to all scans within the frame. Includes number of components per frame, sampling factors, and which quantization table is to be used by each component
EOI	End of image	End of image marker indicates end of configuration data
SOS	Start of scan	Defines the parameters relating to each scan in the frame, including the number of components and the Huffman Tables to be associated with each component
DNL	Define number of lines	Used to redefine number of lines in image for use with ScanEnd signal. Main application is in handheld scanners

Table 3: JPEG Markers Supported for Configuration

CONFIGURATION OF THE CS6100

The CS6100 is configured via the Configuration Port using the standard JPEG markers listed in Table 3. Configuration can be performed either by a simple state machine, which streams data into the configuration port, or by a host system microprocessor. Refer to the CS6100 Databook for more details on the configuration process and the configuration memory.

Data presented to the Configuration Port is stored in the configuration memory of the CS6100. A full (standard) configuration is required after reset to load the quantization and

Huffman Tables. When variable image mode is utilized, abbreviated configuration streams can be employed to control compression of variable sized images or varying scans/image. Examples of both the abbreviated configuration and standard configuration streams are provided in the databook.

The CS6100 can also be configured to operate in AutoMode™ without any further configuration required for each image, therefore minimizing the interaction required from the system.

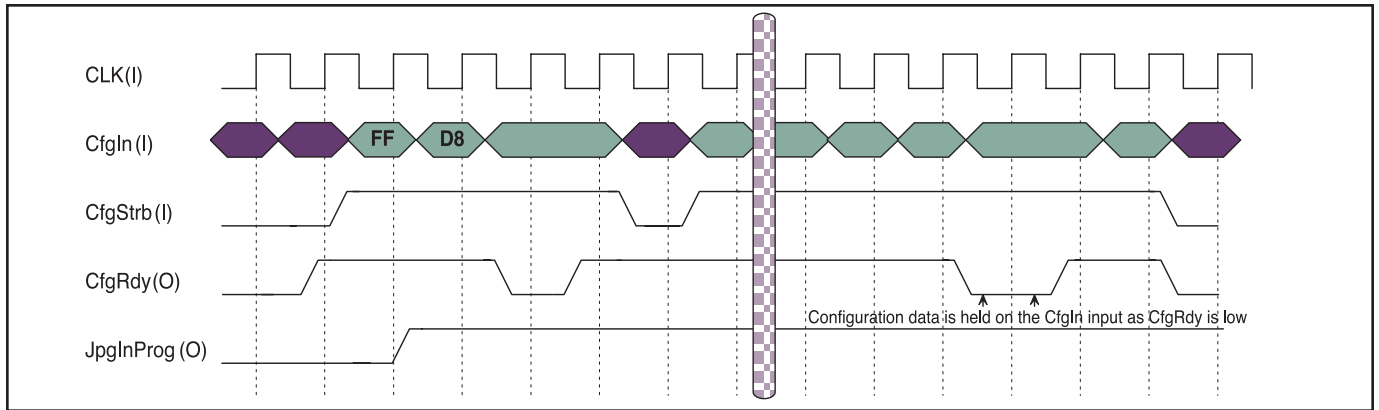


Figure 6: Configuration Stream Interface Timing

AUTOMODE™

For motion-JPEG applications like videoconferencing, the CS6100 AutoMode enables image sequences with the same characteristics to be quickly and easily encoded without the need for configuration data to be loaded for each image. In AutoMode, the CS6100 can run continuously without host system intervention. AutoMode allows the host to utilize its full bandwidth in carrying out other system functionality while the CS6100 autonomously delivers optimal JPEG encoding.

In AutoMode, the CS6100 alternates between two operating states: an AutoAvail idle state and the AutoEncode state. The AutoEncode state is reached when the AutoStart input signal is asserted. When an AutoEncode sequence is completed, the

JpgLast and JpgEnd flags are asserted as shown in Figure 7 and the CS6100 cycles back to the AutoAvail state. While in AutoMode the JPEG markers stored in the Configuration Memory are inserted into the output stream according to control inputs JpgMask.

VARIABLE IMAGE ENCODE MODE

For applications requiring changing or alternating image characteristics, the CS6100 can be configured to operate in Variable Image Encode Mode. Variable Image Encode is especially useful in scanner applications where the number of lines in the image is unknown at the start of the compression sequence.

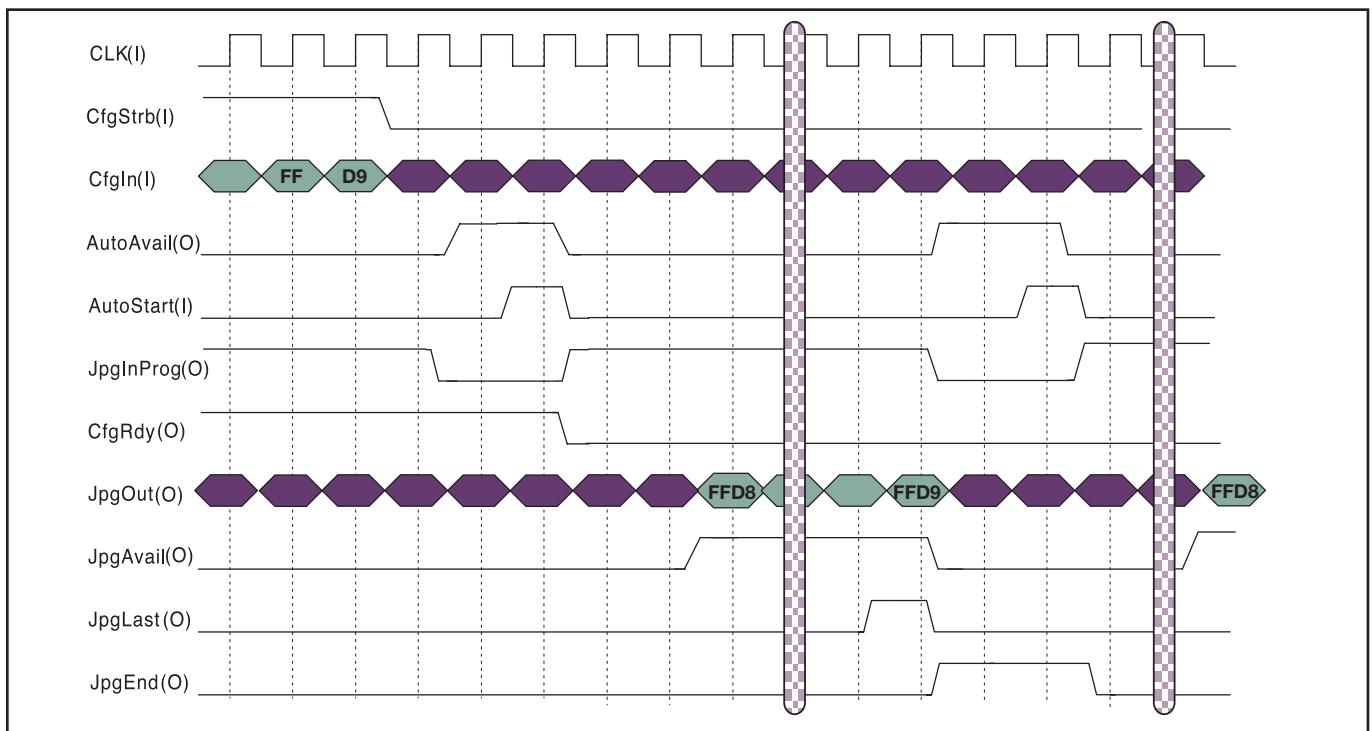


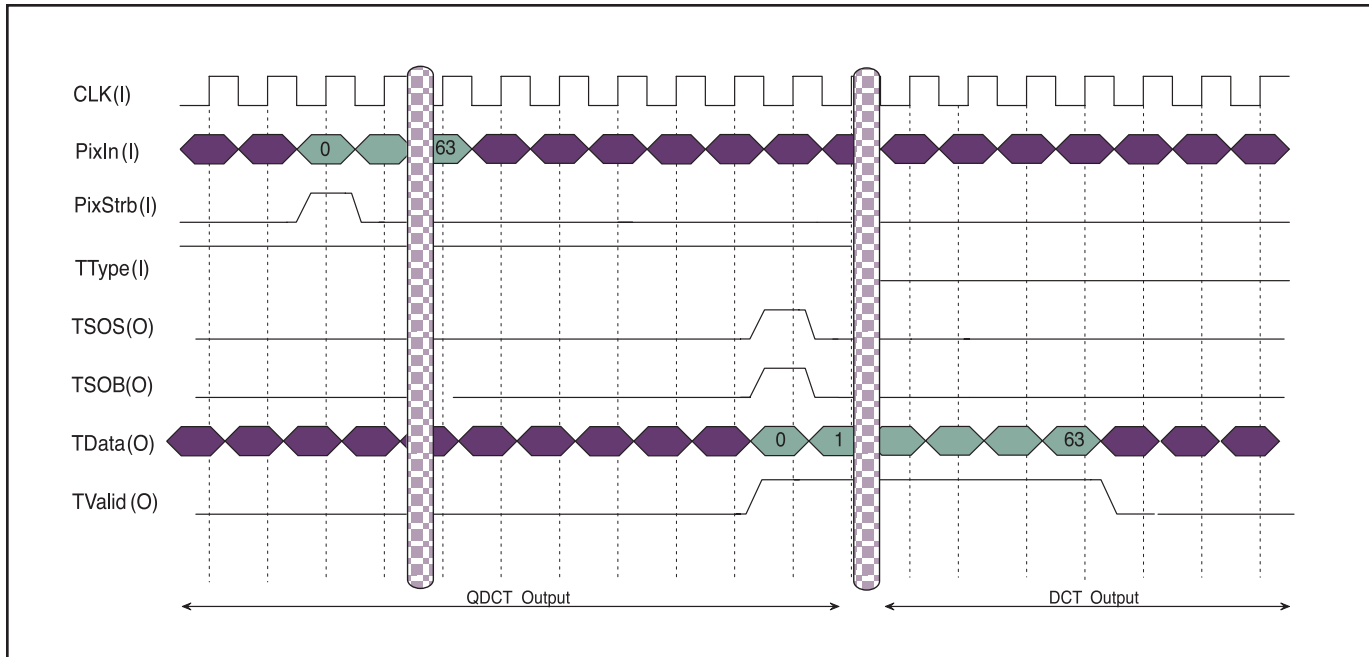
Figure 7: AutoMode Operational Timing

BUS AND PORT DEFINITION AND OPERATION

TEST DATA OUTPUT PORT

For diagnostic purposes the output test data port **TData**[10:0] enables either the DCT coefficients or the quantized DCT coefficients to be displayed, selected by the value of **TType**. The test port operates independently of the normal system

operation. Test data output is accompanied by two status signals [**TSOS**, **TSOB**] which indicate the first output byte of the first 8x8 block of the test data (**TSOS**) and the first output byte of each 8x8 block of test data (**TSOB**).



- **TType** = 0 specifies DCT coefficients, **TType** = 1 selects quantized DCT coefficients. Selectable on a cycle per cycle basis.
- **TSOS** is asserted for one cycle to indicate the first output byte of the first 8x8 block of the test data.
- **TSOB** is asserted for one cycle to indicate the first output byte of each 8x8 block of test data.
- **TValid** is asserted when valid test data is available on the TData output port.

Figure 8: Test Data Output Timing

ENCODING PARAMETER BUS

The encoding parameter bus (PValue[15:0]) is a 16-bit output port used to display configuration and status information stored within the CS6100 configuration memory. The 4-bit selector input PType[3:0] determines which internal parameters are displayed on the parameter bus per Table 4.

The data available on the PValue port does not contain control signals used by the CS6100. Many of the values, however, can be used to control other logic instantiated around the CS6100, i.e. the FX and FY parameters (PType 0x0 and 0x1) could be used to control a raster to block converter.

PType (Decimal Value)	PValue Output {bit position [15:0]}	DESCRIPTION
0	FY[15:0]:	FY Number of lines in frame
1	FX[15:0]	FX Number of lines in image
2	00_YMCU[13:0]	YMCU Number of MCUs in Y direction of current scan
3	00_XMCU[13:0]	XMCU Number of MCUs in X direction of current scan
4	Cs0[7:0]_Tq0[1:0]_V0[2:0]_H0[2:0]	Cs0 Identifier for the first scan component Tq0 Quantization table identifier for the first scan component V0 Vertical sampling factor for the first scan component. Values = 1-4 H0 Horizontal sampling factor for the first scan component. Values = 1-4
5	Cs1[7:0]_Tq1[1:0]_V1[2:0]_H1[2:0]	Cs1 Identifier for the second scan component Tq1 Quantization table identifier for the second scan component V1 Vertical sampling factor for the second scan component, undefined if NS (number of scans) < 2 H1 Horizontal sampling factor for the second scan component, undefined if NS < 2
6	Cs2[7:0]_Tq2[1:0]_V2[2:0]_H2[2:0]	Cs2 Identifier for the third scan component Tq2 Quantization table identifier for the third scan component V2 Vertical sampling factor for the third scan component, undefined if NS < 3 H2 Horizontal sampling factor for the third component, undefined if NS < 3
7	Cs3[7:0]_Tq3[1:0]_V3[2:0]_H3[2:0]	Cs3 Identifier of the fourth component Tq3 Quantization table identifier for the fourth scan component V3 Vertical sampling factor for the fourth scan component, undefined if NS < 4 H3 Horizontal sampling factor for the fourth scan component, undefined if NS < 4
8	CsH[15:0]	Cs3 Number of rows in current scan
9	CsV[15:0]	V3 Number of columns in current scan
10	DRI[15:0]	H3 Restart Interval
11	000_HMAX[2:0]_VMAX[2:0]_MCUBLK[3:0]_NS[2:0]	HMAX Maximal horizontal sampling factor in frame VMAX Maximal vertical sampling factor in frame MCUBLK Number of blocks per MCU of the current scan from 1-10 NS Number of scan components in current scan, 1-4
12	VHM3[3:0]_VHM2[3:0]_VHM1[3:0]_VHM0[3:0]	VHM0 Number of blocks of first component in MCU. Defined as $V0*H0$ where $V0$ and $H0$ are the vertical and horizontal sampling factors for the first scan component if $NS < 1$. Otherwise = 1 VHM1 $V0*H0 + V1*H1$, undefined when $NS < 2$ VHM2 $V0*H0 + V1*H1 + V2*H2$, undefined when $NS < 3$ VHM3 $V0*H0 + V1*H1 + V2*H2 + V3*H3$, undefined when $NS < 4$
13		Reserved
14		Reserved
15		Reserved

Table 4: Parameter Bus Definitions

STATUS REGISTERS

The status register flags (EncFlags[7:0]) indicate the current state of the CS6100 operation. When an error is detected during the coding process, the compression process is suspended and the CS6100 waits until a reset process is invoked by sig-

nal RSTn or CLR. The individual bits are set to zero at reset and active high to indicate an error condition as defined in Table 5:

BIT	NAME	DESCRIPTION
7	EncHfError	Set when an undefined Huffman table symbol is referenced during encoding
6	CtlError	<p>Set when an invalid SOF parameter is detected. This includes detecting:</p> <ul style="list-style-type: none"> • A sample precision which is not equal to 8-bit • The horizontal size of the image set to zero • The number of components in a frame set to zero • Any of the horizontal or vertical sampling ratios set to be greater than 5 • The quantization table ID greater than 3 <p>Set when an invalid SOS parameter is detected. This includes detecting:</p> <ul style="list-style-type: none"> • A reference to an undefined Huffman or quantization table • The number of components in a scan to be zero or more than 4 • More than 10 blocks in an MCU • Incorrect SOS fixed parameter settings (these should be as follows: Ss=0 Se=63 AhAl=0) <p>Set when EncFlags[7] is set</p> <p>Set when there is a mismatch between the DNL segment input to the core and the number of lines in the input image which have already been encoded</p>
5	HtError	<p>Set when an invalid DHT segment is detected. This includes detecting:</p> <ul style="list-style-type: none"> • An all one Huffman code • An invalid Huffman Table class (this should be '0' for DC tables and '1' for AC tables) • An invalid Huffman table identifier (this should be in the range 0 to 3) • The L value limit has been exceeded (this should be 12 for a DC table and 162 for an AC DC table)
4	QtError	<p>Set when an invalid DQT segment is detected. This includes detecting:</p> <ul style="list-style-type: none"> • A zero quantization coefficient • An invalid quantization level precision (this should be set to zero for baseline JPEG) • An invalid quantization table identifier (this should be in range 0 to 3)
3	EncError	<p>Set when the parser detects an error in the configuration stream</p> <p>Set when any of EncFlags[7:4] are set</p> <p>Set when any SOF marker is detected other than SOF0</p> <p>Set when anything other than a JPEG marker or the defined Bit Rate Control marker segment is input</p> <p>This includes the restart marker which should not be included in the configuration stream</p> <p>Set if incomplete Huffman or quantization definition is detected (Huffman/Quantization Table should be complete before the end of the configuration stream)</p>
2	PixInProg	Set when the first sample of the first 8x8 block is input into the core and de-asserted when the last pixel of last block of the scan is input
1	EnclnProg	<p>Set when encoding and de-asserted when encoding of scan is complete</p> <p>The signal is asserted after the SigSOS signal has been output and remains valid until the last Huffman code has been loaded into the data stream generator</p>
0	JpgInProg	Set when core starts to process input CfgIn and when it accepts AutoStart. De-asserted when encoding has been completed, i.e. when the EOI marker has been processed by the core

Table 5: Status Register Pin Definitions

JPEG MASK BUS

The configuration data present in the JPEG output stream is determined by setting the bit-wise value of the inputs JpgMask[4:0] according to Table 6.

DESIGN METHODOLOGY SUPPORT

Amphion's ASVCs support industry standard design flows. The process for integrating the CS6100 into a design flow is shown in the following diagram. Contact Amphion for information on compatibility of the deliverables with specific EDA tools.

BIT	CONFIGURATION DATA
4	SOF+SOS+ECD (entropy coded data)+RSTm
3	COM+APP
2	DRI
1	DQT
0	DHT

Table 6: JpgMask settings

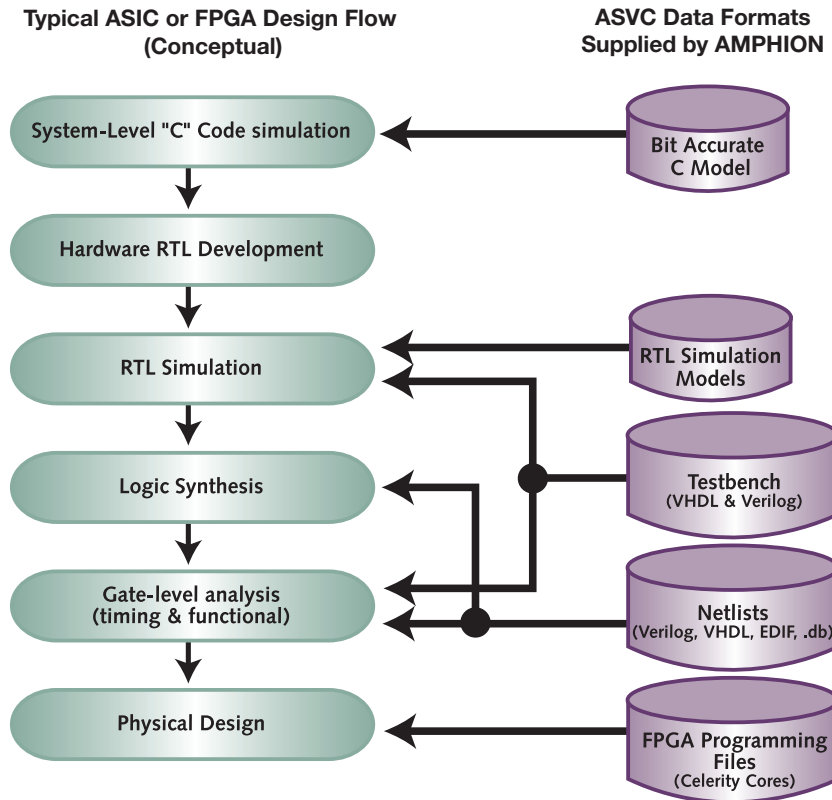


Figure 9: ASVC Design Data Formats Supplied by Amphion

TIMING CHARACTERISTICS

Most inputs and outputs to the CS6100 are registered and fully synchronous. Full pin descriptions and conditional timing behavior for non-registered pins are given in the CS6100 Databook. Example timing characteristics for the CS6100 are given in Table 7. Timing characteristics are technology dependent and will vary by instantiation as signal loading in the target system determines final timing.

SYMBOL	DESCRIPTION	CONDITION	VALUE	COMMENT
t_{cyc}	Clock cycle rate	Worst case	5.5 ns	
t_{su}	Input port set-up time	max	2.0 ns	Except CLR, JpgMask AutoStart, CfgIn, JpgNext, CfgStrb, PType, RSTn at 3.0 ns
t_h	Input port hold time	max	0.2 ns	Varies
t_{co}	Output port clock to output timing	max	2.0 ns	All registered outputs
t_{skew}	Clock skew	max	200 ps	Synthesis value, final skew is design dependent

CSO6100TK: All values reflect pre-layout estimated timing. Wireloading conditions use "Conservative" model supplied by library vendor and worst case commercial operating conditions.

Table 7: CS6100 Timing Characteristics

AVAILABILITY AND IMPLEMENTATION INFORMATION

OPTIMA™ CORES

For applications that require the high performance, low cost and high integration of an ASIC, Amphion delivers the Optima Cores series of multimedia ASVCs that are pre-optimized by Amphion experts to a targeted silicon technology. Choose from off-the-shelf versions of the CSO6100 available for many popular ASIC and foundry silicon supplier technologies, or Amphion can port the CSO6100 to a technology of your choice.

PRODUCT ID#	SILICON VENDOR	PRODUCT NAME/PROCESS	PERFORMANCE* (Msamples/sec)	LOGIC GATES**	MEMORY AREA	AVAILABILITY
CSO6100		Baseline JPEG Encoder – ASIC				Now
CSO6100TK	TSMC	0.18-micron using Artisan standard cell libraries	180	72k	0.52mm ²	Now
CSO6100KJ	Amkor	0.25-micron using Synopsys Odyssey standard cell libraries	140	73k	0.85mm ²	Now

* Performance figures based on silicon vendor design kit information. ASIC performance is pre-layout using vendor-provided statistical wire loading information, under the following conditions: ($T_J = 125^\circ\text{C}$, $V_{CC} -10\%$).

** Logic gates do not include clock circuitry.

Consult your local Amphion representative for product specific performance information, current availability of individual products, and lead times on Optima core porting.

Table 8: CS6100 Optima Cores

CELERITY™ CORES

For ASIC prototyping or for projects requiring the fast time to market of a programmable logic solution, Amphion's Celerity Core solutions offer the silicon-aware performance tuning found in all Amphion products, combined with the rapid design times offered by today's leading programmable logic solutions.

PRODUCT ID#	SILICON VENDOR	PROGRAMMABLE LOGIC PRODUCT	PERFORMANCE* (MSAMPLES/SEC)	DEVICE RESOURCES USED (LOGIC)	DEVICE RESOURCES USED (MEMORY)	AVAILABILITY
CSC6100AA	Altera	Apex 20KE FPGA	40	9200 LEs	17 ESB	Now
CSC6100XV	Xilinx	Virtex-E FPGA	45	4700 slices	8 block RAMs	Now

* Performance represents core only under worst case commercial conditions. Does not include timing effect of external logic and I/O circuitry.

Table 9: CS6100 Celerity Cores

THE PERFORMANCE ADVANTAGE OF AMPHION ASVCs

The performance and cost tradeoffs between general- and fixed-purpose solutions are substantial and the gap grows with every generation of silicon process technology. The difference between general-purpose solutions (microprocessor) and the intrinsic computational efficiency of silicon is nearly three orders of magnitude. This gap is the reason that Amphion fixed-purpose ASVCs deliver a ten to one thousand time improvement in performance when compared to conventional implementations using general-purpose, software-programmable DSP microprocessors.

Using proprietary techniques for direct-mapped implementations of digital signal processing functions and algorithms in hardware, Amphion's ASVCs provide a well-thought-out design approach that will continue to provide extraordinary performance advantages in the future, as well as time-to-market advantages, because they are off-the-shelf.

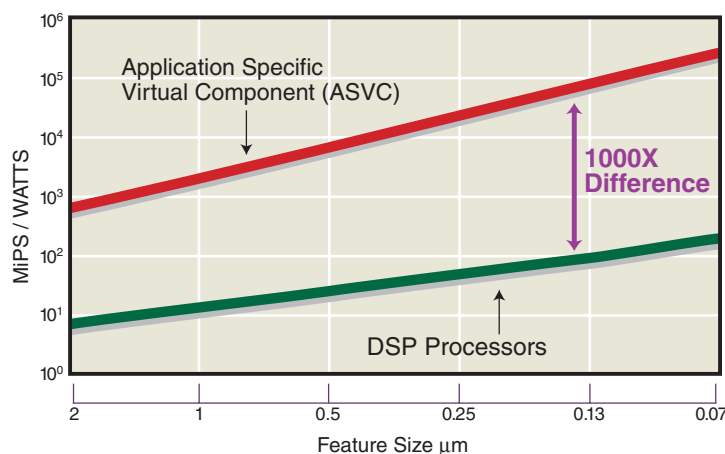


Figure 10: Amphion ASVCs Outperform DSPs by 1000X

Amphion continues to expand its family of ASVC solutions. See <http://www.amphion.com> for a current list of products.

ABOUT AMPHION

Amphion is the leading supplier of speech coding, video/image processing and channel coding ASVCs for system-on-a chip (SoC) solutions in the telecommunications/Internet, consumer/communications and wireless markets.

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SALES AGENTS

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