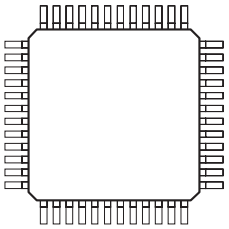
Automotive 3-Phase BLDC Controller and MOSFET Driver

Features and Benefits

- High current 3-phase gate drive for N-channel MOSFETs
- Synchronous rectification
- Cross-conduction protection
- Charge pump and top-off charge pump for 100% PWM
- Integrated commutation decoder logic
- Operation over 5.5 to 50 V supply voltage range
- Extensive diagnostics output
- Provides +5 V Hall sensor power
- Low-current sleep mode

Package: 48 Lead LQFP with exposed thermal pad (suffix JP)



Description

The A3930 and A3931 are 3-phase brushless dc (BLDC) motor controllers for use with N-channel external power MOSFETs. They incorporate much of the circuitry required to design a cost effective three-phase motor drive system, and have been specifically designed for automotive applications.

A key automotive requirement is functionality over a wide input supply range. A unique charge pump regulator provides adequate (>10 V) gate drive for battery voltages down to 7 V, and allows the device to operate with a reduced gate drive at battery voltages down to 5.5 V. Power dissipation in the charge pump is minimized by switching from a voltage doubling mode at low supply voltage to a dropout mode at the nominal running voltage of 14 V.

A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs. An internal charge pump for the high-side drive allows for dc (100% duty cycle) operation.

Internal fixed-frequency PWM current control circuitry can be used to regulate the maximum load current. The peak load current limit is set by the selection of an input reference voltage and external sensing resistor. The PWM frequency is set by a user-selected external RC timing network. For added flexibility, the PWM input can be used to provide speed and

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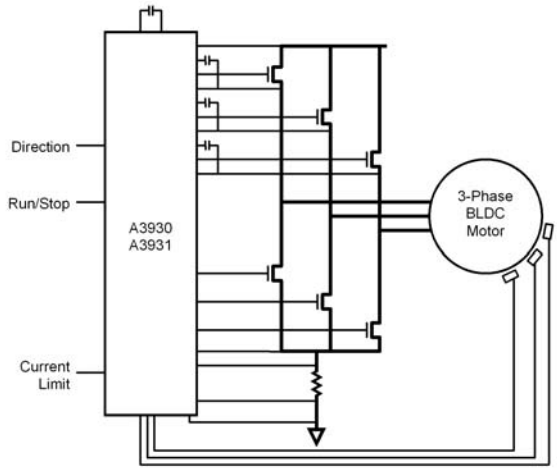
Typical Application



Description (continued)

torque control, allowing the internal current control circuit to set the maximum current limit.

Efficiency is enhanced by using synchronous rectification. The power FETs are protected from shoot-through by integrated crossover control with dead time. The dead time can be set by a single external resistor.

The A3930 and A3931 only differ in their response to the all-zero combination on the Hall inputs. In this state, the A3930 indicates a logic fault, but the A3931 prepositions the motor in an unstable starting position suitable for start-up algorithms in microprocessor-driven "sensor-less" control systems.

Both devices are supplied in a 48-pin LQFP with exposed thermal pad. This is a small footprint (81 mm^2) power package, that is lead (Pb) free, with 100% matte tin leadframe plating.

Selection Guide

Part Number	Option	Packing	Terminals	Package
A3930KJP-T	Hall short detection	250 pieces/tray	48	LQFP surface mount
A3931KJP-T	Prepositioning			

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Load Supply Voltage	V_{BB}	VBB pin	–0.3	–	50	V
Logic Input/Output Voltage	V_{RESET}	RESET pin input	–0.3	–	6	V
		Remaining logic pins	–0.3	–	7	V
Output Voltage Range	V_{GHx}	GHA, GHB, and GHC pins	V_{Sx}	–	V_{Sx}+ 15	V
	V_{GLx}	GLA, GLB, and GLC pins	–5	–	16	V
	V_{Cx}	CA, CB, and CC pins	–	–	V_{Sx}+ 15	V
	V_{Sx}	SA, SB, and SC pins	–5	–	45	V
		CSP, CSN, and LSS pins	–4	–	6.5	V
		CSO, VDSTH pins	–0.3		6.5	
		VDRAIN pin	–	–	55	V
Operating Temperature Range (K)	T_A		–40	–	135	°C
Junction Temperature	T_J		–	–	150	°C
Storage Temperature Range	T_S		–55	–	150	°C

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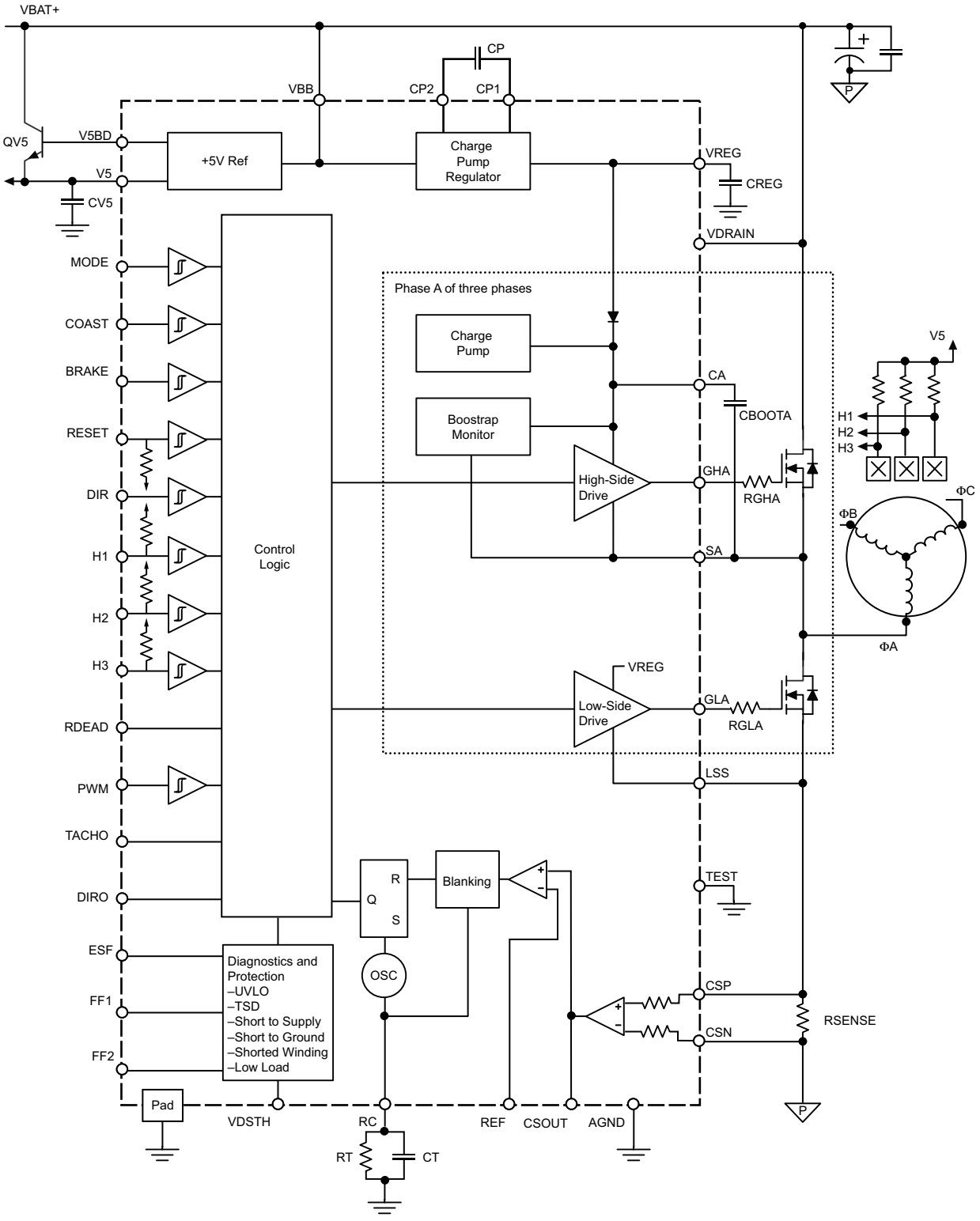
Functional Block Diagram



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ELECTRICAL CHARACTERISTICS at T_J = –40°C to 150°C, V_{BB} = 7 to 45 V, unless otherwise noted[1]

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply and Reference						
VBB Functional Operating Range[6]	V_{BB}	Function correct, parameters not guaranteed	5.5	–	50	V
VBB Quiescent Current	I_{BBQ}	RESET = High, outputs = Low	–	11	14	mA
	I_{BBS}	RESET = Low, sleep mode	–	–	10	µA
V5 Quiescent Current	I_{V5Q}	RESET = High, outputs = Low	–	–	5	mA
VREG Output Voltage	V_{REG}	V_{BB} > 7.5 V, I_{REG} = 0 to 15 mA	12.5	13	13.75	V
		6 V < V_{BB} < 7.5 V I_{REG} = 0 to 15 mA	2 × V_{BB} –2.5	–	–	V
		5.5 V < V_{BB} < 6 V, I_{REG} < 10 mA	9	10	–	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA	0.4	0.7	1.0	V
		I_D = 100 mA	1.5	2.2	2.8	V
Bootstrap Diode Resistance	r_D	$r_{D(100\ mA)} = (V_{fBOOT(150\ mA)} - V_{fBOOT(50\ mA)}) / 100\ mA$	6	10	20	Ω
Bootstrap Diode Current Limit	I_{DBOOT}		250	500	750	mA
Top-off Charge Pump Current Limit	I_{TOCPM}		–	200	–	µA
C*x* Top-off Charge Pump Source Current	I_{Cx}	V_{Cx}-V_{Sx} = 8 V, V_{BB} = 14 V, GHx = High	40	–	–	µA
V5 Output Voltage	V_5		4.75	5	5.25	V
V_{BE} of External Transistor QV5	V_{BEEXT}		–	–	1	V
V5BD Base Drive Capability for QV5[2]	I_{5BD}		–	–	–2	mA
Gate Output Drive						
Turn-On Rise Time	t_r	C_{LOAD} = 3300 pF, 20% to 80% points	–	60	–	ns
Turn-Off Fall Time	t_f	C_{LOAD} = 3300 pF, 80% to 20% points	–	40	–	ns
Pull-Up On Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GHx} = –150 mA	3	4	5	Ω
		T_J = 150°C, I_{GHx} = –150 mA	5	6	7	Ω
Pull-Down On Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GLx} = 150 mA	1	1.5	2	Ω
		T_J = 150°C, I_{GLx} = 150 mA	1.5	2.3	3	Ω
Short-Circuit Current – Source[2]	$I_{SC(source)}$	T_J = 25°C	–	–500	–	mA
Short-Circuit Current – Sink	$I_{SC(sink)}$	T_J = 25°C	–	850	–	mA
GH*x* Output Voltage	V_{GHx}	t_w < 10 µs Bootstrap capacitor fully charged	V_{Cx} – 0.2	–	–	V
GL*x* Output Voltage	V_{GLx}		V_{REG} – 0.2	–	–	V
Turn-Off Propagation Delay	$t_{p(off)}$	From input change to unloaded gate output change	–	90	150	ns
Dead Time (turn-off to turn-on delay)	t_{DEAD}	R_{DEAD} = 5 kΩ	–	180	–	ns
		R_{DEAD} = 50 kΩ	815	960	1110	ns
		R_{DEAD} = 400 kΩ	–	3.3	–	µs
		RDEAD = tied to V5	–	6	–	µs

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Logic Inputs and Outputs						
FFx Fault Output (Open Drain)	V_{OL}	I_{OL} = 1 mA, fault asserted	–	–	0.4	V
FFx Fault Output Leakage Current[2]	I_{OH}	V_O = 5 V, fault not asserted	–1	–	1	µA
TACHO and DIRO Output High Voltage	V_{OH}	I_{OH} = –1 mA	V_5 – 1 V	–	–	V
TACHO and DIRO Output Low Voltage	V_{OL}	I_{OL} = 1 mA	–	–	0.4	V
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage (Except RESET)	V_{IH}		2	–	–	V
RESET Input High Voltage	V_{IHR}		2.2	–	–	V
Input Hysteresis	V_{IHys}		300	500	–	mV
Input Current (Except H1, H2, H3, and RESET)[2]	I_{IN}		–1	–	1	µA
RESET Input Pull-Down Resistor	R_{PD}	V_{IN} = 5 V	–	50	–	kΩ
H*x* Input Pull-Up Resistor	R_{PU}	V_{IN} = 0 V	–	100	–	kΩ
Current Sense Differential Amplifier						
Input Bias Current[2]	I_{IBS}	CSP = CSN = 0 V	–95	–145	–205	µA
Input Offset Current[2]	I_{IOS}	CSP = CSN = 0 V	–20	–	20	µA
CSP Input Resistance	R_{CSP}	Measured with respect to AGND	–	80	–	kΩ
CSN Input Resistance	R_{CSN}	Measured with respect to AGND	–	4	–	kΩ
Differential Input Voltage	V_{ID}	V_{ID} = CSP – CSN, –1.3 V < CSP < 4 V, –1.3 V < CSN < 4 V	0	–	200	mV
Output Offset Voltage	V_{OOS}	CSP = CSN = 0 V	150	375	600	mV
Output Offset Voltage Drift	$V_{OOS(\Delta t)}$	CSP = CSN = 0 V	–	100	–	µV/°C
Input Common Mode Range	V_{CM}	CSP = CSN	–1.5	–	4	V
Differential Input Voltage Gain	A_V	40 mV < V_{ID} < 175 mV, V_{CM} in range	18.2	19	19.4	V/V
Low Output Voltage Error	V_{err}	0 < V_{ID} < 40 mV, $V_{CSOUT} = (19 \times V_{ID}) + V_{OOS} + V_{err}$	–20	–	20	mV
DC Common Mode Gain	A_{CMdc}	CSP = CSN = 200 mV	–	–30	–	dB
Source Resistance	r_{CSOUT}	V_{CSOUT} = 2.0 V, I_{CSOUT} = [TBD] µA	–	30	–	Ω
Output Dynamic Range	V_{CSOUT}	–100 µA < I_{CSOUT} < 100 µA	0.1	–	4.8	V
Output Current – Sink	$I_{CSOUT(sink)}$	V_{CSOUT}= 2 V ±5%	–	1	–	mA
Output Current – Source[2]	$I_{CSOUT(source)}$	V_{CSOUT}= 2 V ±5%	–	–19	–	mA
Supply Rejection	PSRR	CSP = CSN = AGND, 0 to 300 kHz	–	45	–	dB
Small Signal 3dB Bandwidth Frequency	f_{3dB}	V_{ID}=10 mVpp	–	1.6	–	MHz
Settling Time	t_{SETTLE}	To within 10%, V_{CSOUT} = 1 Vpp square wave	–	400	–	ns

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
AC Common Mode Gain	A_{CMac}	V_{ICR}= 250 mVpp, 0 to 1 MHz	–	–28	–	dB
Common Mode Recovery Time	t_{CMrec}	To within 100 mV, V_{ICR}= +4.1 to 0 V step	–	1	–	µs
Output Slew Rate	SR	10% to 90% points, V_{ID}= 0 to 175 mV step	–	20	–	V/µs
Input Overload Recovery Time	t_{IDREC}	To within 10%, V_{ID}=250 mV to 0 V step	–	500	–	ns
Current Limit						
Reference Comparator Input Offset Voltage	V_{IOC}		–15	0	15	mV
Reference Input Clamp Voltage	V_{REFC}	External pull-up to 5 V R_{REF} = 200 kΩ	3.8	4	4.2	V
Comparator Blank Time	t_{RC}	R_T= 56 kΩ, C_T = 470 pF	–	TBD	–	µs
REF Input Bias Current	I_{IBREF}		–	0	–	µA
RC Charge Current[2]	I_{RC}		–1.1	–1	–0.9	mA
RC HIgh Voltage Threshold	V_{RCH}		1.8	2.0	2.5	V
RC Low Voltage Threshold	V_{RCL}		0.6	0.7	0.8	V
Protection						
VREG Undervoltage Lockout	V_{REGUV}	V_{REG} rising	7.5	8	8.5	V
		V_{REG} falling	6.75	7.25	7.75	V
Bootstrap Capacitor Undervoltage Lockout	V_{BOOTUV}	V_{BOOT} falling, $V_{Cx} – V_{Sx}$	59	–	69	%
Bootstrap Capacitor Undervoltage Lockout Hysteresis	$V_{BOOTUVHys}$	$V_{BOOTUVHys}$ = %V_{REG}	–	13	–	%
V5 Undervoltage Lockout	V_{5UV}	V_5 falling	3.4	3.65	4.0	V
V5 Undervoltage Lockout Hysteresis	V_{5UVHys}		300	400	500	mV
VDSTH Input Voltage Range	V_{DSTH}		0.3		4	V
VDSTH Input Current[2]	I_{DSTH}		–1		1	µA
VDRAIN Input Voltage Range	V_{DRAIN}		7	V_{BB}	45	V
Short-to-Ground Threshold Offset[3,5]	V_{STGO}	V_{DSTH} > 1 V	–	±300	–	mV
		V_{DSTH} < 1 V	–150	–	150	mV
Short-to-Battery Threshold Offset[4,5]	V_{STBO}	V_{DSTH} > 1 V	–	±300	–	mV
		V_{DSTH} < 1 V	–150	–	150	mV
Low Load Current Detection Voltage	V_{CSOL}		–	500	–	mV
Overtemperature Flag	T_{JF}	Temperature increasing	–	165	–	ºC
Overtemperature Flag Hysteresis	T_{JFHys}	Recovery = T_{JF} – T_{JFHys}	–	15	–	ºC

[1]Parameters are tested at 135°C. Values at 150°C are guaranteed by design or correlation.
[2]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[3]High side on. As V_{SX} decreases, fault occurs if V_{BAT} -V_{SX}>V_{STG}
[4]Low side on. As V_{SX} increases, fault occurs if V_{SX} -V_{LSS}>V_{STB}
[5]V_{STG} threshold is V_{DTSTH} + V_{STGO}. V_{STB} threshold is V_{DTSTH}+V_{STBO}.
[6]Function is correct but parameters not guaranteed above or below general limits (7 to 45 V).

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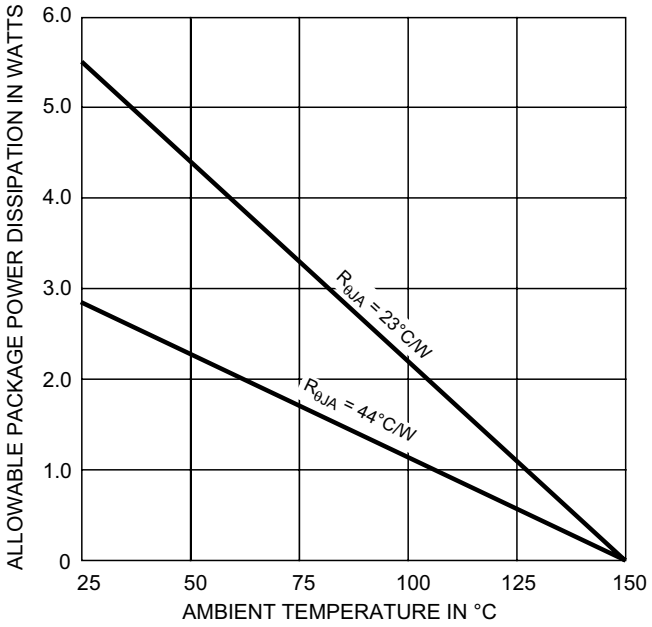
Thermal Characteristics

THERMAL CHARACTERISTICS may require derating at maximum conditions, see Applications Information section

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB, based on JEDEC standard	23	ºC/W
		2-layer PCB, with 3 in.^{2} of copper area each side connected by thermal vias	44	ºC/W
Die-to-Exposed Pad Thermal Resistance	$R_{\theta JP}$		2	ºC/W

*Additional thermal information available on Allegro Web site.

Power Dissipation verus Ambient Temperature



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Functional Description

Basic Operation

The A3930 and A3931 devices provide commutation and current control for 3-phase brushless dc (BLDC) motors with integrated Hall-effect (HE) sensors. The motor current is provided by an external 3-phase N-channel MOSFET bridge which is controlled by the A3930/A3931, using fixed-frequency pulse width modulation (PWM). The use of PWM with N-channel MOSFETs provides the most cost-effective solution for a high-efficiency motor drive.

The A3930/A3931 provides all the necessary circuits to ensure that the gate-source voltage of both high-side and low-side external MOSFETs are above 10 V, at supply voltages down to 7 V. For extreme battery voltage drop conditions, functional operation is guaranteed down to 5.5 V but with a reduced gate drive. The A3930/A3931 also decodes the commutation sequence from three HE sensors spaced at 120° in the electrical cycle, and ensure no cross-conduction (shoot through) in the external bridge. Individual pins provide direction, brake and coast control.

Motor current can be sensed by a low-value sense resistor, RSENSE, in the ground connection to the bridge, amplified and compared to a reference value. The A3930/A3931 then limits the bridge current on a cycle-by-cycle basis. Bridge current can also be controlled using an external PWM signal with the internal current control either disabled or used to set the absolute maximum motor current. Specific functions are described more fully in the following sections.

Power Supplies

Only one power connection is required because all internal circuits are powered by integrated regulators. The main power supply should be connected to VBB through a reverse battery protection circuit.

V5 and V5BD A 5 V supply for external pull-up and bias currents is provided by an integrated 5 V regulator controller and an external NPN transistor, QV5. The A3930/A3931 provides the base drive current on the V5BD pin, and the 5 V reference on the V5 pin. This regulator is also used by the internal logic circuits and must always be decoupled by at least a 200 nF capacitor, CV5, between the V5 pin and AGND. For stability, a 100 nF capacitor, C5BD, also should be connected between V5BD and AGND. If an external 5 V supply is not required, the V5BD pin and the V5 pin should be connected together.

CP1, CP2, and VREG The gate drive outputs are powered by an internal charge pump, which requires a pump capacitor, typically 470 nF, CP, connected between the CP1 and CP2 pins. The output from the charge pump, 13 V nominal, is used to power each of the three high- and low-side driver pairs and is also available on the VREG pin. A sufficiently large storage capacitor, CREG, must be connected to this pin to provide the transient charging current to the low-side drivers. The charge pump also provides the charging current for the bootstrap capacitors, CBOOT*x*.

An additional “top-off” charge pump is provided for each high-side drive which allows the high-side drive to maintain the gate voltage on the external FET indefinitely, ensuring so-called 100% PWM if required. This is a low-current trickle charge pump (< 100 µA typical), and is only operated after a high-side driver has been signaled to turn on. There is a small amount of bias current (<20 µA) drawn from the C*x* pin to operate the floating high-side circuit, and the charge pump simply provides enough drive to ensure that the bootstrap voltage, and hence the gate voltage, will not droop due to this bias current. The charge required for initial turn-on of the high-side gate is always supplied by bootstrap capacitor charge cycles.

Hall Effect Sensor Inputs

H1, H2, and H3 Hall-effect sensor inputs are configured for motors with 120° electrically-spaced HE sensors, but may be used for 60° electrical spacing with an external inverter. HE sensors usually require an additional pull-up resistor to be connected between the sensor output and 5 V. This 5 V can be provided by the integrated 5 V regulator. HE inputs have a hysteresis of typically 500 mV to reduce the effects of switching noise on the HE connections to the motor. These inputs are also filtered to further reduce the effects of switching noise. The HE inputs are pulled-up to 5 V inside the A3930/A3931 through a high value (100 kΩ typical) resistor in series with a diode. This internal pull-up makes the HE input appear high if the Hall sensor signal is missing, allowing detection of an HE input logic fault.

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In order to provide a known start-up position for the motor, an optional prepositioning function is available in the A3931. When the Hall inputs are all driven low (H1 = H2 = H3 = 0), the power FETs in the A phase source current from the supply, and those in both the B and C phases sink current. This forces the motor to move to an unstable position midway between two detent points and allows any start-up algorithm to ensure correct initial direction of rotation. Note that this is only available in the A3931. The A3930 will indicate a logic fault when all Hall inputs are driven low. The commutation truth table for these inputs is shown in table 3. The inputs can also be driven directly from a microcontroller or similar external circuit.

Gate Drive

The A3930/A3931 is designed to drive external N-channel power MOSFETs. They supply the large transient currents necessary to quickly charge and discharge the gate capacitance of the external FETs in order to reduce dissipation in the external FETs during switching. The charge and discharge rate can be controlled using external resistors in series with the connections to the gate of the FETs.

RDEAD Cross-conduction is prevented by the gate drive circuits which introduce a dead time, t_{DEAD}, between switching one FET off and the complementary FET on. The dead time is derived from the value of a resistor, RDEAD, connected between the RDEAD pin and AGND. If RDEAD is connected to V5, t_{DEAD} defaults to 6 µs typical.

GLA, GLB, and GLC Low-side gate drive outputs for external NMOS drivers. External series-gate resistors, RGATE, (as close as possible to the NMOS gate) can be used to control the slew rate seen at the power-driver gate, thereby controlling the *di*/*dt* and *dv*/*dt* of the S*x* outputs. Referring to table 3, *GLx = 1* (high) means that the upper half (PMOS) of the driver is turned on, and that its drain will source current to the gate of the low-side FET in the external motor-driving bridge. *GLx = 0* (low) means that the lower half (NMOS) of the driver is turned on, and that its drain will sink current from the corresponding external FET gate circuit to the LSS pin.

SA, SB, and SC Directly connected to the motor, these terminals sense the voltages switched across the load. These terminals are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drivers. The discharge current from the high-side FET gate capacitance flows through these connections, which should have low-impedance traces to the FET bridge.

GHA, GHB, and GHC High-side gate drive outputs for external NMOS drivers. External series-gate resistors, RGATE, can be used to control the slew rate seen at the power-driver gate, thereby controlling the *di*/*dt* and *dv*/*dt* of the S*x* inputs. Referring to table 3, *GHx = 1* (high) means that the upper half (PMOS) of the driver is turned on, and that its drain will source current to the gate of the high-side FET in the external motor-driving bridge. *GHx = 0* (low) means that the lower half (NMOS) of the driver is turned on, and that its drain will sink current from the corresponding external FET gate circuit to the respective S*x* pin.

CA, CB, and CC High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers. The bootstrap capacitors, CBOOT*x*, are charged to approximately V_{REG} when the corresponding S*x* terminal is low. When the S*x* output swings high, the voltage on the C*x* pin rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs.

VDRAIN High impedance sense input (Kelvin connection) to the top of the external FET bridge. This input allows accurate measurement of the voltage at the drain of the high-side FETs and should be connected directly to the bridge, close to the drain connections of the high-side FETs, with an independent trace.

LSS Low-side return path for discharge of the gate capacitors. It is connected to the common sources of the low-side external FETs through an independent low-impedance trace.

Logic Control Inputs

Additional logic-level inputs are provided to enable specific features described below. These logic inputs all have a nominal hysteresis of 500 mV to improve noise performance.

RESET Allows minimum current consumption from the VBB supply. When RESET is low, all internal circuitry is disabled including the V5 output. When coming out of sleep state, the protection logic ensures that the gate drive outputs are off until the charge pump reaches proper operating conditions. The charge pump stabilizes in approximately 3 ms under nominal conditions.

RESET has an internal pull-down resistor, 50 kΩ typical. However, to allow the A3930/A3931 to start-up without the need for an external logic input, the RESET pin can be pulled to the battery voltage with an external pull-up resistor. Because RESET also has an internal clamp diode, 6 V typical, to limit the input current, the value of the external pull-up resistor should be

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greater than 20 kΩ. The upper limit for the resistor must be low enough to ensure that the input voltage reaches the input high threshold, V_{INR}.

COAST An active-low input which turns all FETs off without disabling the supplies or control logic. This allows the external FETs and the motor to be protected in case of a short circuit.

MODE Sets the current-decay method. Referring to table 4, when in slow-decay mode, *MODE = 1*, only the high-side MOSFET is switched off during a PWM-off cycle. In the fast-decay mode, *MODE = 0*, the device switches both the high-side and low-side MOSFETs.

Slow decay allows a lower ripple current in the motor at the PWM frequency, but reduces the dynamic response of the current control. It is suitable for motors which run at a more-or-less constant speed. Fast decay provides improved current-control dynamic response, but increases the motor current ripple. It is suitable for motors used in start-stop and positioning applications.

DIR Determines the direction of motor torque output, as shown in table 3. For an unloaded, low-inertia motor, this will also usually be the direction of mechanical rotation. With a motor that has a high inertial load, the DIR input can be used to apply a controlled breaking torque, when fast decay is used (MODE = 0).

BRAKE An active-low input that provides a braking function. When BRAKE = 0 (see table 4), all the low-side FETs are turned on and the high-side FETs are turned off. This effectively short-circuits the back EMF in the windings, and brakes the motor. The braking torque applied depends on the speed. RESET = 0 or COAST = 0 overrides BRAKE and coasts the motor. Note that when BRAKE is used to dynamically brake the motor, the windings are shorted with no control over the winding current.

ESF The state of the enable stop on fault (ESF) pin determines the action taken when a short is detected. See the Diagnostics section for details.

TEST Test is for Allegro production use and must be connected to AGND.

Current Regulation

Load current can be regulated by an internal fixed frequency PWM control circuit or by external input on the PWM pin.

Current Sense Amplifier: CSP, CSN, and CSOUT A differential current sense amplifier with a gain, A_V, of 19 typical, is provided to allow the use of low-value sense resistors or current shunts as the current sensing elements. Because the output of this sense amplifier is available at CSOUT, it can be used for either internal or external current sensing. With the sense resistor, RSENSE, connected between CSP and CSN, the output of the sense amplifier will be approximately:

$$V_{CSOUT} \approx (I_{LOAD} \times A_V \times R_{SENSE}) + V_{OOS} ,$$

where V_{OOS} is the output offset voltage (the voltage at zero load current), and A_V is the differential voltage gain of the sense amplifier, 19 typical.

Internal Current Control: REF A fixed reference voltage can be applied to provide a maximum current limit. A variable reference voltage will provide a variable torque control. The output voltage of the current sense differential amplifier, V_{CSOUT}, is compared to the reference voltage available on the REF pin. When the outputs of the MOSFETs are turned on, current increases in the motor winding until it reaches a trip point value, I_{TRIP}, given by:

$$I_{TRIP} = (V_{REF} - V_{OOS}) / (R_{SENSE} \times A_V) .$$

At the trip point, the sense comparator resets the source enable latch, turning off the source driver. At this point, load inductance causes the current to recirculate until the start of the next PWM period.

The current path during recirculation is determined by the configuration of the MODE pin. Torque control can therefore be implemented by varying the voltage on the REF pin, provided that the PWM input remains high. If direct control of the torque or current by PWM input is desired, a voltage can be applied to the REF pin to set an absolute maximum current limit. The REF input is internally limited to 4 V, which allows the use of a simple pull-up resistor to V5, RREF, to set the maximum reference voltage, avoiding the need for an externally generated reference voltage. RREF should have a value between 20 kΩ and 200 kΩ.

Internal PWM Frequency The internal oscillator frequency, f_{OSC}, is determined by an external resistor, RT, and capacitor, CT, connected in parallel from the RC pin to AGND. The frequency is approximately:

$$f_{OSC} \approx 1 / (R_T C_T + t_{BLANK} + t_{DEAD}) .$$

where f_{OSC} in the range 20 to 50 kHz.

PWM Input Can be used to control the motor torque by an external control circuit signal on the PWM pin. Referring to table 4, when PWM = 0, the selected drivers are turned off and the load inductance causes the current to recirculate. The current path during recirculation is determined by the configuration of the MODE pin. Setting PWM = 1 will turn on selected drivers as determined by the H*x* input logic (see table 3). Holding PWM=1 allows speed and torque control solely by the internal current-limit circuit, using the voltage on the REF pin.

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In some circumstances, it may be desirable to completely disable the internal PWM control. This can be done by pulling the RC pin directly to AGND. This will disable the internal PWM oscillator and ensure that the output of the PWM latch is always high.

Blank Time When the source driver is turned on, a current spike occurs due to the reverse-recovery currents of the clamp diodes and switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source enable latch, the current-control comparator output is blanked for a short period of time, t_{BLANK}, when the source driver is turned on.

The length of t_{BLANK} is different for internal versus external PWM. It is set by the value of the timing capacitor, CT, according to the following formulas:

for internal PWM: t_{BLANK} (µs) = 1260 × C_T (µF), and

for external PWM: t_{BLANK} (µs) = 2000 × C_T (µF) .

A nominal C_T value of 680 pF yields a t_{BLANK} of 1.3 µs for external PWM, and 860 ns for internal PWM. The user must ensure that C_T is large enough to cover the current spike duration when using the internal sense amplifier.

Diagnostics

Several diagnostic features integrated into the A3930/A3931 provide speed and direction feedback and indications of fault conditions.

TACHO and DIRO These outputs provide speed and direction information based on the HE inputs from the motor. As shown in figure 1, at each commutation point, the TACHO output changes state independent of motor direction. The DIRO output is updated at each commutation point to show the motor direction. When the motor is rotating in the "forward" or positive direction, DIRO will be high. When rotation is in the "reverse" or negative direction, DIRO will be low. The actual direction of rotation is determined from the sequence of the three Hall inputs, Hx. Forward is when the sequence follows table 3 top-to-bottom and reverse when the sequence follows table 3 bottom-to-top.

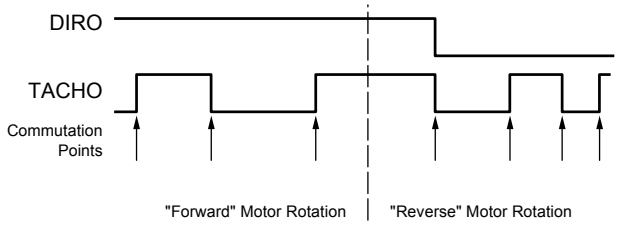

Figure 1. Direction Indication Outputs

Note that there are some circumstances in which the direction reported on the DIRO output pin and the direction demanded on the DIR input pin may not be the same. This may happen if the motor and load have reasonably high inertia. In this case, changing the state of the DIR pin will cause the torque to reverse, braking the motor. During this braking, the direction indicated on the DIRO output will not change.

ESF The state of the enable stop on fault (ESF) pin will determine the action taken when a short is detected. For other fault conditions, the action is defined by the type of fault. The action taken follows the states shown in table 2.

When ESF = 1, any short fault condition will disable all the gate drive outputs and coast the motor. This disabled state will be latched until the next phase commutation or until COAST or RESET go low.

When ESF = 0, under most conditions, although the fault flags, FF1 and FF2, are still activated, the A3930/A3931will not disrupt normal operation and will therefore not protect the motor or the drive circuit from damage. It is imperative that the master control circuit or an external circuit take any necessary action when a fault occurs, to prevent damage to components.

If desired, the active low COAST input can be used as a crude disable circuit by connecting the fault flags FF1 and FF2 to the COAST input and a pull-up resistor to V5.

FF1, FF2, and VDSTH Fault conditions are indicated by the state of two open drain output fault flags, FF1 and FF2, as shown in table 1. In addition to internal temperature, voltage, and logic monitoring, the A3930/A3931 monitors the state of the external MOSFETs and the motor current to determine if short circuit faults occur or a low load condition exists. In the event that two or more faults are detected simultaneously, the state of the fault flags will be determined by a logical AND of the fault states of each flag.

- **Undervoltage** VREG supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the voltages are sufficiently high before enabling any of the outputs. The undervoltage circuit is active during power-up, and will pull both fault flags low and coast the motor (all gate drives low) until V_{REG} is greater than approximately 8 V. Note that this is sufficient to turn on the external power FETs at a battery voltage as low as 5.5 V, but will not normally provide the rated on-resistance of the FET. This could lead to excessive power dissipation in the external FET.

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In addition to a monitor on VREG, the A3930/A3931 also monitors both the bootstrap charge voltage, to ensure sufficient high-side drive, and the 5 V reference voltage at V5, to ensure correct logical operation. If either of these fall below the lock-out voltage level, the fault flags are set.

- **Overtemperature** This event pulls both fault flags low but does not disable any circuitry. It is left to the user to turn off the device to prevent overtemperature damage to the chip and unpredictable device operation.
- **Logic Fault: Hall Invalid** The A3930 and the A3931 differ slightly in how they handle error conditions on the Hall inputs, H*x*. When all H*x* are 1s, both devices evaluate this as an illegal code, and they pull both fault flags, FF*x*, low and coast the motor. This action can be used, if desired, to disable all FET drives under bridge or motor fault conditions. The Hall logic fault condition is not latched, so if the fault occurs while the motor is running, the external FETs will be reenabled, according to the commutation truth table (table 3), when the H*x* inputs become valid.

  When all H*x* are 0s, the A3930 handles this in the same manner as all 1s, described in the preceding paragraph. The A3931, however, evaluates this as a prepositioning code, and does not register it as a fault.

  The H*x* inputs have pull-up resistors to ensure that a fault condition will be indicated in the event of an open connection to a Hall sensor.
- **Short to Ground** A short from any of the motor phase connections to ground is detected by monitoring the voltage across the top FETs in each phase using the appropriate S*x* pin and the voltage at VDRAIN. This drain-source voltage is then compared to the voltage on the VDSTH pin. If the drain source voltage exceeds the voltage at the VDSTH pin, FF2 will be pulled low.
- **Short to Supply** A short from any of the motor phase connections to the battery or VBB connection is detected by monitoring the voltage across the bottom FETs in each phase using the appropriate S*x* pin and the LSS pin. This drain-source voltage is then compared to the voltage on the VDSTH pin. If the drain source voltage exceeds the voltage at the VDSTH pin, FF2 will be pulled low.
- **Shorted Motor Winding** A short across the motor phase winding is detected by monitoring the voltage across both the top and bottom FETs in each phase. This fault will pull FF2 low.
- **Low Load Current** The sense amplifier output is monitored independently to allow detection of a low load current. This can be used to detect if an open load condition is present. If, during a commutation period, the output from the sense amplifier does not go above a minimum value, V_{CSOL}, FF1 will go low. No further action will be taken.

Short Fault Operation Because motor capacitance may cause the measured voltages to show a fault as the phase switches, the voltages are not sampled until one t_{DEAD} interval after the external FET is turned on.

If a short circuit fault occurs when ESF = 0, the external FETs are not disabled by the A3930/A3931. Under some conditions, some measure of protection will be provided by the internal current limit but in many cases, particularly for a short to ground, the current limit will provide no protection for the external FETs. To limit any damage to the external FETs or the motor, the A3930/A3931 can either be fully disabled by the RESET input or all FETs can be switched off by pulling the COAST input low. Alternatively, setting ESF = 1 will allow the A3930/A3931 to disable the outputs as soon as the fault is detected. The fault will be latched until any of the following conditions occur:

- a phase commutation
- RESET goes low
- COAST goes low

This will allow a running motor to coast to the next phase commutation without the risk of damage to the external power MOSFETs.

Low Load Current Fault Operation No action is taken for a low load current condition. If the low load occurs due to an open circuit on a phase connection while the motor is running, the A3930/A3931 will continue to commutate the motor phases according to the commutation truth table, table 3.

In some cases, this will allow the motor to continue operating at a much reduced performance. The low load condition is checked during a commutation period and is only flagged at the next commutation event. The flag is cleared at the end of any subsequent-commutation period where no low load current fault is detected.

If the motor stalls or is stationary, then the remaining phase connections will usually be insufficient to start rotating the motor. At start-up or after a reset, the low load condition is flagged until the first time the motor current exceeds the threshold value, V_{CSOL}. This allows detection of a possible open phase from startup, even if the motor is not able to start running.

Note that a low load current condition can also exist if the motor being driven has no mechanical load.

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Table 1. Fault Action Table

FF1	FF2	Fault	Action*	
			ESF = 0	ESF = 1
0	0	Undervoltage	Disable	Disable
0	0	Overtemperature	No Action	No Action
0	0	Logic Fault	Disable	Disable
1	0	Short to ground	No Action	Disable
1	0	Short to supply	No Action	Disable
1	0	Shorted motor winding	No Action	Disable
0	1	Low load current	No Action	No Action
1	1	None	No Action	No Action

**Disable* indicates that all gate outputs are low and all MOSFETs are turned off.

Table 2. Commutation Truth Table*

Device	H1	H2	H3	DIR	GLA	GLB	GLC	GHA	GHB	GHC	SA	SB	SC
Both	1	0	1	1	0	0	1	1	0	0	High	Z	Low
Both	1	0	0	1	0	0	1	0	1	0	Z	High	Low
Both	1	1	0	1	1	0	0	0	1	0	Low	High	Z
Both	0	1	0	1	1	0	0	0	0	1	Low	Z	High
Both	0	1	1	1	0	1	0	0	0	1	Z	Low	High
Both	0	0	1	1	0	1	0	1	0	0	High	Low	Z
A3930	0	0	0	X	0	0	0	0	0	0	Z	Z	Z
A3931	0	0	0	X	0	1	1	1	0	0	High	Low	Low
Both	1	1	1	X	0	0	0	0	0	0	Z	Z	Z
Both	1	0	1	0	1	0	0	0	0	1	Low	Z	High
Both	1	0	0	0	0	1	0	0	0	1	Z	Low	High
Both	1	1	0	0	0	1	0	1	0	0	High	Low	Z
Both	0	1	0	0	0	0	1	1	0	0	High	Z	Low
Both	0	1	1	0	0	0	1	0	1	0	Z	High	Low
Both	0	0	1	0	1	0	0	0	1	0	Low	High	Z

*X indicates “don’t care,” Z indicates high impedance state

Table 3. INPUT LOGIC

MODE	PWM	BRAKE	COAST	RESET	Decay	Mode of Operation
0	0	1	1	1	Fast	PWM chop – current decay with opposite of selected drivers ON
0	1	1	1	1	Fast	Peak current limit – selected drivers ON
1	0	1	1	1	Slow	PWM chop – current decay with both low-side drivers ON
1	1	1	1	1	Slow	Peak current limit – selected drivers ON
X	X	0	1	1	n/a	Brake mode - All low-side gates ON
X	X	X	0	1	X	Coast mode - All gates OFF
X	X	X	X	0	X	Sleep mode – All gates OFF, low power state, 5 V OFF

*X indicates “don’t care”

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Applications Information

Power

All supply connections to the A3930/A3931 should have capacitors mounted between the supply pins and the ground pin. These capacitors will provide the transient currents which occur during switching and decouple any voltage transients on the pin from the main supply.

VBB Decouple with at least a 100 nF ceramic capacitor mounted between the VBB pin and the AGND pin. A larger electrolytic capacitor, typically 10 µF, in parallel with the ceramic capacitor is also recommended.

VREG Supplies current for the gate-drive circuit. As the gates are driven high, they require current from an external capacitor connected to VREG to support the transients. This capacitor should be placed as close as possible to the VREG pin with the ground connection close to the AGND pin. Its value should be at least 20 times larger than the bootstrap capacitor. The capacitor should have a very low series resistance (ESR) and inductance (ESL) to avoid large voltage drops during the initial transient. The optimum capacitor type is a high quality ceramic such as X7R. However, when the required capacitance is too large, an aluminium electrolytic capacitor may be used, with a smaller ceramic capacitor (≈100 nF) in parallel.

V5 When the 5V regulator is used with an external pass transistor to provide power to other circuits, a 10 µF decoupling capacitor should be connected between the V5 pin and AGND as close to the pins as possible. If an electrolytic capacitor is used, then a 100 nF ceramic capacitor should be added in parallel. To improve stability, a 100 nF capacitor also should be connected between the V5BD pin and AGND. If 5V is not required for external circuits, the external pass transistor may be omitted, but in that case, V5 must connected directly to V5BD and decoupled with at least a 220 nF capacitor between V5 and AGND.

AGND The A3930/A3931 has a single ground connection at the AGND pin. The design ensures that only the operating current for the controller stage passes through this pin. The charge and discharge current for the external FETs does not pass though this pin. The AGND pin is the ground reference for the current trip threshold, the V_{DS} monitor threshold, and the timing components. It should therefor be kept as quiet as possible. A suggested ground connection scheme is described in the layout section below.

Power Dissipation In applications where a high ambient temperature is expected the on-chip power dissipation may become a critical factor. Careful attention should be paid to ensure the operating conditions allow the A3930/A3931 to remain in a safe range of junction temperature.

The power consumed, P_{TOT}, by the A3930/A3931 can be estimated using the following formulas:

$$P_{TOT} = P_{BIAS} + P_{CPUMP} + P_{SWITCHING},$$
$$P_{BIAS} = V_{BB} \times I_{BB},$$

where I_{BB} is 3 mA, typical, and

$$P_{CPUMP} = (2 \times V_{BB} – V_{REG}) \times I_{AV}$$

where $V_{BB} < 15$ V, or

$$P_{CPUMP} = (V_{BB} – V_{REG}) \times I_{AV}$$

where $V_{BB} > 15$ V, and

$$I_{AV} = Q_{GATE} \times N \times f_{PWM},$$
$$P_{SWITCHING} = Q_{GATE} \times V_{REG} \times N \times f_{PWM} \times Ratio$$

where $N = 2$ for slow decay, or $N = 4$ for fast decay, and

$$Ratio = 10 / (R_{GATE} + 10)$$

Bootstrap Capacitors

Bootstrap Capacitor Selection The value for C_{BOOT} must be correctly selected to ensure proper operation of the device. If the value is too large, time will be wasted charging the capacitor, resulting in a limit on the maximum duty cycle and PWM frequency. If the value is too small, there can be a large voltage drop at the time when the charge is transferred from C_{BOOT} to the MOSFET gate.

To keep the voltage drop small, $Q_{BOOT} \gg Q_{GATE}$. A factor of 20 is a reasonable value. To calculate C_{BOOT}, the following formulas can be used:

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT},$$
$$= Q_{GATE} \times 20,$$

therefore

$$C_{BOOT} = Q_{GATE} \times 20 / V_{BOOT}$$

The voltage drop on the C*x* pin as the MOSFET is being turned on can be approximated by:

$$\Delta V = Q_{GATE} / C_{BOOT}$$

Bootstrap Charging It is good practice to ensure that the high-side bootstrap capacitor, CBOOT, is completely charged before a

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high-side PWM cycle is requested. The minimum time required to charge the capacitor is approximated by:

$$t_{CHARGE(min)} \approx C_{BOOT} \times \Delta V / 250\ mA$$

At power-on, and when the drivers have been disabled for a long time, the CBOOT may be completely discharged. In these cases, ΔV can be considered to be the full high-side drive voltage, 12 V. Otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the S*x* pin is pulled low via a GL*x* PWM cycle, and current flows from VREG through the internal bootstrap diode circuit to CBOOT.

Bootstrap Charge Monitor The A3930 and A3931 provide automatic bootstrap capacitor charge management. The bootstrap capacitor voltage for each phase, V_{BOOTx}, is continuously checked to ensure that it is above the bootstrap undervoltage threshold, V_{BOOTUV}. If V_{BOOT} drops below this threshold, the A3930 and A3931 will turn on the necessary low-side FET until the V_{BOOT} exceeds V_{BOOTUV} plus the hysteresis, $V_{BOOTUVHys}$. The minimum charge time is typically 7 µs, but may be longer for very large values of the bootstrap capacitor (C_{BOOT} >1000 nF). If V_{BOOT} does not exceed V_{BOOTUV} within approximately 200 µs, an undervoltage fault will be flagged, as shown in table 2.

PWM Control

The A3930 and A3931 have the flexibility to be used in many different motor control schemes. The internal PWM control can be used to provide fully integrated, closed-loop current control. Alternatively, current-mode or voltage-mode control are possible using external control circuits with either the DIR or the PWM input pins.

Internal PWM Control The internal PWM current control function is useful in applications where motor torque control or simple maximum current limitation is required. However, for motor speed control applications, it is usually better to use external PWM control either as a closed- or open-loop system.

External PWM Control When external PWM control is used, it is possible to completely disable the internal PWM control circuit by connecting the RC pin to AGND.

With the internal control disabled, however, care should be taken to avoid excessive current in the power FETs because the A3930/A3931 will not limit the current. Short-circuit detection will still be available in case of faults. The output of the sense amplifier is also available, but provision must be made in the external control circuits to ignore (blank) the transients at the switching points.

External and Internal Combined PWM Control Where external PWM control is used but current limitation is still required, internal PWM current control can be used at the same time as external PWM control. To do so, usually the internal PWM frequency is set lower than the external PWM frequency. This allows the external PWM signal to dominate and synchronize the internal PWM circuit. It does this by discharging the timing capacitor, CT, when the PWM pin is low. When internal and external PWM control are used together, all control features of the A3930/A3931 are available and active, including: dead time, current comparator, and comparator blanking.

PWM Frequency Should be set high enough to avoid any audible noise, but low enough to ensure adequate charging of the boot capacitor, CBOOT. The external resistor RT and capacitor CT, connected in parallel from the RC pin to AGND, set the PWM frequency to approximately:

$$f_{OSC} \approx 1 / (R_T C_T + t_{BLANK} + t_{DEAD}) .$$

R_T should be in the range of 5 to 400 kΩ.

PWM Blank The timing capacitor, CT, also serves as the means to set the blank time duration. t_{BLANK}. At the end of the PWM off-cycle, a high-side gate selected by the commutation logic turns on. At this time, large current transients can occur during the reverse recovery time of the intrinsic source drain body diodes of the external power MOSFETs. To prevent false tripping of the current-sense comparator, the output of the current comparator is ignored during the blank time.

The length of t_{BLANK} is different for internal versus external PWM. It is set by the value of the timing capacitor, CT, according to the following formulas:

for internal PWM: t_{BLANK} (µs) = 1260 × C_T (µF), and

for external PWM: t_{BLANK} (µs) = 2000 × C_T (µF) .

A nominal C_T value of 680 pF will give a blanking time of 1.3 µs for external PWM and 860 ns for internal PWM. The user must ensure that C_T is large enough to cover the current-spike duration.

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Note that this blank time is only used to mask the internal current comparator. If the current sense amplifier output, CSOUT, is being used in an external PWM control circuit, then it will be necessary to externally generate a blank time for that control loop.

Dead Time The potential for cross-conduction occurs with synchronous rectification, direction changes, PWM, or after a bootstrap capacitor charging cycle. To prevent cross-conduction in any phase of the power FET bridge, it is necessary to have a dead-time delay, t_{DEAD}, between a high- or low-side turn-off and the next turn-on event. t_{DEAD} is in the range of between 96 ns and 6.3 µs, and is set by the value of a resistor, RDEAD, between the RDEAD pin and the GND pin. The maximum dead time of typically 6µs can be set by leaving the RDEAD pin unconnected, or connected to the V5 pin.

At 25°C, the value of t_{DEAD} (µs) can be approximated by:

$$t_{DEAD(nom)} \approx 0.1 + 33 / (5 + I_{DEAD}),$$

$$I_{DEAD} = 2000 / R_{DEAD}$$

where I_{DEAD} is in µA, and R_{DEAD} is between 5 and 400 kΩ. The greatest accuracy is obtained with values of R_{DEAD} between 10 and 100 kΩ.

The choice of power MOSFET and external series gate resistance determines the selection of RDEAD. The dead time should be made long enough to cover the variation of the MOSFET gate capacitance and the tolerances of the series gate resistance, both external and internal to the A3930/A3931.

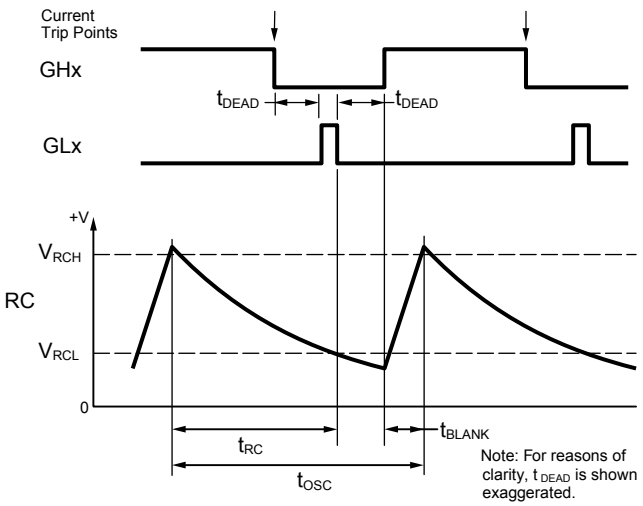

Figure 2. Internal PWM RC Timing

Synchronous Rectification To reduce power dissipation in the external MOSFETs, the A3930/A3931 control logic turns on the appropriate low-side and high-side driver during the load current recirculation PWM-off cycle. Synchronous rectification allows current to flow through the FET selected by the MODE pin setting during the decay time, rather than through the source-drain body diode. The body diodes of the recirculating power FETs conduct only during the dead time that occurs at each PWM transition. For internal current control using fast decay mode, reversal of load current is prevented by turning off synchronous rectification when a zero current level is detected. For external PWM control using fast decay mode, the load current will not be limited to zero but will rise to the set current limit in the reverse direction before disabling synchronous rectification.

Braking. The A3930 and A3931 provide dynamic braking by forcing all low-side MOSFETs on, and all high-side MOSFETs off. This effectively short-circuits the back EMF of the motor, which forces a reverse current in the windings, and creating a breaking torque.

During braking, the load current can be approximated by:

$$I_{BRAKE} \approx V_{BEMF} / R_{LOAD}$$

Because the load current does not flow through the sense resistor, RSENSE, during a dynamic brake, care must be taken to ensure that the power MOSFET maximum ratings are not exceeded.

It is possible to apply a PWM signal to the BRAKE input to limit the motor braking current. However, because there is no measurement of this current, the PWM duty cycle must be determined for each set of conditions. Typically the duty cycle of such a brake PWM input would start at a value which limits the current and then drops to 0%, that is, BRAKE goes to low, to hold the motor stationary.

Setting RESET = 1 and COAST = 0 overrides BRAKE and turns all motor bridge FETs off, coasting the motor.

Driving a Full-Bridge. The A3930 and A3931 may be used to drive a full-bridge (for example, a brush dc motor load) by hard-wiring a single state for the Hall inputs and leaving the corresponding phase driver outputs floating. For example, with a configuration of H1 = H2 = 1, and H3 = 0, the outputs CC, GHC, SC, and GLC would be floated, according to the commutation truth table, table3, which indicates a state of high-impedence (Z) for SC with that Hall input configuration. The DIR input controls the motor rotation, while the PWM and MODE inputs control the motor current behavior, as described in the input logic table, table 4.

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Circuit Layout

Because this is a switch-mode application, where rapid current changes are present, care must be taken during layout of the application PCB. The following points are provided as guidance for layout (refer to figure 3). Following all guidelines will not always be possible. However, each point should be carefully considered as part of any layout procedure.

Ground connection layout recommendations:

1. Sensitive connections such as RDEAD and VDSTH, which have very little ground current, should be referenced to the Quiet ground, which is connected independently closest to the AGND pin. The components associated with these sensitive pins should never be connected directly to the Supply common or to the Power ground; they must be referenced directly to the AGND pin.
2. Supply decoupling for the supply pins VBB, VREG, and V5 should be connected to Controller Supply ground, which is connected independently, close to the AGND pin. The decoupling capacitors should also be connected as close as possible to the corresponding supply pin.
3. The oscillator timing components can be connected to Quiet ground or Controller Supply ground. They should not be connected to the Supply common or the Power ground.
4. The exposed thermal pad on the package should be connected to the AGND pin and may form part of the Controller Supply ground.
5. If the layout space is limited, then the Quiet ground and the Controller Supply ground may be combined, provided that the ground return of the dead-time resistor, RDEAD, is close to the AGND pin.
6. The AGND pin should be connected by an independent low impedance trace to the Supply common at a single point.
7. Check the peak voltage excursion of the transients on the LSS pin with reference to the AGND pin using a close-grounded (tip and barrel) probe. If the voltage at LSS exceeds the absolute maximum specified in this datasheet, add additional clamping, capacitance or both between the LSS pin and the AGND pin.

Other layout recommendations:

1. Gate charge drive paths and gate discharge return paths may carry large transient current pulses. Therefore, the traces from GHx, GLx, Sx, and LSS should be as short as possible to reduce the inductance of the circuit trace.
2. Provide an independent connection from LSS to the common point of the power bridge. It is not recommended to connect LSS directly to the AGND pin, as this may inject noise into sensitive functions such as the dead-timer. The LSS connection should not be used for the CSP connection.
3. The inputs to the sense amplifier, CSP and CSN, should be independent traces and for best results should be matched in length and route.
4. Minimize stray inductance by using short, wide copper runs at the drain and source terminals of all power FETs. This includes motor lead connections, the input power bus, and the common source of the low-side power FETs. This will minimize voltages induced by fast switching of large load currents.
5. Consider the use of small (100 nF) ceramic decoupling capacitors across the source and drain of the power FETs

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to limit fast transient voltage spikes caused by trace inductance.

6. Ensure that the TEST pin is connected to AGND. This pin is used for production test only.

The above are only recommendations. Each application is different and may encounter different sensitivities. A driver running with a few amperes will be less susceptible than one running with 150 A, and each design should be tested at the maximum current, to ensure any parasitic effects are eliminated.

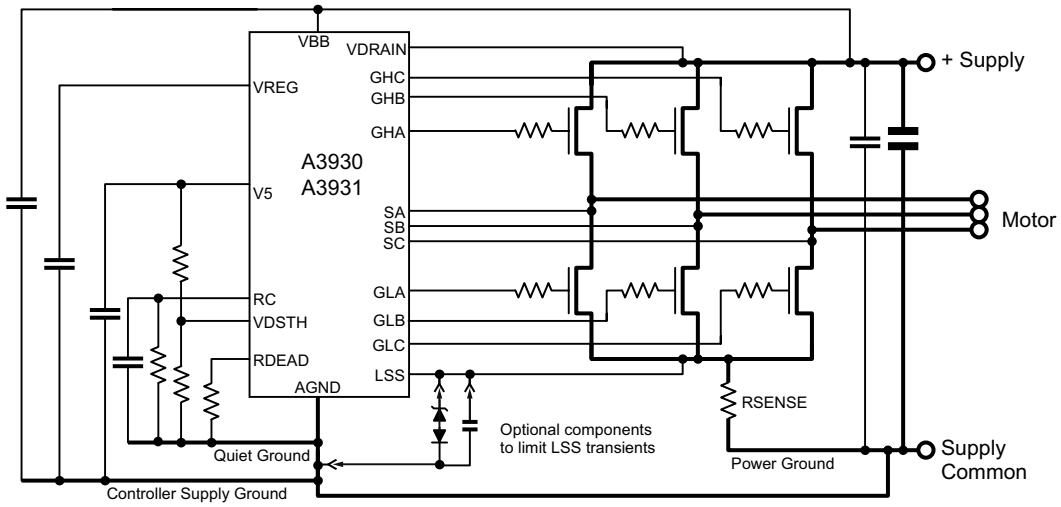

Figure 3. Supply and Ground Connections

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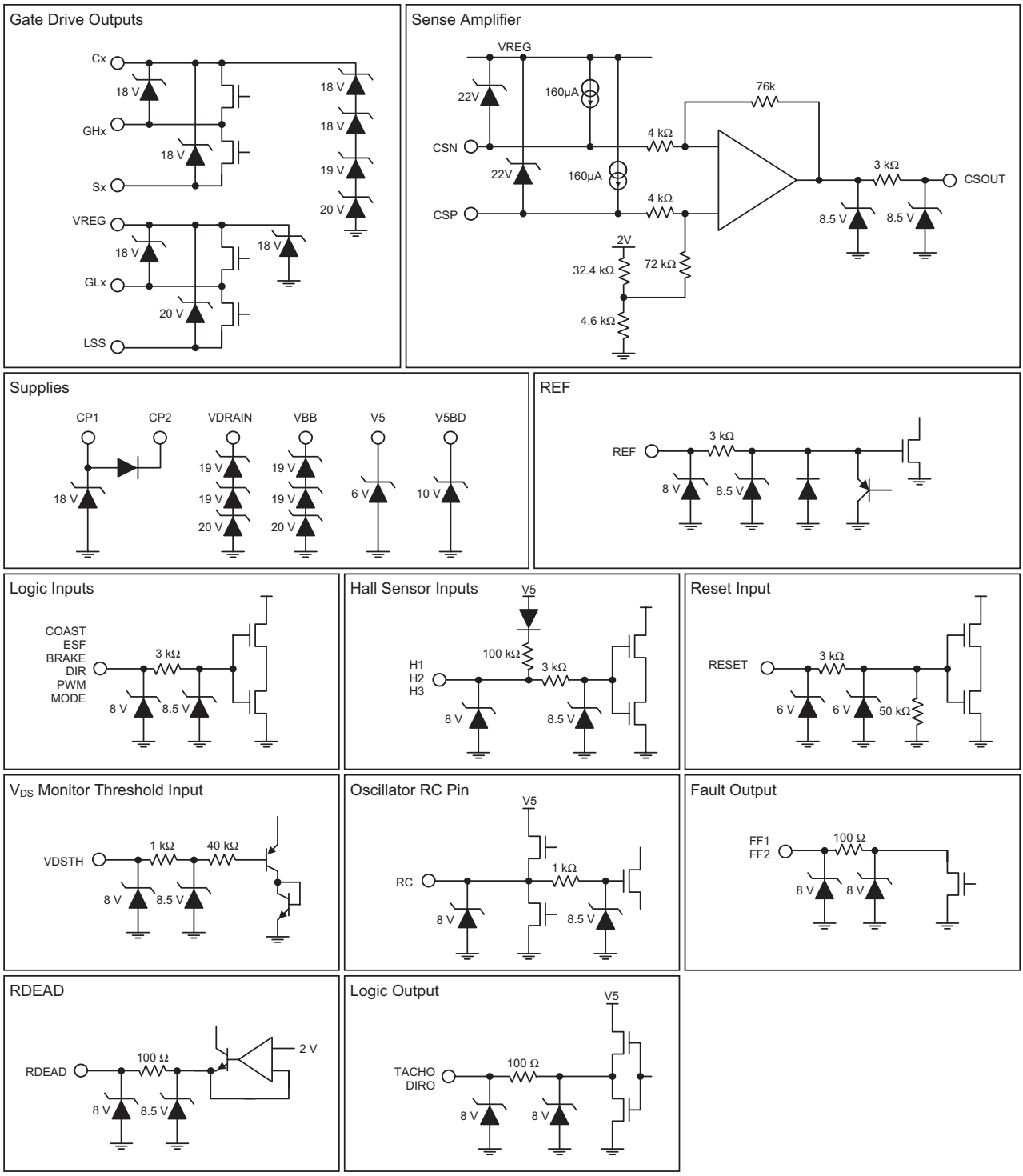

Figure 3. Input and Output Structures

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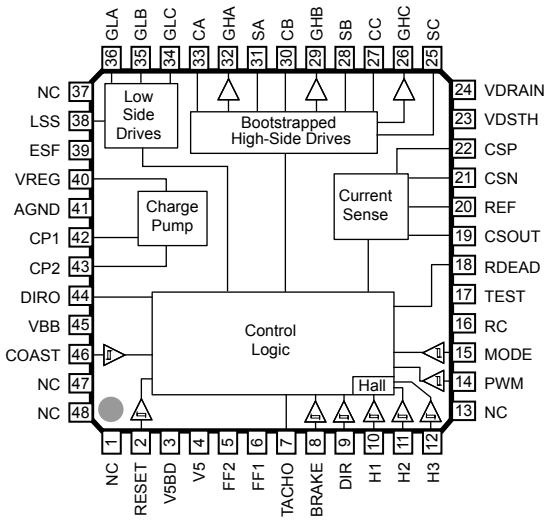
Pin-out Diagrams

JP Package



Terminal List Table

Number	Name	Description
1	N.C.	No connection
2	RESET	Control for sleep mode
3	V5BD	5V regulator base drive
4	V5	5V regulator reference
5	FF2	Fault flag 2
6	FF1	Fault flag 1
7	TACHO	Speed output
8	BRAKE	Brake input
9	DIR	Direction control input
10	H1	Hall sensor input
11	H2	Hall sensor input
12	H3	Hall sensor input
13	N.C.	No connection
14	PWM	Control input
15	MODE	Decay control input
16	RC	PWM oscillator control input
17	TEST	Test pin; tie to AGND
18	RDEAD	Dead time setting
19	CSOUT	Current sense output
20	REF	Current limit setting
21	CSN	Current sense input –
22	CSP	Current sense input +
23	VDSTH	Fault threshold voltage
24	VDRAIN	High-side drain voltage sense

Number	Name	Description
25	SC	Motor connection phase C
26	GHC	High-side gate drive phase C
27	CC	Bootstrap capacitor phase C
28	SB	Motor connection phase B
29	GHB	High-side gate drive phase B
30	CB	Bootstrap capacitor phase B
31	SA	Motor connection phase A
32	GHA	High-side gate drive phase A
33	CA	Bootstrap capacitor phase A
34	GLC	Low-side gate drive phase C
35	GLB	Low-side gate drive phase B
36	GLA	Low-side gate drive phase A
37	N.C.	No connection
38	LSS	Low-side source
39	ESF	Enable stop on fault input
40	VREG	Gate drive supply output
41	AGND	Analog ground
42	CP1	Pump capacitor
43	CP2	Pump capacitor
44	DIRO	Direction output
45	VBB	Supply voltage
46	COAST	Coast input
47	N.C.	No connection
48	N.C.	No connection

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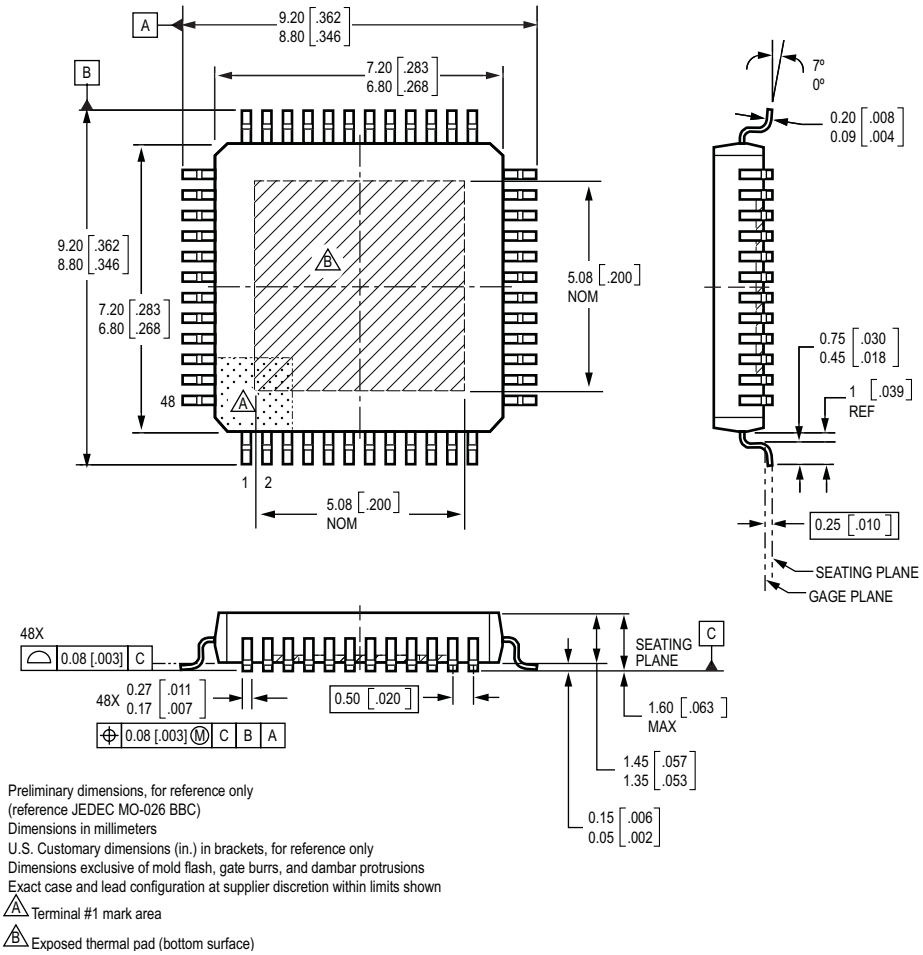
Package JP, 48-pin LQFP with Exposed Thermal Pad



Preliminary dimensions, for reference only
(reference JEDEC MO-026 BBC)
Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

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