

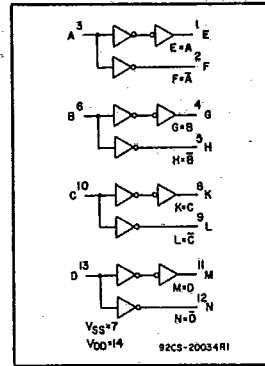
CD4041A Types

CMOS Quad True/Complement Buffer

The RCA-CD4041A types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The CD4041A is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can be used as an ultra-low power

resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T _{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V _{DD}):	
(Voltages referenced to V _{SS} Terminal)	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P _D):	
FOR T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T _A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T _A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T _A = Full Package Temperature Range)	3	12	V

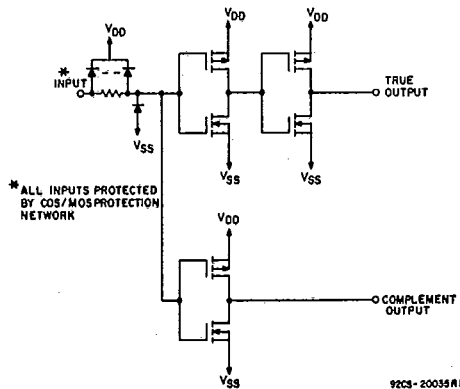


Fig. 1 - CD4041A schematic diagram.

Features:

- True Output
 - High current source and sink capability
 - 8 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V
 - 3.2 mA (typ.) @ V_{DS} = 0.4 V, V_{DD} = 5 V (two TTL loads)
- Complement Output
 - Medium current source and sink capability
 - 3.6 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V
 - 1.6 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 5 V
 - Quiescent current specified to 15 V
 - Maximum input peakage of 1 μA at 15 V (full package-temperature range)
 - 1-V noise margin (full package temperature range)

Applications:

- High current source/sink driver
- CMOS-to-DTL/TTL Converter
- Display driver
- MOS clock driver
- Resistor network driver (Ladder or weighted R)
- Buffer
- Transmission line driver

CD4041A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ and $C_L = 15\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS	
		VDD (Volts)	D, F, K, H Packages		E Package		
			TYP.	MAX.	TYP.		MAX.
Propagation Delay Time: High-to-Low Level t_{PHL}	True Output	5	65	115	65	140	ns
		10	40	75	40	100	
	Comp. Output	5	55	100	55	125	ns
		10	30	45	30	65	
Low-to-High Level t_{PLH}	True Output	5	75	125	75	150	ns
		10	45	75	45	100	
	Comp. Output	5	45	100	45	125	ns
		10	25	50	25	60	
Transition Time: High-to-Low Level t_{THL}	True Output	5	20	40	20	60	ns
		10	13	25	13	40	
	Comp. Output	5	40	60	40	80	ns
		10	25	40	25	50	
Low-to-High Level t_{TLH}	True Output	5	20	40	20	60	ns
		10	13	25	13	40	
	Comp. Output	5	35	55	35	75	ns
		10	25	40	25	50	
Input Capacitance C_i	Any Input		5	—	5	—	pF

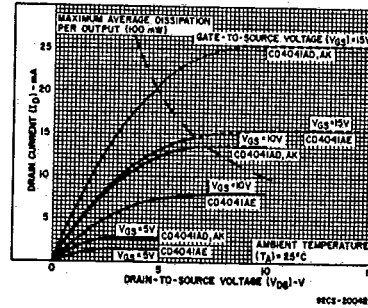


Fig.8 - Minimum output n-channel drain characteristics - complement output.

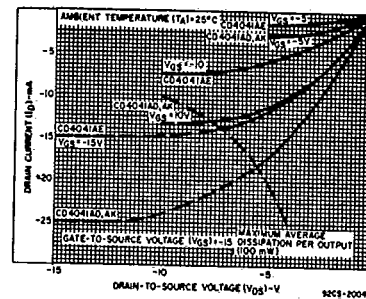


Fig.9 - Minimum output p-channel drain characteristics - complement output.

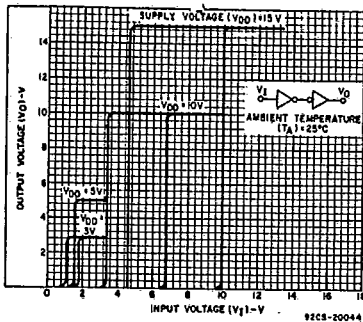


Fig.10 - Minimum and maximum transfer characteristics - true output.

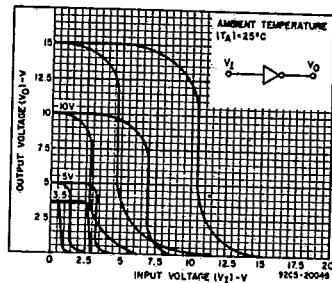


Fig.11 - Minimum and maximum transfer characteristics - complement output.

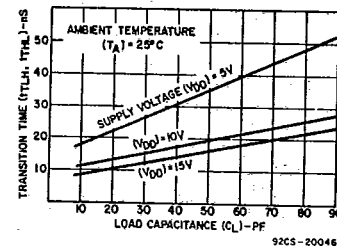


Fig.12 - Typical transition time vs. C_L - true output.

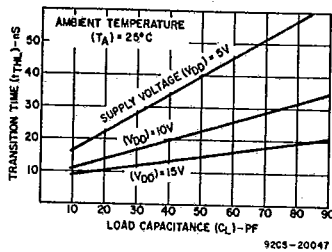


Fig.13 - Typical high-to-low level transition time vs. C_L - complement output.

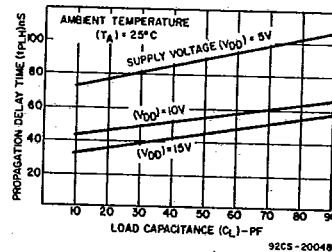


Fig.14 - Typical low-to-high level propagation delay time vs. C_L - true output.

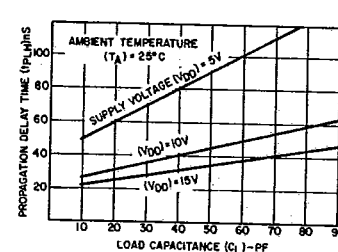


Fig.15 - Typical low-to-high level propagation delay time vs. C_L - complement output.

CD4041A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E ₁ Package				
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25		+125	-40	+25		+85	
Quiescent Device Current, I _Q Max.	-	-	5	1	0.005	1	60	10	0.01	10	140	μA
	-	-	10	2	0.005	2	120	20	0.02	20	280	
	-	-	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V _{OL}	-	0.5	5	0 Typ.; 0.05 Max.								V
	-	0.10	10	0 Typ.; 0.05 Max.								
High-Level, V _{OH}	-	0.5	5	4.95 Min.; 5 Typ.								V
	-	0.10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V _{NL}	3.6	-	5	1.5 Min.; 2.25 Typ.								V
	7.2	-	10	3 Min.; 4.5 Typ.								
Inputs High, V _{NH}	1.4	-	5	1.5 Min.; 2.25 Typ.								V
	2.8	-	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V _{NML}	4.5	-	5	1 Min.								V
	9	-	10	1 Min.								
Inputs High, V _{NMH}	0.5	-	5	1 Min.								V
	1	-	10	1 Min.								
Output Drive Current: N-Channel (Sink), I _{DN} Min.	0.4	True	5	2.1	3.2	1.6	1.2	1	3.2	0.8	0.7	mA
	0.5		10	6.25	10	5	3.5	3	10	2.5	2.2	
	0.5	Comp.	5	1	1.6	0.8	0.55	0.5	1.6	0.4	0.35	
	0.5		10	2.5	4	2	1.4	1.2	4	1	0.9	
P-Channel (Source), I _{DP} Min.	4.5	True	5	-1.75	-2.8	-1.4	-1	-0.85	-2.8	-0.7	-0.6	mA
	9.5		10	-5	-8	-4	-2.8	-2.4	-8	-2	-1.8	
	4.5	Comp.	5	-0.75	-1.2	-0.6	-0.4	-0.35	-1.2	-0.3	-0.27	
	9.5		10	-2.25	-3.6	-1.8	-1.25	-1.1	-3.6	-0.9	-0.8	
Input Leakage Current, I _{IL} , I _{IH}	Any Input		15	±10 ⁻⁵ Typ.; 1 Max.								μA

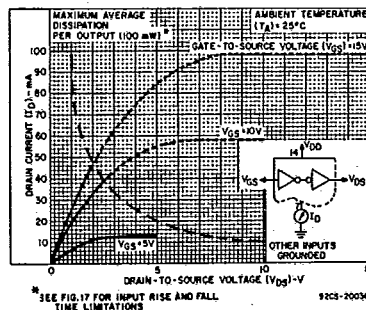


Fig. 2 - Typical output n-channel drain characteristics - true output.

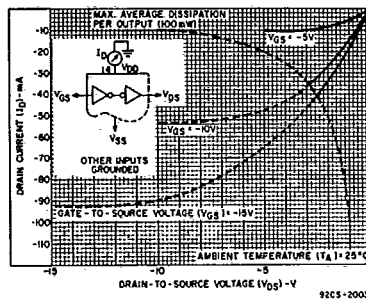


Fig. 3 - Typical output p-channel drain characteristics - true output.

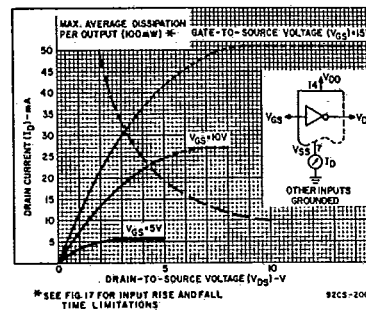


Fig. 4 - Typical output n-channel drain characteristics - complement output.

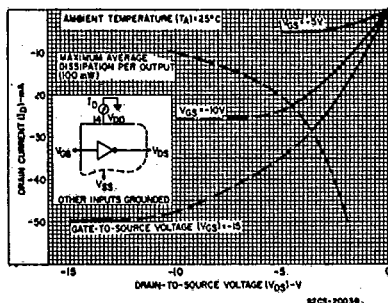


Fig. 5 - Typical output p-channel drain characteristics - complement output.

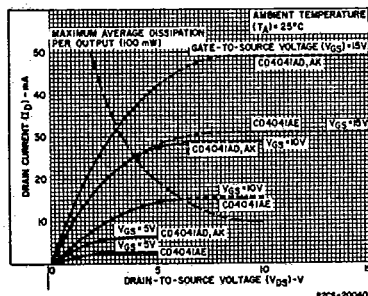


Fig. 6 - Minimum output n-channel drain characteristics - true output.

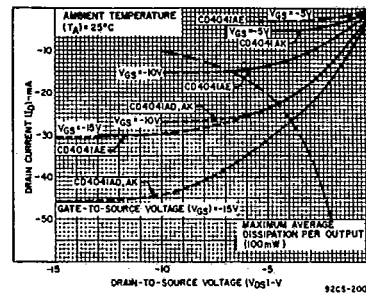


Fig. 7 - Minimum output p-channel drain characteristics - true output.

CD4041A Types

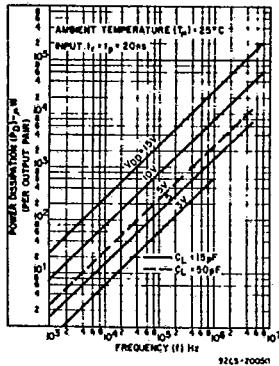


Fig.16 - Typical power dissipation vs. frequency per output pair.

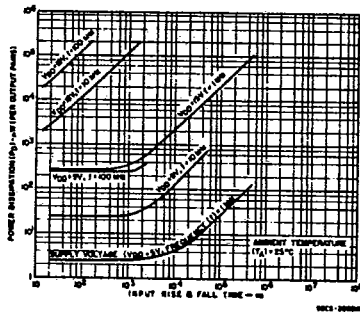


Fig.17 - Typical power dissipation vs. input rise & fall time per output pair.

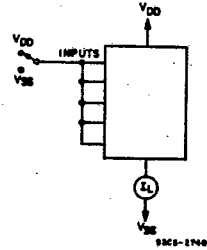


Fig.18 - Quiescent device current test circuit.

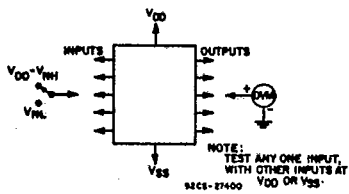


Fig.19 - Noise Immunity test circuit.

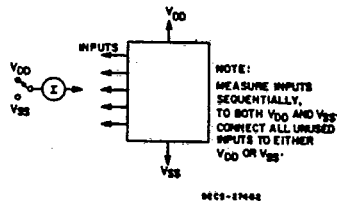
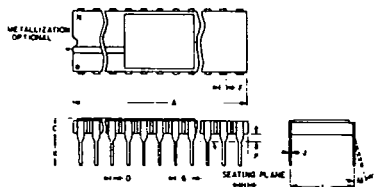


Fig.20 - Input leakage current test circuit.

Dimensional Outlines (Cont'd)

DUAL-IN-LINE SIDE-BRAZED CERAMIC PACKAGES



(D) SUFFIX
18-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.890	0.915		22.606	23.241
C	-	0.200		-	5.080
D	0.015	0.021		0.381	0.533
F	0.054	REF.	1	1.371	REF.
G	0.100	BSC	1	2.54	BSC
H	0.035	0.065		0.889	1.651
J	0.008	0.012	3	0.203	0.304
K	0.125	0.150		3.175	3.810
L	0.290	0.310	2	7.366	7.874
M	-	0°		0°	15°
P	0.025	0.045		0.635	1.143
N	18			18	

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(D) SUFFIX
22-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.065	1.100		27.05	27.94
C	0.085	0.145		2.16	3.68
D	0.017	0.023		0.43	0.58
F	0.040	REF.	1	1.02	REF.
G	0.100	BSC	1	2.54	BSC
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.380	0.420	2	9.65	10.67
M	-	7°		-	7°
P	0.025	0.050		0.64	1.27
N	22			22	

92CS-25186R2

NOTES:

- Leads within 0.005" (0.13 mm)-radius of True Position at maximum material condition.
- Dimension "L" to center of leads when formed parallel.
- When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

(D) SUFFIX
24-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.180	1.220		29.98	30.98
C	0.085	0.145		2.16	3.68
D	0.015	0.023		0.39	0.58
F	0.040	REF.		1.02	REF.
G	0.100	BSC	1	2.54	BSC
H	0.030	0.070		0.77	1.77
J	0.008	0.012	3	0.21	0.30
K	0.125	0.175		3.18	4.44
L	0.580	0.620	2	14.74	15.74
M	-	7°		-	7°
P	0.025	0.050		0.64	1.27
N	24			24	

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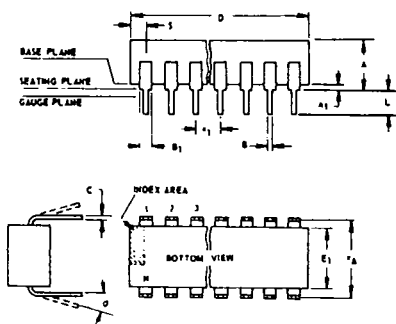
(D) SUFFIX
40-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.980	2.020		50.30	51.30
C	0.095	0.155		2.43	3.93
D	0.017	0.023		0.43	0.58
F	0.050	REF.		1.27	REF.
G	0.100	BSC	1	2.54	BSC
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.580	0.620	2	14.74	15.74
M	-	7°		-	7°
P	0.025	0.050		0.64	1.27
N	40			40	

92CM-27029R2

Dual-In-Line Plastic and Frit-Seal Ceramic Packages

(E) SUFFIX (JEDEC MO-001-AN)
8-Lead Dual-In-Line Plastic
(Mini-DIP) Package



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A ₁	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B ₁	0.035	0.065		0.889	1.65
C	0.008	0.012	1	0.203	0.304
D	0.370	0.400		9.40	10.16
E	0.300	0.325		7.62	8.25
E ₁	0.240	0.260		6.10	6.60
e ₁	0.100	TP	2	2.54	TP
e _A	0.300	TP	2, 3	7.62	TP
L	0.125	0.150		3.18	3.81
L ₂	0.000	0.030		0.000	0.762
a	0	15	4	0	15
N	8		5	8	
N ₁	0		6	0	
O ₁	0.040	0.075		1.02	1.90
S	0.015	0.060		0.381	1.52

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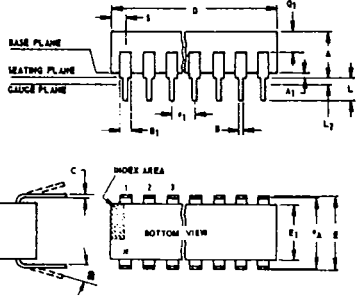
NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

- When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
- Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
- e_A applies in zone L₂ when unit installed.
- a applies to spread leads prior to installation.
- N is the maximum quantity of lead positions.
- N₁ is the quantity of allowable missing leads.

Dimensional Outlines (Cont'd)

Dual-In-Line Plastic and Frit-Seal Ceramic Packages (Cont'd)



- NOTES: Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines. 1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm). 2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed. 3. eA applies in zone L2 when unit installed. 4. a applies to spread leads prior to installation. 5. N is the maximum quantity of lead positions. 6. N1 is the quantity of allowable missing leads.

(E) and (F) SUFFIXES (JEDEC MO-001-AB) 14-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

Table with columns: SYMBOL, INCHES (MIN., MAX.), NOTE, MILLIMETERS (MIN., MAX.). Rows include dimensions A, A1, B, B1, C, D, E, E1, e1, eA, L, L2, a, N, N1, Q1, S.

92SS-4296R3

(E) and (F) SUFFIXES (JEDEC MO-001-AC) 16-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

Table with columns: SYMBOL, INCHES (MIN., MAX.), NOTE, MILLIMETERS (MIN., MAX.). Rows include dimensions A, A1, B, B1, C, D, E, E1, e1, eA, L, L2, a, N, N1, Q1, S.

92CM-15967R4

(E) SUFFIX 18-Lead Dual-In-Line Plastic Package

Table with columns: SYMBOL, INCHES (MIN., MAX.), NOTE, MILLIMETERS (MIN., MAX.). Rows include dimensions A, A1, B, B1, C, D, E1, e1, eA, L, L2, a, N, N1, S.

92CS-30630

(E) SUFFIX 22-Lead Dual-In-Line Plastic Package

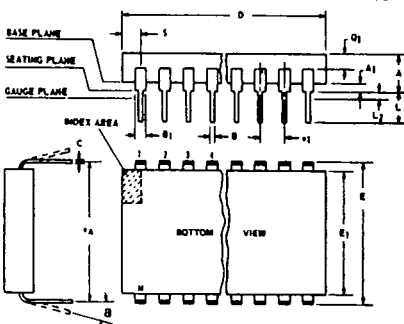
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92CS-30830

(F) SUFFIX (JEDEC MO-001-AG) 16-Lead Dual-In-Line Frit-Seal Ceramic Package

Table with columns: SYMBOL, INCHES (MIN., MAX.), NOTE, MILLIMETERS (MIN., MAX.). Rows include dimensions A, A1, B, B1, C, D, E, E1, e1, eA, L, L2, a, N, N1, Q1, S.

92CM-22284R1



- NOTES: Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines. 1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013". 2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed. 3. eA applies in zone L2 when unit installed. 4. a applies to spread leads prior to installation. 5. N is the maximum quantity of lead positions. 6. N1 is the quantity of allowable missing leads.

(E) and (F) SUFFIXES (JEDEC MO-015-AA) 24-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

Table with columns: SYMBOL, INCHES (MIN., MAX.), NOTE, MILLIMETERS (MIN., MAX.). Rows include dimensions A, A1, B, B1, C, D, E, E1, e1, eA, L, L2, a, N, N1, Q1, S.

92CS26938R2

(E) SUFFIX 40-Lead Dual-In-Line Plastic Package

Table with columns: SYMBOL, INCHES (MIN., MAX.), NOTE, MILLIMETERS (MIN., MAX.). Rows include dimensions A, A1, B, B1, C, D, E1, e1, eA, L, L2, a, N, N1, Q1, S.

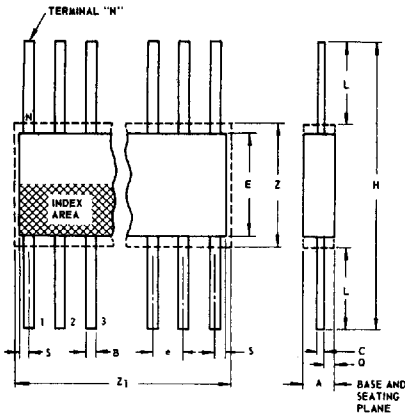
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Dimensional Outlines (Cont'd)

Ceramic Flat Packs

**(K) SUFFIX (JEDEC MO-004-AF)
14-Lead**



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z ₁	0.400		4	10.16	

9288-4300R3

NOTES:

1. Refer to JEDEC Publication No. 95 for Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z₁ determine a zone within which all body and lead irregularities lie.

**(K) SUFFIX (JEDEC MO-004-AG)
16-Lead**

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	16		3	16	
Q	0.005	0.050		0.13	1.27
S	0.000	0.025		0.00	0.63
Z	0.300		4	7.62	
Z ₁	0.400		4	10.16	

92CS-17271R3

**(K) SUFFIX
24-Lead**

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	24		3	24	
Q	0.035	0.070		0.89	1.77
S	0.060	0.110	1	1.53	2.79
Z	0.700		4	17.78	
Z ₁	0.750		4	19.05	

92CS-19949R2

**(K) SUFFIX
28-Lead**

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	28		3	28	
Q	0.035	0.070		0.89	1.77
S	0	0.060	1	0	1.53
Z	0.700		4	17.78	
Z ₁	0.750		4	19.05	

92CS-20972