

T-43-21



CD4030B Types

CMOS Quad Exclusive-OR Gate

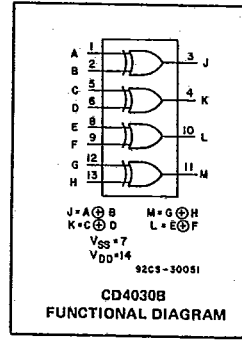
High-Voltage Types (20-Volt Rating)

■ CD4030B types consist of four independent Exclusive-OR gates. The CD4030B provides the system designer with a means for direct implementation of the Exclusive-OR function.

The CD4030B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- Medium-speed operation— t_{PHL} , t_{PLH} = 65 ns (typ.) at V_{DD} = 10 V, C_L = 50 pF
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
 - 1 V at V_{DD} = 5 V
 - 2 V at V_{DD} = 10 V
 - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	\pm 10mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -55°C to +100°C	500mW
For T_A = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package-Types)	100mW
OPERATING-TEMPERATURE RANGE (T_A)	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max	+265°C

RECOMMENDED OPERATING CONDITIONS

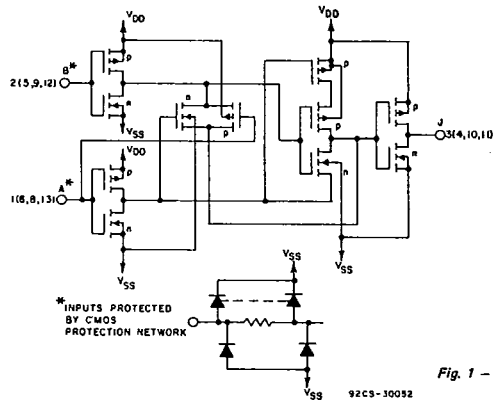
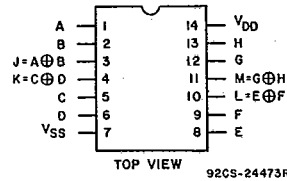
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

Applications:

- Even and odd-parity generators and checkers
- Logical comparators
- Adders/subtractors
- General logic functions

TERMINAL DIAGRAM Top View



TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = HIGH LEVEL
0 = LOW LEVEL

Fig. 1 - Schematic diagram (1 of 4 identical gates).

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0.5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μA
	-	0.10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0.15	15	1	1	30	30	-	0.01	1	
	-	0.20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0.5	5	0.05			-	0	0.05	-	V
	-	0.10	10	0.05			-	-	0.05	-	
	-	0.15	15	0.05			-	0	0.05	-	
Output Voltage: High-Level, V _{OH} Min.	-	0.5	5	4.95			4.95	5	-	-	V
	-	0.10	10	9.95			9.95	10	-	-	
	-	0.15	15	14.95			14.95	15	-	-	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	-	5	1.5			-	-	1.5	-	V
	1.9	-	10	3			-	-	3	-	
	1.5, 13.5	-	15	4			-	-	4	-	
Input High Voltage, V _{IH} Min.	0.5, 4.5	-	5	3.5			3.5	-	-	-	V
	1.9	-	10	7			7	-	-	-	
	1.5, 13.5	-	15	11			11	-	-	-	
Input Current I _{IN} Max.	-	0.18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

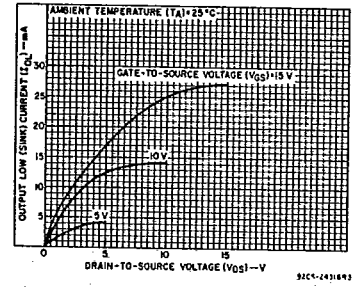


Fig. 2 - Typical output low (sink) current characteristics.

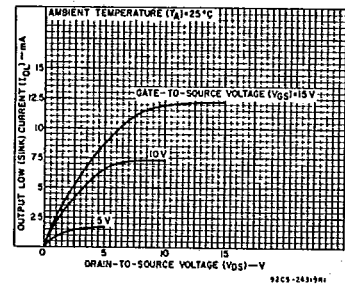


Fig. 3 - Minimum output low (sink) current characteristics.

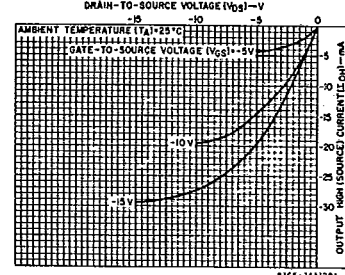


Fig. 4 - Typical output high (source) current characteristics.

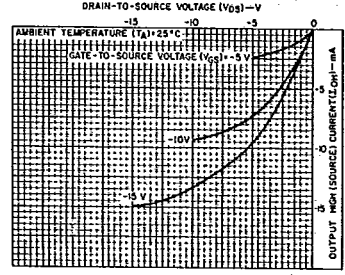


Fig. 5 - Minimum output high (source) current characteristics.

COMMERCIAL CMOS HIGH VOLTAGE ICs

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	CONDITIONS	LIMITS		UNITS	
		V _{DD} (V)			
		Typ.	Max.		
Propagation Delay Time, t _{PLH} , t _{PHL}	Any Input	5	140	280	ns
		10	65	130	
		15	50	100	
Transition Time, t _{THL} , t _{TLH}	Any Input	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C _{IN}	Any Input	5	7.5	pF	

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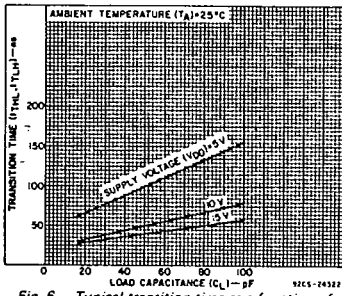


Fig. 6 - Typical transition time as a function of load capacitance.

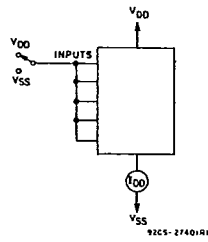


Fig. 10 - Quiescent-device current test circuit.

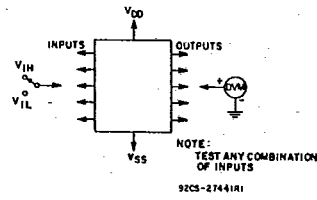


Fig. 11 - Input-voltage test circuit.

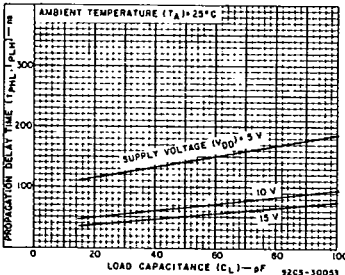


Fig. 7 - Typical propagation delay time as a function of load capacitance.

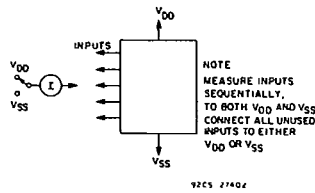


Fig. 12 - Input-current test circuit.

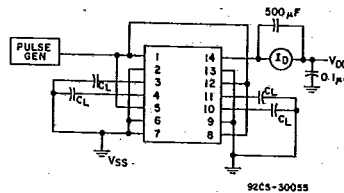


Fig. 13 - Dynamic power dissipation test circuit.

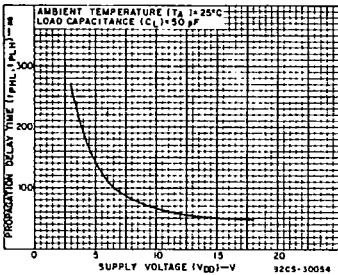


Fig. 8 - Typical propagation delay time as a function of supply voltage.

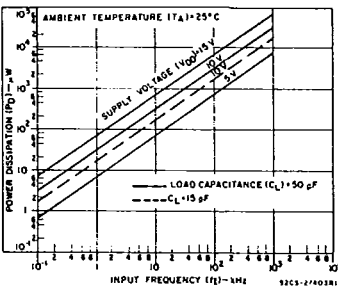
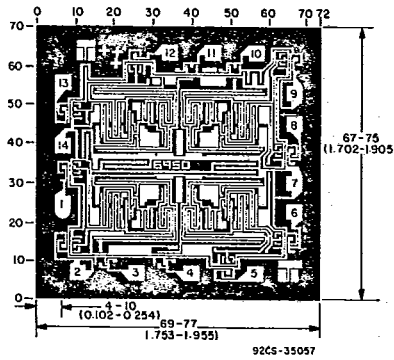


Fig. 9 - Typical dynamic power dissipation as a function of input frequency.



Dimensions and pad layout for CD4030BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).