

T-49-11

CD40181B Types

CMOS 4-Bit Arithmetic Logic Unit

High-Voltage Types (20-Volt Rating)

The RCA-CD40181B is a low-power four-bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive-OR and-NOR in the logic mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The CD40181B operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table.

The CD40181B contains logic for full look-ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs G_n and P_n for the four bits of the CD40181B. Use of the CD40182B look-ahead carry generator in conjunction with multiple CD40181B'S permits high-speed arithmetic operations on long words. A ripple carry output C_{n+4} is available for use in systems where speed is not of primary importance.

Also included in the CD40181B is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. In addition, relative magnitude information may be derived from the carry-in input C_n and ripple carry-out output C_{n+4} by placing the unit in the subtract mode and externally decoding using the information in Table III.

The CD40181B types are supplied in 24-lead hermetic ceramic dual-in-line packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40181 is similar to industry types MC14581 and 74181.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

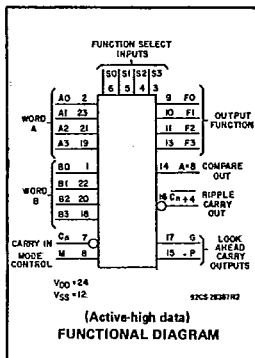
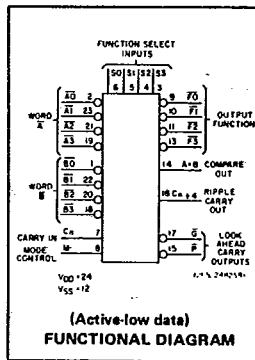
| CHARACTERISTIC | LIMITS | | UNITS |
|--|--------|------|-------|
| | Min. | Max. | |
| Supply-Voltage Range (For T_A =Full Package-Temperature Range) | 3 | 18 | V |

Features:

- Full look-ahead carry for speed operations on long words
- Generates 16 logic functions of two Boolean variables
- Generates 16 arithmetic functions of two 4-bit binary words
- A = B comparator output available
- Ripple-carry input and output available
- Typical addition time 200 ns @ $V_{DD} = 10 V$
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range)
 - = 1 V at $V_{DD} = 5 V$
 - = 2 V at $V_{DD} = 10 V$
 - = 2.5 V at $V_{DD} = 15 V$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Parallel arithmetic units
- Process controllers
- Low-power minicomputers



MAXIMUM RATINGS, Absolute-Maximum Values:

- DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal) -0.5 to +20 V
- INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5 V$
- DC INPUT CURRENT, ANY ONE INPUT $\pm 10 \mu A$
- POWER DISSIPATION PER PACKAGE (P_D):
 - For $T_A = -40$ to $+60^\circ C$ (PACKAGE TYPE E) 500 mW
 - For $T_A = +60$ to $+85^\circ C$ (PACKAGE TYPE E) Derate Linearly at 12 mW/ $^\circ C$ to 200 mW
 - For $T_A = -55$ to $+100^\circ C$ (PACKAGE TYPES D, F, K) 500 mW
 - For $T_A = +100$ to $+125^\circ C$ (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/ $^\circ C$ to 200 mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
 - For $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW
- OPERATING-TEMPERATURE RANGE (T_A):
 - PACKAGE TYPES D, F, K, H -55 to $+125^\circ C$
 - PACKAGE TYPE E -40 to $+85^\circ C$
- STORAGE TEMPERATURE RANGE (T_{stg}) -65 to $+150^\circ C$
- LEAD TEMPERATURE (DURING SOLDERING):
 - At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ C$

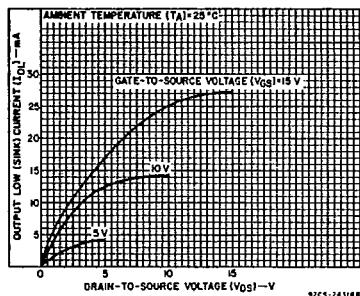


Fig. 1 - Typical output low (sink) current characteristics.

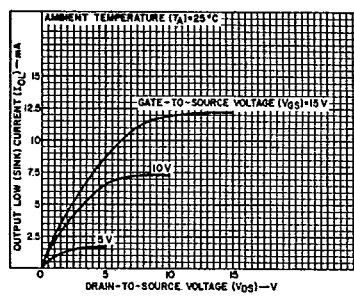


Fig. 2 - Minimum output low (sink) current characteristics.

CD40181B Types

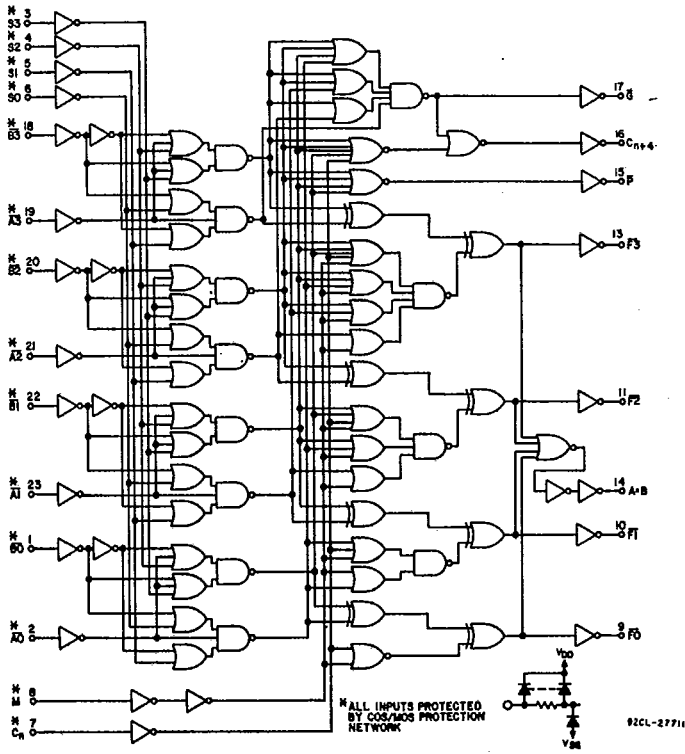


Fig. 3 - CD40181B logic diagram (active-low data).

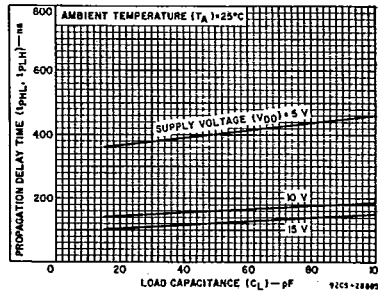


Fig. 6 - Typical propagation delay time as a function of load capacitance (for A or B to F, logic mode).

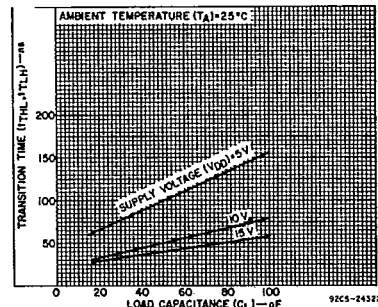


Fig. 7 - Typical transition time as a function of load capacitance.

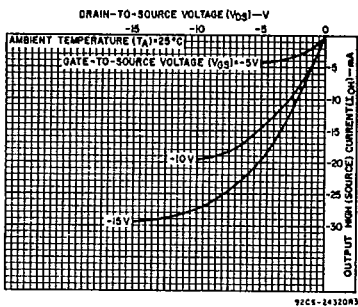


Fig. 4 - Typical output high (source) current characteristics.

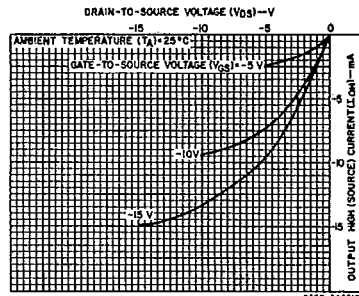


Fig. 5 - Minimum output high (source) current characteristics.

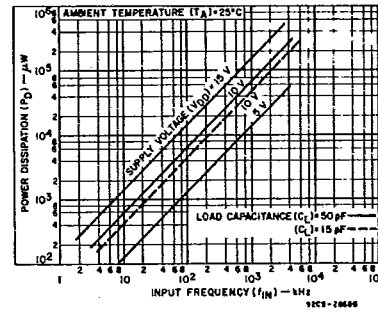


Fig. 8 - Typical dynamic dissipation as a function of input frequency (see Fig. 11 - dynamic power dissipation test circuit).

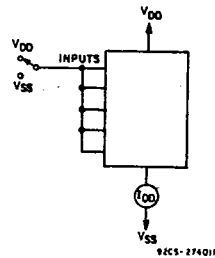


Fig. 9 - Quiescent device current test circuit.

CD40181B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | +25 | | | | | | | |
| | | | | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | - | 0.5 | 5 | 5 | 5 | 150 | 150 | - | 0.04 | 5 | μA |
| | - | 0.10 | 10 | 10 | 10 | 300 | 300 | - | 0.04 | 10 | |
| | - | 0.15 | 15 | 20 | 20 | 600 | 600 | - | 0.04 | 20 | |
| | - | 0.20 | 20 | 100 | 100 | 3000 | 3000 | - | 0.08 | 100 | |
| Output Low (Sink) Current I _{OL} Min. | 0.4 | 0.5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | - | mA |
| | 0.5 | 0.10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | - | |
| | 1.5 | 0.15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | - | |
| Output High (Source) Current, I _{OH} Min. | 4.6 | 0.5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | - | mA |
| | 2.5 | 0.5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | - | |
| | 9.5 | 0.10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | - | |
| | 13.5 | 0.15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | - | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0.5 | 5 | 0.05 | | | - | 0 | 0.05 | - | V |
| | - | 0.10 | 10 | 0.05 | | | - | 0 | 0.05 | - | |
| | - | 0.15 | 15 | 0.05 | | | - | 0 | 0.05 | - | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0.5 | 5 | 4.95 | | | 4.95 | 5 | - | - | V |
| | - | 0.10 | 10 | 9.95 | | | 9.95 | 10 | - | - | |
| | - | 0.15 | 15 | 14.95 | | | 14.95 | 15 | - | - | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | - | 5 | 1.5 | | | - | - | 1.5 | - | V |
| | 1, 9 | - | 10 | 3 | | | - | - | 3 | - | |
| | 1.5, 13.5 | - | 15 | 4 | | | - | - | 4 | - | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | - | 5 | 3.5 | | | 3.5 | - | - | - | V |
| | 1, 9 | - | 10 | 7 | | | 7 | - | - | - | |
| | 1.5, 13.5 | - | 15 | 11 | | | 11 | - | - | - | |
| Input Current I _{IN} Max. | - | 0.18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0.1 | μA |

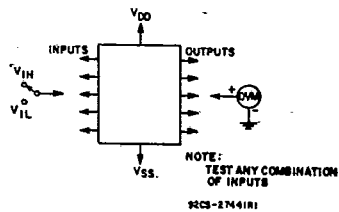
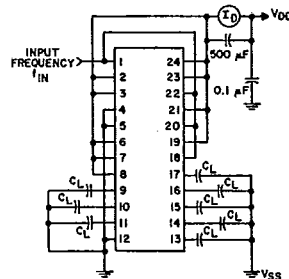


Fig. 10 - Input-voltage test circuit.



TEST CONDITIONS:
A0, A1, A2, A3, S0, S3, M, Cn = V_{DD}
B0, B1, B2, B3 = f_{IN}
S1, S2 = V_{SS}
(ALL OUTPUTS SWITCHING EXCEPT G)

92CS-26687

Fig. 11 - Dynamic power dissipation test circuit.

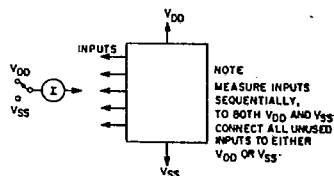
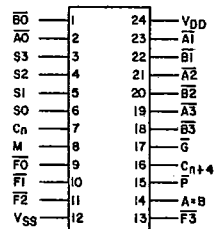


Fig. 12 - Input current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

| CHARACTERISTIC | V _{DD} (V) | LIMITS | | UNITS |
|---|---------------------|--------|------|-------|
| | | Typ. | Max. | |
| Propagation Delay Time: t _{pHL} , t _{pLH} A or B to F (logic mode), A or B to G or P, | 5 | 400 | 800 | ns |
| | 10 | 160 | 320 | |
| | 15 | 120 | 240 | |
| A or B to F, C _n +4, or A = B, | 5 | 500 | 1000 | ns |
| | 10 | 200 | 400 | |
| | 15 | 140 | 280 | |
| C _n to F | 5 | 320 | 640 | ns |
| | 10 | 135 | 270 | |
| | 15 | 100 | 200 | |
| C _n to C _n +4 | 5 | 200 | 400 | ns |
| | 10 | 100 | 200 | |
| | 15 | 70 | 140 | |
| Transition Time: t _{THL} , t _{TLH} | 5 | 100 | 200 | ns |
| | 10 | 50 | 100 | |
| | 15 | 40 | 80 | |
| Input Capacitance, C _{IN} (Any Input) | - | 5 | 7.5 | pF |



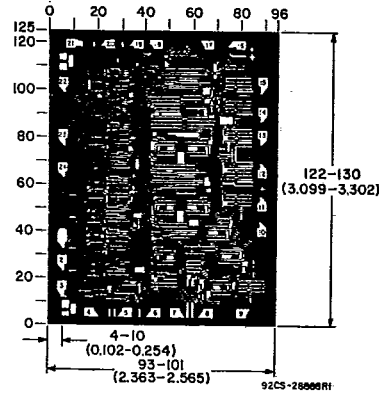
Top View

Terminal Assignment
(Active-low Data)

CD40181B Types

TABLE I
TRUTH TABLE

| FUNCTION SELECT | | | | INPUTS/OUTPUT ACTIVE LOW | | |
|-----------------|----|----|----|--------------------------|-------------------------------|--------------------------------------|
| | | | | LOGIC FUNCTION M = H | ARITHMETIC* FUNCTION M = L | |
| | | | | | C _n = L | C _n = H |
| S3 | S2 | S1 | S0 | | | |
| 0 | 0 | 0 | 0 | \bar{A} | A minus 1 | A |
| 0 | 0 | 0 | 1 | $\bar{A}\bar{B}$ | AB minus 1 | $\bar{A}\bar{B}$ |
| 0 | 0 | 1 | 0 | $\bar{A} + \bar{B}$ | $\bar{A}\bar{B}$ minus 1 | $\bar{A}\bar{B}$ |
| 0 | 0 | 1 | 1 | Logic 1 | minus 1 | Zero |
| 0 | 1 | 0 | 0 | $\bar{A} + \bar{B}$ | A plus (A + \bar{B}) | A plus (A + \bar{B}) plus 1 |
| 0 | 1 | 0 | 1 | \bar{B} | AB plus (A + \bar{B}) | AB plus (A + \bar{B}) plus 1 |
| 0 | 1 | 1 | 0 | $\bar{A} \oplus \bar{B}$ | A minus B minus 1 | A minus B |
| 0 | 1 | 1 | 1 | A + \bar{B} | A + \bar{B} | (A + \bar{B}) plus 1 |
| 1 | 0 | 0 | 0 | $\bar{A}\bar{B}$ | A plus (A + B) | A plus (A + B) plus 1 |
| 1 | 0 | 0 | 1 | A \oplus B | A plus B | A plus B plus 1 |
| 1 | 0 | 1 | 0 | B | $\bar{A}\bar{B}$ plus (A + B) | $\bar{A}\bar{B}$ plus (A + B) plus 1 |
| 1 | 0 | 1 | 1 | A + B | A + B | A + B plus 1 |
| 1 | 1 | 0 | 0 | Logic 0 | A plus A | A plus A plus 1 |
| 1 | 1 | 0 | 1 | $\bar{A}\bar{B}$ | $\bar{A}\bar{B}$ plus A | $\bar{A}\bar{B}$ plus A plus 1 |
| 1 | 1 | 1 | 0 | AB | $\bar{A}\bar{B}$ plus A | $\bar{A}\bar{B}$ plus A plus 1 |
| 1 | 1 | 1 | 1 | A | A | A plus 1 |



Dimensions and pad layout for CD40181BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

| FUNCTION SELECT | | | | INPUTS/OUTPUTS ACTIVE HIGH | | |
|-----------------|----|----|----|----------------------------|-------------------------------|--------------------------------------|
| | | | | LOGIC FUNCTION M = H | ARITHMETIC* FUNCTION M = L | |
| | | | | | C _n = H | C _n = L |
| S3 | S2 | S1 | S0 | | | |
| 0 | 0 | 0 | 0 | \bar{A} | A | A plus 1 |
| 0 | 0 | 0 | 1 | $\bar{A} + \bar{B}$ | A + B | (A + B) plus 1 |
| 0 | 0 | 1 | 0 | $\bar{A}\bar{B}$ | A + \bar{B} | (A + \bar{B}) plus 1 |
| 0 | 0 | 1 | 1 | Logic 0 | minus 1 | Zero |
| 0 | 1 | 0 | 0 | $\bar{A}\bar{B}$ | A plus $\bar{A}\bar{B}$ | A plus $\bar{A}\bar{B}$ plus 1 |
| 0 | 1 | 0 | 1 | \bar{B} | (A + B) plus $\bar{A}\bar{B}$ | (A + B) plus $\bar{A}\bar{B}$ plus 1 |
| 0 | 1 | 1 | 0 | $\bar{A} \oplus \bar{B}$ | A minus B minus 1 | A minus B |
| 0 | 1 | 1 | 1 | $\bar{A}\bar{B}$ | $\bar{A}\bar{B}$ minus 1 | $\bar{A}\bar{B}$ |
| 1 | 0 | 0 | 0 | $\bar{A} + \bar{B}$ | A plus AB | A plus AB plus 1 |
| 1 | 0 | 0 | 1 | $\bar{A} \oplus \bar{B}$ | A plus B | A plus B plus 1 |
| 1 | 0 | 1 | 0 | B | (A + \bar{B}) plus AB | (A + \bar{B}) plus AB plus 1 |
| 1 | 0 | 1 | 1 | AB | AB minus 1 | AB |
| 1 | 1 | 0 | 0 | Logic 1 | A plus A | A plus A plus 1 |
| 1 | 1 | 0 | 1 | A + \bar{B} | (A + B) plus A | (A + B) plus A plus 1 |
| 1 | 1 | 1 | 0 | A + B | (A + \bar{B}) plus A | (A + \bar{B}) plus A plus 1 |
| 1 | 1 | 1 | 1 | A | A minus 1 | A |

* Expressed as two's complement. 1 = HIGH LEVEL 0 = LOW LEVEL

CD40181B Types

TABLE II
AC TEST SETUP REFERENCE (ACTIVE-LOW DATA)

| TEST DELAY TIMES | AC PATHS | | DC DATA INPUTS | | MODE* |
|---|-----------------------|--------------------|---|---|-----------------|
| | INPUTS | OUTPUTS | TO V _{SS} | TO V _{DD} | |
| SUM _{IN} to SUM _{OUT} | $\overline{B0}$ | Any \overline{F} | $\overline{B1}, \overline{B2}, \overline{B3},$ M, C _n | All \overline{A} 's | ADD |
| SUM _{IN} to \overline{P} | $\overline{A0}$ | \overline{P} | $\overline{A1}, \overline{A2}, \overline{A3},$ M, C _n | All \overline{B} 's | ADD |
| SUM _{IN} to \overline{G} | $\overline{B0}$ | \overline{G} | All \overline{A} 's M, C _n | $\overline{B1}, \overline{B2}, \overline{B3}$ | ADD |
| SUM _{IN} to C _{n+4} | $\overline{B0}$ | C _{n+4} | All \overline{A} 's, M, C _n | $\overline{B1}, \overline{B2}, \overline{B3}$ | ADD |
| C _n to SUM _{OUT} | C _n | Any \overline{F} | All \overline{A} 's, M | All \overline{B} 's | ADD |
| C _n to C _{n+4} | C _n | C _{n+4} | All \overline{A} 's, M | All \overline{B} 's | ADD |
| SUM _{IN} to A = B | $\overline{B0}$ | A = B | All \overline{A} 's, $\overline{B1}, \overline{B2}, \overline{B3},$ M | C _n | SUBTRACT |
| SUM _{IN} to SUM _{OUT} (Logic Mode) | All \overline{B} 's | Any \overline{F} | All \overline{A} 's, C _n | M | EXCLUSIVE OR |

* ADD Mode: S0, S3 = V_{DD}; S1, S2 = V_{SS}.

SUBTRACT Mode: S0, S3 = V_{SS}; S1, S2 = V_{DD}.

TABLE III
MAGNITUDE COMPARISON

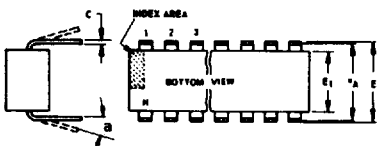
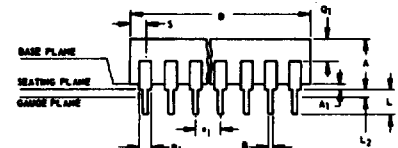
ACTIVE - HIGH DATA ACTIVE - LOW DATA

| INPUT C _n | OUTPUT C _{n+4} | MAGNITUDE | INPUT C _n | OUTPUT C _{n+4} | MAGNITUDE |
|----------------------|-------------------------|-----------|----------------------|-------------------------|-----------|
| 1 | 1 | A ≤ B | 0 | 0 | A ≤ B |
| 0 | 1 | A < B | 1 | 0 | A < B |
| 1 | 0 | A > B | 0 | 1 | A > B |
| 0 | 0 | A ≥ B | 1 | 1 | A ≥ B |

1 = HIGH LEVEL
0 = LOW LEVEL

Dimensional Outlines

Dual-In-Line Welded-Seal Ceramic Packages



- NOTES:**
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
- When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
 - Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
 - e_A applies in zone L₂ when unit installed.
 - a applies to spread leads prior to installation.
 - N is the maximum quantity of lead positions.
 - N₁ is the quantity of allowable missing leads.

(D) SUFFIX (JEDEC MO-001-AD)
14-Lead Dual-In-Line Welded-Seal Ceramic Package

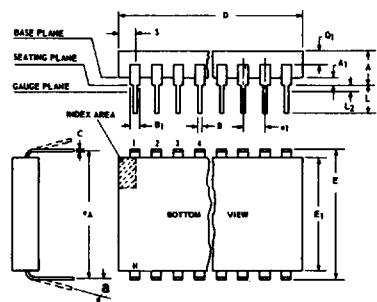
| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|----------------|----------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.120 | 0.160 | | 3.05 | 4.06 |
| A ₁ | 0.020 | 0.065 | | 0.51 | 1.65 |
| B | 0.014 | 0.020 | | 0.356 | 0.508 |
| B ₁ | 0.060 | 0.065 | | 1.27 | 1.65 |
| C | 0.008 | 0.012 | 1 | 0.204 | 0.304 |
| D | 0.745 | 0.770 | | 18.93 | 19.55 |
| E | 0.300 | 0.325 | | 7.62 | 8.25 |
| E ₁ | 0.240 | 0.260 | | 6.10 | 6.60 |
| e ₁ | 0.100 TP | | 2 | 2.54 TP | |
| e _A | 0.300 TP | | 2, 3 | 7.62 TP | |
| L | 0.125 | 0.150 | | 3.18 | 3.81 |
| L ₂ | 0.000 | 0.030 | | 0.000 | 0.76 |
| a | 0° | 15° | 4 | 0° | 15° |
| N | 14 | | 5 | 14 | |
| N ₁ | 0 | | 6 | 0 | |
| Q ₁ | 0.050 | 0.085 | | 1.27 | 2.15 |
| S | 0.065 | 0.090 | | 1.66 | 2.28 |

92SS-4411R2

(D) SUFFIX (JEDEC MO-001-AE)
16-Lead Dual-In-Line Welded-Seal Ceramic Package

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|----------------|----------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.120 | 0.160 | | 3.05 | 4.06 |
| A ₁ | 0.020 | 0.065 | | 0.51 | 1.65 |
| B | 0.014 | 0.020 | | 0.356 | 0.508 |
| B ₁ | 0.035 | 0.065 | | 0.89 | 1.65 |
| C | 0.008 | 0.012 | 1 | 0.204 | 0.304 |
| D | 0.745 | 0.785 | | 18.93 | 19.93 |
| E | 0.300 | 0.325 | | 7.62 | 8.25 |
| E ₁ | 0.240 | 0.260 | | 6.10 | 6.60 |
| e ₁ | 0.100 TP | | 2 | 2.54 TP | |
| e _A | 0.300 TP | | 2, 3 | 7.62 TP | |
| L | 0.125 | 0.150 | | 3.18 | 3.81 |
| L ₂ | 0.000 | 0.030 | | 0.000 | 0.76 |
| a | 0° | 15° | 4 | 0° | 15° |
| N | 16 | | 5 | 16 | |
| N ₁ | 0 | | 6 | 0 | |
| Q ₁ | 0.050 | 0.085 | | 1.27 | 2.15 |
| S | 0.015 | 0.060 | | 0.39 | 1.52 |

92SS-4266R5



- NOTES:**
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
- When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
 - Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
 - e_A applies in zone L₂ when unit installed.
 - a applies to spread leads prior to installation.
 - N is the maximum quantity of lead positions.
 - N₁ is the quantity of allowable missing leads.

(D) SUFFIX (JEDEC MO-015-AG)
24-Lead Dual-In-Line Welded-Seal Ceramic Package

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|----------------|----------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.090 | 0.200 | | 2.29 | 5.08 |
| A ₁ | 0.020 | 0.070 | | 0.51 | 1.78 |
| B | 0.015 | 0.020 | | 0.381 | 0.508 |
| B ₁ | 0.045 | 0.055 | | 1.143 | 1.397 |
| C | 0.008 | 0.012 | 1 | 0.204 | 0.304 |
| D | 1.15 | 1.22 | | 29.21 | 30.98 |
| E | 0.600 | 0.625 | | 15.24 | 15.87 |
| E ₁ | 0.480 | 0.520 | | 12.20 | 13.20 |
| e ₁ | 0.100 TP | | 2 | 2.54 TP | |
| e _A | 0.600 TP | | 2, 3 | 15.24 TP | |
| L | 0.100 | 0.180 | | 2.54 | 4.57 |
| L ₂ | 0.000 | 0.030 | | 0.00 | 0.76 |
| a | 0° | 15° | 4 | 0° | 15° |
| N | 24 | | 5 | 24 | |
| N ₁ | 0 | | 6 | 0 | |
| Q ₁ | 0.020 | 0.080 | | 0.51 | 2.03 |
| S | 0.020 | 0.060 | | 0.51 | 1.52 |

92CS-19948R4

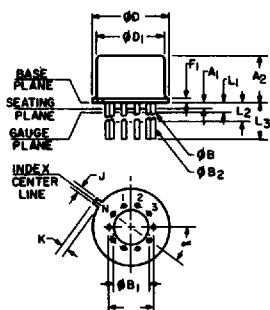
(D) SUFFIX (JEDEC MO-015-AH)
28-Lead Dual-In-Line Welded-Seal Ceramic Package

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|----------------|----------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.090 | 0.200 | | 2.29 | 5 |
| A ₁ | 0 | 0.070 | 2 | 0 | 1.77 |
| B | 0.015 | 0.020 | | 0.381 | 0.508 |
| B ₁ | 0.015 | 0.065 | | 0.39 | 1.39 |
| C | 0.008 | 0.012 | 1 | 0.204 | 0.304 |
| D | 1.380 | 1.420 | | 35.06 | 36.06 |
| E | 0.600 | 0.625 | | 15.24 | 15.87 |
| E ₁ | 0.485 | 0.515 | | 12.32 | 13.08 |
| e ₁ | 0.100 TP | | 2 | 2.54 TP | |
| e _A | 0.600 TP | | 2, 3 | 15.24 TP | |
| L | 0.100 | 0.200 | | 2.6 | 5 |
| L ₂ | 0 | 0.030 | | 0 | 0.76 |
| a | 0° | 15° | 4 | 0° | 15° |
| N | 28 | | 5 | 28 | |
| N ₁ | 0 | | 6 | 0 | |
| Q ₁ | 0.020 | 0.070 | | 0.51 | 1.77 |
| S | 0.040 | 0.070 | | 1.02 | 1.77 |

92CM-20250R2

TO-5 Style Package

(T) SUFFIX (JEDEC MO-006-AG)
12-Lead Metal Package



92CS-19774

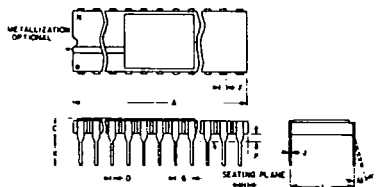
| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|-----------------|--------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| a | 0.230 | | 2 | 5.84 TP | |
| A ₁ | 0 | 0 | | 0 | 0 |
| A ₂ | 0.165 | 0.185 | | 4.19 | 4.70 |
| φB | 0.016 | 0.019 | 3 | 0.407 | 0.482 |
| φB ₁ | 0 | 0 | | 0 | 0 |
| φB ₂ | 0.016 | 0.021 | 3 | 0.407 | 0.533 |
| φD | 0.335 | 0.370 | | 8.51 | 9.39 |
| φD ₁ | 0.305 | 0.335 | | 7.75 | 8.50 |
| F ₁ | 0.020 | 0.040 | | 0.51 | 1.01 |
| j | 0.028 | 0.034 | | 0.712 | 0.863 |
| k | 0.029 | 0.045 | 4 | 0.74 | 1.14 |
| L ₁ | 0.000 | 0.050 | 3 | 0.00 | 1.27 |
| L ₂ | 0.250 | 0.500 | 3 | 6.4 | 12.7 |
| L ₃ | 0.500 | 0.562 | 3 | 12.7 | 14.27 |
| a | 30° TP | | | 30° TP | |
| N | 12 | | 6 | 12 | |
| N ₁ | 1 | | 5 | 1 | |

NOTES:

- Refer to Rules for Dimensioning Axial Lead Product Outlines.
- Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
- φB applies between L₁ and L₂. φB₂ applies between L₂ and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L₁ and beyond 0.500" (12.70 mm).
- Measure from Max. φD.
- N₁ is the quantity of allowable missing leads.
- N is the maximum quantity of lead positions.

Dimensional Outlines (Cont'd)

DUAL-IN-LINE SIDE-BRAZED CERAMIC PACKAGES



(D) SUFFIX
18-Lead Dual-In-Line
Side-Brazed Ceramic Package

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|--------|--------|-------|------|-------------|--------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.890 | 0.915 | | 22.606 | 23.241 |
| C | - | 0.200 | | - | 5.080 |
| D | 0.015 | 0.021 | | 0.381 | 0.533 |
| F | 0.054 | REF. | 1 | 1.371 | REF. |
| G | 0.100 | BSC | 1 | 2.54 | BSC |
| H | 0.035 | 0.065 | | 0.889 | 1.651 |
| J | 0.008 | 0.012 | 3 | 0.203 | 0.304 |
| K | 0.125 | 0.150 | | 3.175 | 3.810 |
| L | 0.290 | 0.310 | 2 | 7.366 | 7.874 |
| M | 0° | 15° | | 0° | 15° |
| P | 0.025 | 0.045 | | 0.635 | 1.143 |
| N | 18 | | | 18 | |

92CS-27231R1

(D) SUFFIX
22-Lead Dual-In-Line
Side-Brazed Ceramic Package

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|--------|--------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 1.065 | 1.100 | | 27.05 | 27.94 |
| C | 0.085 | 0.145 | | 2.16 | 3.68 |
| D | 0.017 | 0.023 | | 0.43 | 0.58 |
| F | 0.040 | REF. | 1 | 1.02 | REF. |
| G | 0.100 | BSC | 1 | 2.54 | BSC |
| H | 0.030 | 0.070 | | 0.76 | 1.78 |
| J | 0.008 | 0.012 | 3 | 0.20 | 0.30 |
| K | 0.125 | 0.175 | | 3.18 | 4.45 |
| L | 0.380 | 0.420 | 2 | 9.65 | 10.67 |
| M | - | 7° | | - | 7° |
| P | 0.025 | 0.050 | | 0.64 | 1.27 |
| N | 22 | | | 22 | |

92CS-25186R2

NOTES:

- Leads within 0.005" (0.13 mm)-radius of True Position at maximum material condition.
- Dimension "L" to center of leads when formed parallel.
- When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

(D) SUFFIX
24-Lead Dual-In-Line
Side-Brazed Ceramic Package

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|--------|--------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 1.180 | 1.220 | | 29.98 | 30.98 |
| C | 0.085 | 0.145 | | 2.16 | 3.68 |
| D | 0.015 | 0.023 | | 0.39 | 0.58 |
| F | 0.040 | REF. | | 1.02 | REF. |
| G | 0.100 | BSC | 1 | 2.54 | BSC |
| H | 0.030 | 0.070 | | 0.77 | 1.77 |
| J | 0.008 | 0.012 | 3 | 0.21 | 0.30 |
| K | 0.125 | 0.175 | | 3.18 | 4.44 |
| L | 0.580 | 0.620 | 2 | 14.74 | 15.74 |
| M | - | 7° | | - | 7° |
| P | 0.025 | 0.050 | | 0.64 | 1.27 |
| N | 24 | | | 24 | |

92CS-30968R1

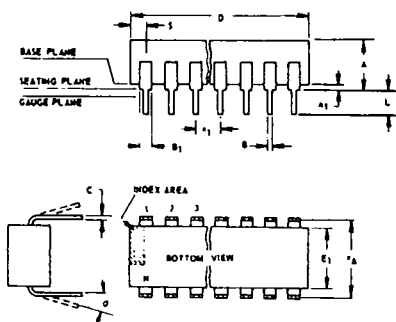
(D) SUFFIX
40-Lead Dual-In-Line
Side-Brazed Ceramic Package

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|--------|--------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 1.980 | 2.020 | | 50.30 | 51.30 |
| C | 0.095 | 0.155 | | 2.43 | 3.93 |
| D | 0.017 | 0.023 | | 0.43 | 0.58 |
| F | 0.050 | REF. | | 1.27 | REF. |
| G | 0.100 | BSC | 1 | 2.54 | BSC |
| H | 0.030 | 0.070 | | 0.76 | 1.78 |
| J | 0.008 | 0.012 | 3 | 0.20 | 0.30 |
| K | 0.125 | 0.175 | | 3.18 | 4.45 |
| L | 0.580 | 0.620 | 2 | 14.74 | 15.74 |
| M | - | 7° | | - | 7° |
| P | 0.025 | 0.050 | | 0.64 | 1.27 |
| N | 40 | | | 40 | |

92CM-27029R2

Dual-In-Line Plastic and Frit-Seal Ceramic Packages

(E) SUFFIX (JEDEC MO-001-AN)
8-Lead Dual-In-Line Plastic
(Mini-DIP) Package



| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|----------------|--------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.155 | 0.200 | | 3.94 | 5.08 |
| A ₁ | 0.020 | 0.050 | | 0.508 | 1.27 |
| B | 0.014 | 0.020 | | 0.356 | 0.508 |
| B ₁ | 0.035 | 0.065 | | 0.889 | 1.65 |
| C | 0.008 | 0.012 | 1 | 0.203 | 0.304 |
| D | 0.370 | 0.400 | | 9.40 | 10.16 |
| E | 0.300 | 0.325 | | 7.62 | 8.25 |
| E ₁ | 0.240 | 0.260 | | 6.10 | 6.60 |
| e ₁ | 0.100 | TP | 2 | 2.54 | TP |
| e _A | 0.300 | TP | 2, 3 | 7.62 | TP |
| L | 0.125 | 0.150 | | 3.18 | 3.81 |
| L ₂ | 0.000 | 0.030 | | 0.000 | 0.762 |
| a | 0 | 15 | 4 | 0 | 15 |
| N | 8 | | 5 | 8 | |
| N ₁ | 0 | | 6 | 0 | |
| O ₁ | 0.040 | 0.075 | | 1.02 | 1.90 |
| S | 0.015 | 0.060 | | 0.381 | 1.52 |

92CS-24026 R1

NOTES:

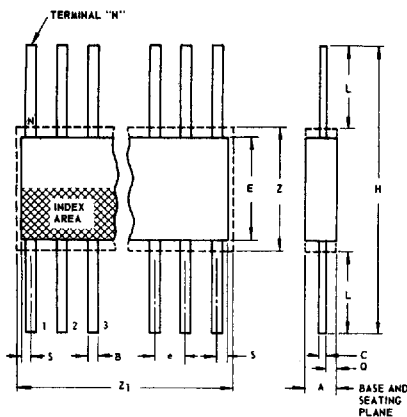
- Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
- When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
 - Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
 - e_A applies in zone L₂ when unit installed.
 - a applies to spread leads prior to installation.
 - N is the maximum quantity of lead positions.
 - N₁ is the quantity of allowable missing leads.

T-90-20

Dimensional Outlines (Cont'd)

Ceramic Flat Packs

**(K) SUFFIX (JEDEC MO-004-AF)
14-Lead**



| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|----------------|----------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.008 | 0.100 | | 0.21 | 2.54 |
| B | 0.015 | 0.019 | 1 | 0.381 | 0.482 |
| C | 0.003 | 0.006 | 1 | 0.077 | 0.152 |
| e | 0.050 TP | | 2 | 1.27 TP | |
| E | 0.200 | 0.300 | | 5.1 | 7.6 |
| H | 0.600 | 1.000 | | 15.3 | 25.4 |
| L | 0.150 | 0.350 | | 3.9 | 8.8 |
| N | 14 | | 3 | 14 | |
| Q | 0.005 | 0.050 | | 0.13 | 1.27 |
| S | 0.000 | 0.050 | | 0.00 | 1.27 |
| Z | 0.300 | | 4 | 7.62 | |
| Z ₁ | 0.400 | | 4 | 10.16 | |

9288-4300R3

NOTES:

1. Refer to JEDEC Publication No. 95 for Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z₁ determine a zone within which all body and lead irregularities lie.

**(K) SUFFIX (JEDEC MO-004-AG)
16-Lead**

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|----------------|----------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.008 | 0.100 | | 0.21 | 2.54 |
| B | 0.015 | 0.019 | 1 | 0.381 | 0.482 |
| C | 0.003 | 0.006 | 1 | 0.077 | 0.152 |
| e | 0.050 TP | | 2 | 1.27 TP | |
| E | 0.200 | 0.300 | | 5.1 | 7.6 |
| H | 0.600 | 1.000 | | 15.3 | 25.4 |
| L | 0.150 | 0.350 | | 3.9 | 8.8 |
| N | 16 | | 3 | 16 | |
| Q | 0.005 | 0.050 | | 0.13 | 1.27 |
| S | 0.000 | 0.025 | | 0.00 | 0.63 |
| Z | 0.300 | | 4 | 7.62 | |
| Z ₁ | 0.400 | | 4 | 10.16 | |

92CS-17271R3

**(K) SUFFIX
24-Lead**

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|----------------|----------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.075 | 0.120 | | 1.91 | 3.04 |
| B | 0.018 | 0.022 | 1 | 0.458 | 0.558 |
| C | 0.004 | 0.007 | 1 | 0.102 | 0.177 |
| e | 0.050 TP | | 2 | 1.27 TP | |
| E | 0.600 | 0.700 | | 15.24 | 17.78 |
| H | 1.150 | 1.350 | | 29.21 | 34.29 |
| L | 0.225 | 0.325 | | 5.72 | 8.25 |
| N | 24 | | 3 | 24 | |
| Q | 0.035 | 0.070 | | 0.89 | 1.77 |
| S | 0.060 | 0.110 | 1 | 1.53 | 2.79 |
| Z | 0.700 | | 4 | 17.78 | |
| Z ₁ | 0.750 | | 4 | 19.05 | |

92CS-19949R2

**(K) SUFFIX
28-Lead**

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|----------------|----------|-------|------|-------------|-------|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.075 | 0.120 | | 1.91 | 3.04 |
| B | 0.018 | 0.022 | 1 | 0.458 | 0.558 |
| C | 0.004 | 0.007 | 1 | 0.102 | 0.177 |
| e | 0.050 TP | | 2 | 1.27 TP | |
| E | 0.600 | 0.700 | | 15.24 | 17.78 |
| H | 1.150 | 1.350 | | 29.21 | 34.29 |
| L | 0.225 | 0.325 | | 5.72 | 8.25 |
| N | 28 | | 3 | 28 | |
| Q | 0.035 | 0.070 | | 0.89 | 1.77 |
| S | 0 | 0.060 | 1 | 0 | 1.53 |
| Z | 0.700 | | 4 | 17.78 | |
| Z ₁ | 0.750 | | 4 | 19.05 | |

92CS-20972