

## CMOS Quad 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

**Features:**

- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25° C
- Noise margin (full package-temperature range) =
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- 5-V, 10-V, and 15-V parametric ratings

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Output compatible with two HTL loads, two low power TTL loads, or one low power Schottky TTL load
- Functional equivalent to TTL 74175
- Standardized symmetrical output characteristics

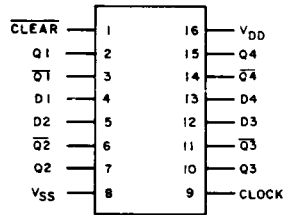
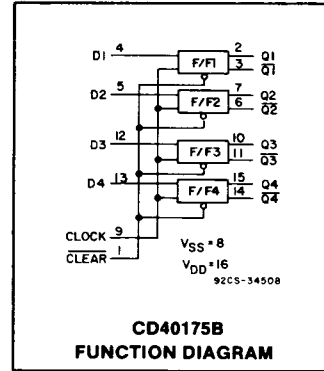
**Applications:**

- Shift registers
- Buffer/storage registers
- Pattern generators

■ CD40175B consists of four identical D-type flip-flops. Each flip-flop has an independent DATA D input and complementary Q and  $\bar{Q}$  outputs. The CLOCK and CLEAR inputs are common to all flip-flops. Data are transferred to the Q outputs on the positive-going transition of the clock pulse. All four flip-flops are simultaneously reset by a low level on the CLEAR input.

These devices can function as shift register elements or as T-type flip-flops for toggle and counter applications.

The CD40175B is supplied in hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



$V_{DD}$  = PIN 16  
 $V_{SS}$  = PIN 8  
 92CS-34507

**TERMINAL ASSIGNMENT**

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	.....	-0.5V to +20V
Voltages referenced to $V_{SS}$ Terminal	.....	-0.5V to $V_{DD} + 0.5V$
INPUT VOLTAGE RANGE, ALL INPUTS	.....	$\pm 10$ mA
DC INPUT CURRENT, ANY ONE INPUT	.....	.....
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	.....	.....
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	.....	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	.....	Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	.....	.....
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	.....	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	.....	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	.....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	.....	.....
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max	.....	$+265^\circ\text{C}$



## CD40175B Types

### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current Max.	—	0, 5	5	1	1	30	30	—	0.02	1	μA
I <sub>DD</sub>	—	0, 10	10	2	2	60	60	—	0.02	2	
	—	0, 15	15	4	4	120	120	—	0.02	4	
—	0, 20	20	20	20	600	600	—	0.04	20	↕	
Output Low (Sink) Current Min.	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
I <sub>OL</sub>	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
—	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current Min.	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
I <sub>OH</sub>	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
—	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level Max.	—	0, 5	5	0.05				—	0	0.05	V
V <sub>OL</sub>	—	0, 10	10	0.05				—	0	0.05	
	—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min.	—	0, 5	5	4.95				4.95	5	—	V
V <sub>OH</sub>	—	0, 10	10	9.95				9.95	10	—	
	—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
V <sub>IL</sub>	1, 9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V
V <sub>IH</sub>	1, 9	—	10	7				7	—	—	
	1.5, 13.5	—	15	11				11	—	—	
Input Current Max.	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA

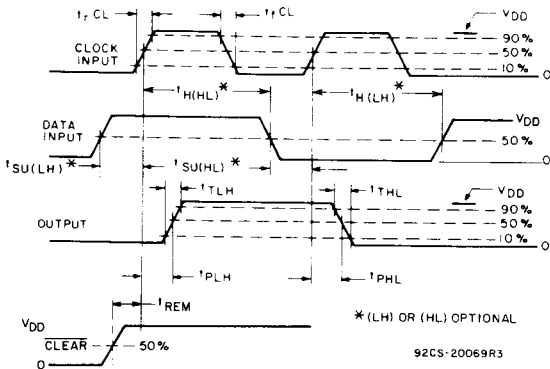


Fig. 2 - Definition of setup, hold, propagation delay, and removal times.

TRUTH TABLE FOR 1 OF 4 FLIP-FLOPS (Positive Logic)

INPUTS			OUTPUTS	
CLOCK	DATA	CLEAR	Q	$\bar{Q}$
	0	1	0	1
	1	1	1	0
	X	1	Q	$\bar{Q}$
X	X	0	0	1

1=High Level      X=Don't Care      0=Low Level

92CS-20069R3

## CD40175B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC		TEST CONDITIONS $V_{DD}$ (V)	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Transition Time	$t_{THL}, t_{TLH}$	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time Clock to Q Output	$t_{PHL}, t_{PLH}$	5	—	220	400	
		10	—	90	160	
		15	—	70	120	
Propagation Delay Time $\overline{\text{CLEAR}}$ to Q Output	$t_{PHL}$	5	—	325	500	
		10	—	130	200	
		15	—	100	150	
Minimum Pulse Width Clock	$t_{WH}$	5	—	110	250	
		10	—	45	100	
		15	—	35	75	
$\overline{\text{Clear}}$	$t_{WL}$	5	—	100	200	
		10	—	40	80	
		15	—	30	60	
Maximum Clock Frequency	$f_{CL}$	5	2	4.5	—	MHz
		10	5	11	—	
		15	6.5	14	—	
Maximum Clock Rise or Fall Time	$t_{rCL}, t_{fCL}$	5	15	—	—	$\mu\text{s}$
		10	15	—	—	
		15	15	—	—	
Minimum Data Setup Time	$t_{SU}$	5	—	60	120	ns
		10	—	25	50	
		15	—	20	40	
Minimum Data Hold Time	$t_H$	5	—	40	80	
		10	—	20	40	
		15	—	15	30	
Minimum $\overline{\text{Clear}}$ Removal Time ‡	$t_{REM}$	5	—	125	250	
		10	—	50	100	
		15	—	40	80	
Input Capacitance	$C_{IN}$	—	—	5	7.5	pF

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COMMERCIAL CMOS  
HIGH VOLTAGE ICs

‡  $\overline{\text{CLEAR}}$  signal must be high prior to positive-going transition of  $\text{CLOCK}$  pulse.

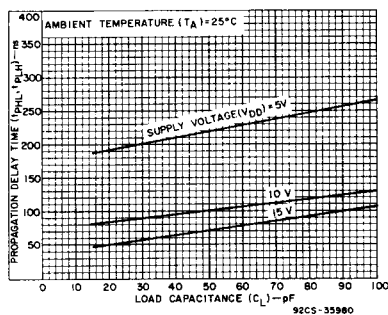


Fig. 3 - Typical propagation delay time (CLOCK to OUTPUT) as a function of load capacitance.

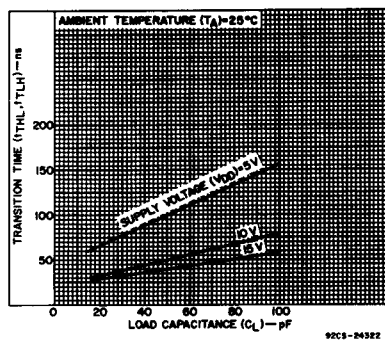


Fig. 4 - Typical transition time as a function of load capacitance.

# CD40175B Types

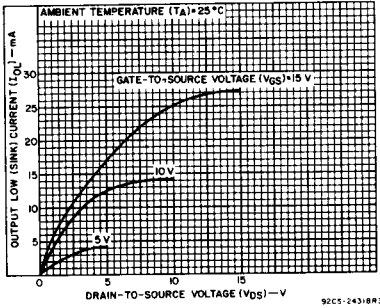


Fig. 5 - Typical output low (sink) current characteristics.

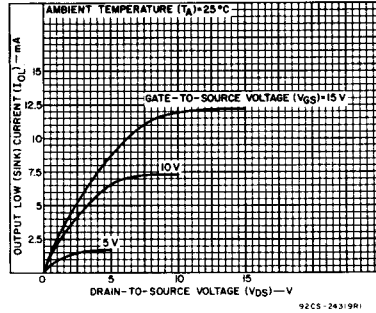


Fig. 6 - Minimum output low (sink) current characteristics.

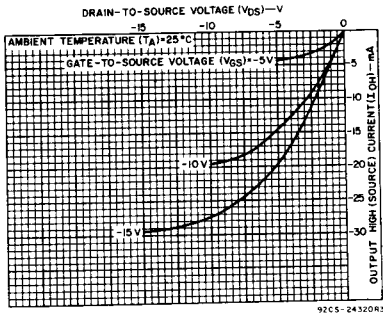


Fig. 7 - Typical output high (source) current characteristics.

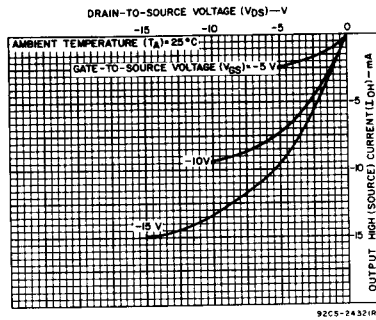


Fig. 8 - Minimum output high (source) current characteristics.

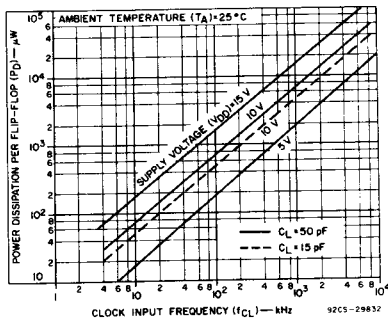


Fig. 9 - Typical dynamic power dissipation as a function of CLOCK frequency.

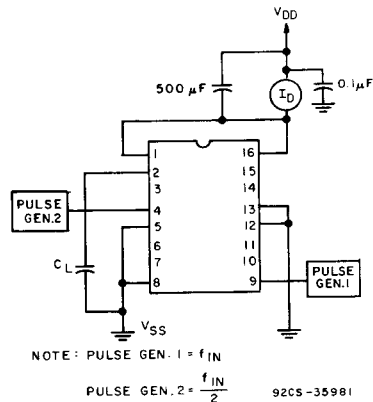


Fig. 10 - Dynamic power dissipation test circuit.

## CD40175B Types

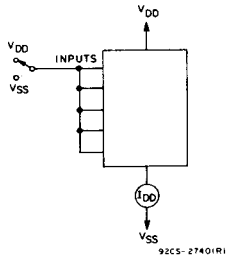


Fig. 11 - Quiescent device current test circuit.

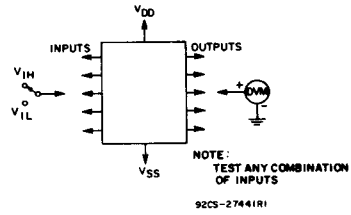


Fig. 12 - Noise immunity test circuit.

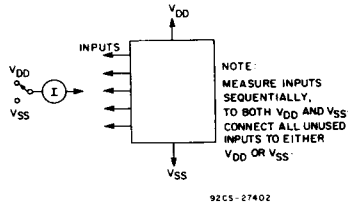
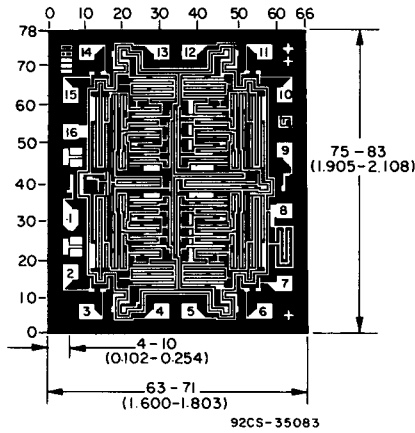


Fig. 13 - Input leakage current test circuit.



Dimensions and pad layout for CD40175BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).