

CMOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter

Features:

- Eight inverting channels with conversion from V_{DD} to V_{CC} or V_{CC} to V_{DD} ($4V \leq V_{DD} \leq 12V$ and $4V \leq V_{CC} \leq V_{DD}$)
- Three operating modes:
 CMOS-to-TTL level conversion
 TTL-to-CMOS level conversion
 Interface off; high-impedance on both sides

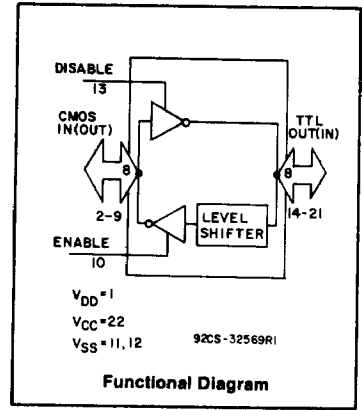
The RCA-CD40116 is a high-speed 8-bit integrated circuit designed to interface CMOS logic levels with TTL logic levels on the data bus of microprocessor-based systems. CMOS/TTL interface is provided by eight parallel bidirectional buffer/level converters. Buffer INPUT/OUTPUT terminals are either inputs or outputs depending on the desired direction of data flow.

A low level on the DISABLE input with the ENABLE input either high or low, permits conversion of CMOS inputs to TTL outputs. A high level on both the DISABLE and ENABLE inputs permits data flow from TTL inputs to CMOS outputs. A low level on the ENABLE input and a high level on the DISABLE input sets both inputs/outputs to the high-impedance state.

The TTL Input/Output terminals and the ENABLE and DISABLE control inputs are TTL-compatible without the use of external pull-up resistors. The TTL input logic 0 to logic 1 transition occurs at a level of approximately 1.5 volts. The ENABLE and DISABLE inputs may be driven to the V_{DD} rail; therefore, either TTL or CMOS logic drivers, capable of sinking one TTL load, may be used to determine the direction of data flow. The large CMOS and TTL output buffers in this device have high output sink and source current capability and can drive the data bus capacitance with a transition time of approximately 0.25 ns/pF. This fast output transition time, together with the small propagation delay time of the device, allow high-speed operation.

Pin 12 is an additional V_{SS} Pin which is connected directly to the TTL-to-CMOS converters to avoid oscillation in these amplifiers. Pin 12 is connected to Pin 11 through a poly resistor which isolated Pin 12 from V_{SS} switching noise (ground noise).

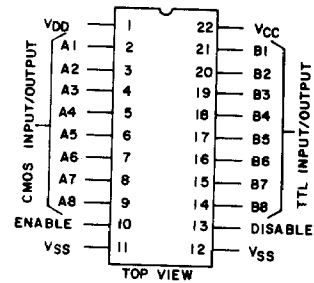
The CD40116 is supplied in a 22-lead hermetic dual-in-line ceramic package (D suffix), 22-lead plastic package (E suffix), and in chip form (H suffix).



- Low propagation delay time:
 CMOS-to-TTL conversion - 25 ns typ.
 TTL-to-CMOS conversion - 30 ns typ.
 ($V_{DD} = 12V$, $V_{CC} = 5V$)
- High TTL sink current - 11 mA typ.
- No external TTL input pull-up resistors required
- High speed drive of large data bus capacitances
- Input/output and power supply terminals located for ease of PC board layout

Applications:

- Interface CMOS microprocessor with TTL memories and peripheral devices
- Interface between and within logic systems which combine CMOS and TTL devices



92CS-30245

TERMINAL ASSIGNMENT

CD40116 Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE (Voltage reference to V_{SS} Terminal)	
V_{DD}	-0.5 to +12.6 V*
V_{CC}	-0.5 to V_{DD}
INPUT VOLTAGE RANGE:	
Data Inputs, CMOS to TTL	-0.5 to $V_{DD} + 0.5$ V
Data Inputs, TTL to CMOS	-0.5 to $V_{CC} + 0.5$ V
Enable, Disable Inputs	-0.5 to $V_{DD} + 0.5$ V
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40^\circ\text{C}$ to $+60^\circ\text{C}$ (E)	500 mW
For $T_A = +60^\circ\text{C}$ to $+85^\circ\text{C}$ (E)	Derate linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ (D)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (D)	Derate linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For $T_A =$ Full Package-Temperature Range	100 mW
OPERATING TEMPERATURE RANGE (T_A)	
Package Type D	-55 to $+125^\circ\text{C}$
Package Type E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance of 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm)	
from case for 10 s max	$+265^\circ\text{C}$

*At 125°C V_{DD} should not exceed +12 V.

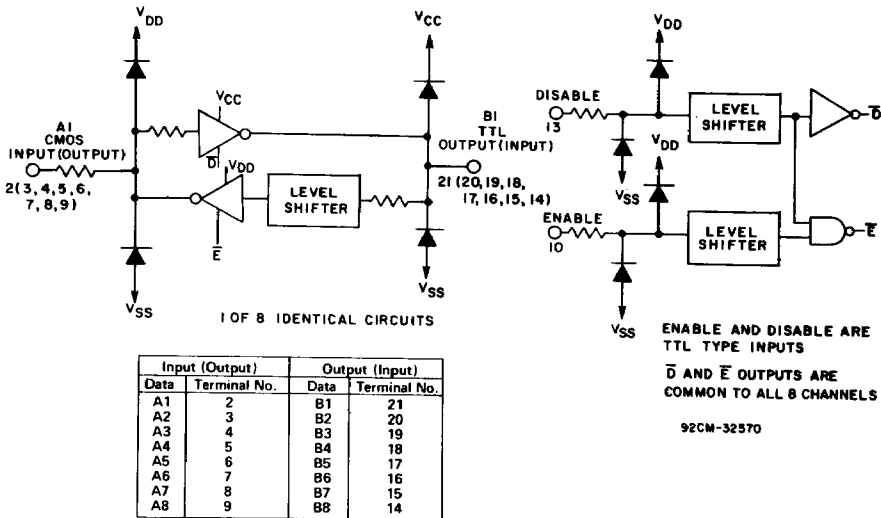


Fig. 1 - Functional block diagram.

TRUTH TABLE

ENABLE	DISABLE	FUNCTION
X	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z)

0 = Low Level 1 = High Level X = Don't Care

Z = High Impedance on both CMOS and TTL sides.

See Operating and Handling Considerations — Bypassing and Unused Inputs.

CD40116 Types

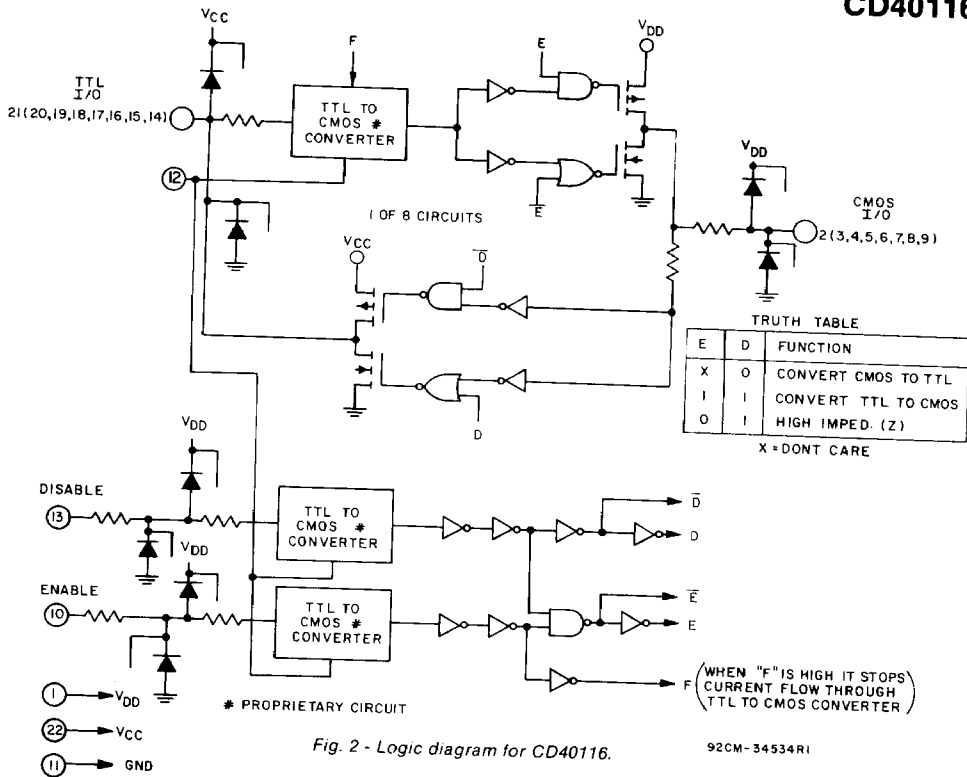


Fig. 2 - Logic diagram for CD40116.

STATIC CHARACTERISTICS $V_{DD} = 12\text{ V}$, $V_{CC} = 5\text{ V}$

CHARACTERISTIC	TEST CONDITIONS	Limits at Indicated Temperatures ($^{\circ}\text{C}$)							UNITS
		Values at -55, +25, +125 for D, H Packages				Values at -40, +25, +85 for E Packages			
		-55	-40	+85	+125	+25			
		MIN.	TYP.	MAX.					
Quiescent Device Current, From V_{DD} Supply, $I_{DD}\text{ MAX}$ From V_{CC} Supply, $I_{CC}\text{ MAX}$	ENABLE = 1	5	5	5	5	—	1	5	mA
	ENABLE = 0	5	5	5	5	—	0.2	5	
Data Flow — CMOS Inputs to TTL Outputs									
Input Current, $I_{IN}\text{ MAX}$	$V_{IN} = 0, 12\text{ V};$ Any CMOS input	± 60	± 60	± 60	± 60	—	± 5	± 60	μA
Output Current, $I_{OH}\text{ MIN}$ $I_{OL}\text{ MIN}$	$V_{OH} = 3\text{ V},$ $V_{IL} = 2\text{ V}$	-7.5	-7	-4.9	-4.2	-6	-12	—	mA
	$V_{OL} = 0.4\text{ V},$ $V_{IH} = 10\text{ V}$	7.5	7	4.9	4.2	6	11	—	
TTL 3-State Output Leakage Current $I_{OUT}\text{ MAX}$	ENABLE = 1 ENABLE = 0	-500 ± 100	-500 ± 100	-500 ± 100	-500 ± 100	— —	-250 ± 5	-500 ± 100	μA
Data Flow — TTL Inputs to CMOS Outputs									
Input Current, $I_{IL}\text{ MAX}$ $I_{IH}\text{ MAX}$ $I_{IH}\text{ MAX}$	$V_{IL} = 0\text{ to }0.7\text{ V};$	-500	-500	-500	-500	—	-250	-500	μA
	$V_{IH} = 2.3\text{ V};$	-450	-350	-350	-350	—	-175	-350	
	$V_{IH} = 5\text{ V};$ Any TTL input	+100	+100	+100	+100	—	+50	+100	
Output Current, $I_{OH}\text{ MIN}$ $I_{OL}\text{ MIN}$	$V_{OH} = 11.5\text{ V},$ $V_{IL} = 0.7\text{ V}$	-4.3	-4.2	-2.9	-2.5	-3.5	-6.5	—	mA
	$V_{OL} = 0.5\text{ V},$ $V_{IH} = 2.3\text{ V}$	4.3	4.2	2.9	2.5	3.5	6.5	—	
CMOS 3-State Output Leakage Current $I_{OUT}\text{ MAX}$	$V_O = 0, 12\text{ V},$ $V_{IN} = 0, 5\text{ V}$	± 60	± 60	± 60	± 60	—	± 5	± 60	μA
Enable and Disable Inputs									
Input Current, $I_{IL}\text{ MAX}$ $I_{IH}\text{ MAX}$ $I_{IH}\text{ MAX}$	$V_{IL} = 0\text{ to }0.7\text{ V}$	-500	-500	-500	-500	—	-250	-500	μA
	$V_{IH} = 2.3\text{ (TTL)}$	-450	-350	-350	-350	—	-175	-350	
	$V_{IH} = 12\text{ V (CMOS)}$	60	60	60	60	—	5	60	

CD40116 Types

DYNAMIC ELECTRICAL CHARACTERISTICS AT $T_A = 25^\circ\text{C}$; $V_{DD} = 12\text{ V}$, $V_{CC} = 5\text{ V}$

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
	INPUT	OUTPUT	$C_L = 50\text{ pF}$		$C_L = 200\text{ pF}$	
			TYP	MAX	TYP	
Propagation Delay Times, Data-In to Data-Out, t_{PHL} , t_{PLH}	CMOS TTL	TTL CMOS	25 30	35 45	35 50	ns
Disable to TTL Out, $t_{PHZ/LZ}$ $t_{PZH/ZL}$			30 35	45 50	30 35	ns
Enable to CMOS Out, $t_{PHZ/LZ}$ $t_{PZH/ZL}$			20 45	30 60	20 45	ns
Transition Time, t_{THL} , t_{TLH}	CMOS TTL	TTL CMOS	20 20	40 40	55 55	ns

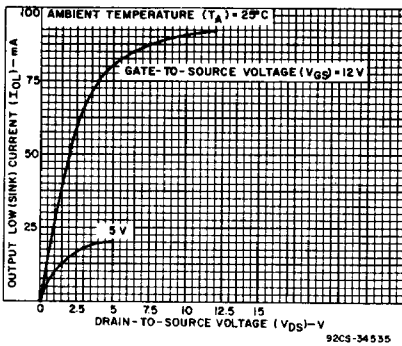


Fig. 3 - Typical N-Channel output low (sink) current characteristics - CMOS to TTL.

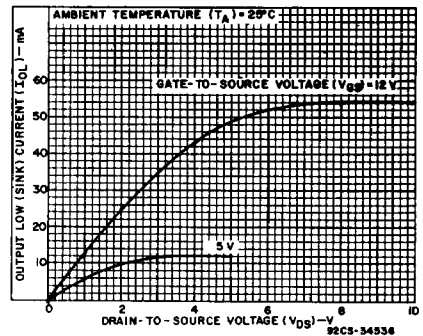


Fig. 4 - Typical output low (sink) current characteristics - TTL to CMOS.

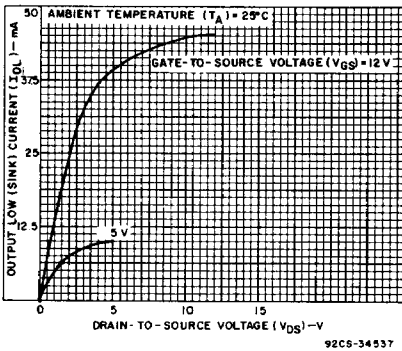


Fig. 5 - Minimum N-Channel output low (sink) current characteristics - CMOS

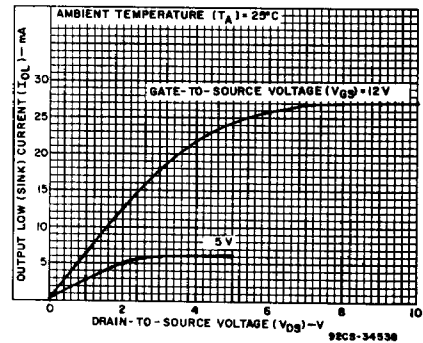


Fig. 6 - Minimum output low (sink) current characteristics - TTL to CMOS.

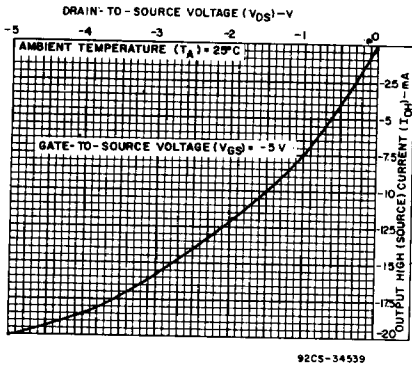


Fig. 7 - Typical P-channel output high (source) current characteristics - CMOS to TTL.

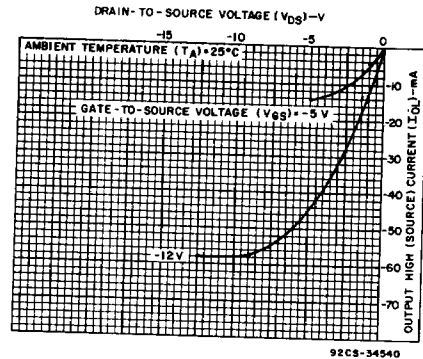


Fig. 8 - Typical output high (source) current characteristics - TTL to CMOS.

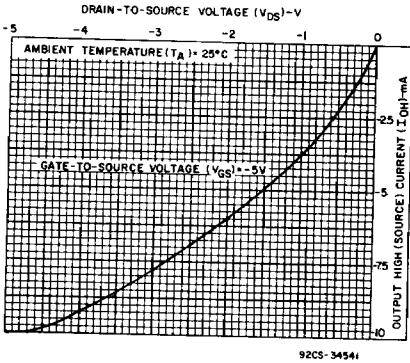


Fig. 9 - Minimum P-Channel output high (source) current characteristic - CMOS to TTL.

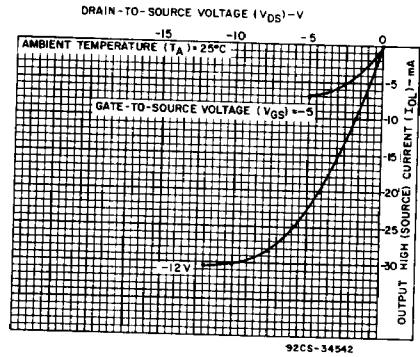


Fig. 10 - Minimum output high (source) current characteristics - TTL to CMOS.

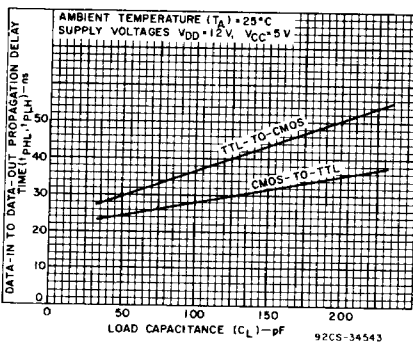


Fig. 11 - Typical DATA-IN to DATA-OUT propagation delay as a function of load capacitance.

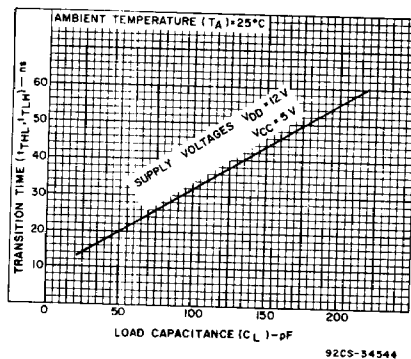


Fig. 12 - Typical transition time as a function of load capacitance CMOS-to-TTL or TTL-to-CMOS.

CD40116 Types

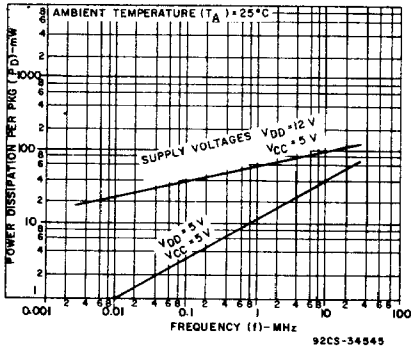


Fig. 13 - Power dissipation as a function of frequency - CMOS to TTL.

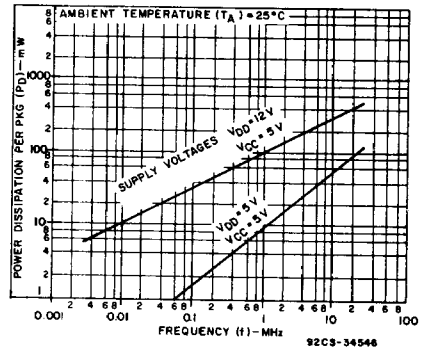
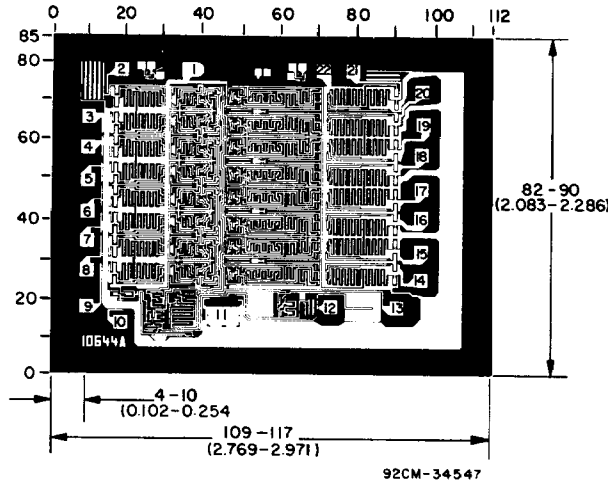


Fig. 14 - Power dissipation as a function of frequency - TTL to CMOS.



The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to $+16$ mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basis inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and Pad Layout for CD40116H