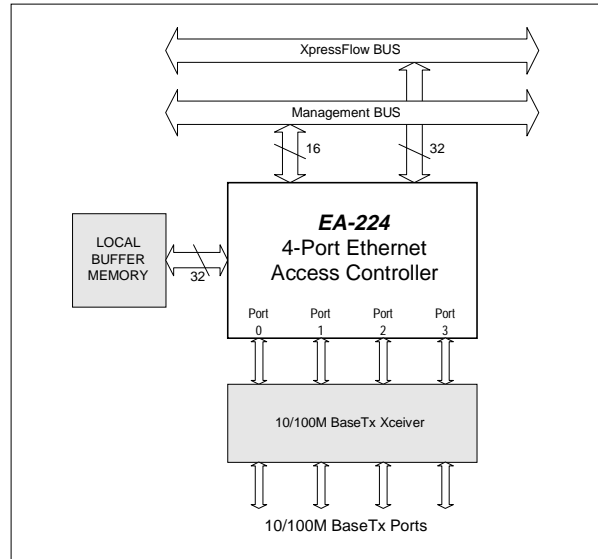


EA-224 – 4-Port Fast Ethernet Access Controller (XpressFlow™ 2001 Series 10/100 Ethernet Switch Chipset)

1. DISTINCTIVE CHARACTERISTICS

- ◆ 4 independent 10/100Mbps Ethernet Access Ports
 - ◇ Direct interface with 10BaseT transceiver
 - ◇ IEEE 802.3u compliant MII (Media Independent Interface) and Serial Management interface
 - ◇ Direct interface with 100BaseTX, -T2, -T4, or -TF physical transceivers
- ◆ State of the art 0.5 micron 3.3Volt CMOS process
- ◆ 352-PIN BGA package
- ◆ Operating frequency
 - ◇ -33 33 MHz maximum
 - ◇ -40 40 MHz maximum
 - ◇ -50 50 MHz maximum
- ◆ 32-bit Local Buffer Memory Interface
 - ◇ Supports 128k to 1M bytes
 - ◇ Utilize high performance 32-bit Synchronous Burst SRAM
- ◆ Hardware assisted Buffer and Queue Management to minimized CPU overhead
- ◆ 16-bit Processor Bus I/O Interface
 - ◇ Allows host to access Control Registers & Local Buffer Memory
 - ◇ Supports Big and Little Endian CPUs
 - ◇ Direct interface with various different standard microprocessors including 386, 486 families and Motorola MPC series embedded processors.
- ◆ 32-bit XpressFlow Bus Interface
 - ◇ Uses Granule for frame transferring between Access Controllers
- ◆ Supports unicast, multicast, and broadcast frames
 - ◇ Also detects IEEE 802.3X MAC Control frames
- ◆ Works together with SC-201 XpressFlow Engine
 - ◇ Capable to forward frames at full line-rate
 - ◇ Distributed Flow Caching™ to reduce frame forwarding latency
- ◆ Supports both Half & Full Duplex operation
- ◆ Programmable Flow Control Enable
 - ◇ Jam Fake Collision for Half Duplex Mode
 - ◇ Transmit Flow Control Frame for IEEE 802.3x Full Duplex Mode

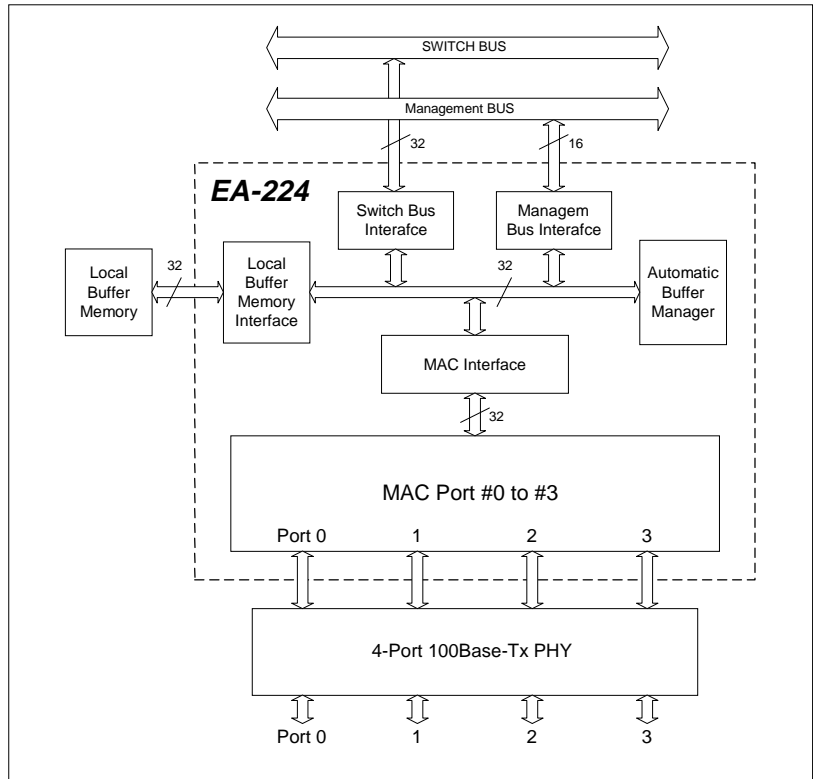


- ◆ Three frame forwarding modes
 - ◇ Store-&-Forward
 - ◇ Safe Cut-Thru (Runt Free)
 - ◇ Turbo Cut-Thru (10Mbps Mode only)
 - ◇ Automatically selects the optimized mode for forwarding
 - ◇ Allows manual frame forwarding mode selection override
- ◆ Multi-Media ready with QoS supports
 - ◇ Four frame transmission priority queues
- ◆ Complies with IEEE 802.1 Bridge Standard
 - ◇ Assigns one unique MAC Address for each port
- ◆ VLAN ID Tagging & Stripping
 - ◇ Auto padding if necessary after stripping
- ◆ Automatic retry frame transmission
 - ◇ Transmit collision
 - ◇ Transmit buffer under-run
- ◆ Automatic receive filtering for bad frames for Store & Forward Mode
 - ◇ Bad FCS
 - ◇ Short events or frames under 64 bytes
 - ◇ Long events or frames over 1518 bytes
- ◆ Automatic statistic collection for RMON

2. GENERAL DESCRIPTION:

The EA-224 provides four 10/100Mbps Ethernet network access interface ports. MII interface is used to connect external PHY devices for 100 Mbps Ethernet. They also can direct connect with standard 10Mbps serial interface.

The EA-224 provides the Ethernet MAC protocols, handles the local buffer memory interface and management, arbitrates among multiple priority queues, and interfaces with the XpressFlow Engine and other Access Controllers through the XpressFlow message passing protocol.



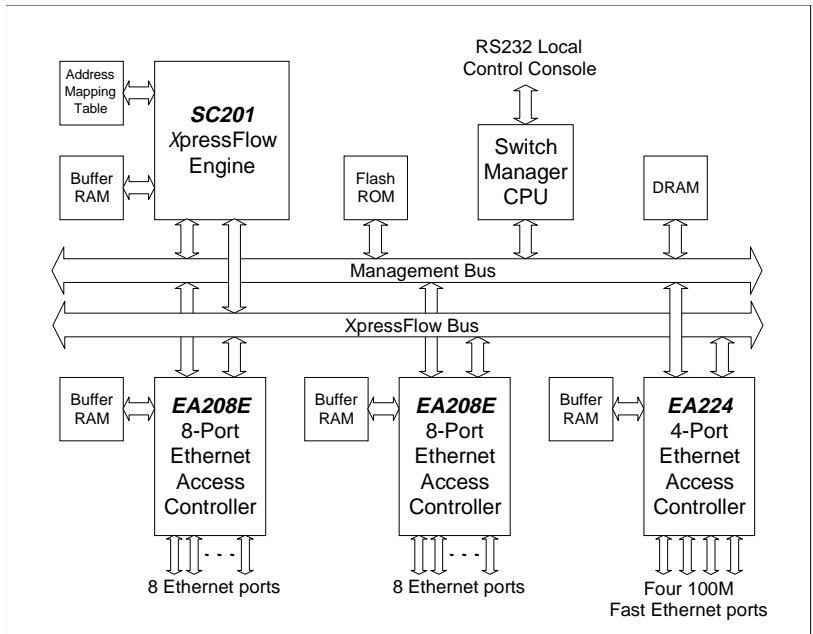
**Block Diagram –
EA-224 4-Port Ethernet Access Controller**

2.1 Related Components:

- ◆ **SC-201** – XpressFlow Engine
- ◆ **EA-208E** – 8-port 10Mbps Ethernet Access Controller
- ◆ **EA-208** – 6-port 10 + 2-port 10/100 Ethernet Access Controller
- ◆ **EA-222** – 2-port 10/100 Fast Ethernet Access Controller

2.2 Typical Application:

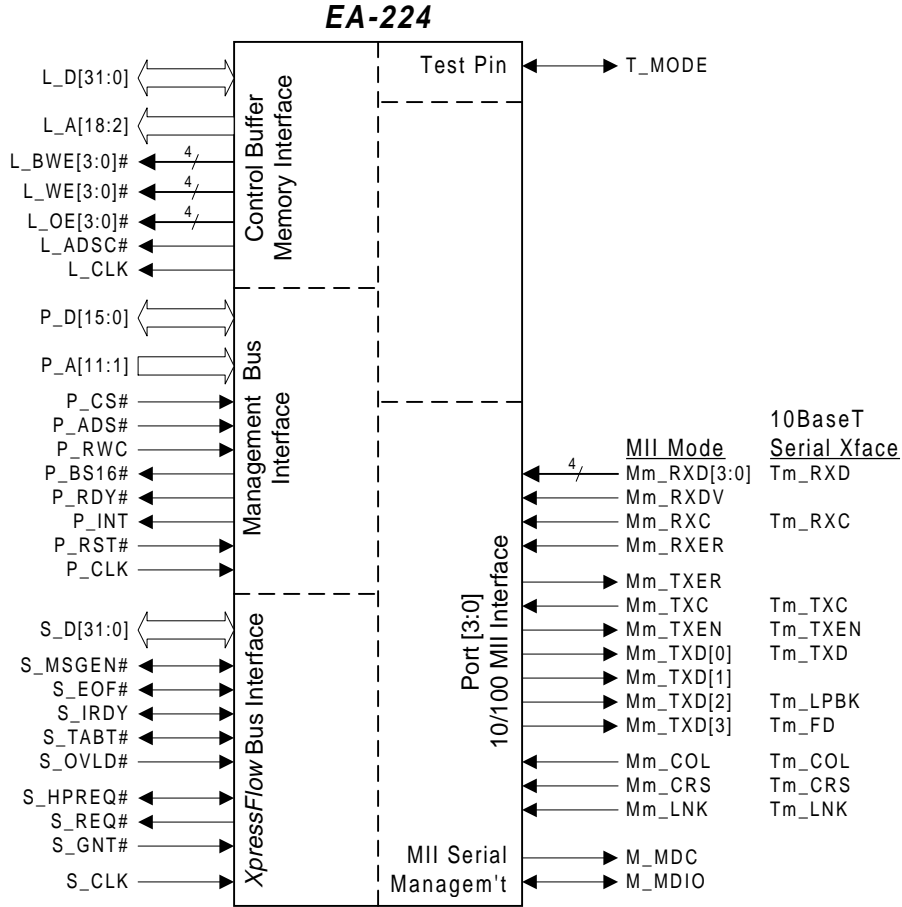
- ◆ A 16-port Ethernet Switch with 4 Fast Ethernet Up-Links



**System Block Diagram --
16-Port Ethernet Switch with 4 Fast Ethernet Up-Links**

3. PIN ASSIGNMENT

3.1 Logic Symbol



3.2 Pin Assignment (Preliminary)

- Note:**
- # Active low signal
 - Input Input signal
 - I-ST Input signal with Schmitt-Trigger
 - Output Output signal (Tri-State driver)
 - Out-OD Output signal with Open-Drain driver
 - I/O-TS Input & Output signal with Tri-State driver
 - I/O-OD Input & Output signal with Open-Drain driver
 - 5VT Input with 5V Tolerance
 - ① Output signal with programmable polarity.
 - ② Input or output pins with weak internal pull up resistors (50k to 100k Ohms each)
 - ③ These pins are reserved for internal use only. They should be left unconnected.

| Pin No(s). | Symbol | Type | Max I _{OL} / I _{OH} | Name & Functions |
|---|--------------------------|---------------------|--|---|
| Management Bus Interface | | | | |
| J25,K26,L24,K25,L26, M24,L25,M26,N24,M25, P24,N26,N25,R24,P26, P25 | P_D[15:0] | TTL I/O-TS (5VT) | 16mA | Management Bus – Data Bit [15:0] |
| C26,D24,C25,E24,D26, D25,F24,E26,E25,G24, F26 | P_A[11:1] | TTL In (5VT) | | Management Bus – Address Bit [11:1] |
| F25 | P_ADS# | TTL In (5VT) | | Management Bus – Address Strobe |
| H25 | P_RWC | TTL In (5VT) | | Management Bus – Read/Write Control |
| J24 | P_RDY# | TTL Out-OD | 16mA | Management Bus – Data Ready |
| G25 | P_BS16# | TTL Out-OD | 16mA | Management Bus – 16 bit Data Bus |
| G26 | P_CS# | TTL In (5VT) | | Management Bus – Chip Select |
| H26 | P_INT ① | CMOS Output | 4mA | Management Bus – Interrupt Request |
| J26 | P_RST# | TTL In-ST (5VT) | | Management Bus – Master Reset |
| K24 | P_CLK | TTL In (5VT) | | Management Bus – Bus Clock |
| XpressFlow Bus Interface | | | | |
| C23,A23,B22,C22,A22 | S_D[31:27] / P_C[0:4] | CMOS I/O-TS | 12 mA | XpressFlow Bus – Data Bit [31:27] or Management Bus Interface Configuration bit [0:4] |
| B21,D20,C21,A21,B20, A20,C20,B19,A19,C19, B18,A18,B17,C18,A17, D17,B16,C17,A16,B15, A15,C16,B14,D15,A14, C15,B13 | S_D[26:0] | CMOS I/O-TS | 12mA | XpressFlow Bus – Data Bit [26:0] |
| B12 | S_MSGEN# | CMOS I/O-TS | 12 mA | XpressFlow Bus – Message Envelope |
| A12 | S_EOF# | CMOS I/O-TS | 12mA | XpressFlow Bus – End of Frame |
| C14 | S_IRDY | CMOS I/O-TS | 12 mA | XpressFlow Bus – Initiator Ready |
| C13 | S_TABT# | CMOS I/O-OD | 12 mA | XpressFlow Bus – Target Abort |
| B23 | S_HPREQ# | CMOS I/O-OD | 12mA | XpressFlow Bus – High Priority Request |
| A24 | S_REQ# | CMOS Output | 4mA | XpressFlow Bus – Bus Request to SC201 |
| B24 | S_GNT# | CMOS Input | | XpressFlow Bus – Bus Grant from SC201 |
| A13 | S_OVLD# | CMOS Input | | XpressFlow Bus – Bus Overload |
| D13 | S_CLK | CMOS Input | | XpressFlow Bus – Clock |

**XpressFlow-2001 Series –
Ethernet Switch Chip-set**

**EA-224
4-Port 10/100M Ethernet Access Controller**

| Pin No(s). | Symbol | Type | Max I _{OL} / I _{OH} | Name & Functions |
|---|-----------------------|--------------------|--|---|
| Control Buffer Memory Interface | | | | |
| M4,N2,L3,M1,M2,L1,K3, L2,K4,K1,J3,K2,J1,J2, H3,H1,H2,G3,G1,G2,F1, F3,F2,E1,E3,E2,D1,D3, D2,C1,C2,B1 | L_D[31:0] | TTL I/O-TS ② | 8mA | Local Memory Bus – Data Bit [31:0] |
| A6,B6,C8,A7,D8,D7,C9, A8,B8,A9,C10,B9,D10, A10,C11,B10,A11 | L_A[18:2] | CMOS Output | 8mA | Local Memory Bus – Address Bit [17:2] |
| C7 | L_A[19] / L_OE[3]# | CMOS Output | 8mA | Local Memory Bus – Address Bit [19] or Memory Read Chip Select [3] |
| D5,A5,A3 | L_OE[2:0]# | CMOS Output | 2mA | Local Memory Read Chip Select [2:0] |
| D7,E4,B5,C4 | L_WE[3:0]# | CMOS Output | 2mA | Local Memory Write Chip Select [3:0] |
| C6,B4,A4,C5 | L_BWE[3:0]# | CMOS Output | 8mA | Local Memory Byte Write Enable, Byte [3:0] |
| B3 | L_ADSC# | CMOS Output | 8mA | Local Memory Controller Address Status |
| G4 | L_CLK | CMOS Output | 8mA | Local Memory Clock input |
| Fast Ethernet Access Port [3:0] | | | | |
| T24 | M_MDC | CMOS Output | 4mA | MII Management Data Clock – (common for all MII Ports – Port [1:0]) |
| R26 | M_MDIO | TTL IO-TS (5VT) | 4mA | MII Management Data I/O – (common for all MII Ports – Port [1:0]) |
| AB2,U25,AE26,AF5 | M[3:0]_RXD[3] | TTL In (5VT) ② | | Port [3:0] – MII Receive Data Bit [3] |
| AB1,V24,AD25,AE6 | M[3:0]_RXD[2] | TTL In (5VT) ② | | Port [3:0] -- Receive Data Bit [2] |
| AA3,U26,AD26,AD6 | M[3:0]_RXD[1] | TTL In (5VT) ② | | Port [3:0] -- Receive Data Bit [1] |
| AC2,T25 | M[3:2]_RXD[0] | TTL In (5VT) ② | | Port [3:0] -- Receive Data Bit [0] |
| AC25,AF6 | M[1:0]_RXD[0] | TTL In (5VT) | | |
| Y3,V26,AF24,AD5 | M[3:0]_RXDV | TTL In (5VT) ② | | Port [3:0] -- Receive Data Valid |
| AC1,U24 | M[3:2]_RXC | TTL In (5VT) ② | | Port [3:0] -- Receive Clock |
| AC24,AE7 | M[1:0]_RXC | TTL In (5VT) | | |
| AA1,V25,AD23,AE5 | M[3:0]_RXER | | | Port [3:0] -- Receive Error |
| AA2,W24,AE24,AF4 | M[3:0]_TXER | CMOS Output | 4mA | Port [3:0] -- Transmit Error |
| W2,AA25,AE22,AD1 | M[3:0]_TXC | TTL In (5VT) | | Port [3:0] -- Transmit Clock |
| W1,AA24,AF22,AF2 | M[3:0]_TXEN | CMOS Output | 4mA | Port [3:0] -- Transmit Enable |
| V3,AA26,AD21,AE3 | M[3:0]_TXD[3] | CMOS Output | 4mA | Port [3:0] -- Transmit Data Bit [3] |
| Y2,Y26,AE23,AF3 | M[3:0]_TXD[2] | CMOS Output | 4mA | Port [3:0] -- Transmit Data Bit [2] |
| W3,W26,AD22,AD4 | M[3:0]_TXD[1] | CMOS Output | 4mA | Port [3:0] -- Transmit Data Bit [1] |
| Y1,W25,AF23,AE4 | M[3:0]_TXD[0] | CMOS Output | 4mA | Port [3:0] -- Transmit Data Bit [0] |
| V1,AB26 | M[3:2]_COL | TTL In (5VT) ② | | Port [3:0] -- Collision Detected |
| AD20,AC3 | M[1:0]_COL | TTL In (5VT) | | |
| U3,AB24 | M[3:2]_CRS | TTL In (5VT) ② | | Port [3:0] -- Carrier Sense |
| AF21,AD2 | M[1:0]_CRS | TTL In (5VT) | | |
| V2,AB25 | M[3:2]_LNK ① | TTL In (5VT) ② | | Port [3:0] -- Link Status |
| AE21,AB3 | M[1:0]_LNK ① | TTL In (5VT) | | |
| Test Facility | | | | |
| A25 | T_MODE | CMOS I/O-TS ② | 2mA | Test Pin – Set Test Mode upon Reset, and provides test status output during test mode |
| N1,M3,P2,P1,N3,R2,P3, R1,T2,R3,T1,R4,U2,T3, U1,U4 | T_D[15:10] ③ | CMOS Output | 4mA | Test Pins – Reserved for internal use only |

**XpressFlow-2001 Series –
Ethernet Switch Chip-set**

**EA-224
4-Port 10/100M Ethernet Access Controller**

| Pin No(s). | Symbol | Type | Name & Functions |
|--|--------|-------|---------------------|
| Power Pins | | | |
| D6,D11,D16,D21,F4, F23,L4,L23,T4,T23,AA4, AA23,AC6,AC11,AC16, AC21 | VDD | Power | +3.3 Volt DC Supply |
| A1,A2,A26,B2,B25,B26, C3,C24,D4,D9,D14,D19, D23,H4,J23,N4,P23,V4, W23,AC4,AC8,AC13, AC18,AC23,AD3,AD24, AE1,AE2,AE25,AF1, AF25 | VSS | Power | Ground |

**XpressFlow-2001 Series –
Ethernet Switch Chip-set**

**EA-224
4-Port 10/100M Ethernet Access Controller**

3.3 Pin Reference Table: (352 pin BGA)

| Pin # | Signal Name | Pin # | Signal Name | Pin # | Signal Name | Pin # | Signal Name | Pin # | Signal Name |
|-------|-------------|-------|------------------|-------|---------------------|-------|---------------------|-------|-------------|
| F26 | P_A[1] | D17 | S_D[11] | D2 | L_D[3] | AF23 | M1_TXD[0] / T1_TXD | R1 | T_D[8] |
| G24 | P_A[2] | A17 | S_D[12] | D3 | L_D[4] | AF22 | M1_TXEN / T1_TXEN | P3 | T_D[9] |
| E25 | P_A[3] | C18 | S_D[13] | D1 | L_D[5] | AE22 | M1_TXC / T1_TXC | R2 | T_D[10] |
| E26 | P_A[4] | B17 | S_D[14] | E2 | L_D[6] | AE24 | M1_TXER | N3 | T_D[11] |
| F24 | P_A[5] | A18 | S_D[15] | E3 | L_D[7] | AD23 | M1_RXER | P1 | T_D[12] |
| D25 | P_A[6] | B18 | S_D[16] | E1 | L_D[8] | AC24 | M1_RXC / T1_RXC | P2 | T_D[13] |
| D26 | P_A[7] | C19 | S_D[17] | F2 | L_D[9] | AF24 | M1_RXDV | M3 | T_D[14] |
| E24 | P_A[8] | A19 | S_D[18] | F3 | L_D[10] | AC25 | M1_RXD[0] / T1_RXD | N1 | T_D[15] |
| C25 | P_A[9] | B19 | S_D[19] | F1 | L_D[11] | AD26 | M1_RXD[1] | | |
| D24 | P_A[10] | C20 | S_D[20] | G2 | L_D[12] | AD25 | M1_RXD[2] | D6 | VDD |
| C26 | P_A[11] | A20 | S_D[21] | G1 | L_D[13] | AE26 | M1_RXD[3] | D11 | VDD |
| F25 | P_ADS# | B20 | S_D[22] | G3 | L_D[14] | AB25 | M2_LNK / T2_LNK | D16 | VDD |
| G26 | P_CS# | A21 | S_D[23] | H2 | L_D[15] | AB24 | M2_CRS / T2_CRS | D21 | VDD |
| H25 | P_RWC | C21 | S_D[24] | H1 | L_D[16] | AB26 | M2_COL / T2_COL | F4 | VDD |
| G25 | P_BS16# | D20 | S_D[25] | H3 | L_D[17] | AA26 | M2_TXD[3] / T2_FD | F23 | VDD |
| J24 | P_RDY# | B21 | S_D[26] | J2 | L_D[18] | Y26 | M2_TXD[2] / T2_LPBK | L4 | VDD |
| J26 | P_RST# | A22 | S_D[27] / P_C[4] | J1 | L_D[19] | W26 | M2_TXD[1] | L23 | VDD |
| H26 | P_INT | C22 | S_D[28] / P_C[3] | K2 | L_D[20] | W25 | M2_TXD[0] / T2_TXD | T4 | VDD |
| K24 | P_CLK | B22 | S_D[29] / P_C[2] | J3 | L_D[21] | AA24 | M2_TXEN / T2_TXEN | T23 | VDD |
| P25 | P_D[0] | A23 | S_D[30] / P_C[1] | K1 | L_D[22] | AA25 | M2_TXC / T2_TXC | AA4 | VDD |
| P26 | P_D[1] | C23 | S_D[31] / P_C[0] | K4 | L_D[23] | W24 | M2_TXER | AA23 | VDD |
| R24 | P_D[2] | | | L2 | L_D[24] | V25 | M2_RXER | AC6 | VDD |
| N25 | P_D[3] | A11 | L_A[2] | K3 | L_D[25] | U24 | M2_RXC / T2_RXC | AC11 | VDD |
| N26 | P_D[4] | B10 | L_A[3] | L1 | L_D[26] | V26 | M2_RXDV | AC16 | VDD |
| P24 | P_D[5] | C11 | L_A[4] | M2 | L_D[27] | T25 | M2_RXD[0] / T2_RXD | AC21 | VDD |
| M25 | P_D[6] | A10 | L_A[5] | M1 | L_D[28] | U26 | M2_RXD[1] | A1 | GND |
| N24 | P_D[7] | D10 | L_A[6] | L3 | L_D[29] | V24 | M2_RXD[2] | A2 | GND |
| M26 | P_D[8] | B9 | L_A[7] | N2 | L_D[30] | U25 | M2_RXD[3] | A26 | GND |
| L25 | P_D[9] | C10 | L_A[8] | M4 | L_D[31] | V2 | M3_LNK / T3_LNK | B2 | GND |
| M24 | P_D[10] | A9 | L_A[9] | | | U3 | M3_CRS / T3_CRS | B25 | GND |
| L26 | P_D[11] | B8 | L_A[10] | T24 | M_MDC | V1 | M3_COL / T3_COL | B26 | GND |
| K25 | P_D[12] | A8 | L_A[11] | R26 | M_MDIO | V3 | M3_TXD[3] / T3_FD | C3 | GND |
| L24 | P_D[13] | C9 | L_A[12] | | | Y2 | M3_TXD[2] / T3_LPBK | C24 | GND |
| K26 | P_D[14] | B7 | L_A[13] | AB3 | M0_LNK / T0_LNK | W3 | M3_TXD[1] | D4 | GND |
| J25 | P_D[15] | D8 | L_A[14] | AD2 | M0_CRS / T0_CRS | Y1 | M3_TXD[0] / T3_TXD | D9 | GND |
| | | A7 | L_A[15] | AC3 | M0_COL / T0_COL | W1 | M3_TXEN / T3_TXEN | D14 | GND |
| D13 | S_CLK | C8 | L_A[16] | AE3 | M0_TXD[3] / T0_FD | W2 | M3_TXC / T3_TXC | D19 | GND |
| A13 | S_OVLD# | B6 | L_A[17] | AF3 | M0_TXD[2] / T0_LPBK | AA2 | M3_TXER | D23 | GND |
| B23 | S_HPREQ# | A6 | L_A[18] | AD4 | M0_TXD[1] | AA1 | M3_RXER | H4 | GND |
| A24 | S_REQ# | C7 | L_A[19] / OE[3]# | AE4 | M0_TXD[0] / T0_TXD | AC1 | M3_RXC / T3_RXC | J23 | GND |
| B24 | S_GNT# | D5 | L_OE[2]# | AF2 | M0_TXEN / T0_TXEN | Y3 | M3_RXDV | N4 | GND |
| B12 | S_MSGEN# | A5 | L_OE[1]# | AD1 | M0_TXC / T0_TXC | AC2 | M3_RXD[0] / T3_RXD | P23 | GND |
| A12 | S_EOF# | A3 | L_OE[0] | AF4 | M0_TXER | AA3 | M3_RXD[1] | V4 | GND |
| C14 | S_IRDY | D7 | L_WE[3]# | AE5 | M0_RXER | AB1 | M3_RXD[2] | W23 | GND |
| C13 | S_TABT# | E4 | L_WE[2]# | AE7 | M0_RXC / T0_RXC | AB2 | M3_RXD[3] | AC4 | GND |
| B13 | S_D[0] | B5 | L_WE[1]# | AD5 | M0_RXDV | | | AC8 | GND |
| C15 | S_D[1] | C4 | L_WE[0]# | AF6 | M0_RXD[0] / T0_RXD | A25 | T_MODE | AC13 | GND |
| A14 | S_D[2] | C6 | L_BWE[3]# | AD6 | M0_RXD[1] | | | AC18 | GND |
| D15 | S_D[3] | B4 | L_BWE[2]# | AE6 | M0_RXD[2] | U4 | T_D[0] | AC23 | GND |
| B14 | S_D[4] | A4 | L_BWE[1]# | AF5 | M0_RXD[3] | U1 | T_D[1] | AD3 | GND |
| C16 | S_D[5] | C5 | L_BWE[0]# | AE21 | M1_LNK / T1_LNK | T3 | T_D[2] | AD24 | GND |
| A15 | S_D[6] | B3 | L_ADSC# | AF21 | M1_CRS / T1_CRS | U2 | T_D[3] | AE1 | GND |
| B15 | S_D[7] | G4 | L_CLK | AD20 | M1_COL / T1_COL | R4 | T_D[4] | AE2 | GND |
| A16 | S_D[8] | B1 | L_D[0] | AD21 | M1_TXD[3] / T1_FD | T1 | T_D[5] | AE25 | GND |
| C17 | S_D[9] | C2 | L_D[1] | AE23 | M1_TXD[2] / T1_LPBK | R3 | T_D[6] | AF1 | GND |
| B16 | S_D[10] | C1 | L_D[2] | AD22 | M1_TXD[1] | T2 | T_D[7] | AF25 | GND |

- Note:**
- ① Output signals with programmable polarity.
 - ② Input or output pins with weak internal pull up resistors (50k to 100k Ohms each)
 - ③ These pins are reserved for internal use only. They should be left unconnected.

4. FUNCTIONAL DESCRIPTION

4.1 Local Memory (Local Buffer Memory) Interface

- ◆ Use industry standard Synchronous Burst Mode SRAM up to 1M bytes
 - ◇ 32k x 32, 64k x 32, 128k x 32, or 256k x 32
- ◆ Provides 4 individual *Byte Write Enable* controls (L_BWE[3:0]#)
- ◆ Provides separate Read and Write Chip Selects (L_OE[3:0]# and L_WE[3:0]#) for each memory chip
- ◆ Supports back to back Read or Write operations across memory chips

4.1.1 Pin Description

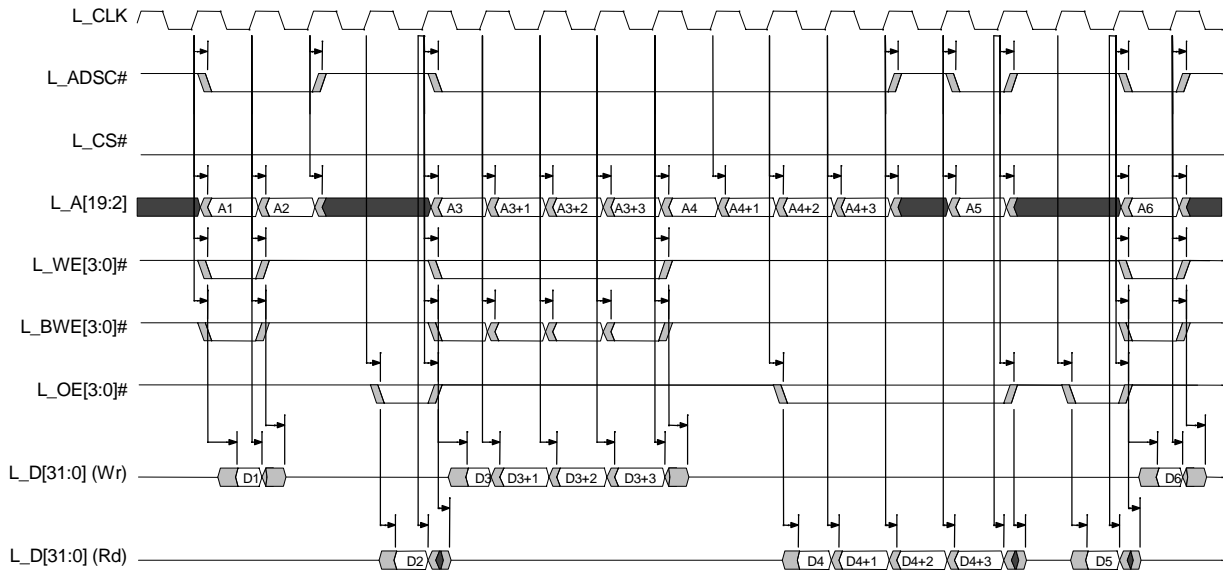
| Symbol | Type | Name & Functions |
|-----------------------|----------------|---|
| L_D[31:0] ② | TTL I/O-TS | Local Memory Data Bus Bit [31:0] – a 32-bit synchronous data bus. |
| L_A[18:2] | CMOS Output | Local Memory Address Bus Bit [18:2] – Bit [18:2] of a synchronous address bus. The memory address is sampled when L_CS# is enabled and L_ADSC# is asserted. |
| L_A[19] / L_OE[3]# | CMOS Output | Local Memory Address Bus Bit [19] or Local Memory Read Chip Select [3] – Depends on memory configuration, this pin can be used as the Local Memory Address Bit [19] or as the Local Memory Read Chip Select [3]. |
| L_OE[2:0]# | CMOS Output | Local Memory Read Chip Select [2:0] – allows up to read one of the 4 banks of memory. |
| L_WE[3:0]# | CMOS Output | Local Memory Write Chip Select [3:0] – allows up to write one of the 4 banks of memory. |
| L_BWE[3:0]# | CMOS Output | Local Memory Byte Write Enable [3:0] – use to write individual bytes. |
| L_ADSC# | CMOS Output | Local Memory Controller Address Status – to load a new address. |
| L_CLK | CMOS Output | Local Memory Clock – a synchronous clock to memory devices. |

Note: ② These pins have weak internal pull up resistors (50k to 100k Ohms each).

4.1.2 Supported Memory Configurations

| RAM Chip Size | # of RAM Chips | Total Buffer Memory Size | Read/Write Chip Select and High Address Bits | | | | | | | |
|---------------|----------------|--------------------------|--|--------------------|----------|----------|----------|----------|----------|----------|
| | | | Chip #3 | | Chip #2 | | Chip #1 | | Chip #0 | |
| | | | L_WE[3]# | L_A[19] / L_OE[3]# | L_WE[2]# | L_OE[2]# | L_WE[1]# | L_OE[1]# | L_WE[0]# | L_OE[0]# |
| 32k x 32 | 1 | 128k bytes | ---- | ---- | ---- | ---- | ---- | ---- | L_WE[0]# | L_OE[0]# |
| | 2 | 256k bytes | ---- | ---- | ---- | ---- | L_WE[1]# | L_OE[1]# | L_WE[0]# | L_OE[0]# |
| | 4 | 512k bytes | L_WE[3]# | L_OE[3]# | L_WE[2]# | L_OE[2]# | L_WE[1]# | L_OE[1]# | L_WE[0]# | L_OE[0]# |
| 64k x 32 | 1 | 256k bytes | ---- | ---- | ---- | ---- | ---- | ---- | L_WE[0]# | L_OE[0]# |
| | 2 | 512k bytes | ---- | ---- | ---- | ---- | L_WE[1]# | L_OE[1]# | L_WE[0]# | L_OE[0]# |
| | 4 | 1M bytes | L_WE[3]# | L_OE[3]# | L_WE[2]# | L_OE[2]# | L_WE[1]# | L_OE[1]# | L_WE[0]# | L_OE[0]# |
| 128k x32 | 1 | 512k bytes | ---- | ---- | ---- | ---- | ---- | ---- | L_WE[0]# | L_OE[0]# |
| | 2 | 1M bytes | ---- | ---- | ---- | ---- | L_WE[1]# | L_OE[1]# | L_WE[0]# | L_OE[0]# |
| 256k x32 | 1 | 1M bytes | ---- | L_A[19] | ---- | ---- | ---- | ---- | L_WE[0]# | L_OE[0]# |

4.1.3 Bus Cycle Waveforms



Typical Local Memory Access Operations

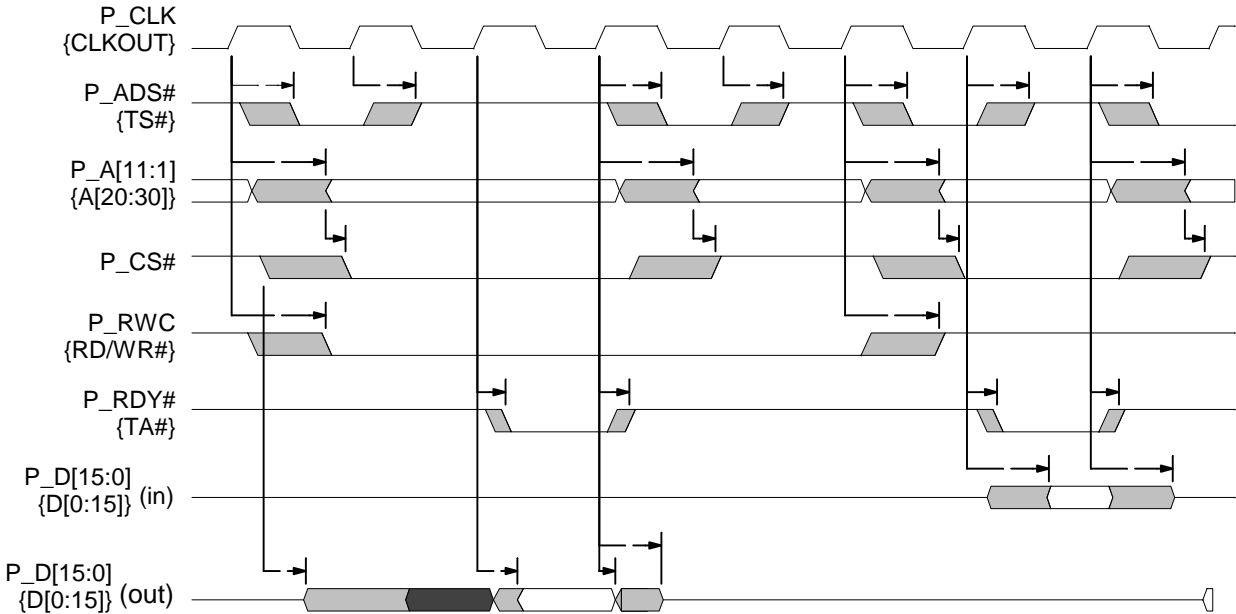
4.2 Management Bus Interface

- ◆ Supports various industry standard micro-processors including:
 - ◇ Intel 186, 386, and 486 family or equivalent
 - ◇ Motorola MPC series embedded processors
- ◆ Easily adapts to other industry standard CPUs
- ◆ Provides separate Address and Data bus
- ◆ Supports Big & Little Endian byte ordering
- ◆ Supports 16-bit Data Bus
- ◆ Supports early RDY cycle
 - ◇ Meets timing requirement for Intel/AMD 186 family processors
- ◆ Supports 1X or 2X CPU Clock
 - ◇ 2X CPU Clock for 386 family processors
- ◆ Provides a single interrupt signal to Switch Manager CPU

4.2.1 Pin Description

| Symbol | Type | Name & Functions | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|------------------|---|--------|----------|------------|------|------|------|--|-----------|------------|-----|----------|------------|----|----------|---------------|--------|-----|--------|----|----------|------------|--------|-----|-------|
| P_C[4:0] | CMOS Input | <p>Processor Configuration bit [4:0]: – During the Reset Cycle, the P_C[4:0] pins provides the processor configuration. By using external weak pull-up or -down resistors, they define the External Management Bus Interface Configuration. These inputs are sampled at the trailing edge of the Reset cycle.</p> <p>C[0] – Defines the CPU Clock input is 1X or 2X clock C[1] – Selects either Big or Little Endian byte ordering C[2] – Defines the polarity of the P_RWC (Rd/Wr Control) input C[3] – Defines the CPU Bus width – For EA-208, it is default to 16-bit CPU Bus interface, and the setting of this bit is ignored. C[4] – Defines the timing relationship between P_RDY and P_D[15:0] valid. If C[4] is High, the P_D[15:0] are valid along in the same clock period as P_RDY is asserted. If C[4] is Low, the P_RDY is asserted one clock period <u>early</u> ahead of the P_D[15:0] are valid.</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>C[0]</th> <th>C[1]</th> <th>C[2]</th> <th>C[3]</th> <th>C[4]</th> </tr> <tr> <th></th> <th>CPU Clock</th> <th>Byte Order</th> <th>RWC</th> <th>Bus Size</th> <th>RDY Timing</th> </tr> </thead> <tbody> <tr> <td>Lo</td> <td>1X Clock</td> <td>Little Endian</td> <td>P_R/W#</td> <td>n/a</td> <td>Normal</td> </tr> <tr> <td>Hi</td> <td>2x Clock</td> <td>Big Endian</td> <td>P_W/R#</td> <td>n/a</td> <td>Early</td> </tr> </tbody> </table> <p>After RESET, these pins are used as XpressFlow Bus Data bit [31:27].</p> | | C[0] | C[1] | C[2] | C[3] | C[4] | | CPU Clock | Byte Order | RWC | Bus Size | RDY Timing | Lo | 1X Clock | Little Endian | P_R/W# | n/a | Normal | Hi | 2x Clock | Big Endian | P_W/R# | n/a | Early |
| | C[0] | C[1] | C[2] | C[3] | C[4] | | | | | | | | | | | | | | | | | | | | | |
| | CPU Clock | Byte Order | RWC | Bus Size | RDY Timing | | | | | | | | | | | | | | | | | | | | | |
| Lo | 1X Clock | Little Endian | P_R/W# | n/a | Normal | | | | | | | | | | | | | | | | | | | | | |
| Hi | 2x Clock | Big Endian | P_W/R# | n/a | Early | | | | | | | | | | | | | | | | | | | | | |
| P_A[11:1] | TTL In (5VT) | Address Bus Bit [11:1] – I/O port address | | | | | | | | | | | | | | | | | | | | | | | | |
| P_D[15:0] | TTL I/O-TS (5VT) | Data Bus Bit [15:0] – a 16-bit synchronous data bus. | | | | | | | | | | | | | | | | | | | | | | | | |
| P_ADS# | TTL In (5VT) | Address Strobe – indicates valid address is on the bus | | | | | | | | | | | | | | | | | | | | | | | | |
| P_RWC | TTL Input (5VT) | Read/Write Control – indicates the current bus cycle is a read or write cycle. C[1] defines the polarity of this signal during the Reset cycle. C[1]=0 P_R/W# is used for PowerPC or other similar processors. C[1]=1 P_W/R# is used for 386, 486 or other similar processors | | | | | | | | | | | | | | | | | | | | | | | | |
| P_RDY# | TTL Out-OD | Data Ready – timing indicates for bus data valid | | | | | | | | | | | | | | | | | | | | | | | | |
| P_BS16# | TTL Out-OD | Bus Size 16 – response to bus master that the EA208 only supports 16-bit data bus width. | | | | | | | | | | | | | | | | | | | | | | | | |
| P_CS# | TTL Input (5VT) | Chip Select – indicates the XpressFlow Engine is the target for the current bus operation. | | | | | | | | | | | | | | | | | | | | | | | | |
| P_INT ① | CMOS Output | Interrupt Request to Switch Manager CPU <i>The polarity of this signal output is programmable via chip configuration register.</i> | | | | | | | | | | | | | | | | | | | | | | | | |
| P_RST# | TTL In-ST (5VT) | CPU Reset – Synchronous reset Input from Switch Manager CPU | | | | | | | | | | | | | | | | | | | | | | | | |
| P_CLK | TTL In (5VT) | CPU Clock – 2X Clock for 386 family, and 1X Clock for the others | | | | | | | | | | | | | | | | | | | | | | | | |

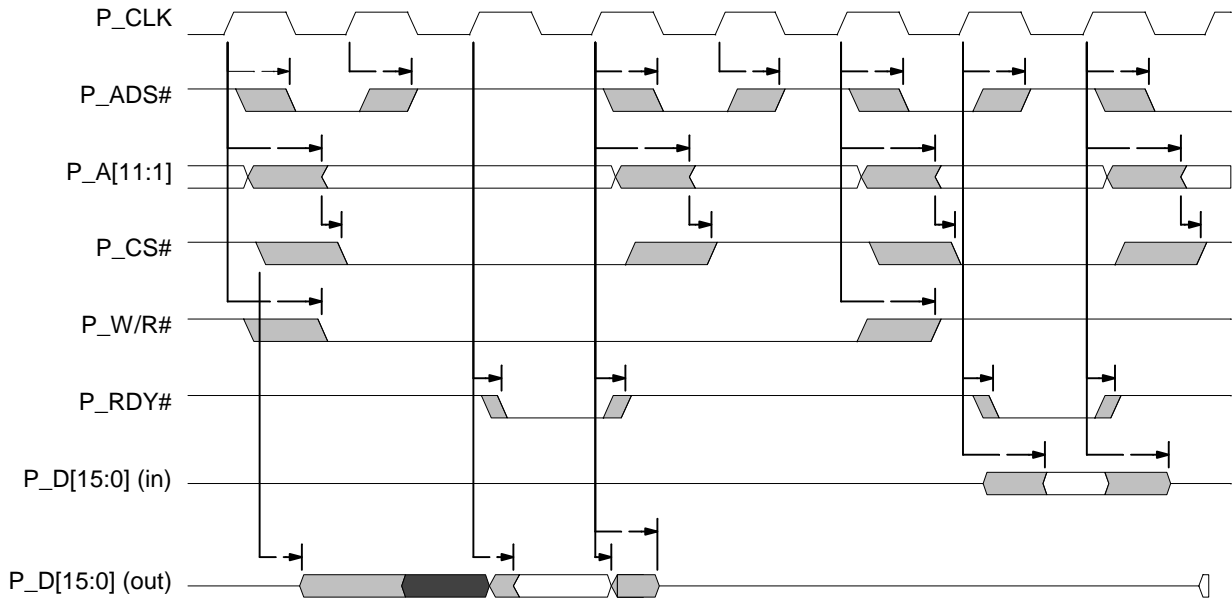
4.2.2 Motorola MPC801 Processor Interface



Note: Mnemonics with in {} are the equivalent signals defined by MPC801

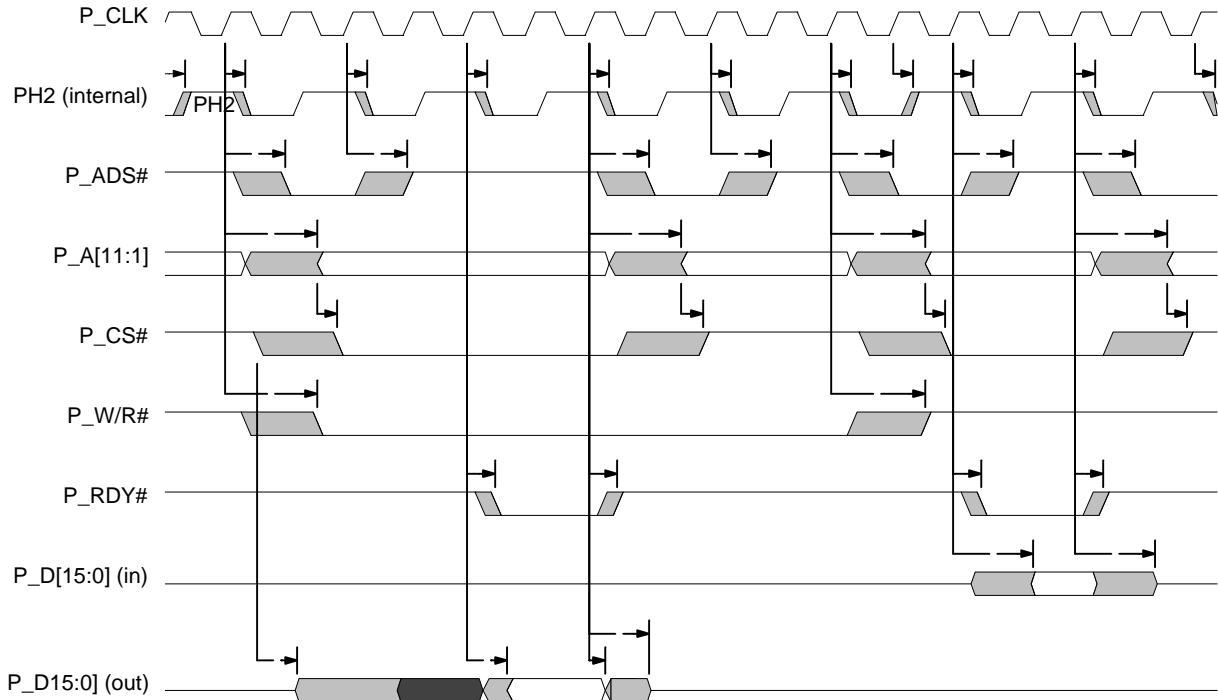
Typical Motorola MPC801 CPU I/O Access Operations

4.2.3 Intel 486 Processor Interface

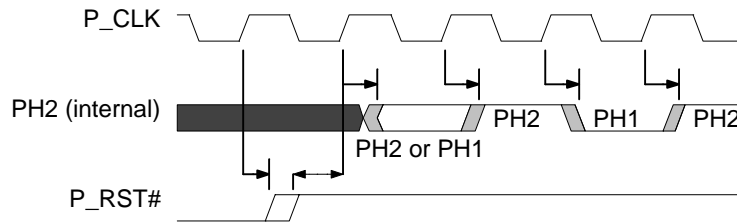


Typical 486 CPU I/O Access Operations

4.2.4 Intel 386 Processor Interface



Typical 386 CPU I/O Access Operations



Internal PH2 Clock Synchronization **

Note: ** See Intel 386 Processor Data Book for more details

4.2.5 Register Map

Note: All 32-bit registers are D-word aligned.

All 16-bit registers are also D-word aligned and right justified.

For the Little Endian CPUs, register offset bit [1,0] are always set to be 00.

For the Big Endian CPUs, register offset bit [1,0] are always set to be 10.

- ① This is a Global Register. CPU is allowed to write the Global Register of all devices by a single operation.
- ② These registers are reserved for system diagnostic usage only.

| Register | Description | I/O Offset | | Reg. Size | W/R | Note: |
|---|--|---------------|------------|-----------|------|-------|
| | | Little Endian | Big Endian | | | |
| Device Configuration Registers (DCR) | | | | | | |
| GCR | Global Control Register | hF00 | hF02 | 16-bit | W/-- | ① |
| DCR0 | Device Status Register | hF00 | hF02 | 16-bit | --/R | |
| DCR1 | Signature & Revision Register | hF10 | hF12 | 16-bit | --/R | |
| DCR2 | ID Register | hF20 | hF22 | 16-bit | W/R | |
| DCR3 | Device Configuration Register | hF30 | hF32 | 16-bit | W/R | |
| DCR4 | Interfaces Status Register | hF40 | hF42 | 16-bit | --/R | |
| DTSR | Test Register | hF70 | hF72 | 16-bit | W/R | |
| Interrupt Controls | | | | | | |
| ISR | Interrupt Status Register – Unmasked | hF80 | hF82 | 16-bit | --/R | |
| ISRM | Interrupt Status Register – Masked | hF90 | hF92 | 16-bit | --/R | |
| IMSK | Interrupt Mask Register | hFA0 | hFA2 | 16-bit | W/R | |
| IAR | Interrupt Acknowledgment Register | hFB0 | hFB2 | 16-bit | W/-- | |
| Buffer Memory Interface | | | | | | |
| MWAR | Memory Write Address Reg. – Single Cycle | hE08 | hE08 | 32-bit | W/R | |
| MRAR | Memory Read Address Reg. – Single Cycle | hE18 | hE18 | 32-bit | W/R | |
| MBAR | Memory Address Register – Burst Mode | hE28 | hE28 | 32-bit | W/R | |
| MWBS | Memory Write Burst Size (in D-words) | hE40 | hE42 | 16-bit | W/R | |
| MRBS | Memory Read Burst Size (in D-words) | hE50 | hE52 | 16-bit | W/R | |
| MWDR | Memory Write Data Register | hE68 | hE68 | 32-bit | W/-- | |
| MWDX | Memory Write Data Reg. – Byte Swapping | hE6C | hE6C | 32-bit | W/-- | |
| MRDR | Memory Read Data Register | hE68 | hE68 | 32-bit | --/R | |
| MRDX | Memory Read Data Reg. – Byte Swapping | hE6C | hE6C | 32-bit | --/R | |
| FCB Buffer & Stack Management | | | | | | |
| FCBBA | Frame Control Buffer – Base Address | hD00 | hD02 | 16-bit | W/R | |
| FCBAG | Frame Control Buffer – Buffer Aging Status | hD30 | hD32 | 16-bit | --/R | ② |
| FCBSL | Frame Ctrl Buffer Stack – Size Limit | hD90 | hD92 | 16-bit | W/R | |
| FCBST | Frame Ctrl Buffer Stack – Buffer Low Threshold | hDA0 | hDA2 | 16-bit | W/R | |
| FCBSS | Frame Ctrl Buffer Stack – Allocation Status | hDB0 | hDB2 | 16-bit | --/R | ② |

| Register | Description | I/O Offset | | Reg. Size | W/R | Note: |
|---|---|---------------|------------|-----------|------|-------|
| | | Little Endian | Big Endian | | | |
| Access Control Function (Chip Level controls) | | | | | | |
| AVXR | VLAN Control Table (VCT) Index Register | hC00 | hC02 | 16-bit | W/-- | |
| AVDR | VCT Data Register | hC10 | hC12 | 16-bit | W/R | |
| AVTC | VLAN Type Code | hC20 | hC22 | 16-bit | W/R | |
| AXSC | Transmission Scheduling Control Register | hC30 | hC32 | 16-bit | W/R | |
| AMIIC | MII Command Register | hC40 | hC40 | 32-bit | W/-- | |
| AMIIS | MII Status Register | hC40 | hC40 | 32-bit | --/R | |
| AFCR | Flow Control Register | hC70 | hC72 | 16-bit | W/R | |
| AMAR0 | Multicast Address. for MAC Control Frames Byte [1,0] | hC80 | hC82 | 16-bit | W/R | |
| AMAR1 | Byte [3,2] | hC90 | hC92 | 16-bit | W/R | |
| AMAR2 | Byte [5,4] | hCA0 | hCA2 | 16-bit | W/R | |
| AMCT | MAC Control FrameType Code Register | hCB0 | hCB2 | 16-bit | W/R | |
| ADAR0 | Base MAC Address Register – Byte [1,0] | hCC0 | hCC2 | 16-bit | W/R | |
| ADAR1 | Base MAC Address Register – Byte [3,2] | hCD0 | hCD2 | 16-bit | W/R | |
| ADAR2 | Base MAC Address Register – Byte [5,4] | hCE0 | hCE2 | 16-bit | W/R | |
| Ethernet MAC Port Control Registers – (substitute [n] with Port Number, n = {0..3}) | | | | | | |
| ECR0 | MAC Port Control Register | hn00 | hn02 | 16-bit | W/R | |
| ECR1 | MAC Port Configuration Register | hn10 | hn12 | 16-bit | W/R | |
| ECR2 | MAC Port Interrupt Mask Register | hn20 | hn22 | 16-bit | W/R | |
| ECR3 | MAC Port Interrupt Status Register | hn30 | hn32 | 16-bit | --/R | |
| EXSR | MAC Tx Status Register | hn40 | hn42 | 16-bit | --/R | ② |
| EXEC | MAC Tx Error Counters | hn50 | hn52 | 16-bit | --/R | ② |
| ERSR | MAC Rx Status Register | hn68 | hn68 | 32-bit | --/R | ② |
| EREC | MAC Rx Error Counters | hn78 | hn78 | 32-bit | --/R | ② |

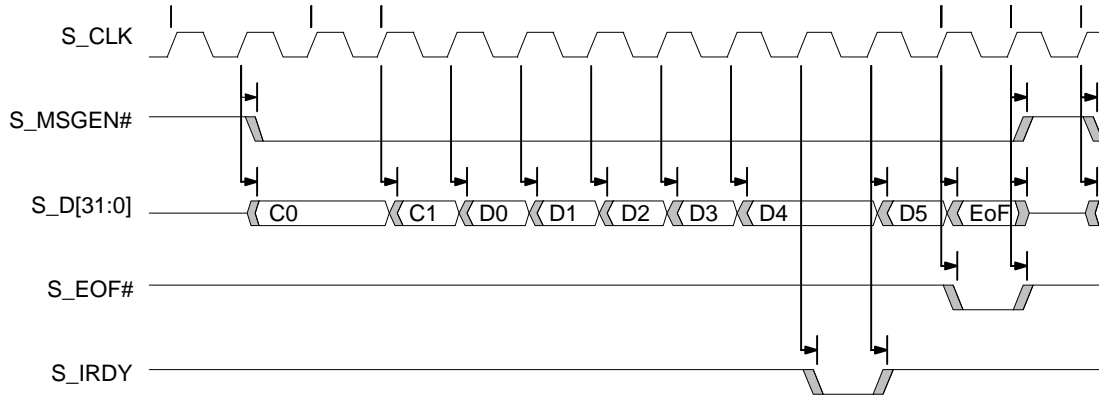
4.3 XpressFlow Bus Operation

- ◆ Vertex's optimized XpressFlow Bus architecture
- ◆ Provides up to 1.6G bps switching bandwidth
 - ◇ -33 1.07G bps
 - ◇ -40 1.28G bps
 - ◇ -50 1.60G bps
- ◆ Full multi bus master structure
- ◆ Allows Access Controllers to communicate with XpressFlow Engine and other Access Controllers via a message passing protocol
- ◆ Two level bus request priorities
 - ◇ High priority for Data Messages
 - ◆ for forwarding an Ethernet frame from receiving port to transmission port
 - ◇ Low priority for Command Messages
 - ◆ for passing control information between devices

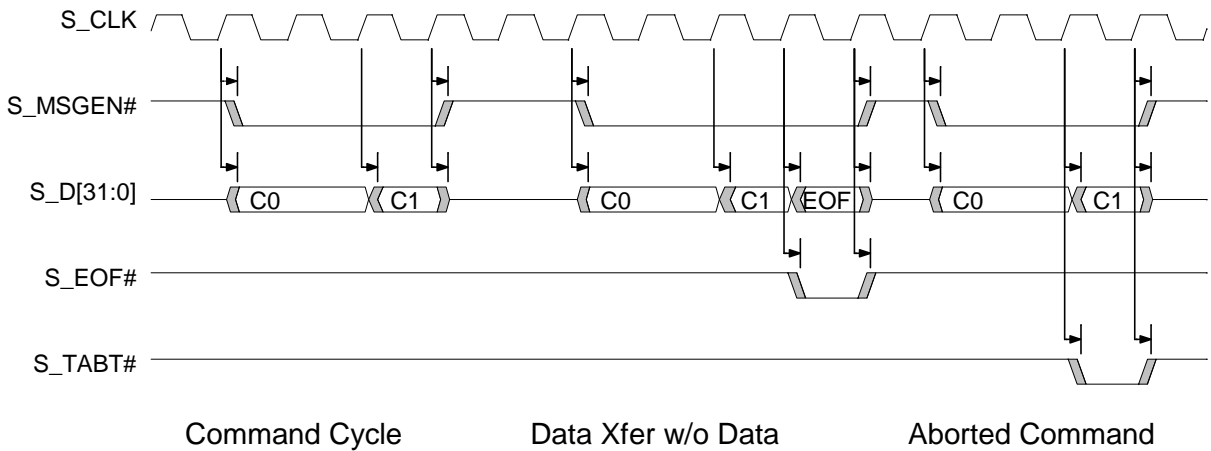
4.3.1 Pin Description

| Symbol | Type | Name & Functions |
|-----------|-------------|--|
| S_D[31:0] | CMOS I/O-TS | Data Bus Bit [31:0] – a 32-bit synchronous data bus. Note: During the system RESET period, Data Bit [31:27] are used as Processor Interface Configuration bit [0:3] |
| S_MSGEN# | CMOS I/O-TS | Message Envelope – encompasses the entire period of a message transfer. Targets use the leading edge of this signal to detect the beginning of a message transfer, and to decode the message header for the intended target(s). |
| S_EOF# | CMOS I/O-TS | End of Frame – only used by frame data transfer messages to identify the end of frame condition. This signal is synchronous with the Rx Frame Status word appended to the end of the message. |
| S_IRDY | CMOS I/O-TS | Initiator Ready – a normal true signal. When negated, it indicates the initiator had asserted wait state(s) in between command words. Target should use this signal as enable signal for latching the data from the bus. |
| S_TABT# | CMOS I/O-OD | Target Abort – when asserted, the target had aborted the reception of current message on the bus. |
| S_HPREQ# | CMOS I/O-OD | High Priority Request – indicates one or more Bus Requester is requesting for high priority message transfer. |
| S_REQ# | CMOS Output | Bus Request – Bus Request signal from Access Controller to Bus Access Arbitrator in XpressFlow Engine |
| S_GNT# | CMOS Input | Bus Grant – Bus Grant signal from Bus Arbitrator to Bus Requester |
| S_OVLD# | CMOS Input | Bus Over-load – when asserted, all data forwarding bus bandwidth has been allocated. Cannot support additional load for data forwarding traffic. |
| S_CLK | CMOS Input | XpressFlow Bus Clock – up to 50MHz system clock |

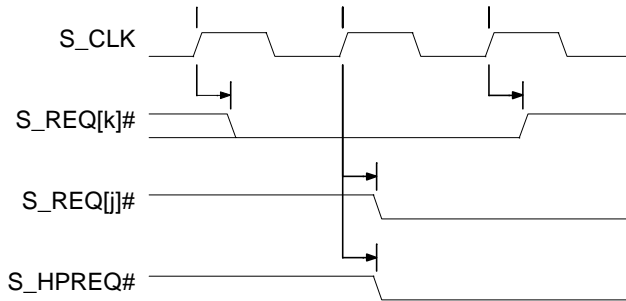
4.3.2 Bus Cycle Waveforms



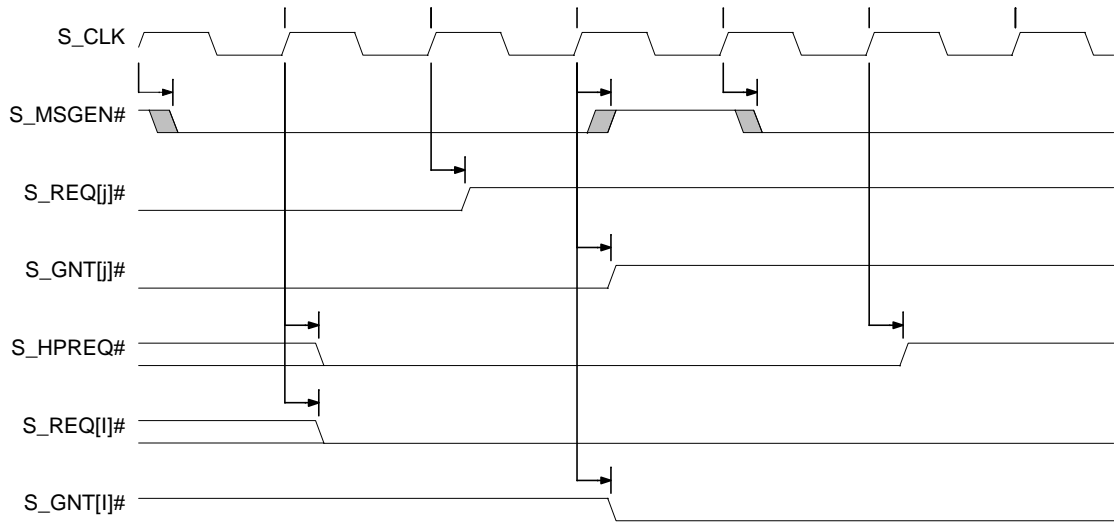
XpressFlow Bus Data Transfer Cycle



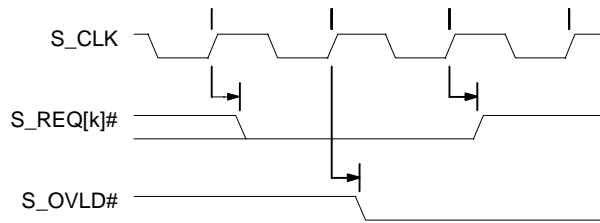
Other XpressFlow Bus Cycles



High Priority Request pre-empts the low priority request.



XpressFlow Bus arbitration



Bus Overload pre-empts the data transfer request

4.4 MII Interface

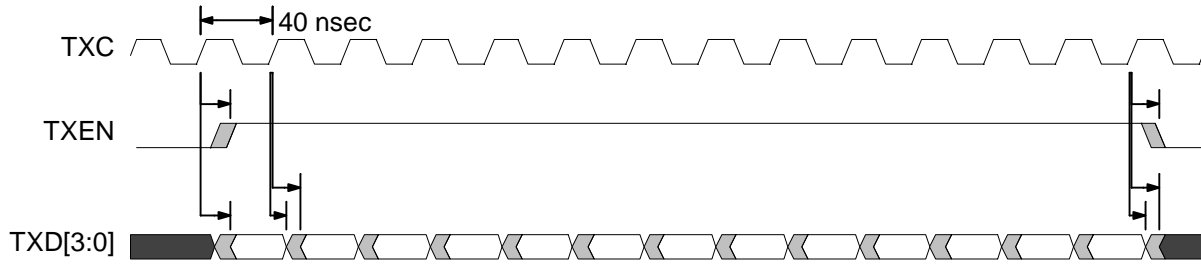
- ◆ Fully compliant with IEEE 802.3u Media Independent Interface for connecting with external 10/100M Ethernet Physical Layer Transceiver
- ◆ Supports both 10Mbps 10BaseT interface and 100Mbps 100BaseTx interface
- ◆ Supports both half and full duplex operation
- ◆ Shared Station Management interface (one for all MII channels with in the Access Controller)
- ◆ All ports can also support 10Mbps Serial Interface
 - ◇ If 10Mbps Serial Interface is used, the MII port pin assignment are re-mapped for 10Mbps Serial Interface.

4.4.1 Pin Description

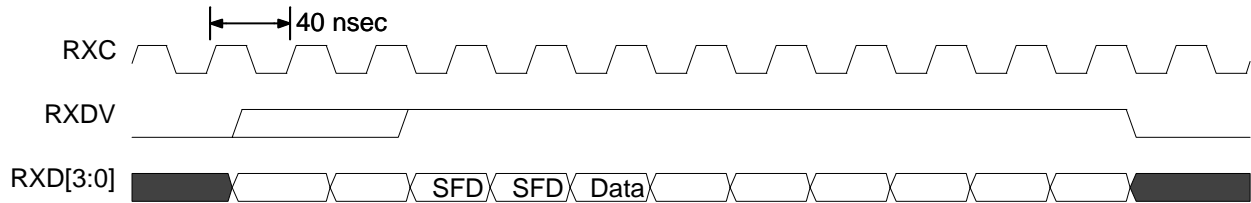
| Symbol | Type | Name & Functions |
|-------------|-----------------|---|
| M_MDC | CMOS Output | MII Management Data Clock – (common for all MII Ports) used to synchronize the MII data stream (MDIO) for transferring between the Access Controller and the MII Transceivers. |
| M_MDIO | TTL IO-TS (5VT) | MII Management Data I/O – (common for all MII Ports) a serial management data stream synchronous with MDC. |
| Mm_RXD[3:0] | TTL In (5VT) | Receive Data [3:0] – (one set for each MII Port) a four-bit transmit data nibble. Bit 0 is the least significant bit, and bit 3 is the most significant bit. |
| Mm_RXDV | TTL In (5VT) | Receive Data Valid – (one for each MII Port) instructs the MAC to begin moving data nibbles from the receive data lines. |
| Mm_RXC | TTL In (5VT) | Receive Clock – (one for each MII Port) a 25MHz clock input with 35% to 65% duty cycles. |
| Mm_RXER | TTL In (5VT) | Receive Error – (one for each MII Port) |
| Mm_TXER | CMOS Output | Transmit Error – (one for each MII Port) |
| Mm_TXC | TTL In (5VT) | Transmit Clock – (one for each MII Port) a continuous clock input with 35% to 65% duty cycles. |
| Mm_TXEN | CMOS Output | Transmit Enable – (one for each MII Port) instructs the transceiver to begin moving data nibbles on the transmit data lines. |
| Mm_TXD[3:0] | CMOS Output | Transmit Data [3:0] – (one set for each MII Port) a four-bit transmit data nibble. Bit 0 is the least significant bit, and bit 3 is the most significant bit. |
| Mm_COL | TTL In (5VT) | Collision Detected – (one for each MII Port) |
| Mm_CRS | TTL In (5VT) | Carrier Sense – (one for each MII Port) |
| Mm_LNK ① | TTL In (5VT) | Link Status – (one for each MII Port) The polarity of this signal is programmable via Port Configuration Register |

Note: “m” is the port number [3:0].

① These signals have programmable output polarity.



100M MII Transmit Timing



100M MII Receive Timing

4.4.2 PIN Mapping between MII Interface and 10Mbps Serial Interface

| MII Interface | | 10Mbps Serial Interface | | |
|---------------|--------------|-------------------------|--------------|---|
| Symbol | Type | Symbol | Type | Name & Functions |
| Mm_RXD[3:1] | TTL In (5VT) | | | Not used by Serial Interface Ports. <i>Has a weak internal pull-up resistor.</i> |
| Mm_RXD[0] | TTL In (5VT) | Tm_RXD | TTL In (5VT) | Receive Data – (one for each Serial Interface Port) a receive data stream. |
| Mm_RXDV | TTL In (5VT) | | | Not used by Serial Interface Ports. <i>Has a weak internal pull-up resistor.</i> |
| Mm_RXC | TTL In (5VT) | Tm_RXC | TTL In (5VT) | Receive Clock – (one for each Serial Interface Port) |
| Mm_RXER | TTL In (5VT) | | | Not used by Serial Interface Ports. <i>Has a weak internal pull-up resistor.</i> |
| Mm_TXER | CMOS Output | | | Not used by Serial Interface Ports. |
| Mm_TXC | TTL In (5VT) | Tm_TXC | TTL In (5VT) | Transmit Clock – (one for each Serial Interface Port) a continuous clock input with 35% to 65% duty cycles. |
| Mm_TXEN | CMOS Output | Tm_TXEN | CMOS Output | Transmit Enable – (one for each Serial Interface Port) |
| Mm_TXD[0] | CMOS Output | Tm_TXD | CMOS Output | Transmit Data – (one for each Serial Interface Port) a transmit data stream. |
| Mm_TXD[1] | CMOS Output | | | Not used by Serial Interface Ports |
| Mm_TXD[2] | CMOS Output | Tm_LPBK ① | CMOS Output | Loop Back Enable – (one for each Serial Interface Port) <i>The polarity of this signal is programmable via Port Configuration Register</i> |
| Mm_TXD[3] | CMOS Output | Tm_FD ① | CMOS Output | Full Duplex Mode – (one for each Serial Interface Port) <i>The polarity of this signal is programmable via Port Configuration Register</i> |
| Mm_COL | TTL In (5VT) | Tm_COL | TTL In (5VT) | Collision Detected – (one for each Serial Interface Port) |
| Mm_CRS | TTL In (5VT) | Tm_CRS | TTL In (5VT) | Carrier Sense – (one for each Serial Interface Port) |
| Mm_LNK ① | TTL In (5VT) | Tm_LNK ① | TTL In (5VT) | Link Status – (one for each Port) <i>The polarity of this signal is programmable via Port Configuration Register</i> |

Note: “m” is the port number [3:0].

① These signals have programmable output polarity.

4.5 Test Facility

| Symbol | Type | Name & Functions |
|--------|-------------|---|
| T_MODE | CMOS I/O TS | Test Mode Selection & Test Output – Set Test Mode upon Reset, and provides test status output during test mode |

5. DC SPECIFICATION

5.1 ABSOLUTE MAXIMUM RATINGS

| | |
|--|-------------------------------|
| Storage Temperature | -65°C to +150°C |
| Operating Temperature | 0°C to +70°C |
| Supply Voltage V_{DD} with Respect to V_{SS} | +3.0 V to +3.6 V |
| Voltage on 5V Tolerant Input Pins | -0.5 V to ($V_{DD} + 2.5$ V) |
| Voltage on Other Pins | -0.5 V to ($V_{DD} + 0.5$ V) |

Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

5.2 DC CHARACTERISTICS

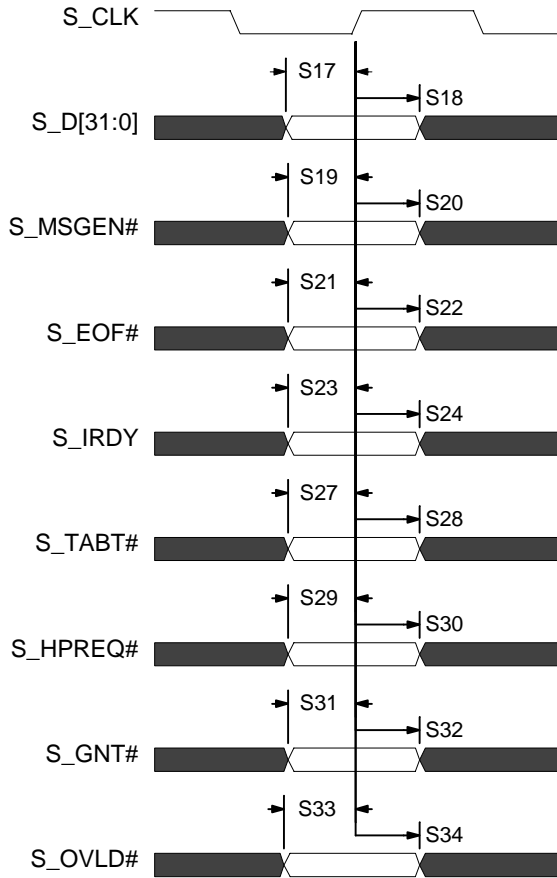
$V_{DD} = +3.0$ V to +3.6 V $T_{AMBIENT} = 0^{\circ}$ C to +70°C

| Symbol | Parameter Description | Preliminary | | | Unit |
|---------------|--|----------------------|-----|----------------------|---------------|
| | | Min | Typ | Max | |
| f_{osc} | Frequency of Operation (-33) | 20 | | 33.3333 | MHz |
| | Frequency of Operation (-40) | 20 | | 40.0000 | MHz |
| | Frequency of Operation (-50) | 20 | | 50.0000 | MHz |
| I_{DD} | Supply Power – @ 33.3333 MHz ($V_{DD}=3.3$ V) | | | TBD | mA |
| | Supply Power – @ 40 MHz ($V_{DD}=3.3$ V) | | | TBD | mA |
| | Supply Power – @ 50 MHz ($V_{DD}=3.3$ V) | | | TBD | mA |
| $V_{OH-CMOS}$ | Output High Voltage (CMOS) $I_{OH} = \text{maximum}$ | $V_{DD} - 0.5$ | | | V |
| $V_{OL-CMOS}$ | Output Low Voltage (CMOS) $I_{OL} = \text{maximum}$ | | | 0.45 | V |
| V_{OH-TTL} | Output High Voltage (TTL) $I_{OH} = \text{maximum}$ | 2.4 | | | V |
| V_{OL-TTL} | Output Low Voltage (TTL) $I_{OL} = \text{maximum}$ | | | 0.45 | V |
| $V_{IH-CMOS}$ | Input High Voltage (CMOS) | $V_{DD} \times 70\%$ | | $V_{DD} + 10\%$ | V |
| $V_{IL-CMOS}$ | Input Low Voltage (CMOS) | -0.5 | | $V_{DD} \times 30\%$ | V |
| V_{IH-TTL} | Input High Voltage (TTL) | 2.0 | | $V_{DD} + 10\%$ | V |
| V_{IL-TTL} | Input Low Voltage (TTL) | -0.3 | | +0.8 | V |
| V_{IH-5VT} | Input High Voltage (TTL 5V tolerant) | 2.0 | | $V_{DD} + 1.8$ | V |
| V_{IL-5VT} | Input Low Voltage (TTL 5V tolerant) | -0.3 | | +0.8 | V |
| I_{LI} | Input Leakage Current ($0.1 \text{ V} \leq V_{IN} \leq V_{DD}$) (all pins except those with internal pull-up/pull-down resistors) | | | ± 10 | μA |
| I_{LO} | Output Leakage Current ($0.1 \text{ V} \leq V_{OUT} \leq V_{DD}$) | | | ± 15 | μA |
| I_{IH} | Input Leakage Current $V_{IH} = V_{DD} - 0.1$ V (pins with internal pull-down resistors) | | | 60 | μA |
| I_{IL} | Input Leakage Current $V_{IL} = 0.1$ V (pins with internal pull-up resistors) | | | -60 | μA |
| C_{IN} | Input Capacitance | | 8 | | pF |
| C_{OUT} | Output Capacitance | | 8 | | pF |
| $C_{I/O}$ | I/O Capacitance | | 10 | | pF |

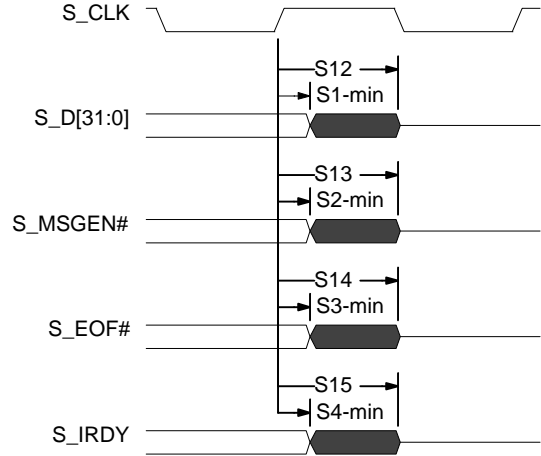
Notes:

6. AC SPECIFICATION

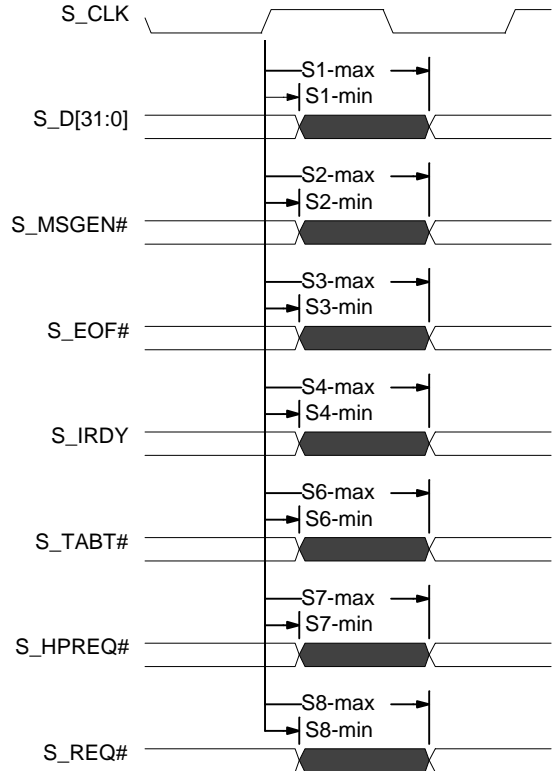
6.1 XpressFlow Bus Interface:



**XpressFlow Bus Interface –
Input setup and hold timing**



**XpressFlow Bus Interface –
Output float delay timing**

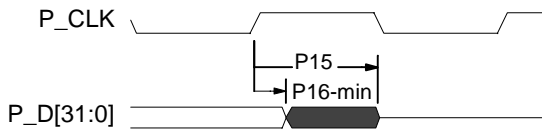


**XpressFlow Bus Interface –
Output valid delay timing**

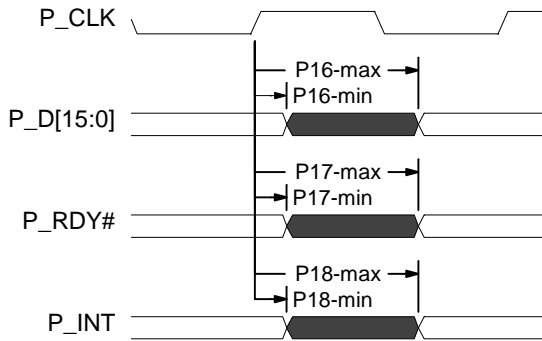
| Symbol | Parameter | -33 | | -40 | | -50 | | Note: |
|--------|------------------------------|----------|----------|----------|----------|----------|----------|-----------------------|
| | | Min (ns) | Max (ns) | Min (ns) | Max (ns) | Min (ns) | Max (ns) | |
| S1 | S_D[31:0] output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 50pf |
| S2 | S_MSGEN# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 50pf |
| S3 | S_EOF# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 50pf |
| S4 | S_IRDY output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 50pf |
| S6 | S_TABT# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 50pf |
| S7 | S_HPREQ# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 50pf |
| S8 | S_REQ# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 20pf |
| S12 | S_D[31:0] output float delay | | 15 | | 13 | | 10 | |
| S13 | S_MSGEN# output float delay | | 15 | | 13 | | 10 | |
| S14 | S_EOF# output float delay | | 15 | | 13 | | 10 | |
| S15 | S_IRDY output float delay | | 15 | | 13 | | 10 | |
| S17 | S_D[31:0] input set-up time | 5 | | 4.5 | | 4 | | |
| S18 | S_D[31:0] input hold time | 2 | | 1.5 | | 1.5 | | |
| S19 | S_MSGEN# input set-up time | 5 | | 4.5 | | 4 | | |
| S20 | S_MSGEN# input hold time | 2 | | 1.5 | | 1.5 | | |
| S21 | S_EOF# input set-up time | 5 | | 4.5 | | 4 | | |
| S22 | S_EOF# input hold time | 2 | | 1.5 | | 1.5 | | |
| S23 | S_IRDY input set-up time | 5 | | 4.5 | | 4 | | |
| S24 | S_IRDY input hold time | 2 | | 1.5 | | 1.5 | | |
| S27 | S_TABT# input set-up time | 5 | | 4.5 | | 4 | | |
| S28 | S_TABT# input hold time | 2 | | 1.5 | | 1.5 | | |
| S29 | S_HPREQ# input set-up time | 5 | | 4.5 | | 4 | | |
| S30 | S_HPREQ# input hold time | 2 | | 1.5 | | 1.5 | | |
| S31 | S_GNT# input set-up time | 5 | | 4.5 | | 4 | | |
| S32 | S_GNT# input hold time | 2 | | 1.5 | | 1.5 | | |
| S33 | S_OVLD# input set-up time | 5 | | 4.5 | | 4 | | |
| S34 | S_OVLD# input hold time | 2 | | 1.5 | | 1.5 | | |

AC Characteristics – XpressFlow Bus Interface

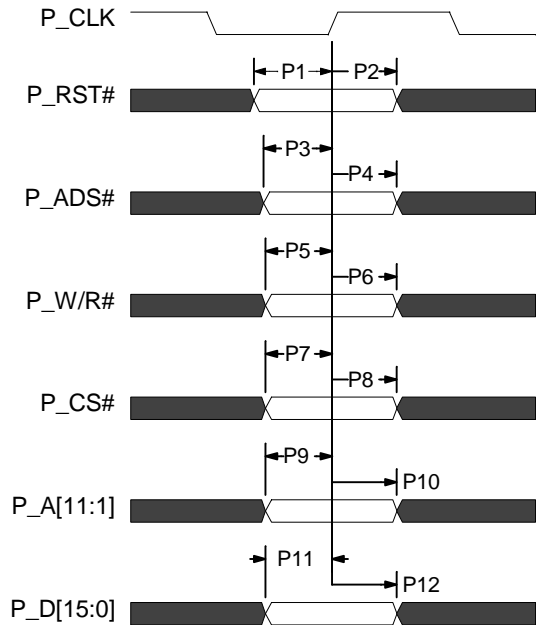
6.2 CPU Bus Interface:



**CPU Bus Interface –
Output float delay timing**



**CPU Bus Interface –
Output valid delay timing**

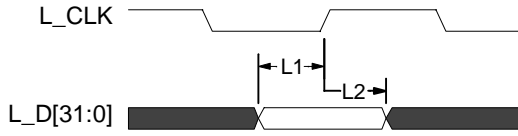


**CPU Bus Interface –
Input setup and hold timing**

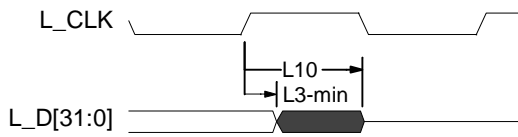
| Symbol | Parameter | -33 | | -40 | | -50 | | Note: |
|--------|---------------------------------|----------|----------|----------|----------|----------|----------|-----------------------|
| | | Min (ns) | Max (ns) | Min (ns) | Max (ns) | Min (ns) | Max (ns) | |
| P1 | P_RST# input setup time | 5 | | 4.5 | | 4 | | |
| P2 | P_RST# input hold time | 2 | | 1.5 | | 1.5 | | |
| P3 | P_ADS# input set-up time | 5 | | 4.5 | | 4 | | |
| P4 | P_ADS# input hold time | 2 | | 1.5 | | 1.5 | | |
| P5 | P_W/R# input set-up time | 5 | | 4.5 | | 4 | | |
| P6 | P_W/R# input hold time | 2 | | 1.5 | | 1.5 | | |
| P7 | P_CS# input set-up time | 5 | | 4.5 | | 4 | | |
| P8 | P_CS# input hold time | 2 | | 1.5 | | 1.5 | | |
| P9 | P_A[11:1] input set-up time | 5 | | 4.5 | | 4 | | |
| P10 | P_A[11:1] input hold time | 2 | | 1.5 | | 1.5 | | |
| P11 | P_D[31:0]# input set-up time | 5 | | 4.5 | | 4 | | |
| P12 | P_D[31:0]# input hold time | 2 | | 1.5 | | 1.5 | | |
| P15 | P_D[31:0]# output float delay | | 15 | | 13 | | 10 | |
| P16 | P_D[31:0]# # output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 60pf |
| P17 | P_RDY# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 60pf |
| P18 | P_INT# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 20pf |

AC Characteristics -- CPU Bus Interface

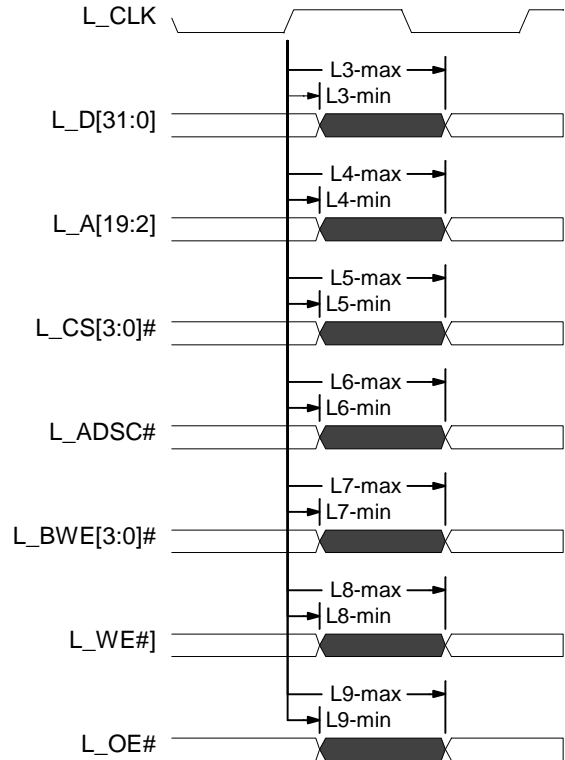
6.3 Local Memory Interface:



**Local Memory Interface –
Input setup and hold timing**



**Local Memory Interface –
Output float delay timing**



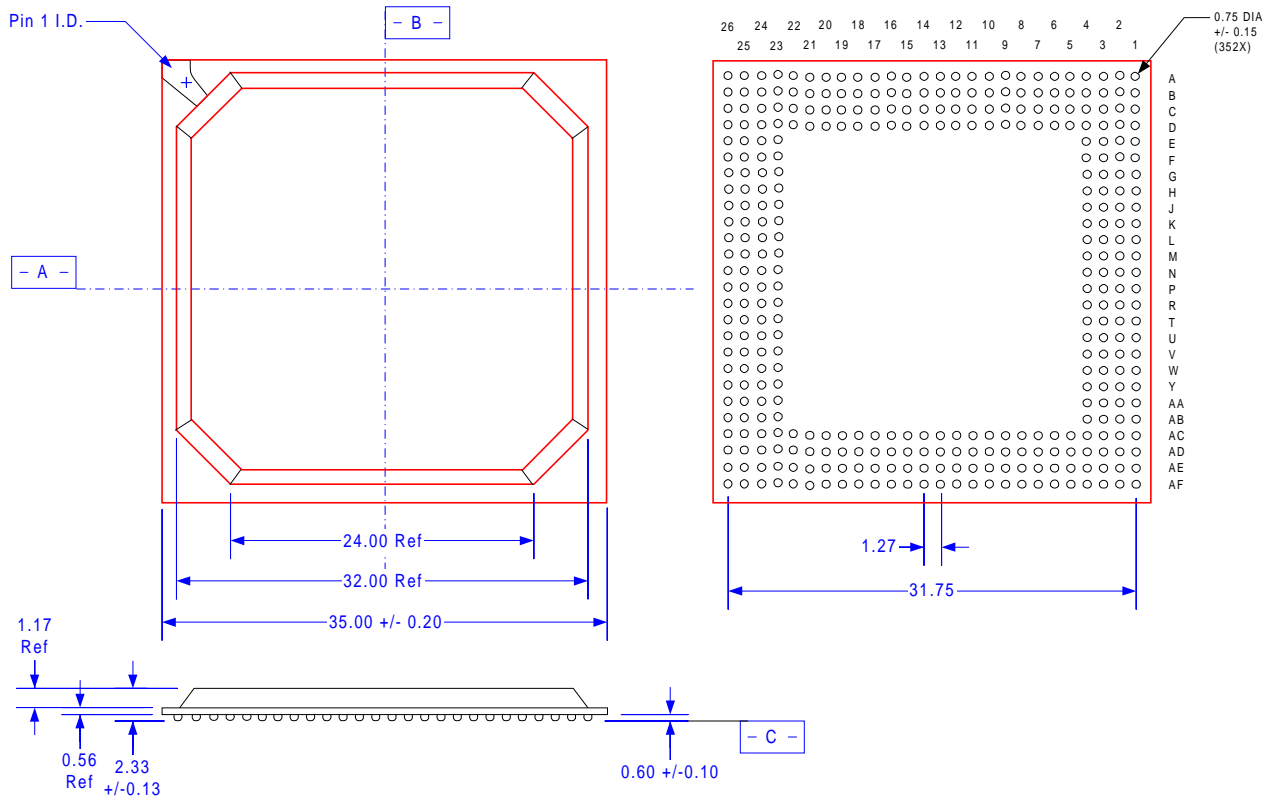
**Local Memory Interface –
Output valid delay timing**

| Symbol | Parameter | -33 | | -40 | | -50 | | Note: |
|--------|--------------------------------|----------|----------|----------|----------|----------|----------|-----------------------|
| | | Min (ns) | Max (ns) | Min (ns) | Max (ns) | Min (ns) | Max (ns) | |
| L1 | L_D[31:0]# input set-up time | 5 | | 4.5 | | 4 | | |
| L2 | L_D[31:0]# input hold time | 2 | | 1.5 | | 1.5 | | |
| L3 | L_D[31:0]# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 30pf |
| L4 | L_A[19:2] output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 30pf |
| L5 | L_CS[3:0]# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | |
| L6 | L_ADSC# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 30pf |
| L7 | L_BWE[3:0]# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 30pf |
| L8 | L_WE# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 10pf |
| L9 | L_OE# output valid delay | 6 | 20 | 5 | 18 | 4 | 15 | C _L = 10pf |
| L10 | L_D[31:0]# output float delay | | 15 | | 13 | | 10 | |

AC Characteristics – Local Memory Interface

7. PACKAGING INFORMATION

**352-PIN BGA
(35x35x2.33mm)**



This Document contains advance information on a product under development. Vertex reserves the right to make any changes without notice.



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