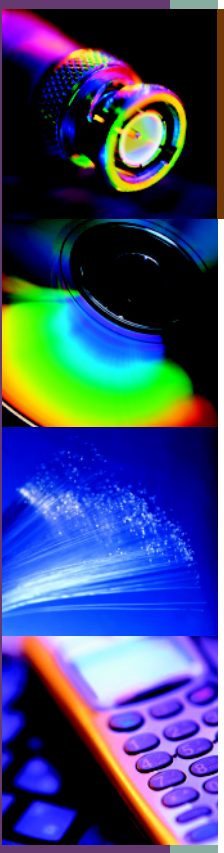

CS3410

High Speed Viterbi/TCM Decoder

AMPHION™
Virtual Components for the Converging World

The CS3410 Viterbi/TCM Decoder is a high performance implementation suitable for a range of Forward Error Correction applications. This highly integrated Application Specific Virtual Component (ASVC) can be used in conjunction with other FEC related cores available from Amphion to rapidly construct complete FEC solutions. The Viterbi/TCM decoder operates in Viterbi or Trellis modes and provides a wide range of coding rates. The CS3410 is available in both ASIC and programmable logic versions that have been hand crafted by Amphion to deliver high performance while minimizing power consumption and silicon area.

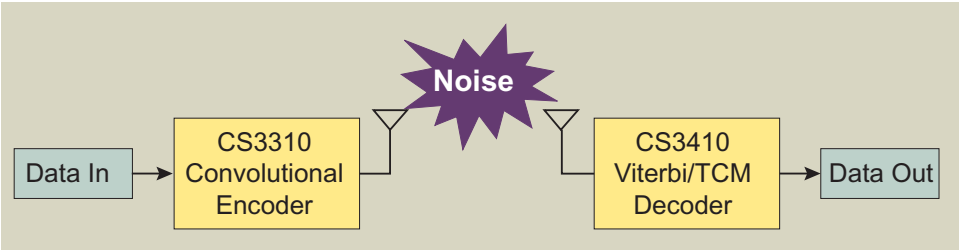

Figure 1: Typical Transmission System Mode

DECODER FEATURES

- **Viterbi/TCM decoder**
  - Constraint length = 7
  - Traceback length = 170
- **Supports block and continuous mode operations**
- **Generator polynomials**
  - G0 = 171 (octal)
  - G1 = 133 (octal)
  - G2 = 165 (octal) Viterbi $\frac{1}{3}$ mode
- **High coding gains at 10^{-5} BER**
  - 5.6dB rate $\frac{1}{3}$ Viterbi
  - 5.2dB rate $\frac{1}{2}$ Viterbi
  - 3.3dB rate $\frac{2}{3}$ TCM
  - 3.5dB rate $\frac{3}{4}$ TCM
- **Synchronization status monitoring**
- **Microprocessor style interface for setup/ control and status monitoring**
- **Automatic phase synchronization**
- **"Force-to-Zero" mechanism (block mode)**
- **Viterbi mode:**
  - Fully compliant with:
    INTELSAT IESS-308/ 309
    DVB ETS 300-421
    DVB-T ETSI 300-744
  - 4-bit soft decision OR 1-bit hard decision inputs
  - Coding rates:
    1/2, 1/3 for QPSK
    2/3, 3/4, 5/6, 7/8 obtainable via external puncture control
  - BER monitoring
- **Trellis mode:**
  - 8-bit I/Q input (direct from demodulator)
  - Coding rates:
    2/3 (8-PSK), 3/4 (16-PSK)

KEY METRICS

- **Size: 272K Gates (STD Cells)**
- **Memory: 203K Gates**
- **Logic area: 69K Gates**
- **Input clock: 100 MHz**

See Tables 7-8 for more details.

APPLICATIONS

- **Wireless LANs**
- **Digital cellular phones**
- **Satellite communications**

CS3410 SYMBOL AND PIN DESCRIPTION

Table 1 provides the descriptions of the input and output ports of the CS3410 Viterbi/TCM decoder (shown graphically in Figure 2). Unless otherwise stated, all signals are active high and bit(0) is the least significant bit.

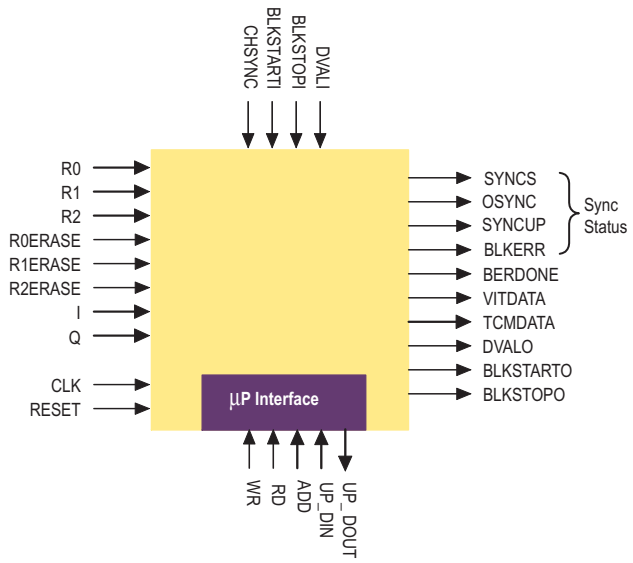

Figure 2: CS3410 Symbol

Table 1: CS3410 - Viterbi/TCM Decoder Interface Signal Definitions

Signal	I/O	Width (Bits)	Description
R0	I	4	Soft decision vector from demodulator (Viterbi mode)
R1	I	4	Soft decision vector from demodulator (Viterbi mode)
R2	I	4	Soft decision vector from demodulator (Viterbi mode – rate 1/3)
R0ERASE	I	1	Erase flag (used to obtain external punctured codes in Viterbi mode) – when active, internal circuitry ignores R0 vector contribution during branch metric calculations.
R1ERASE	I	1	Erase flag (used to obtain external punctured codes in Viterbi mode) – when active, internal circuitry ignores R1 vector contribution during branch metric calculations.
R2ERASE	I	1	Erase flag (used to obtain external punctured codes in Viterbi mode) – when active, internal circuitry ignores R2 vector contribution during branch metric calculations (Viterbi mode – rate 1/3)
I	I	8	I vector direct from demodulator (TCM mode)
Q	I	8	Q vector direct from demodulator (TCM mode)
CLK	I	1	Clock
RESET	I	1	Asynchronous reset
CHSYNC	I	1	External synchronization control (see ADD8 register) – rising edge sensitive.
BLKSTARTI	I	1	Start of block marker – marks the first valid input data symbol
BLKSTOPI	I	1	End of block marker – marks the last valid input data symbol
DVALI	I	1	Input data valid
SYNCS	O	1	Synchronization status: 0 indicates perfect synchronization; 1 indicates that input data is rotated and synchronization is required - updated on SYNCUP.
OSYNC	O	1	'Out-of-sync' as a result of THRES comparison – high if THRES is exceeded during any test period. This signal indicates a loss of synchronization – updated on SYN-CUP (valid for one clock cycle).

Table 1: CS3410 - Viterbi/TCM Decoder Interface Signal Definitions

Signal	I/O	Width (Bits)	Description
SYNCUP	O	1	Indicates synchronization update period – valid for one clock cycle.
BLKERR	O	1	Indicates synchronization loss in block mode – updated on SYNCUP
BERDONE	O	1	BER register updated (Viterbi mode only)
VITDATA	O	1	Viterbi Decoder output
TCMDATA	O	3	TCM decoder output
DVALO	O	1	Output data (decoded) valid
BLK-STARTO	O	1	Start of block marker – marks the first valid output bit(s) of a burst
BLKSTOPO	O	1	End of block marker – marks the last valid output bit(s) of a burst
Microprocessor Interface			
WR	I	1	Write strobe
RD	I	1	Read strobe
ADD	I	4	Address bus
UP_DIN	I	8	Input data
UP_DOUT	O	8	Output data

CONVOLUTIONAL CODES FOR ERROR CORRECTION

Convolutional error-correction capabilities result from outputs that depend on past data values. Each coded bit is generated by convolving the input bit with the previous uncoded bits. Convolving a signal with itself adds a level of dependence on the past values. This mechanism provides the ability to correct (to a certain level) a signal that has been corrupted with noise such as Additive White Gaussian Noise (AWGN).

Data that is convolutionally encoded can be decoded through knowledge of the possible state transitions, created from the dependence of the current symbol on past data. The allowable state transitions are represented by a trellis diagram. Both the Viterbi and TCM (Trellis Coded Modulation) decoder functions supported by CS3410 utilize this principal.

FUNCTIONAL DESCRIPTION

The CS3410 has been designed with high performance applications in mind, e.g. DVB. The speed, error correcting performance and flexibility of CS3410 makes it an all-round contender for many FEC applications. The Viterbi mode is typically used for systems that are power-limited but not bandwidth-limited, whereas the TCM mode is typically used for systems that are both power-limited and bandwidth-limited. As a result, the CS3410 is well suited to many FEC applications including satellite communication networks (IMARSAT and INTELSAT IESS-308/9), microwave links and modems. The following sections describe the main functional blocks for CS3410 configured for Viterbi (Figure 3) or TCM (Figure 4) decoding respectively. These blocks conceptually describe the operation of the CS3410 in these two different modes of operation.

VITERBI MODE

Input Data Interface

Input Data Interface block, formats and arranges data ready for branch metric calculation. This includes a soft decision "swap-and-invert" function as well as erasure tracking control for punctured code rates, where certain bits of the encoded data may be 'punctured', or deleted, and not transmitted. At the receiver, these punctured bits are replaced with null bits prior to decoding with the rate 1/2 decoder. For punctured operation, inserted null bits are marked using the RxERASE input pins. The CS3410 supports signed magnitude or offset binary formatted soft decision input vectors. Table 2 describes these formats.

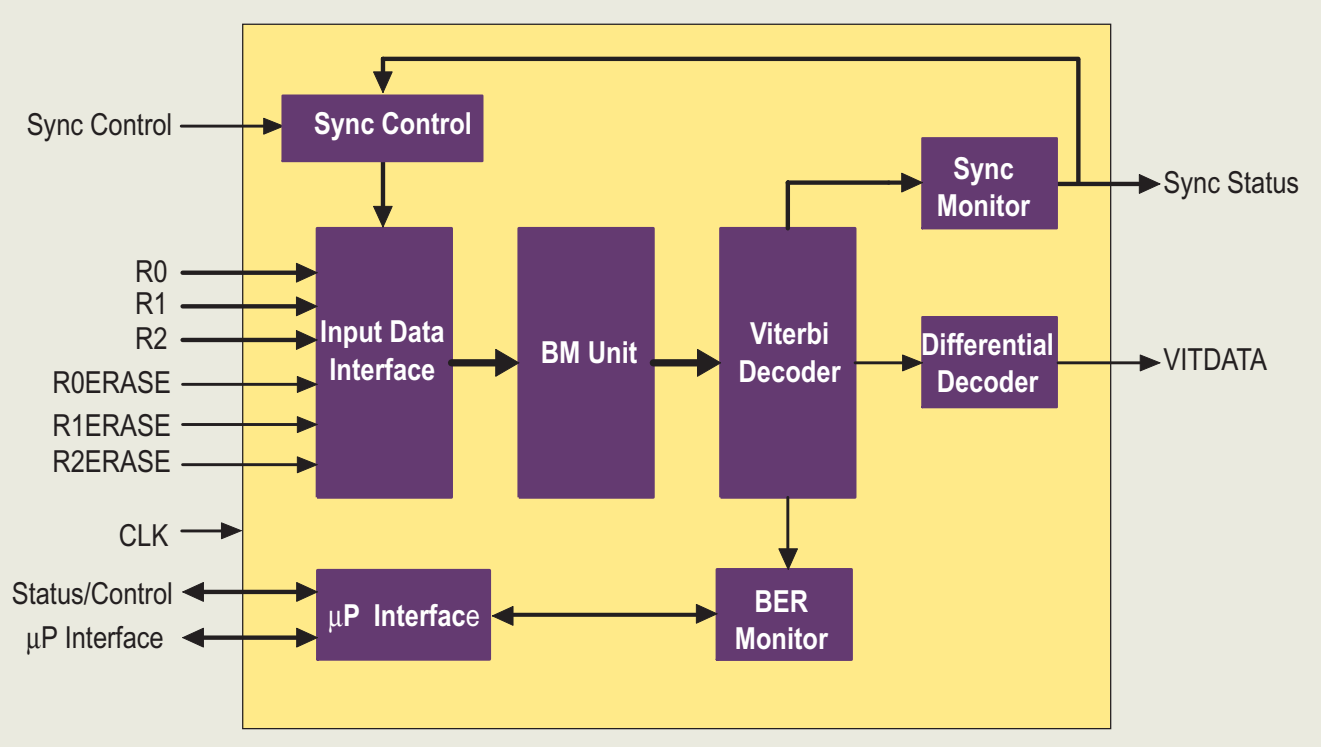

Figure 3: Viterbi Decoder BLock Diagram

Table 2: Input Data Format (Viterbi Mode)

FSEL = 0 (Sign Magnitude)	FSEL = 1 (Offset Binary)	Value
1111	1111	Most confident +
1110	1110	(Data = 1)
1101	1101	
1100	1100	
1011	1011	
1010	1010	
1001	1001	
1000	1000	Least confident +
0000	0111	Least confident -
0001	0110	
0010	0101	
0011	0100	
0100	0011	
0101	0010	
0110	0001	(Data = 0)

Table 2: Input Data Format (Viterbi Mode)

FSEL = 0 (Sign Magnitude)	FSEL = 1 (Offset Binary)	Value
0111	0000	Most confident -

A hard decision mode of operation is also available in Viterbi mode. In this case the input data bits must be connected to the MSB of the Rx ports on the core.

Sync Control

Sync Control block provides a method to control/adjust the phase synchronization of input soft decision vectors ("swap-and-invert"). Used to eliminate ±90° phase ambiguities introduced by QPSK demodulation.

BM Unit

This block is the Branch Metric calculator for Viterbi decoder. When the RxERASE flags are active, the internal circuitry ignores their vector contribution during branch metric calculations.

Viterbi Decoder Core

This block is a 64-state Viterbi core and associated control and memory units.

Differential Decoder

Differential Decoder block is required to eliminate ±180° phase ambiguities introduced by QPSK demodulation (assumes that input data to convolutional encoder has been differentially encoded). A bypass mode is also available.

Sync Monitor

Synchronisation monitor indicates the phase synchronisation status/error with respect to the input data vectors.

BER Monitor

Channel bit error rate estimation unit

µP Interface

Microprocessor interface facilitates the decoder setup/control and status monitoring.

TCM MODE

Input Data Format

In TCM mode, input I/Q vectors must be provided in a signed magnitude form.

TCM BM Unit

This unit provides the branch metric calculator and rotation logic for TCM decoder. It computes branch metrics using 8-bit signed magnitude formatted I/Q vectors. Branch metric rotation is supported for 'out-of-sync' states thus eliminating any ±π/4 (8-PSK) and ±π/8 (16-PSK) phase ambiguities that may arise. A sector number which describes a receive point in PSK space is generated for the PARD unit.

Sync Control

Provides a method to control/adjust the phase synchronization of input I/Q vectors through the rotation of branch metrics in the TCM BM unit.

Viterbi Decoder Core

This block is a 64-state Viterbi core and associated control and memory units.

Differential Decoder/PARD

Differential Decoder and Phase Ambiguity Resolution Decoder (PARD) are used to obtain TCM decoded bits (includes a PARD pre-processor). A differential bypass mode is also available.

Sync Monitor

Synchronization monitor indicates the phase synchronization status/error with respect to the input data vectors.

µP Interface

Microprocessor interface facilitates the decoder setup/control and status monitoring.

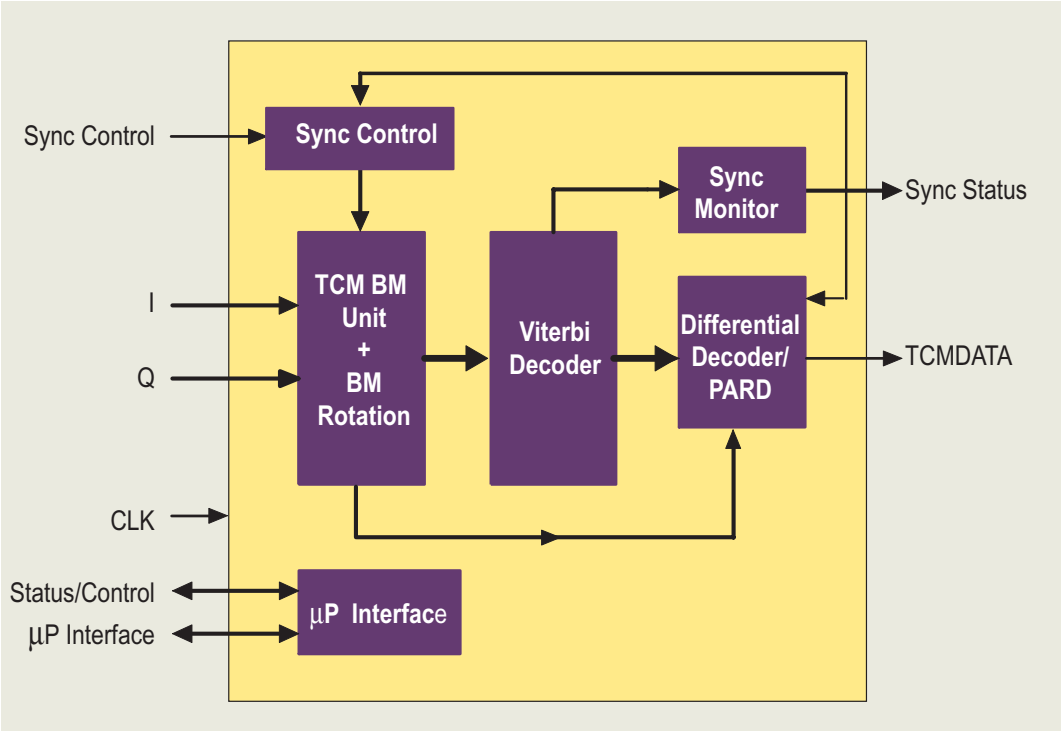

Figure 4: TCM Decoder Block Diagram

THEORY OF OPERATION

VITERBI DECODING

To provide a description of the Viterbi decoder, a brief summary of the main features of its complementary part, the CS3310 Convolutional Encoder is necessary. The CS3310 provides encoded data in a range of rates including 1/3 and 1/2. Other rates are achievable through internal puncture circuitry that deletes bits in a predefined pattern from the symbol stream. Possible data inversion may arise if the receiver/demodulator circuitry is unable to determine the rotation/phase relationship of PSK modulated data. To cope with data inversion, the CS3310 input data stream can be passed through a Differential Encoder prior to encoding (Figure 5). The Differential Encoder effectively transforms an input data stream into an indication of transitions rather than 1's or 0's. On the decoder side (CS3410), a complementary Differential Decoder (Figure 6) converts the output from the Viterbi decoder (transition data) into the original data stream.

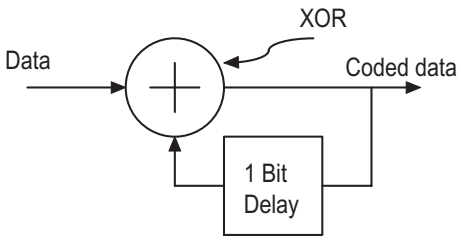

Figure 5: Differential Encoder

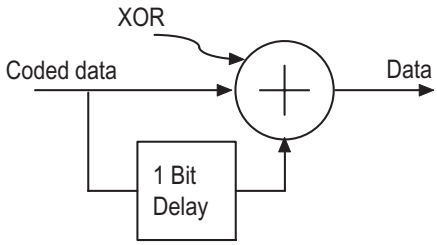

Figure 6: Differential Decoder

It should be noted that the inclusion of the differential encoder/decoder elements marginally degrade the error correcting performance of the core (typical coding gain loss in Viterbi mode ~0.2 dB). To achieve optimal error correcting performance, both the differential encoder and decoder should be bypassed. Therefore, a configuration option is available for both the CS3310 and CS3410 to by pass differential encoder/decoder (Core Control register/ADD8).

The CS3410 core is capable of de-puncturing both rate 1/2 and 1/3 symbol streams although its complementary encoder (CS3310) provides other rates, apart from rate 1/2 and 1/3, based upon a punctured 1/2 symbol stream. Refer to CS3310 literature regarding the puncture pattern usage. RxERASE flags mark the deleted bits on the input symbol to the decoder. For example, when R1ERASE is asserted, the R1 soft decision vector contribution during branch metric calculation will be ignored.

Figure 7 represents a typical transmission using QPSK modulation with its corresponding encoder mapping. Viterbi rate 1/2 mode is well suited to this type of modulation scheme, as 1 uncoded bit becomes 2 coded bits when passed through the Viterbi encoder (CS3310) and QPSK can only transmit one 2-bit symbol at a time.

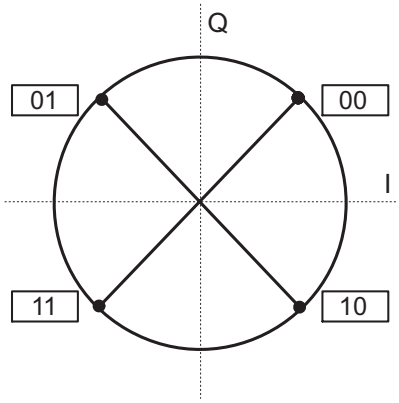

Figure 7: Encoder Output Mapping for QSPK

Since QPSK is only capable of transmitting one 2-bit symbol at a time the encoder mapping becomes more complicated when Viterbi 1/3 is considered. In conjunction with this problem, a suitable input data interface is provided to enable correct data alignment for 'in-sync' and 'out-of-sync' conditions. Figure 8 and Figure 9 illustrate the issue of 'out-of-sync' data vectors thus highlighting the requirement of a suitable data interface.

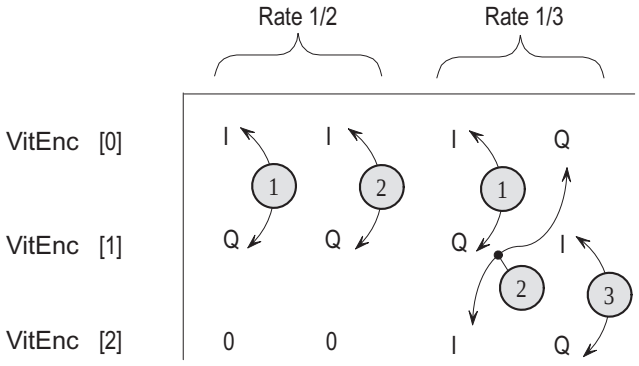

Figure 8: Data Interface Pattern

Figure 8 demonstrates the intended order of an encoded sequence for QPSK modulation and transmission. In Viterbi rate 1/3 mode, output symbols are shared across subsequent QPSK transmissions. If the receiver/demodulator circuitry is unable to determine the rotation/phase relationship of the PSK modulated data, three other rotation positions, illustrated in Figure 9, may exist.

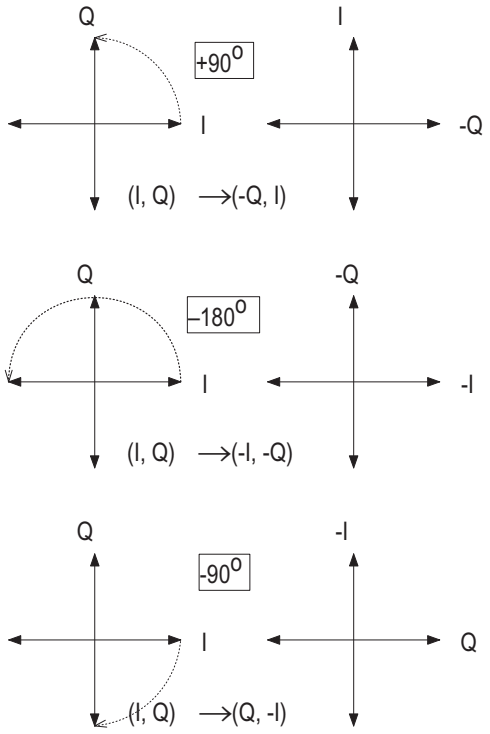

Figure 9: IQ Rotation Pattern

Automatic protection from a ±180° phase ambiguity is available through the use of onboard differential encoding/ decoding blocks (if enabled). The detection of ±90° phase ambiguities is deterministic and can only be reliably judged using the Decoders built-in statistical monitoring circuitry. This case is explained in more detail in Phase Synchronization section.

Table 3 summarizes the methods by which a Viterbi mode of operation may lose synchronization.

Table 3: Phase Synchronization Dependence

Viterbi Rate	Data Interface Pattern	IQ Rotation Pattern
1/2	-	YES
1/3	YES	YES

Data Interface Pattern refers to the input I/Q data sequence of the core illustrated in Figure 8. Therefore, it is evident that in the case of Viterbi rate 1/3, the core may incorrectly lock onto a receive sequence, such as Q/I/Q instead I/Q/I. Also if the received I/Q data sequence is rotated as shown in Figure 8 a vector swap and single vector inversion is required to correct it. Therefore, the built-in data interface in conjunction with the cores Sync Monitor circuitry, is capable of resolving these issues.

Note: Viterbi rate 1/3 phase synchronization may take 1.5x longer than that of the Viterbi rate 1/2 configuration.

The following list summarizes the capability of the Decoders input data interface to handle the issues described above:

- Provision of an input data buffer for Viterbi 1/3 modes where output symbols are shared across subsequent QPSK transmissions.
- A "swap-and-invert" function to correct for ±90° phase ambiguities. This maybe triggered manually or automatically when the core is deemed 'out-of-sync'.

Viterbi decoding consists of 3 main steps: Branch Metric (BM) Calculation, Trellis Computation, and Traceback.

Branch Metric (BM) Calculation

This indicates the correlation between the received code words and all possible code word combinations. Computed BM values are fed into a 64-state Add Compare Select (ACS) block that represents the trellis structure applicable to this core. The decoder determines the state of the encoder using a maximum likelihood technique. The value of the encoder memory is determined as its previous state is already known. For each ACS state, a winning BM value is accumulated in a Path Metric (PM) register.

Trellis Computation

To determine the encoder state, the PM state is monitored for the occurrence probability for each of the 64 possible encoder memory states. As Path Metrics are computed, a binary decision is formed for each of the possible trellis states, thus determining the probable path taken to arrive at a particular state. These binary decisions are stored in 'Decision' memory.

Traceback

Decoded output data is formed from following the path of the current state to a finite past state whilst monitoring the appropriate state transition for each iteration. The effects of noise are minimized as paths to the correct (ideal) path converge after some history (or 'Traceback Length'). The CS3410 Decoder core has a 'Traceback length' of 170 memory and is more than adequate for other higher code rates.

TCM DECODING

Providing a description of the TCM decoding mode of operation also requires a brief summary of the main features of its complementary part, the CS3310 encoder. This core provides encoded data for rate 2/3 (8-PSK) and 3/4 (16-PSK) respectively. The TCM encoding process is a three-stage process as shown in Figure 10.

ENCDAT[0] is differentially encoded (if enabled). Next an industry standard k=7 rate=1/2 Viterbi Encoder is used to encode the subsequent bit into two output bits, TCMEnc[1] and TCMEnc[0], which become the two least significant bits of the PSK phase. Phase Ambiguity Resolution Encoding (PARE) is applied to ENCDAT[1] for 2/3 8-PSK; ENCDAT[1] and ENCDAT[2] for 3/4 16-PSK, modes of operation. The remaining PSK inputs are passed through the PARE (using TCMEnc[1]) to produce corresponding outputs.

Phase Ambiguity Encoding (and subsequent decoding) provides a mechanism to ensure the correct decoding of a data stream once it is known that a locked PSK state is rotated 'out-of-sync'. 'Sync Monitor' circuitry in CS3410 is used in conjunction with other circuit components to compensate for rotated phases. In addition, input and output differential blocks, if enabled, automatically compensate for certain rotated (orthogonal) phases that are shown in Phase Synchronization section, Table 7.

TCM decoding uses the same Viterbi decoder core (k=7, rate = 1/2) already described. Additional circuitry is provided to decode trellis encoded data as shown in Figure 11.

TCM decoding consists of three main steps: Branch Metric and Sector Number Calculation, Viterbi Decoder, and Phase Ambiguity Resolution Decoder (PARD).

Branch Metric (BM) and Sector Number Calculation

Four BM values are calculated directly from the two 8-bit I/Q input vectors that feed the core in this configuration. Internal circuitry computes the 4 closest points to the received point. BM values are determined for each of the four points using the Euclidean distance squared technique. These BM values then fed to a standard k=7, rate =1/2 Viterbi decoder and a sector number is also computed. This value defines a region in which the transmitted point was received. Figure 12 and Figure 13 describe the TCM encoder mapping (and sector number) used by 8-PSK and 16-PSK respectively.

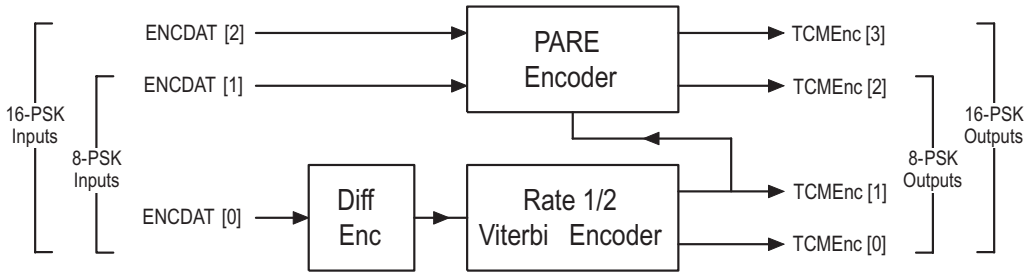

Figure 10: TCM Encoder

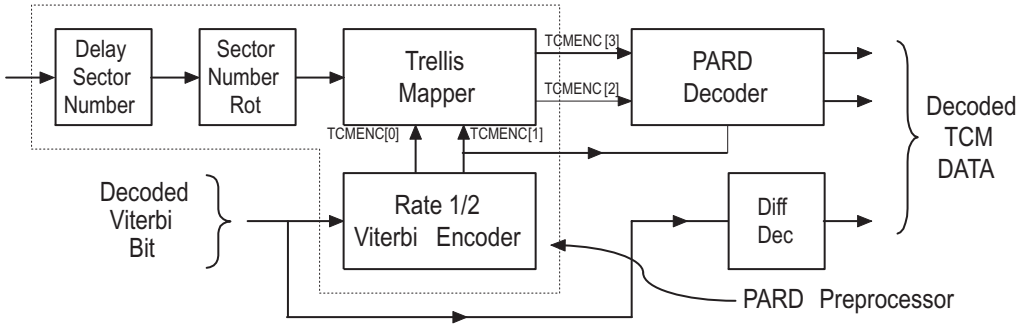

Figure 11: PARD Pre-processor and Decoder

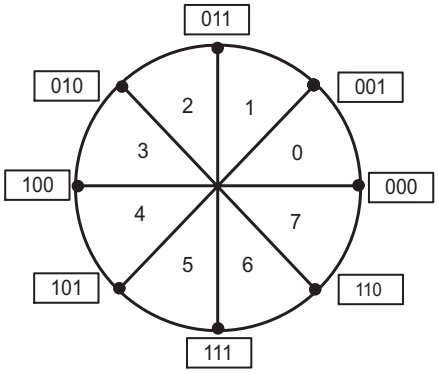

Figure 12: Encoder Output Mapping for 8-PSK

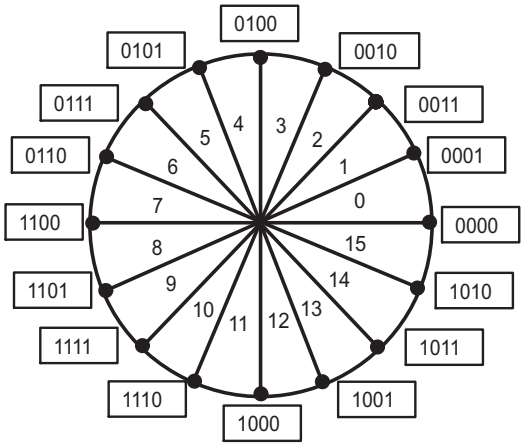

Figure 13: Encoder Output Mapping for 16-PSK

Viterbi Decoder

BM values are processed using a k = 7, rate = 1/2 Viterbi decoder to obtain a decoded output bit.

Phase Ambiguity Resolution Decoding (PARD)

The output of the Viterbi decoder is passed into the PARD pre-processor shown in Figure 11. The pre-processor estimates the original TCM encoded sequence for the PARD and re-encodes the decoded bit from the Viterbi decoder core to generates the best estimate of the transmitted bits, TCMEnc[0] and TCMEnc[1]. These bits correspond to multiple possible phase angles (Figure 12 and Figure 13) in PSK transmission. In 8-PSK, this corresponds to 2 possible phases while in 16-PSK this corresponds to 4 possible phases. The computed sector number for that point is delayed to arrive with its corresponding decoded bit through the Viterbi. The trellis mapper is employed to determine the correct phase angle for that instance, TCMEnc[2] (8-PSK/16-PSK) and TCMEnc[3] (16-PSK). The pre-processed data is then passed through a PARD to produce decoded TCM data.

An 'out-of-sync' condition can arise in TCM mode when input vectors (signed magnitude I/Q) are rotated. In this case two scenarios are possible:

1. Sector Number Rotator ('Sector Number Rot') rotates the sector number by 1 (anti-clock wise)
2. BM values are rotated. Both these events enable the core to establish a correct phase lock and successfully decode data (refer to Phase Synchronization Section).

MICROPROCESSOR INTERFACE DESCRIPTION

This byte-wide interface allows the configuration of the CS3410 to be set by a microprocessor. Twelve 8-bit setup/ control registers are accessible through this interface (see Table 2). Address lines (ADD) select an 8-bit register for a read (RD) or write (WR) access. Write and read data are supplied to/from CS3410 on the UP_DIN and UP_DOUT buses respectively. To write to a register the WR signal must be set high with the associated address value on the ADD bus. On the next positive clock edge after WR has been asserted high the core is configured. The registers may be read by asserting the RD line high with the address bus ADD being set to the address of the register to be read.

MICROPROCESSOR CONFIGURATION REGISTERS

Table 4 provides detailed information on the configuration registers of the CS3410.

Table 4: CS3410 Configuration Registers

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
0	0	BPERIOD LS BYTE							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	BPERIOD MS BYTE							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Table 4: CS3410 Configuration Registers

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
2	2	TPERIOD LS BYTE							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	3	TPERIOD MS BYTE							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
4	4	THRES LS BYTE							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5	5	THRES MS BYTE							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
6	6	CORE SETUP							
							BLK	FSEL	VSD
7	7	CORE MODE							
								RATE1	RATE0
8	8	CORE CONTROL							
						SBD	AUTO	SWAP	DIFF
9	9	CORE STATUS (Read only)							
								SYNCS	ERR
10	A	BER LS BYTE (Read only)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11	B	BER MS BYTE (Read only)							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Table 5: CS3410 Configuration Register Details

Register	Address	Default Value	Description
BPERIOD	0,1	0xFFFF	BER count period value. Sets the range of an internal counter that is used to determine the error rate of the communications channel (Viterbi mode only).
TPERIOD	2,3	0xFFFF	Normalization count period value. Sets the internal range of an internal counter that is used to determine the synchronization status of the CS3410 (using THRES).
THRES	4,5	0xFFFF	Threshold value is used in conjunction with accumulated-metric-normalization count (over TPERIOD) to ascertain synchronization status of CS3410. If the normalization count exceeds THRES then the core is deemed to be 'out-of-sync' (SYNCS on output).
CORE SETUP	6	0x01	**Bit Name Description** D2 BLK Block Mode 0: Continuous Operation 1: Block based operation D1 FSEL Viterbi input data format 0: Signed magnitude 1: Offset binary Note: TCM requires sign magnitude formatted I/Q vectors D0 VSD Viterbi soft decision selector 0: Hard decision, only MSBs of Rx vectors are utilized 1: 4-bit Rx/soft decision vectors are processed by the core.
CORE MODE	7	0x02	D1 RATE1 Viterbi/TCM rate selector (see below) D0 RATE0 TCM 2/3 = 00 TCM 3/4 = 01 VIT 1/2 = 10 VIT 1/3 = 11
CORE CONTROL	8	0x01	D3 SBD Block Mode synchronization update control 0: Continuous 1: Block dependant (resets every block) D2 AUTO Phase synchronization control 0: External synchronization control – Decoder sync state toggles on every rising edge of CHSYNC 1: Automatic phase synchronization – Decoder sync state toggles on every rising edge of OSYNC (internally routed) D1 SWAP Viterbi erasure tracking control 0: Direct mapping of R0/R1/R2ERASE flags 1: Internal swap/tracking of R0/R1/R2ERASE flags D0 DIFF Viterbi/TCM differential decoding control 0: Disable differential decoder/PARD 1: Enable differential decoder/PARD
CORE STATUS	9	This register is Read-only	D1 SYNCS Synchronization status: 0: Indicates perfect synchronization 1: Indicates that input data is rotated and synchronization is required D0 ERR Core configuration error
BER	10, 11	This register is Read-only	Channel bit error rate register (Viterbi only)

Note The default operation of CS3410 (without configuration) is as follows:

- Continuous Viterbi operation at rate 1/2
- Differential decoding ON
- Automatic phase synchronization OFF

The default input vector format to the core is signed magnitude.

ERROR CORRECTING PERFORMANCE

The CS3410 demonstrates high coding gains in all modes of operation. In Viterbi mode a coding gain of 5.6 dB is achievable in rate 1/3 and 5.2 dB in rate 1/2 with a decoded BER of 10-5, as shown in Figure 14. In both TCM 2/3 and 3/4 modes coding gains of 3.3 dB and 3.5 dB respectively are achievable, also with a decoded BER of 10-5 as shown in Figure 15.

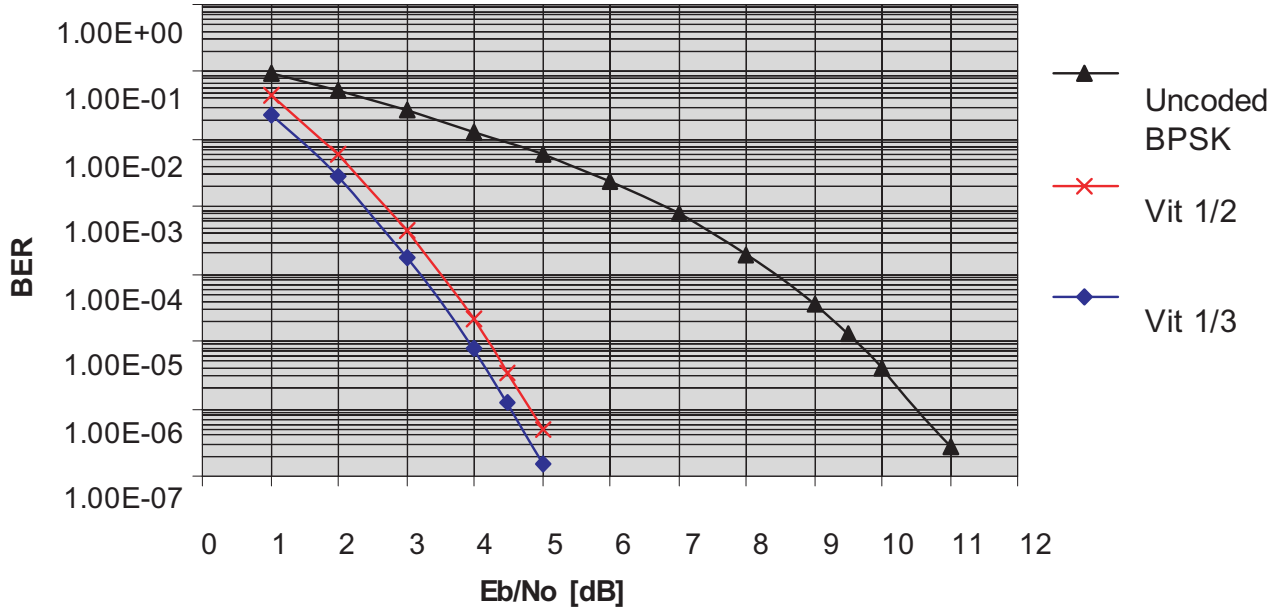

Figure 14: Viterbi Mode Coding Performance

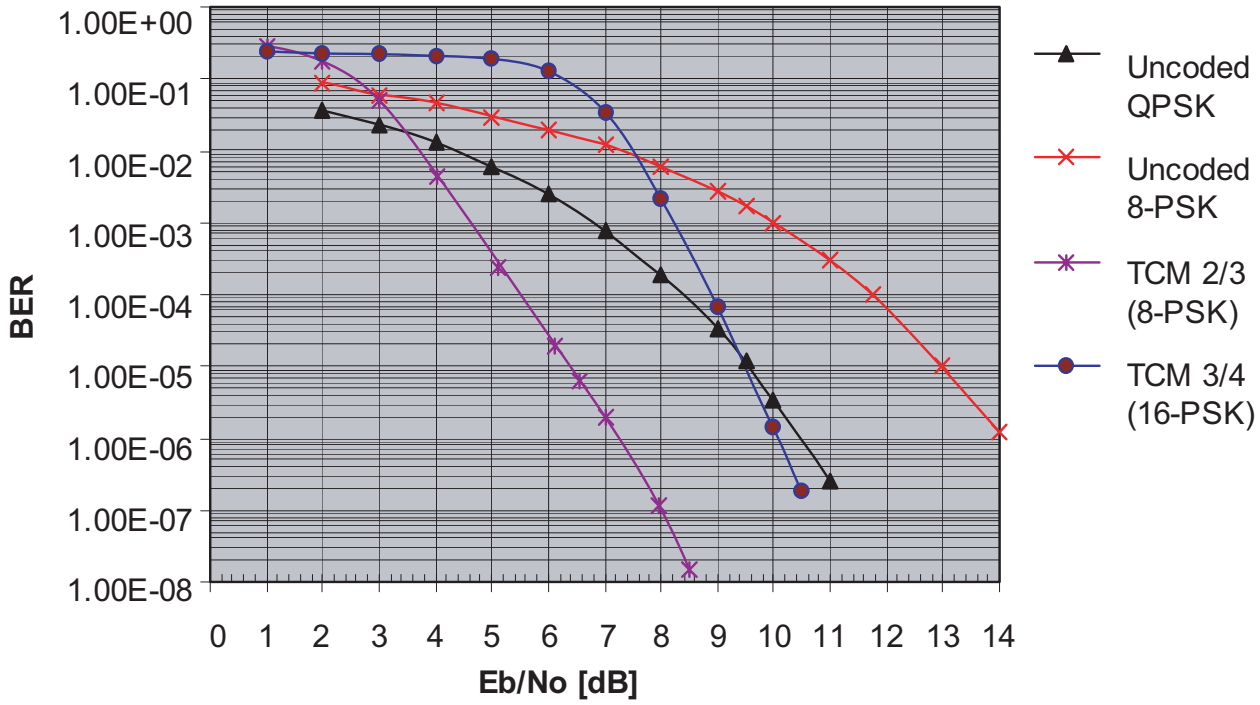

Figure 15: TCM Mode Coding Performance

Differential encoding/decoding marginally degrade (~0.2 dB) these gains.

CS3410 OPERATION AND STRUCTURE

TRACEBACK ARCHITECTURE AND CORE LATENCY

The latency of the core is split into two categories dependant upon burst length.

Bursts <= 340 bitsLatency = Burstlength + Burstlength/2 +16

Bursts > 340 bitsLatency = 526 clocks

The 526 clock cycle latency of the decoder can be attributed mainly to the writing/read-back of decision memory (510 clocks) and some pipeline timing cuts (16 clocks). The 510-clock latency is observed in Figure 16.

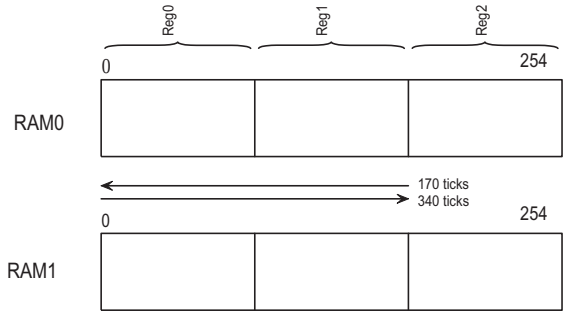

Figure 16: Decoder Clock Cycle Latency

Synchronous dual-port RAM banks, RAM0 and RAM1, are identically configured as 255x64 bits. Processed decisions are always written to memory in the forward direction with a traceback occurring in the reverse direction (only when two regions have been traversed). Processed decisions are written to alternate memory locations in RAM0 and RAM1 and thus require 340 clocks. Traceback starts when two regions have been written to, in which two regions (in this case), Reg1 followed by Reg0, are read back in parallel (170 ticks). Only valid decisions are produced (in this example) during the traceback of Reg0. During the Reg0 traceback a time reversal LIFO buffer is filled. When traceback reaches location 0 of RAM0/1 the LIFO buffer is ready to empty and produce valid output bits.

DECODER BURST DEADTIME

The burst processing nature of the CS3410 decoder requires that there be a minimum deadtime (in clock cycles) between bursts. Bursts types/ranges can be categorized to describe this deadtime. Burst ranges (length) are described by the equation 1. The minimum deadtime for each burst range category (n) is described in Table 6.

$$(n \times 170) + 1 \rightarrow (n+1) \times 170 \qquad \text{where n ranges } 0, 1, 2 \quad \text{[EQN 1]}$$

Table 6: Deadtime burst length dependency

N	Burst range (bits)	Deadtime (clocks)
0	1 to 170	90
1,2	171 to 510	260
3,4,5,6….	511 to …	430

MICROPROCESSOR CONFIGURATION

The microprocessor interface allows the configuration of the CS3410. Address lines (ADD) select an 8-bit register for a read (RD) or write (WR) access. Write and read data are supplied to/from CS3410 on the UP_DIN and UP_DOUT buses respectively. To write to a register the WR signal must be set high with the associated address value on the ADD bus. On the next positive clock edge after WR has been asserted high the core is configured. The registers may be read by asserting the RD line high with the address bus ADD being set to the address of the register to be read. The configuration timing information is shown in Figure 17.

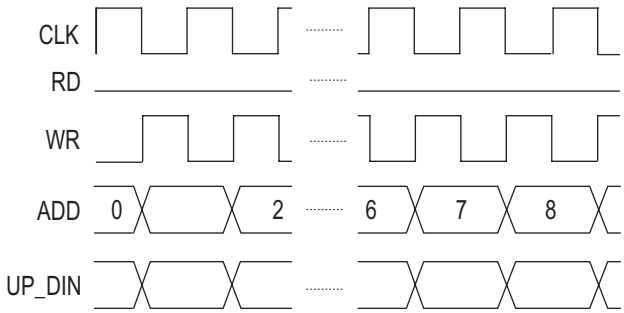

Figure 17: Microprocessor Configuration Signal Timing

CONTINUOUS AND BLOCK MODE

Continuous or Block Mode operation may be applied when CS3410 is configured in Viterbi or Trellis Mode.

In Continuous Mode a high value on DVALI indicates valid input data. DVALO will go high 526 clock cycles (526 clock cycles = latency of the core) after DVALI has been clocked into the core. DVALO will indicate when data at the output is valid as shown in Figure 18.

Figure 19 illustrates the core in Continuous Mode with a random DVALI signal. Here DVALO goes high for 170 clock cycles and then low, depending on the nature of the DVALI signal.

In Block Mode a high value on DVALI indicates valid input data. BLKSTARTI goes high to indicate the start of a block of data. After the block length is reached, BLKSTOPI goes high to signify the end of a block. After the latency of the core has expired (526 clock cycles, assuming a constant DVALI) DVALO and BLKSTARTO go high to indicate valid data, and the start of a decoded block respectively. At the end of a block BLKSTOPO will go high and DVALO goes low. This is shown in Figure 20

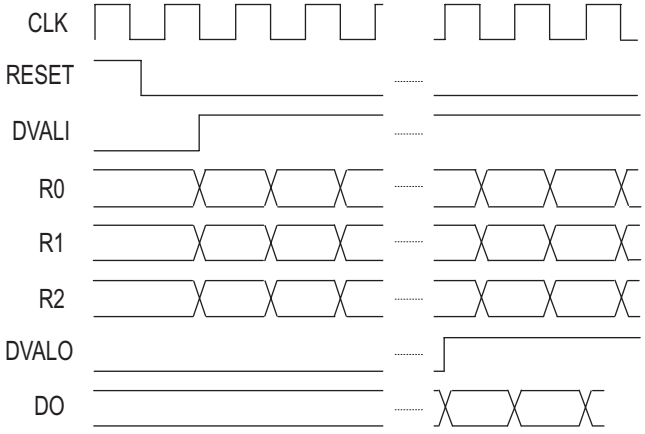

Figure 18: Continuous Mode Operation

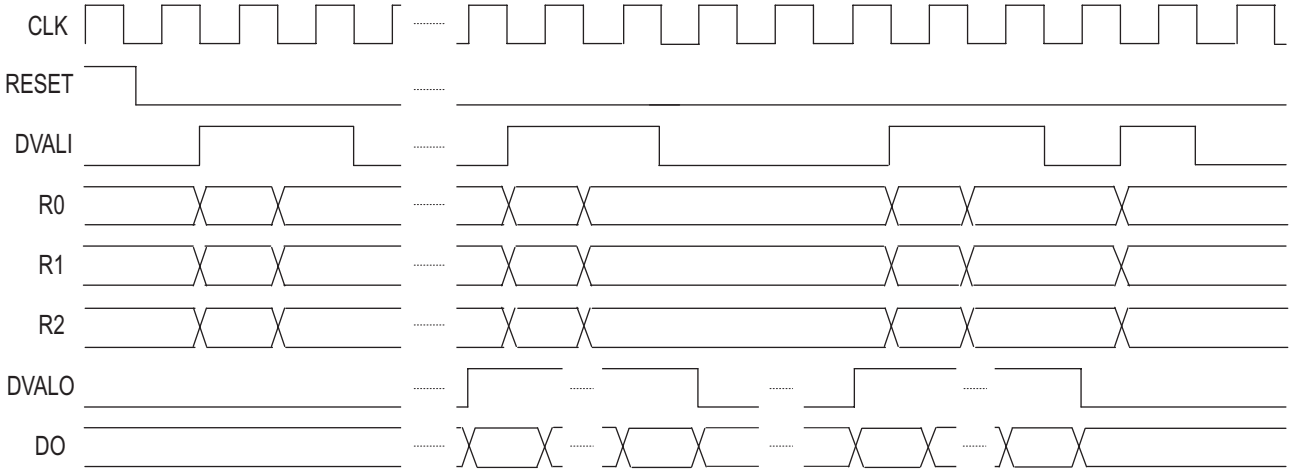

Figure 19: Continuous Mode Operation with a Variable DVALI Signal

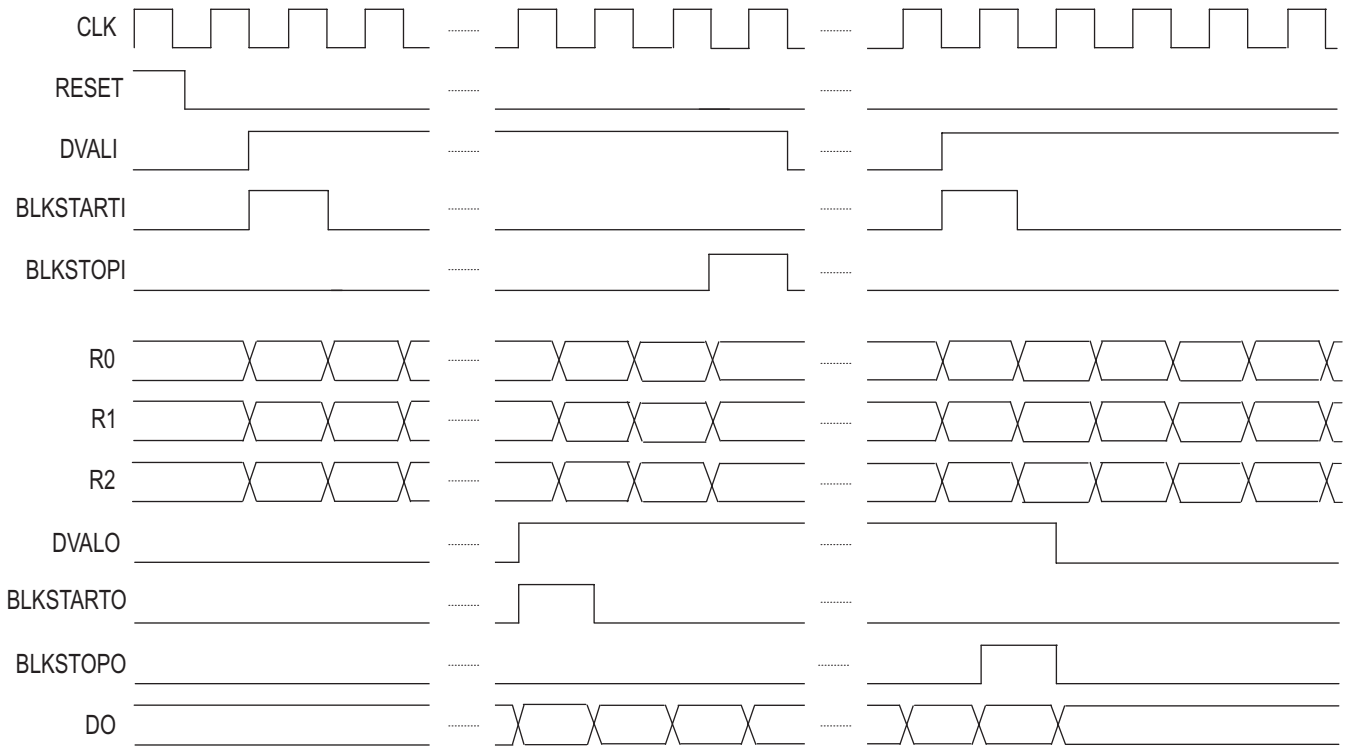

Figure 20: Block Mode Operation

PHASE SYNCHRONIZATION

In both Viterbi and TCM modes of operation, an 'out-of-sync' condition occurs when a tracked internal path metric state (most likely path through 'Decision' memory) grows at an unacceptable 'Normalization' rate. This rate is monitored by the core's 'Sync Monitor' circuitry. The measurement period and threshold value that control this measurement are defined by the core's microprocessor registers, TPERIOD (ADD2/3) and THRES (ADD4/5). TPERIOD defines the count period that increments on DVALI. THRES signal defines a threshold value that an accumulated 'Normalization' count value is compared against. If the THRES value is exceeded when the count period (TPERIOD) has expired an 'out-of-sync' condition is flagged. Table 7 summarizes the phase ambiguity resolution of the core in all modes of operation. For both Viterbi and TCM modes of operation, input and output differential blocks, if enabled, automatically compensate for rotated orthogonal phases. Compensation for other phase angles is implied once the core is deemed 'out-of-sync'.

Table 7: Modulation Type vs Phase Shift

Modulation Type	Possible Phase Shifts	Resolved by Differential Encoders/ Decoder	Resolved by Phase Ambiguity*
QPSK	0°, 90°, 180°, 270°	0°, 180°	90°, 270°
8-PSK	0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°	0°, 90°, 180°, 270°	45°, 135°, 225°, 315°
16-PSK	0°, 22.5°, 45°, 67.5°, 90°, 112.5°, 135°, 157.5°, 180°, 202.5°, 225°, 247.5°, 270°, 292.5°, 315°, 227.5°	0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°	22.5°, 67.5°, 112.5°, 157.5°, 202.5°, 247.5°, 292.5°, 337.5°

Note: 'out-of-sync' condition triggers correction for these phase angles

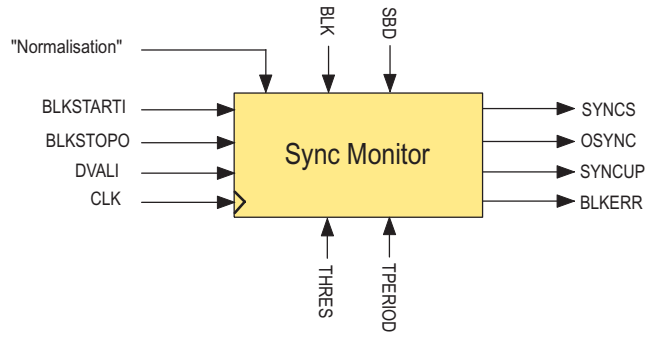

Figure 21: Sync Monitor

Figure 21 conceptually illustrates the Sync Monitor circuitry used to phase lock 'out-of-sync' states. When both BLK and SBD signals are high, the Sync Monitor circuitry operates in a burst mode fashion. This provides a mechanism to flag BLKERR as well as resetting BLKERR at the end of an output decoded Viterbi/TCM data stream, on BLKSTOPO. Figure 22 graphically demonstrates both 'in-sync' and 'out-of-sync' conditions.

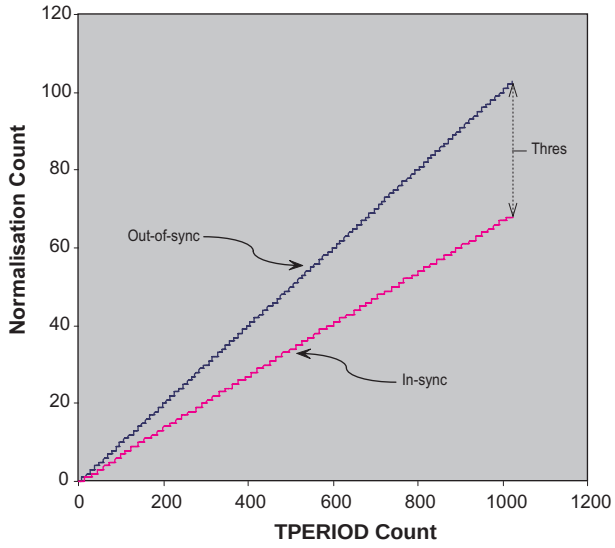

Figure 22: Sync Monitor Operation

The y-axis describes the accumulated 'Normalization' count value and the x-axis defines count period for this measurement (TPERIOD). If THRES signal is set somewhere between a worst case and best case the 'Normalization' value at 'time' TPERIOD (which is incremented on DVALI signal) then an 'out'-of-sync' case be easily discerned. It should be noted that the value of THRES depends upon noise on the received data and thus a THRES searching technique should be employed to establish a phase lock. This would involve the step-by-step reduction of an initially high THRES value (over time) until a lock is established and the core correctly decodes data. Such values are determined experimentally. Figures 23 through 26 show the waveform operation of the Sync Monitor circuitry. Figure 23 and Figure 24 demonstrate the core configured to provide phase synchronisation information that is burst dependent.

This mode of operation is defined as follows: BLK = 1, and SBD = 1; internal TPERIOD/Normalization count values are reset on BLKSTARTI; BLKERR is reset on BLKSTOPO. This mode of operation is useful in cases where input symbol data arrive from multiple demodulator sources. In this case it is possible that each demodulator may have established a separate and independent phase lock. Figure 25 and Figure 26 demonstrate the core configured to provide continuous phase synchronisation information regardless of BLK (BLK=0/1; SBD = 0).

In this case BLKERR is never asserted and BLKSTARTI/ BLKSTOPO has no effect on TPERIOD/Normalization values. Note SBD signal should never be asserted when BLK = 0 as this will activate the ERR flag of the CORE STATUS register in the microprocessor interface.

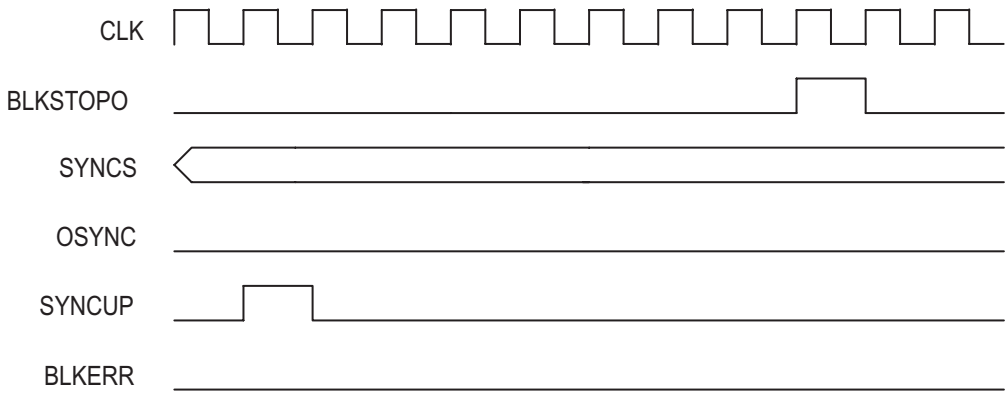

Figure 23: 'In Sync' Burst Dependent Phase Lock Monitoring

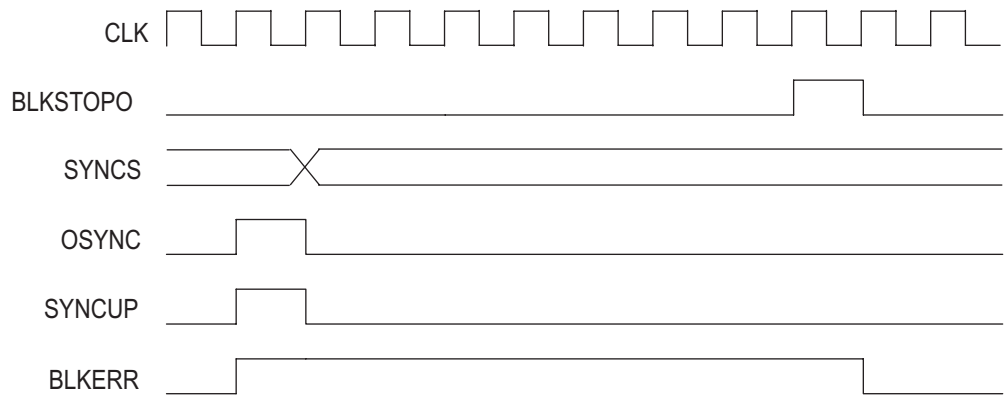

Figure 24: 'Out-of-Sync' Burst Dependent Phase Lock Monitoring

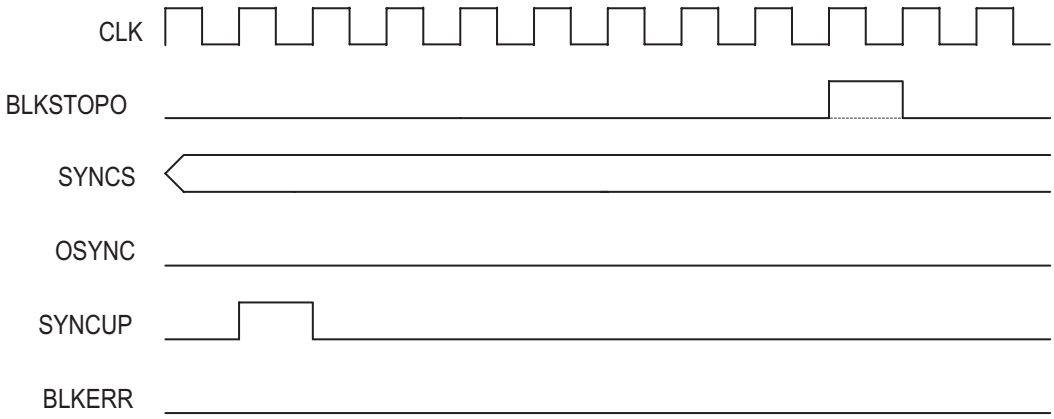

Figure 25: 'In-sync' Burst Independent Phase Lock Monitoring

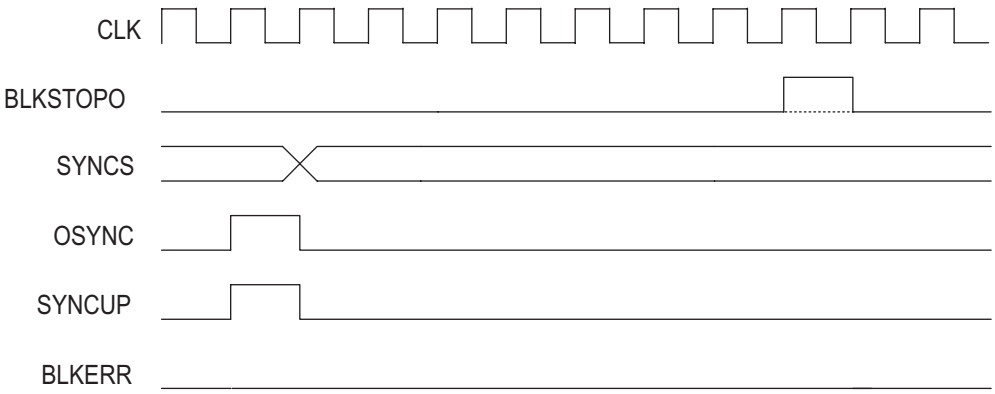

Figure 26: 'Out-of-'sync' Burst Independent Phase Lock Monitoring

BER Estimation

BER, a microprocessor register value, contains an estimation of the communications channel bit error rate in Viterbi mode only. A BER monitor is employed to provide this value at an interval defined by BPERIOD. Figure 27 describes the BER Monitor circuitry.

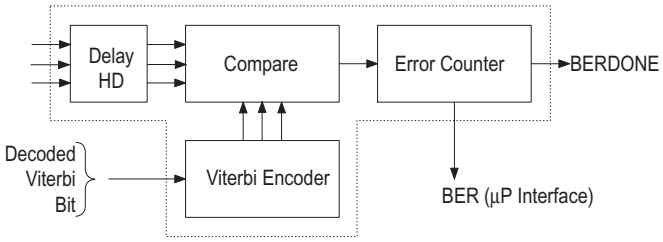

Figure 27: BER Monitor

Input hard decisions bits (MSB's of R0/R1/R2) are delayed by the latency of the Viterbi decoder core to coincide with the re-encoded decoded Viterbi bit. A mismatch in these values indicates a channel bit error. This bit error is counted over a period defined by the microprocessor register BPERIOD. This value is accumulated during the active state of a BPERIOD counter that is incremented on every CLK cycle during DVALO signal. Once the BPERIOD counter has reached the BPERIOD value, the accumulated bit error value is made available to the microprocessor interface. The BERDONE flag indicates that BER has been updated as shown in Figure 28.

It should be noted that the BPERIOD counter is a modulo type that is free running during all active DVALO intervals and is not reset between bursts. The minimum count value is 1024 cycles with BPERIOD = 0, i.e. count period = (BPERIOD+1)*1024 cycles during DVALO. The maximum count value available from the 16-bit BPERIOD register is 67.1E6 cycles. The BER of the channel is simply the number of accumulated error mismatches divided by the time period defined by BPERIOD and CLK. This value should be determined/calibrated externally as the BER register only contains the accumulated error count value for that period. It should be noted that the BER of the communications channel approximately equals the BER of the complete system since the probability of the decoder incorrectly decoding a bit is at least two orders of magnitude below the probability of a channel bit error.

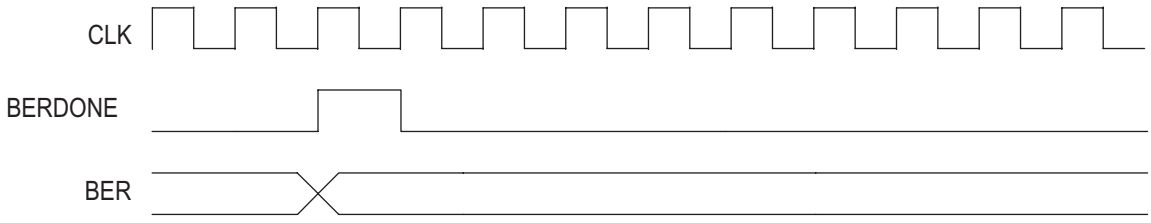

Figure 28: BER Register Update

AVAILABILITY AND IMPLEMENTATION INFORMATION

ASIC CORES

For applications that require the high performance, low cost and high integration of an ASIC, Amphion delivers the ASIC Core series of multimedia ASVCs that are pre-optimized to a targeted silicon technology by Amphion experts. Choose from off-the-shelf versions of the CS3410 available for many popular ASIC and foundry silicon supplier technologies or Amphion can port the CS3410 to a technology of your choice.

Table 8: CS3410 ASIC Cores

PRODUCT ID	SILICON VENDOR	PROCESS TECHNOLOGY	PERFORMANCE* (MSAMPLES/SEC)	LOGIC GATES**	MEMORY AREA	AVAILABILITY
CS3410TK	TSMC	180 nm using Artisan standard cell libraries	100	69k	203k gates equivalent	NOW

*Performance figures based on silicon vendor design kit information. ASIC design is pre-layout using vendor-provided statistical wire loading information, under the following condition: (T_J = 125^{o}C, V_{CC} -10%)

**Logic gates do not include clock circuitry

Consult your local Amphion representative for product specific performance information, current availability of individual products, and lead times on ASIC core porting.

PROGRAMMABLE LOGIC CORES

For ASIC prototyping or for projects requiring the fast time-to-market of a programmable logic solution, Amphion's programmable logic core solutions offer the silicon-aware performance tuning found in all Amphion products, combined with the rapid design times offered by today's leading programmable logic solution.

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Table 9: CS3410 Programmable Logic Cores

PRODUCT ID	SILICON VENDOR	PROGRAMMABLE LOGIC PRODUCT	PERFORMANCE* (MSAMPLES/SEC)	DEVICE RESOURCES USED (LOGIC)	DEVICE RESOURCES USED (MEMORY)	AVAILABILITY
CS3410AA	Altera	Apex 20KE	40	11090 LEs	41984 ESB bits	NOW
CS3410XE	Xilinx	Virtex-E	40	4192 Slices	11 block RAMs	NOW

*Performance represents core only under worst case commercial condition. Does not include timing effect of external logic and I/O circuitry.

ABOUT AMPHION

Amphion (formerly Integrated Silicon Systems) is the leading supplier of speech coding, video/image processing and channel coding ASVCs for system-on-a-chip (SoC) solutions in the telecommunications/Internet, consumer / communications and wireless markets.

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