N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FET

FEATURES

- Lateral D-MOS Design
- Low ON Resistance — 1.1 ohms (typ)
- Extremely Low Drive Current
- Linear Transfer Characteristic

APPLICATIONS

- Broadband, High-Gain, RF Power Amplifiers
- Ultra High-Speed Logic Compatible Switches
- High-Speed Line Drivers
- Power Switches

ABSOULTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DS}	Drain-Source Voltage	+30V
V_{GS}	Gate-Source Voltage	±20V
V_{GD}	Gate-Drain Voltage	+20V −30V
$I_{D(on)}$	Continuous Drain Current (Note 1, Note 3)	2.0A
$I_{D(on)}$	Peak Drain Current (Note 1, Note 3)	3.0A
P_D	Continuous Power Dissipation (Note 1)	
	T_A = +25°C (Note 2)	1.0W
	T_C = +25°C (Note 3)	6.25W
	Power Derating Factors (Note 1)	
	Free Air	10mW/°C
	Infinite Heat Sink	62.5mW/°C
	Thermal Resistance (Note 1)	
θ_{ja}	Junction to Ambient	100°C/W
θ_{jc}	Junction to Case	16°C/W
T_{op}	Operating Junction Temperature Range	−55 to +125°C
T_{stg}	Storage Temperature Range	−55 to +150°C

Note 1: Not applicable to chips. Final value depends upon mounting.

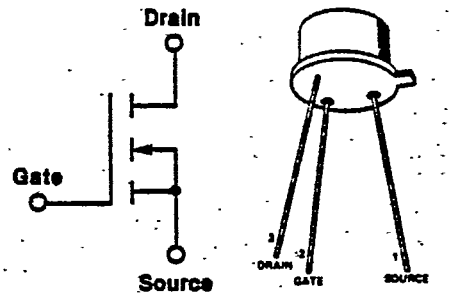
Note 2: Free Air

Note 3: Infinite Heat Sink

ORDERING INFORMATION

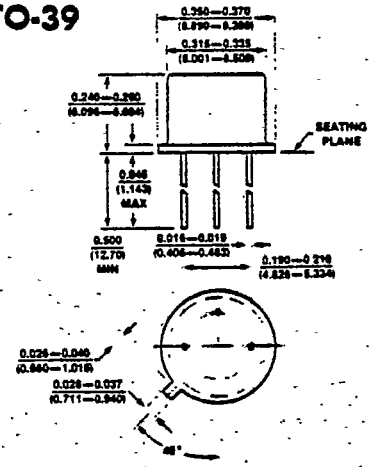
Sorted Chips in Carriers	XSD226
TO-39 Package	SD226H

SCHEMATIC DIAGRAM



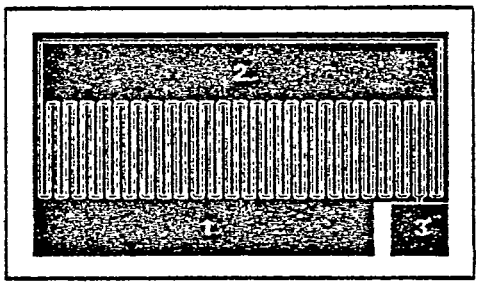
Body Internally connected to Source.

PACKAGE DIMENSIONS TO-39



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



PAD NO.	FUNCTION
1	SOURCE
2	DRAIN
3	GATE

Dimensions: .091 x .055 x .010 inches

2146 F-13

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC	SD226 MIN	SD226 TYP	SD226 MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	30	35		V	I_D = 1.0μA, V_{GS} = 0	
2	STATIC	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.1	1.0	2.3	V	I_D = 10μA	V_{DS} = V_{GS}
3	STATIC	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.5	1.5	3.0	V	I_D = 1.0mA	V_{DS} = V_{GS}
4	STATIC	I_{GSS} Gate Reverse Leakage Current			±1.0	nA	V_{GS} = 20V, V_{DS} = 0	
5	STATIC	I_{DSS} Drain-Source OFF Leakage Current		0.1	1.0	μA	V_{DS} = 30V, V_{GS} = 0	
6	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance		1.4	2.0	ohms	V_{GS} = 5V	I_D = 50mA (Note 4)
7	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance		1.1	1.5	ohms	V_{GS} = 10V	I_D = 50mA (Note 4)
8	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance		1.1	1.5	ohms	V_{GS} = 10V	I_D = 500mA (Note 4)
9	STATIC	$I_{D(on)}$ Drain-Source ON Current	1.4	2.0		A	V_{DS} = 2.2V	V_{GS} = 10V (Note 4)
10	STATIC	$I_{D(on)}$ Drain-Source ON Current	2.2	3.0		A	V_{DS} = 3.3V	V_{GS} = 10V (Note 4)
11	DYNAMIC	g_{fs} Common-Source Forward Transconductance	700	750		mmhos	V_{DS} = 15V, I_D = 2.0A f = 1KHz (Note 4)	
12	DYNAMIC	C_{iss} Common-Source Input Capacitance		35	45	pF	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	
13	DYNAMIC	C_{rss} Common-Source Reverse Transfer Capacitance		5.0	6.0	pF	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	
14	DYNAMIC	C_{oss} Common-Source Output Capacitance		20	25	pF	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	
15	DYNAMIC	$t_{d(on)}$ Turn-On Delay Time		1.0	2.0	nSec	V_{DD} = 25V, R_L = 25 ohm R_G = 51 ohm V_{IN} = 5V	
16	DYNAMIC	t_r Rise Time		1.0	3.0	nSec	V_{DD} = 25V, R_L = 25 ohm R_G = 51 ohm V_{IN} = 5V	
17	DYNAMIC	t_f Fall Time		3.0	5.0	nSec	V_{DD} = 25V, R_L = 25 ohm R_G = 51 ohm V_{IN} = 5V	

Note 4: Pulse Test 80μSec, 1% Duty Cycle