LINEAR SYSTEMS

Linear Integrated Systems

SD210DE/214DE

N-CHANNEL LATERAL DMOS SWITCH

Product Summary

Part Number	$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD210DE	30	1.5	45 @ V_{GS} = 10 V	0.5	2
SD214DE	20	1.5	45 @ V_{GS} = 10 V	0.5	2

Features

- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @5 V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

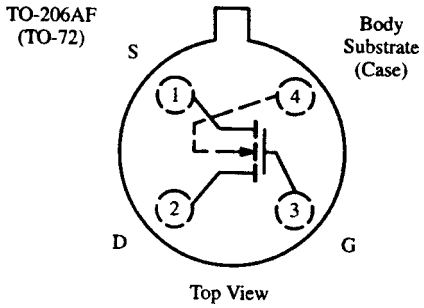
Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

Description

The SD210DE/214DE are enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video, and high-frequency applications. The SD214DE is normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. These MOSFETs do not have a gate protection Zener diode which results in lower gate leakage and ± voltage capability from gate to substrate. A poly-silicon gate is featured for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, and Zener protected—SD211DE/SST211 series.



Top View

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage		± 40 V
Gate-Substrate Voltage		± 30 V
Drain-Source Voltage	(SD210DE)	30 V
	(SD214DE)	20 V
Source-Drain Voltage	(SD210DE)	10 V
	(SD214DE)	20 V
Drain-Substrate Voltage	(SD210DE)	30 V
	(SD214DE)	25 V
Source-Substrate Voltage	(SD210DE)	15 V
	(SD214DE)	25 V
Drain Current		50 mA
Lead Temperature (1/16" from case for 10 seconds)		300°C
Storage Temperature		-65 to 150°C
Operating Junction Temperature		-55 to 125°C
Power Dissipation[a]		300 mW

Notes:
a. Derate 3 mW/°C above 25°C

Specifications[a]

Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits SD210DE Min	Limits SD210DE Max	Limits SD214DE Min	Limits SD214DE Max	Unit
Static									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10$ µA		35	30				V
		$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DBO}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source Open		35	15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SBO}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain Open		35	15		25		
Drain-Source Leakage	$I_{DS(off)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10			nA
			$V_{DS} = 20$ V	0.9				10	
Source-Drain Leakage	$I_{SD(off)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10			
			$V_{SD} = 20$ V	0.8				10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = \pm 40$ V		0.001		0.1		0.1	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1$ µA, $V_{SB} = 0$ V		0.8	0.5	1.5	0.1	1.5	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58		70		70	Ω
			$V_{GS} = 10$ V	38		45		45	
			$V_{GS} = 15$ V	30					
			$V_{GS} = 20$ V	26					
			$V_{GS} = 25$ V	24					
Dynamic									
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, f = 1 kHz		11	10		10		mS
	g_{os}			0.9					
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, f = 1 MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5	
Switching									
Turn-On Time	$t_{d(on)}$	$V_{SB} = 0$ V, V_{IN} 0 to 5 V, $R_G = 25$ Ω, $V_{DD} = 5$ V, $R_L = 680$ Ω		0.5		1		1	ns
	t_r			0.6		1		1	
Turn-Off Time	$t_{d(off)}$			2					
	t_f			6					

Notes:
a. $T_A = 25^0$C unless otherwise noted.
b. B is the body (substrate) and $V_{(BR)}$ is breakdown.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.