



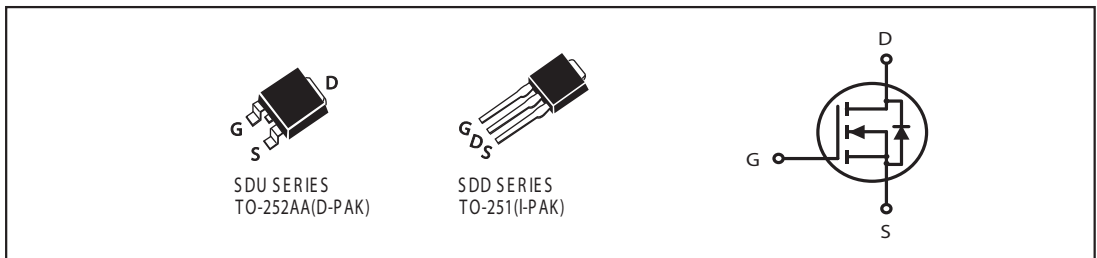
# SDU/D40N03L

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> ( mΩ ) TYP
30V	40A	9 @ V <sub>GS</sub> = 10V
		13 @ V <sub>GS</sub> = 4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- TO-252 and TO-251 Package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous @ T <sub>J</sub> =125°C -Pulsed <sup>a</sup>	I <sub>D</sub>	40	A
	I <sub>DM</sub>	120	A
Drain-Source Diode Forward Current	I <sub>S</sub>	40	A
Maximum Power Dissipation @ T <sub>C</sub> =25°C Derate above 25°C	P <sub>D</sub>	50	W
		0.3	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 175	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	3	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	50	°C/W

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ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V			10	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS <sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA	1	1.5	3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A		9	10	m ohm
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A		13	16	m ohm
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	40			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 20A		30		S
<b>DYNAMIC CHARACTERISTICS <sup>b</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 0V f = 1.0MHz		1375		pF
Output Capacitance	C <sub>OSS</sub>			670		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			200		pF
<b>SWITCHING CHARACTERISTICS <sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 15V, I <sub>D</sub> = 1A, V <sub>GS</sub> = 10V, R <sub>GEN</sub> = 6 ohm		30		ns
Rise Time	t <sub>r</sub>			32		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			132		ns
Fall time	t <sub>f</sub>			30		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 40A, V <sub>GS</sub> = 10V		40	50	nC
		V <sub>DS</sub> = 10V, I <sub>D</sub> = 40A, V <sub>GS</sub> = 4.5V		19.5	23.5	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 40A, V <sub>GS</sub> = 10V		8.2		nC
Gate-Drain Charge	Q <sub>gd</sub>			5.3		nC

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## ELECTRICAL CHARACTERISTICS ( $T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS <sup>a</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0\text{V}, I_s = 25\text{A}$			1.3	V

### Notes

- a. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

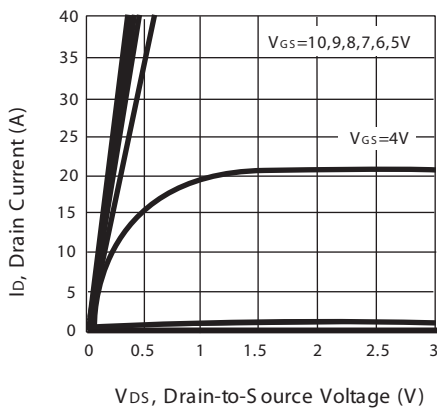


Figure 1. Output Characteristics

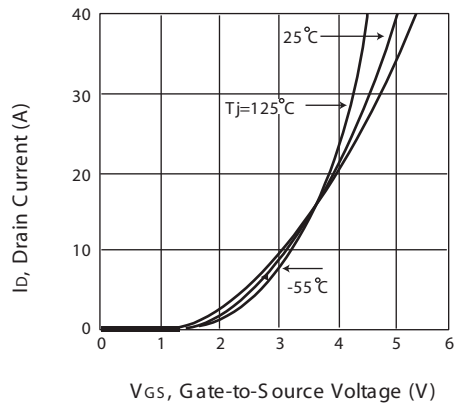


Figure 2. Transfer Characteristics

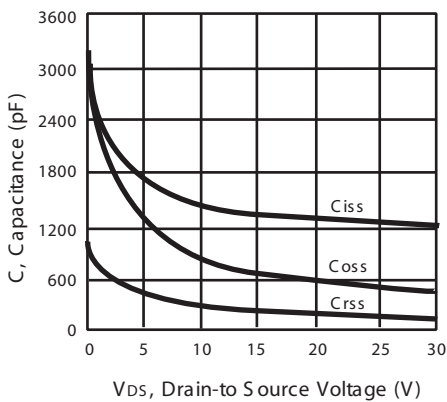


Figure 3. Capacitance

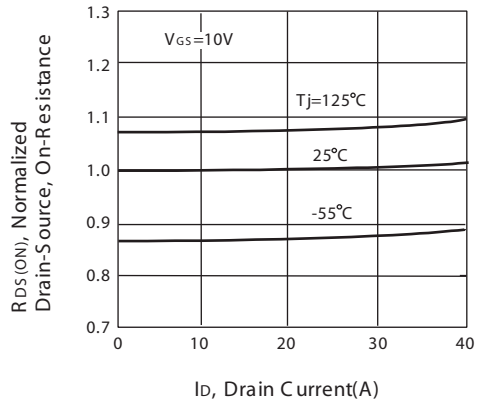


Figure 4. On-Resistance Variation with Drain Current and Temperature

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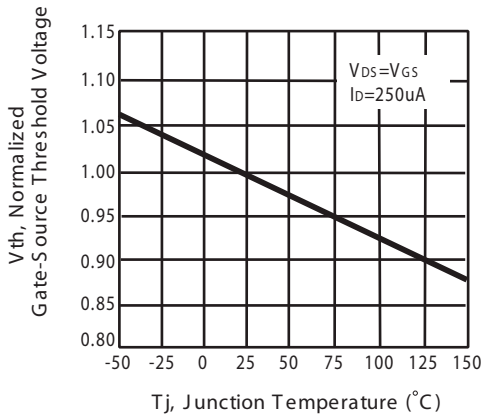


Figure 5. Gate Threshold Variation with Temperature

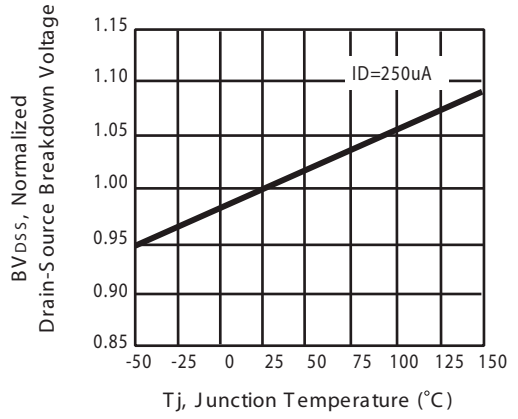


Figure 6. Breakdown Voltage Variation with Temperature

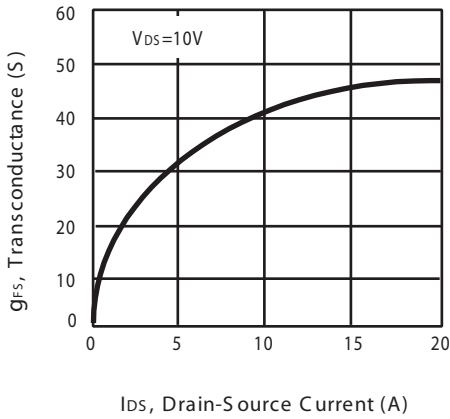


Figure 7. Transconductance Variation with Drain Current

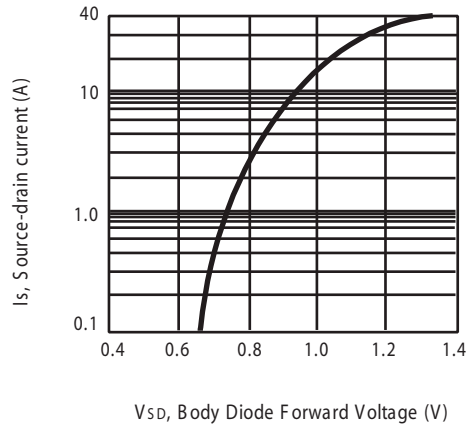


Figure 8. Body Diode Forward Voltage Variation with Source Current

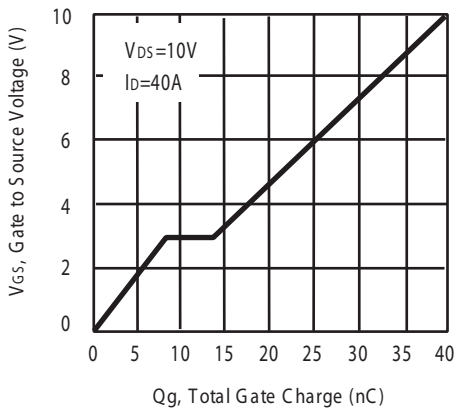


Figure 9. Gate Charge

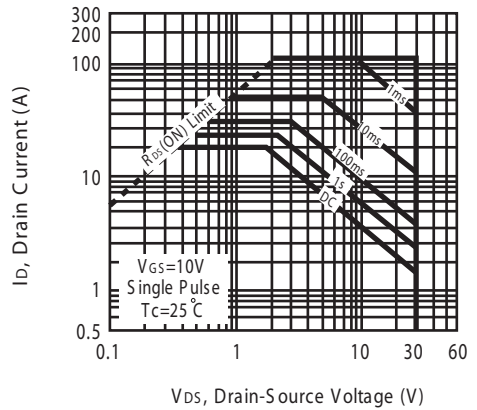


Figure 10. Maximum Safe Operating Area

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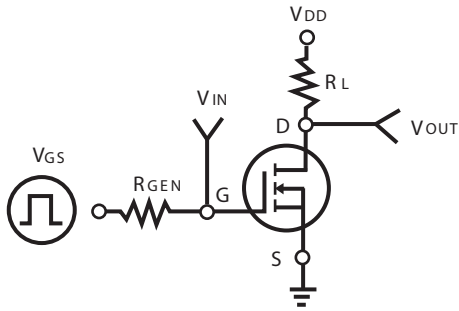


Figure 11. Switching Test Circuit

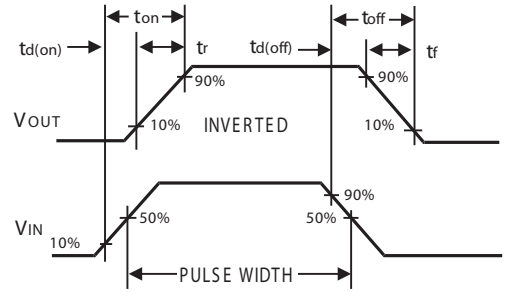


Figure 12. Switching Waveforms

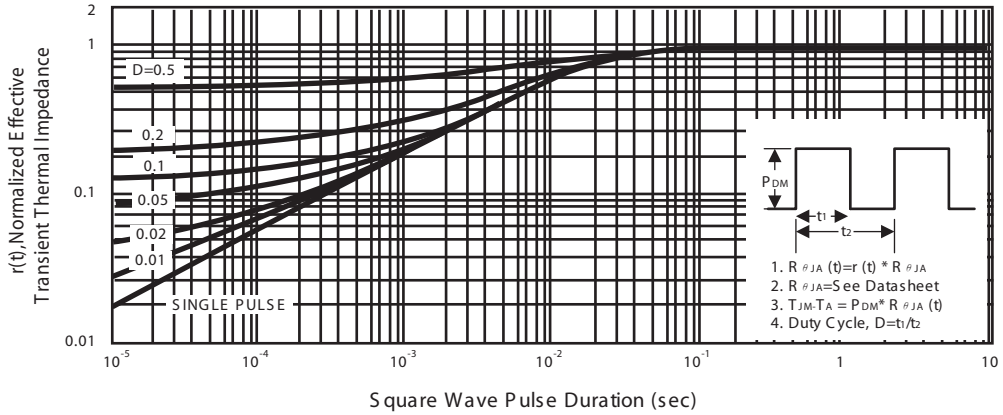


Figure 13. Normalized Thermal Transient Impedance Curve