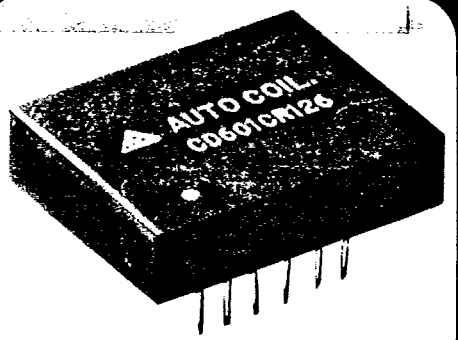
CD601CR Series
TTL Digital Delay Module, 14 PIN, 10 TAP

T-47-13

- TTL input and outputs
- Precise and stable delays
- Reliable hybrid construction
- No external components required
- Fan out 10TTL loads/tap, 20TTL loads/package
- Operating temperature 0° to 70°C
- Storage temperature –55° to +125°C



Electrical Characteristics:

VIH	(High level input voltage)	2.0 to 5.0V
IIH	(High level input current)	50 μA Max.
VIL	(Low level input voltage)	0.8 V Max.
IIL	(Low level input current)	–2 ma Max.
VOH	(High level output voltage)	2.5 V Min.
VOL	(Low level output voltage)	0.5 V Max.
VCC	(Supply voltage)	5.0 V ± 0.25 V DC
ICC	(Supply current)	150 ma Max.

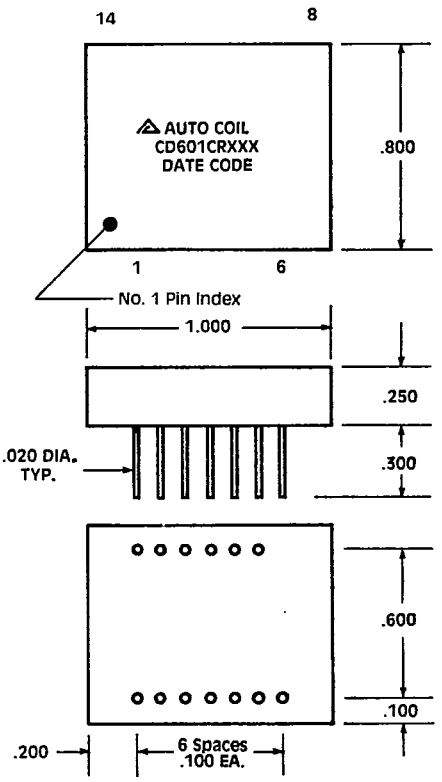
Mechanical Specifications:
Case: Epoxy filled D.A.P.
Leads: Tinned Cu. or equiv.
Marking: White epoxy ink

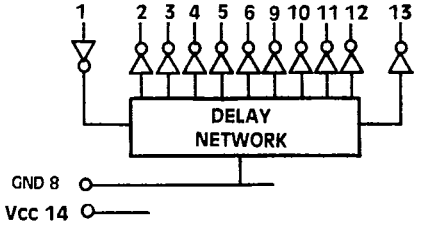
Also Available:
Intermediate delays
Non-symmetrical tap delays
Tighter delay tolerances
Falling edge delay specifications

Input & test conditions are not limiting parameters
All digital delay modules can be operated at conditions other than specified.
Since accuracies may be slightly affected, we suggest that the module be evaluated under specific operating conditions.

Specifications subject to change without notice.

Pin numbers for reference only





Automatic Coil Part Number	Total Delay (NS ± 5%)	Tap Intervals (NS ± 10% or ± 2NS Whichever is Greater)
CD601CR126	100	10
CD601CR127	150	15
CD601CR128	200	20
CD601CR129	250	25
CD601CR130	500	50
CD601CR131	1000	100

Output rise times (TPLH) 2 NS max.(.8 to 2.0 V level).

Test Conditions:
1) All measurements are made @ 25°C
2) VCC is maintained @ 5.0 VDC
3) All measurements are made with no loads on outputs
4) Delays are measures @ 1.5V level
5) Delays & tolerances for leading edges only (TPLH)-falling edges (TPHL) closely matched to TPLH

Input Conditions:
1) Pulse amplitude: 3.20V
2) Input rise time: 3.0 NS (10 to 90%)
3) Pulse width: 2 x total delay
4) Duty cycle: < 25%

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