

# DS90CR285/DS90CR286

## +3.3V Rising Edge Data Strobe LVDS 28-Bit Channel Link-66 MHz

### General Description

The DS90CR285 transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR286 receiver converts the LVDS data streams back into 28 bits of LVCMOS/LVTTL data. At a transmit clock frequency of 66 MHz, 28 bits of TTL data are transmitted at a rate of 462 Mbps per LVDS data channel. Using a 66 MHz clock, the data throughput is 1.848 Gbit/s (231 Mbytes/s).

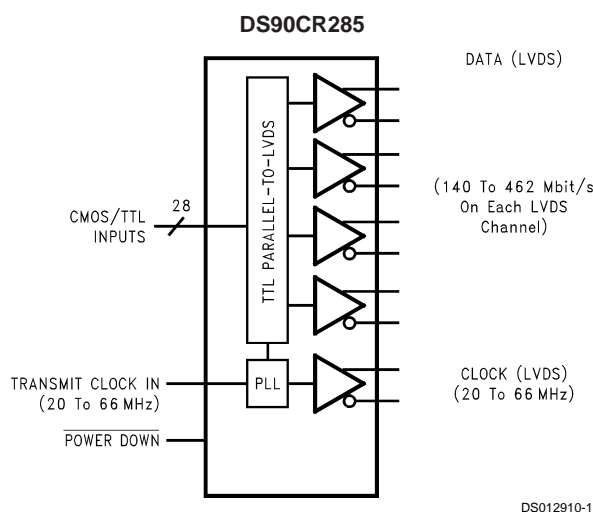
The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 28-bit wide data and one clock, up to 58 conductors are required. With the Channel Link chipset as few as 11 conductors (4 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides a 80% reduction in required cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

The 28 LVCMOS/LVTTL inputs can support a variety of signal combinations. For example, seven 4-bit nibbles or three 9-bit (byte + parity) and 1 control.

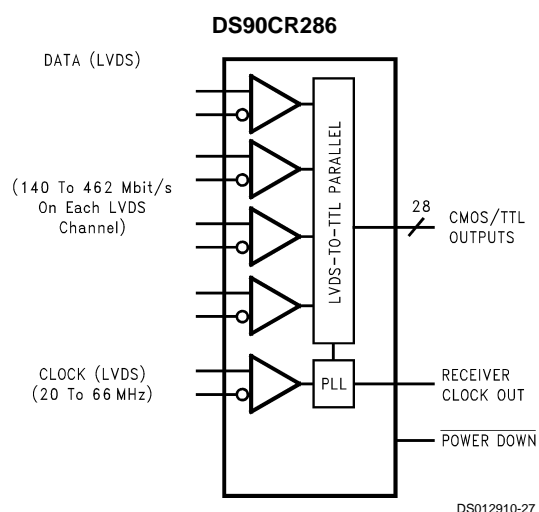
### Features

- Single +3.3V supply
- Chipset (Tx + Rx) power consumption <250 mW (typ)
- Power-down mode (<0.5 mW total)
- Up to 231 Megabytes/sec bandwidth
- Up to 1.848 Gbps data throughput
- Narrow bus reduces cable size
- 290 mV swing LVDS devices for low EMI
- +1V common mode range (around +1.2V)
- PLL requires no external components
- Both devices are offered in a Low profile 56-lead TSSOP package
- DS90CR285SLC is offered in a 64 ball, 0.8mm fine pitch ball grid array (FBGA) package for use with the DS90CR286ASLC
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- ESD Rating > 7 kV
- Operating Temperature: -40°C to +85°C

### Block Diagrams

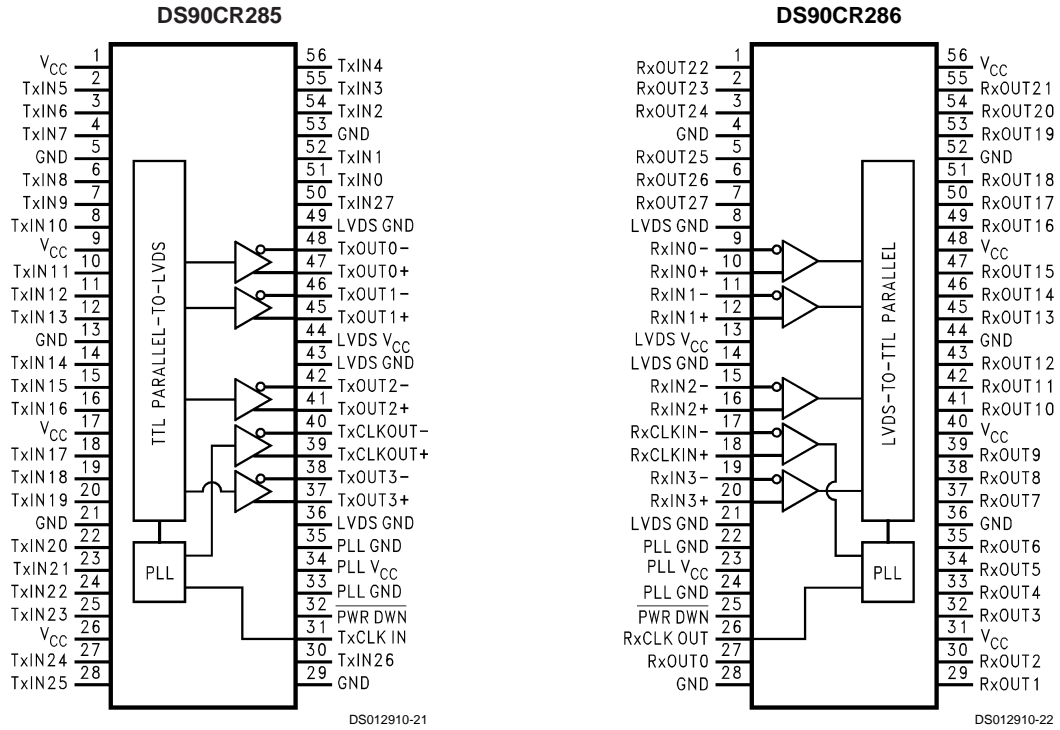


Order Number DS90CR285MTD or DS90CR285SLC  
See NS Package Number MTD56 or SLC64A

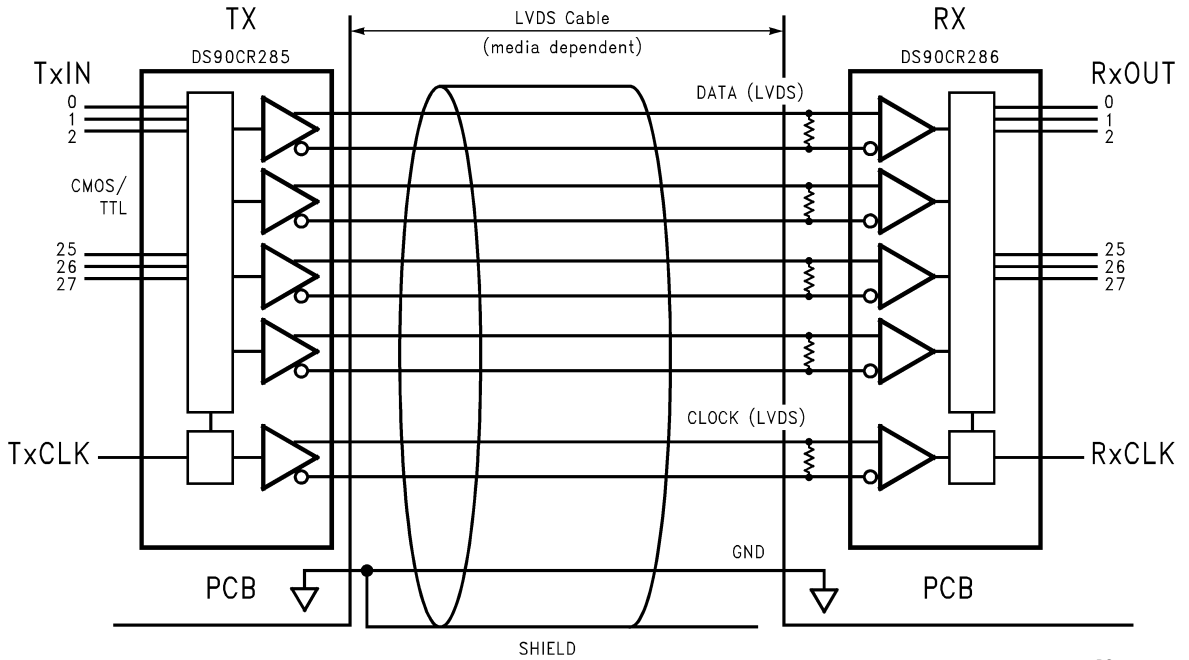


Order Number DS90CR286MTD  
See NS Package Number MTD56

## Pin Diagrams for TSSOP Packages



## Typical Application



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.3V to +4V
CMOS/TTL Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
CMOS/TTL Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Receiver Input Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Driver Output Voltage	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Output Short Circuit	
Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature	
(Soldering, 4 sec.)	+260°C
Solder Reflow Temperature	
(20 sec for FBGA)	+220°C

Maximum Package Power Dissipation @ +25°C

DS90CR285MTD	1.63 W
DS90CR285SLC	2.0 W
DS90CR286MTD	1.61 W

Package Derating:

DS90CR285MTD	12.5 mW/°C above +25°C
DS90CR285SLC	10.2 mW/°C above +25°C
DS90CR286MTD	12.4 mW/°C above +25°C

ESD Rating

(HBM, 1.5 k $\Omega$ , 100 pF)	> 7 kV
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## Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage ( $V_{CC}$ )	3.0	3.3	3.6	V
Operating Free Air Temperature ( $T_A$ )	-40	+25	+85	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage ( $V_{CC}$ )				100 mV <sub>PP</sub>

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LVCMOS/LVTTL DC SPECIFICATIONS</b>						
$V_{IH}$	High Level Input Voltage		2.0		$V_{CC}$	V
$V_{IL}$	Low Level Input Voltage		GND		0.8	V
$V_{OH}$	High Level Output Voltage	$I_{OH} = -0.4$ mA	2.7	3.3		V
$V_{OL}$	Low Level Output Voltage	$I_{OL} = 2$ mA		0.06	0.3	V
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18$ mA		-0.79	-1.5	V
$I_{IN}$	Input Current	$V_{IN} = V_{CC}$ , GND, 2.5V or 0.4V		$\pm 5.1$	$\pm 10$	$\mu$ A
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0V$		-60	-120	mA
<b>LVDS DRIVER DC SPECIFICATIONS</b>						
$V_{OD}$	Differential Output Voltage	$R_L = 100\Omega$	250	290	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between Complimentary Output States				35	mV
$V_{OS}$	Offset Voltage (Note 4)		1.125	1.25	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ between Complimentary Output States				35	mV
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0V$ , $R_L = 100\Omega$		-3.5	-5	mA
$I_{OZ}$	Output TRI-STATE® Current	$\overline{PWR\ DWN} = 0V$ , $V_{OUT} = 0V$ or $V_{CC}$		$\pm 1$	$\pm 10$	$\mu$ A
<b>LVDS RECEIVER DC SPECIFICATIONS</b>						
$V_{TH}$	Differential Input High Threshold	$V_{CM} = +1.2V$			+100	mV
$V_{TL}$	Differential Input Low Threshold		-100			mV
$I_{IN}$	Input Current	$V_{IN} = +2.4V$ , $V_{CC} = 3.6V$			$\pm 10$	$\mu$ A
		$V_{IN} = 0V$ , $V_{CC} = 3.6V$			$\pm 10$	$\mu$ A

## Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>TRANSMITTER SUPPLY CURRENT</b>							
$I_{CCTW}$	Transmitter Supply Current Worst Case (with Loads)	$R_L = 100\Omega$ , $C_L = 5\text{ pF}$ , Worst Case Pattern (Figures 1, 2), $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$	$f = 32.5\text{ MHz}$		31	45	mA
			$f = 37.5\text{ MHz}$		32	50	mA
			$f = 66\text{ MHz}$		37	55	mA
		$R_L = 100\Omega$ , $C_L = 5\text{ pF}$ , Worst Case Pattern (Figures 1, 2), $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$f = 40\text{ MHz}$		38	51	mA
			$f = 66\text{ MHz}$		42	55	mA
$I_{CCTZ}$	Transmitter Supply Current Power Down	$\overline{\text{PWR DWN}} = \text{Low}$ Driver Outputs in TRI-STATE under Powerdown Mode		10	55	$\mu\text{A}$	
<b>RECEIVER SUPPLY CURRENT</b>							
$I_{CCRW}$	Receiver Supply Current Worst Case	$C_L = 8\text{ pF}$ , Worst Case Pattern (Figures 1, 3), $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$	$f = 32.5\text{ MHz}$		49	65	mA
			$f = 37.5\text{ MHz}$		53	70	mA
			$f = 66\text{ MHz}$		78	105	mA
		$C_L = 8\text{ pF}$ , Worst Case Pattern (Figures 1, 3), $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$f = 40\text{ MHz}$		55	82	mA
			$f = 66\text{ MHz}$		78	105	mA
$I_{CCRZ}$	Receiver Supply Current Power Down	$\overline{\text{PWR DWN}} = \text{Low}$ Receiver Outputs Stay Low during Powerdown Mode		10	55	$\mu\text{A}$	

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

**Note 2:** Typical values are given for  $V_{CC} = 3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ .

**Note 3:** Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except  $V_{OD}$  and  $\Delta V_{OD}$ ).

**Note 4:**  $V_{OS}$  previously referred as  $V_{CM}$ .

## Transmitter Switching Characteristics

Over recommended operating supply and  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	
LLHT	LVDS Low-to-High Transition Time (Figure 2)		0.5	1.5	ns	
LHLT	LVDS High-to-Low Transition Time (Figure 2)		0.5	1.5	ns	
TCIT	TxCLK IN Transition Time (Figure 4)			5	ns	
TCCS	TxOUT Channel-to-Channel Skew (Figure 5)		250		ps	
TPPos0	Transmitter Output Pulse Position for Bit0 (Note 7) (Figure 16)	$f = 40\text{ MHz}$	-0.4	0	0.4	ns
TPPos1	Transmitter Output Pulse Position for Bit1		3.1	3.3	4.0	ns
TPPos2	Transmitter Output Pulse Position for Bit2		6.5	6.8	7.6	ns

## Transmitter Switching Characteristics (Continued)

Over recommended operating supply and  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	
TPPos3	Transmitter Output Pulse Position for Bit3	10.2	10.4	11.0	ns	
TPPos4	Transmitter Output Pulse Position for Bit4	13.7	13.9	14.6	ns	
TPPos5	Transmitter Output Pulse Position for Bit5	17.3	17.6	18.2	ns	
TPPos6	Transmitter Output Pulse Position for Bit6	21.0	21.2	21.8	ns	
TPPos0	Transmitter Output Pulse Position for Bit0 (Note 6) (Figure 16)	f = 66 MHz	-0.4	0	0.3	ns
TPPos1	Transmitter Output Pulse Position for Bit1		1.8	2.2	2.5	ns
TPPos2	Transmitter Output Pulse Position for Bit2		4.0	4.4	4.7	ns
TPPos3	Transmitter Output Pulse Position for Bit3		6.2	6.6	6.9	ns
TPPos4	Transmitter Output Pulse Position for Bit4		8.4	8.8	9.1	ns
TPPos5	Transmitter Output Pulse Position for Bit5		10.6	11.0	11.3	ns
TPPos6	Transmitter Output Pulse Position for Bit6		12.8	13.2	13.5	ns
TCIP	TxCLK IN Period (Figure 6)	15	T	50	ns	
TCIH	TxCLK IN High Time (Figure 6)	0.35T	0.5T	0.65T	ns	
TCIL	TxCLK IN Low Time (Figure 6)	0.35T	0.5T	0.65T	ns	
TSTC	TxIN Setup to TxCLK IN (Figure 6)	2.5			ns	
THTC	TxIN Hold to TxCLK IN (Figure 6)	0			ns	
TCCD	TxCLK IN to TxCLK OUT Delay @ $25^{\circ}\text{C}$ , $V_{\text{CC}}=3.3\text{V}$ (Figure 8)	3	3.7	5.5	ns	
TPLLS	Transmitter Phase Lock Loop Set (Figure 10)			10	ms	
TPDD	Transmitter Powerdown Delay (Figure 14)			100	ns	

## Receiver Switching Characteristics

Over recommended operating supply and  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 3)		2.2	5.0	ns	
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 3)		2.2	5.0	ns	
RSPos0	Receiver Input Strobe Position for Bit 0 (Note 7)(Figure 17)	f = 40 MHz	1.0	1.4	2.15	ns
RSPos1	Receiver Input Strobe Position for Bit 1		4.5	5.0	5.8	ns
RSPos2	Receiver Input Strobe Position for Bit 2		8.1	8.5	9.15	ns
RSPos3	Receiver Input Strobe Position for Bit 3		11.6	11.9	12.6	ns
RSPos4	Receiver Input Strobe Position for Bit 4		15.1	15.6	16.3	ns
RSPos5	Receiver Input Strobe Position for Bit 5		18.8	19.2	19.9	ns
RSPos6	Receiver Input Strobe Position for Bit 6		22.5	22.9	23.6	ns

## Receiver Switching Characteristics (Continued)

Over recommended operating supply and  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
RSPos0	Receiver Input Strobe Position for Bit 0 (Note 6)(Figure 17)	f = 66 MHz	0.7	1.1	1.4	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.9	3.3	3.6	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.1	5.5	5.8	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.3	7.7	8.0	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.5	9.9	10.2	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.7	12.1	12.4	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.9	14.3	14.6	ns
RSKM	RxIN Skew Margin (Note 5) (Figure 18)	f = 40 MHz	490			ps
		f = 66 MHz	400			ps
RCOP	RxCLK OUT Period (Figure 7)		15	T	50	ns
RCOH	RxCLK OUT High Time (Figure 7)	f = 40 MHz	6.0	10.0		ns
		f = 66 MHz	4.0	6.1		ns
RCOL	RxCLK OUT Low Time (Figure 7)	f = 40 MHz	10.0	13.0		ns
		f = 66 MHz	6.0	7.8		ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 7)	f = 40 MHz	6.5	14.0		ns
		f = 66 MHz	2.5	8.0		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 7)	f = 40 MHz	6.0	8.0		ns
		f = 66 MHz	2.5	4.0		ns
RCCD	RxCLK IN to RxCLK OUT Delay (Figure 9)	f = 40 MHz	4.0	6.7	8.0	ns
		f = 66 MHz	5.0	6.6	9.0	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 11)				10	ms
RPDD	Receiver Powerdown Delay (Figure 15)				1	$\mu\text{s}$

**Note 5:** Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window). This margin allows LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter less than 250 ps).

**Note 6:** The min. and max. limits are based on the worst bit by applying a  $-400\text{ps}/+300\text{ps}$  shift from ideal position.

**Note 7:** The min. and max. are based on the actual bit position of each of the 7 bits within the LVDS data stream across PVT.

## AC Timing Diagrams

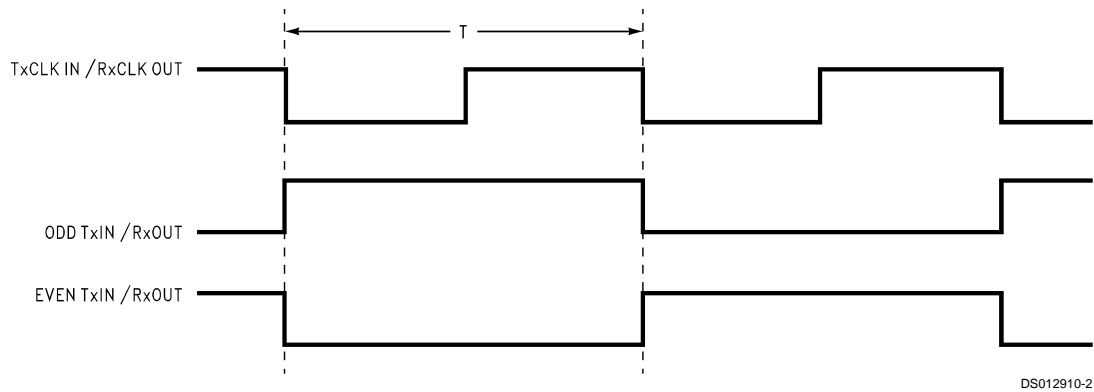


FIGURE 1. "Worst Case" Test Pattern

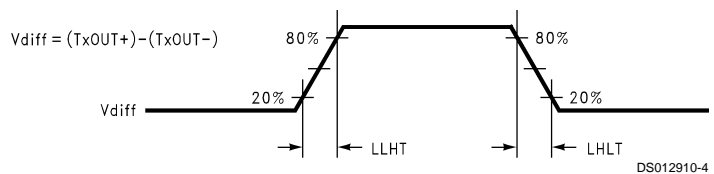
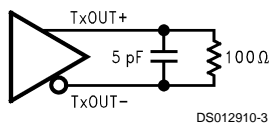


FIGURE 2. DS90CR285 (Transmitter) LVDS Output Load and Transition Times

AC Timing Diagrams (Continued)

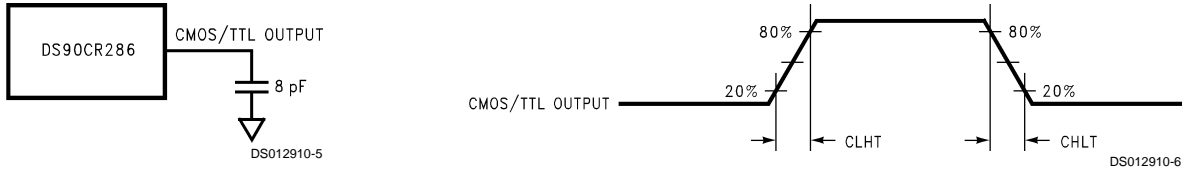


FIGURE 3. DS90CR286 (Receiver) CMOS/TTL Output Load and Transition Times

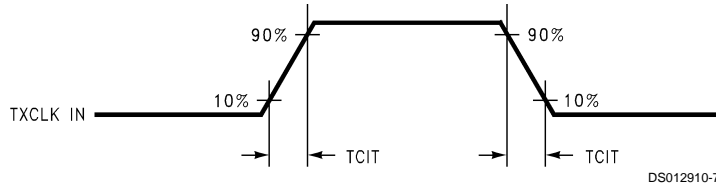
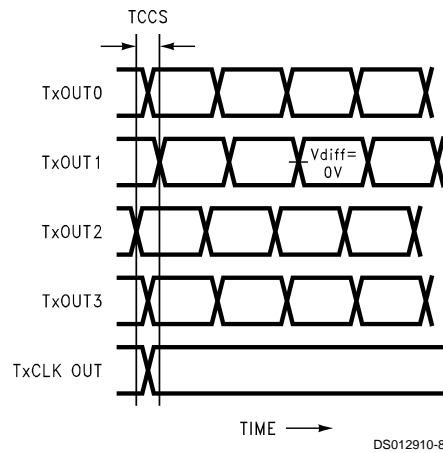


FIGURE 4. DS90CR285 (Transmitter) Input Clock Transition Time



Note 8: Measurements at  $V_{DIFF} = 0V$

Note 9: TCCS measured between earliest and latest LVDS edges.

Note 10: TxCLK Differential Low→High Edge

FIGURE 5. DS90CR285 (Transmitter) Channel-to-Channel Skew

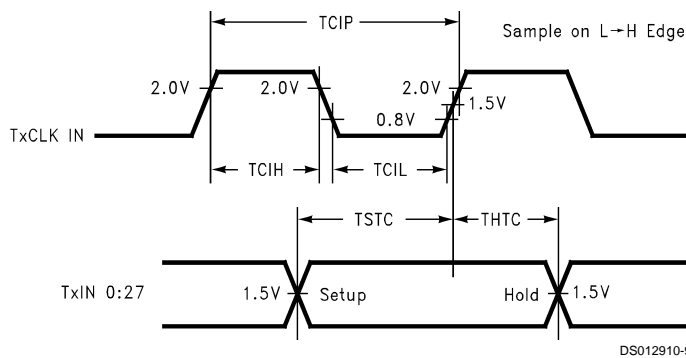


FIGURE 6. DS90CR285 (Transmitter) Setup/Hold and High/Low Times

AC Timing Diagrams (Continued)

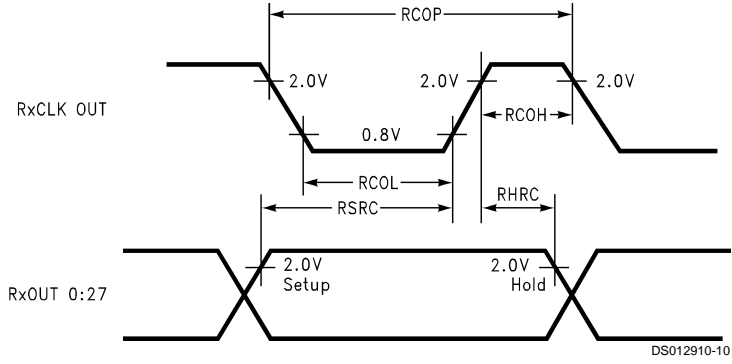


FIGURE 7. DS90CR286 (Receiver) Setup/Hold and High/Low Times

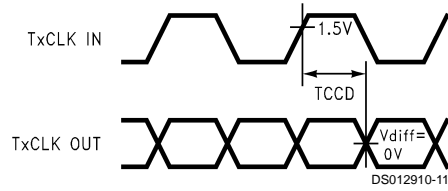


FIGURE 8. DS90CR285 (Transmitter) Clock In to Clock Out Delay

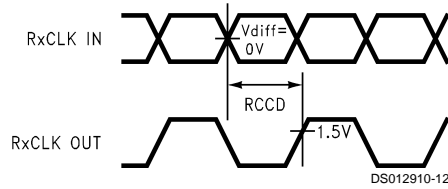


FIGURE 9. DS90CR286 (Receiver) Clock In to Clock Out Delay

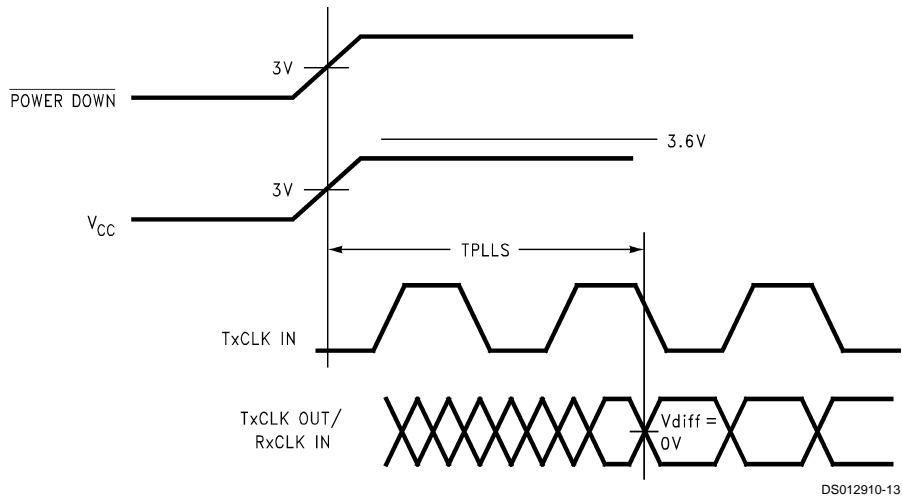


FIGURE 10. DS90CR285 (Transmitter) Phase Lock Loop Set Time



AC Timing Diagrams (Continued)

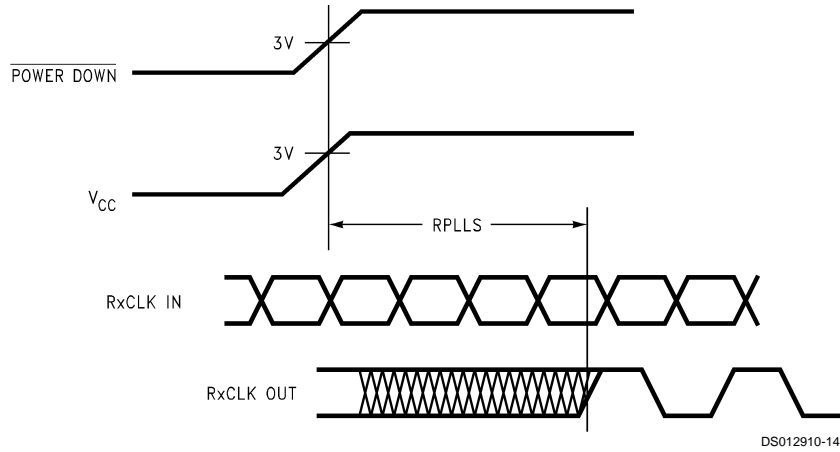


FIGURE 11. DS90CR286 (Receiver) Phase Lock Loop Set Time

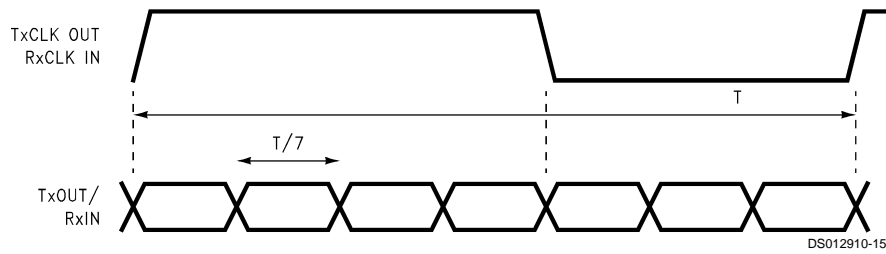


FIGURE 12. Seven Bits of LVDS in Once Clock Cycle

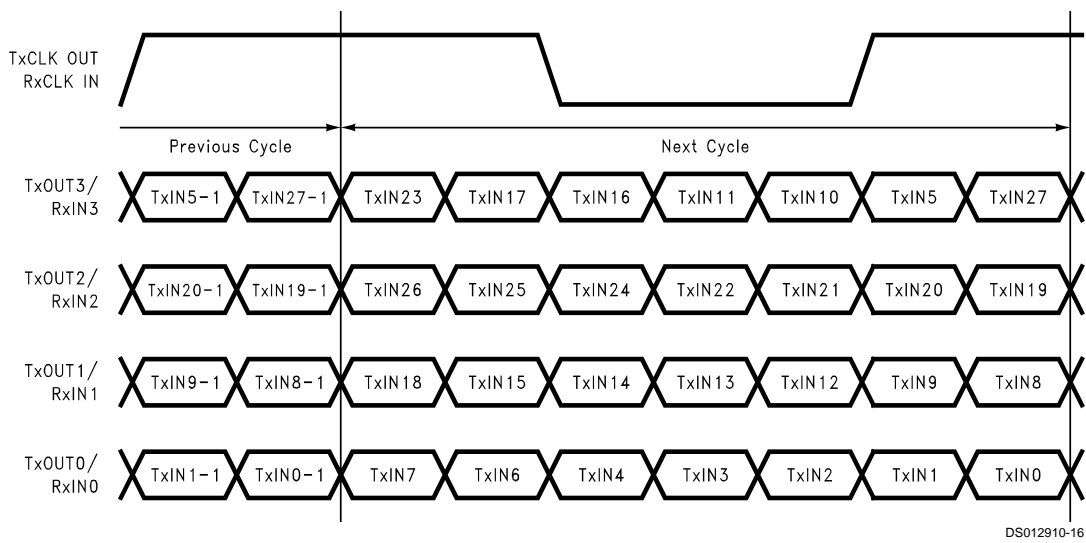


FIGURE 13. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs

AC Timing Diagrams (Continued)

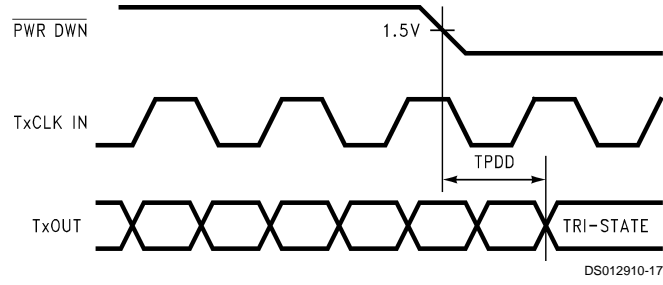


FIGURE 14. Transmitter Powerdown Delay

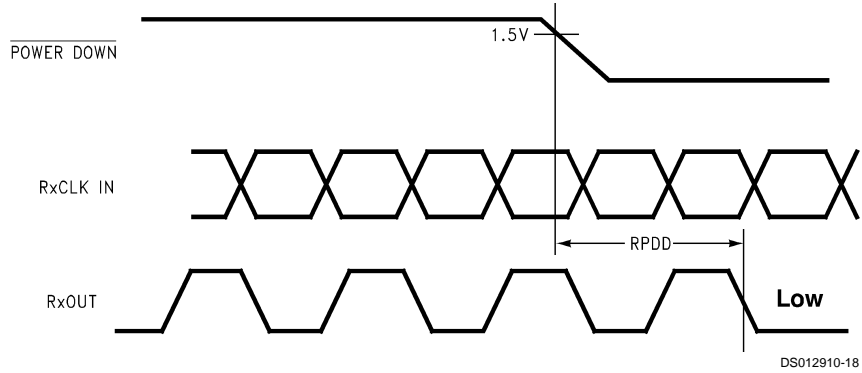


FIGURE 15. Receiver Powerdown Delay

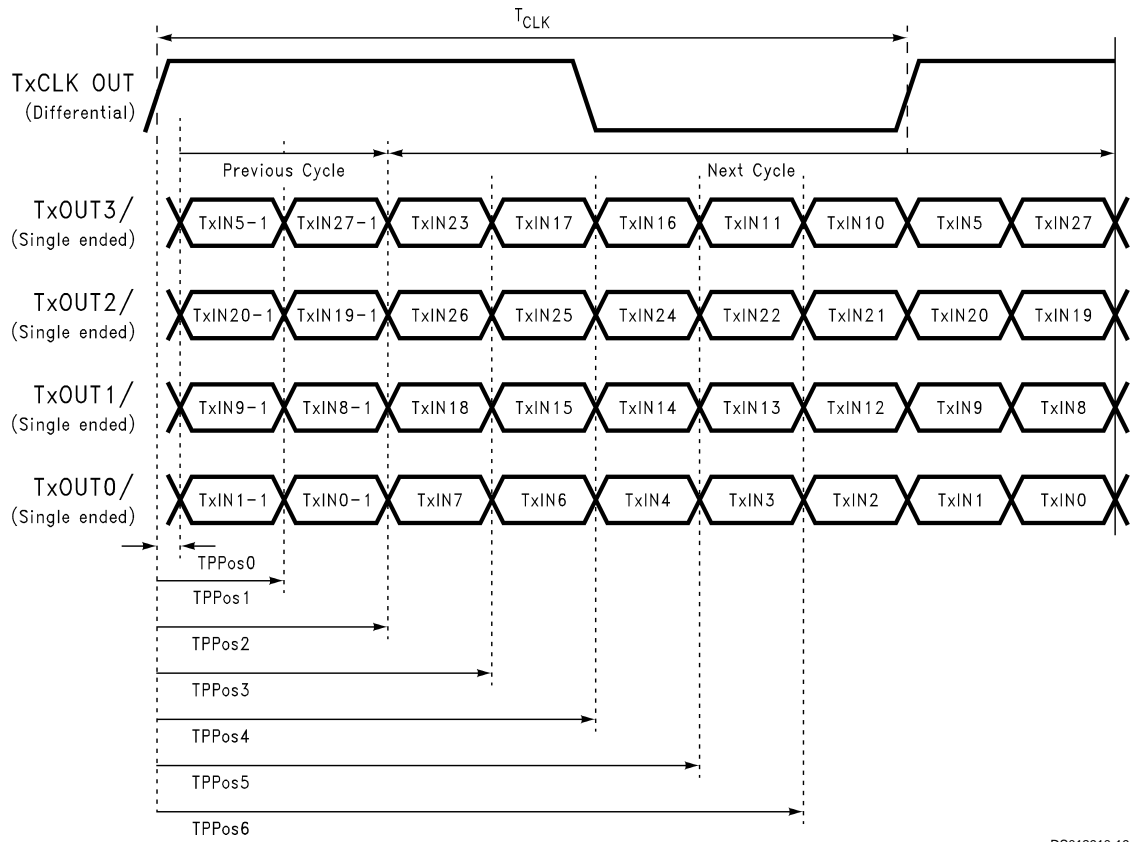
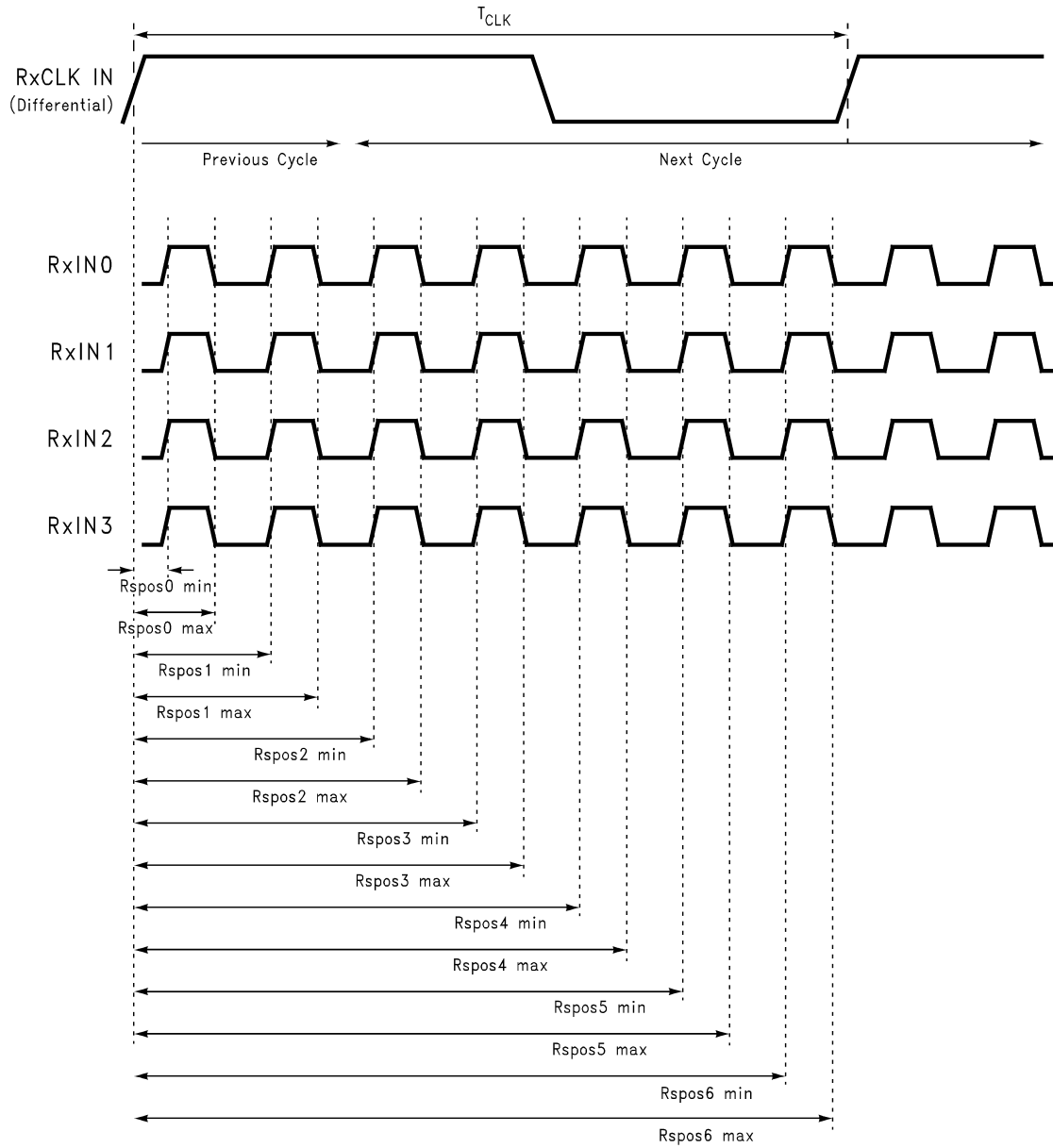


FIGURE 16. Transmitter LVDS Output Pulse Position Measurement

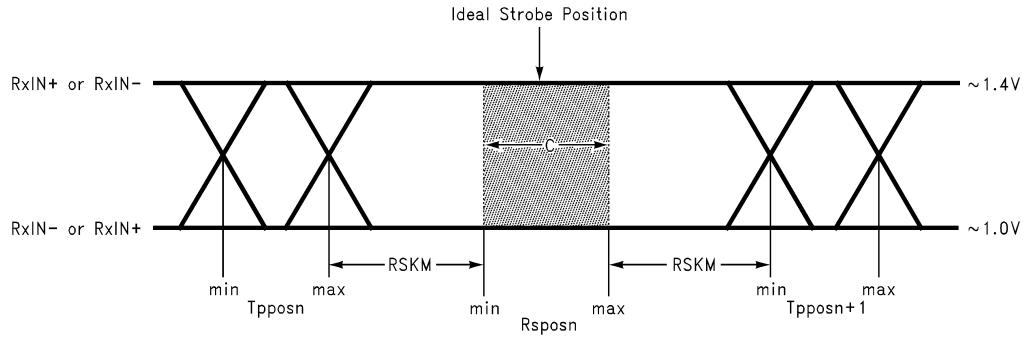
AC Timing Diagrams (Continued)



DS012910-28

FIGURE 17. Receiver LVDS Input Strobe Position

## AC Timing Diagrams (Continued)



DS012910-20

C — Setup and Hold Time (Internal data sampling window) defined by Rspn (receiver input strobe position) min and max  
 Tpposn — Transmitter output pulse position (min and max)  
 $RSKM \geq \text{Cable Skew (type, length) + Source Clock Jitter (cycle to cycle)(Note 11) + ISI (Inter-symbol interference)(Note 12)}$   
 Cable Skew — typically 10 ps–40 ps per foot, media dependent

**Note 11:** Cycle-to-cycle jitter is less than 250 ps

**Note 12:** ISI is dependent on interconnect length; may be zero

**FIGURE 18. Receiver LVDS Input Skew Margin**

## Pin Descriptions

### DS90CR285 MTD56 (TSSOP) Package Pin Description — Channel Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input.
TxOUT+	O	4	Positive LVDS differential data output.
TxOUT-	O	4	Negative LVDS differential data output.
TxCLK IN	I	1	TTL level clock input. The rising edge acts as data strobe. Pin name TxCLK IN.
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT-	O	1	Negative LVDS differential clock output.
PWR DWN	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
V <sub>CC</sub>	I	4	Power supply pins for TTL inputs.
GND	I	5	Ground pins for TTL inputs.
PLL V <sub>CC</sub>	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V <sub>CC</sub>	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

### DS90CR285 SLC64A (FBGA) Package Pin Summary — Channel Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input.
TxOUT+	O	4	Positive LVDS differential data output.
TxOUT-	O	4	Negative LVDS differential data output.
TxCLKIN	I	1	TTL level clock input. The rising edge acts as data strobe. Pin name TxCLK IN.
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT-	O	1	Negative LVDS differential clock output.
PWR DWN	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
V <sub>CC</sub>	I	4	Power supply pins for TTL inputs.

## Pin Descriptions (Continued)

DS90CR285 SLC64A (FBGA) Package Pin Summary —  
Channel Link Transmitter (Continued)

Pin Name	I/O	No.	Description
GND	I	5	Ground pins for TTL inputs.
PLL V <sub>CC</sub>	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V <sub>CC</sub>	I	2	Power supply pin for LVDS outputs.
LVDS GND	I	4	Ground pins for LVDS outputs.
NC		6	Pins not connected.

DS90CR285 SLC64A (FBGA) Package Pin Description —  
Channel Link Transmitter

By Pin			By Pin Type		
Pin	Pin Name	Type	Pin	Pin Name	Type
A1	TxIN27	I	D3	GND	G
A2	TxOUT0-	O	E4	GND	G
A3	TxOUT0+	O	E8	GND	G
A4	LVDS VCC	P	G1	GND	G
A5	LVDS VCC	P	G6	GND	G
A6	TxCLKOUT-	O	B3	LVDS GND	G
A7	TxCLKOUT+	O	B4	LVDS GND	G
A8	TxOUT3+	O	B7	LVDS GND	G
B1	TxIN1	I	D5	LVDS GND	G
B2	TxIN0	I	C6	PLL GND	G
B3	LVDS GND	G	D6	PLL GND	G
B4	LVDS GND	G	D7	PWR DWN	I
B5	TxOUT2-	O	C8	TxCLKIN	I
B6	TxOUT3-	O	B2	TxIN0	I
B7	LVDS GND	G	B1	TxIN1	I
B8	NC		D2	TxIN2	I
C1	TxIN3	I	C1	TxIN3	I
C2	NC		D1	TxIN4	I
C3	NC		F1	TxIN5	I
C4	TxOUT1-	O	E2	TxIN6	I
C5	TxOUT2+	O	E3	TxIN7	I
C6	PLL GND	G	G2	TxIN8	I
C7	PLL VCC	P	H1	TxIN9	I
C8	TxCLKIN	I	G3	TxIN10	I
D1	TxIN4	I	H3	TxIN11	I
D2	TxIN2	I	F4	TxIN12	I
D3	GND	G	G4	TxIN13	I
D4	TxOUT1+	O	H4	TxIN14	I
D5	LVDS GND	G	H5	TxIN15	I
D6	PLL GND	G	E5	TxIN16	I
D7	PWR DWN	I	F5	TxIN17	I
D8	TxIN26	I	H6	TxIN18	I
E1	VCC	P	H7	TxIN19	I
E2	TxIN6	I	H8	TxIN20	I

**Pin Descriptions** (Continued)**DS90CR285 SLC64A (FBGA) Package Pin Description — Channel Link Transmitter** (Continued)

By Pin			By Pin Type		
E3	TxIN7	I	G7	TxIN21	I
E4	GND	G	F7	TxIN22	I
E5	TxIN16	I	G8	TxIN23	I
E6	VCC	P	E7	TxIN24	I
E7	TxIN24	I	F8	TxIN25	I
E8	GND	G	D8	TxIN26	I
F1	TxIN5	I	A1	TxIN27	I
F2	NC		A6	TxCLKOUT-	O
F3	NC		A7	TxCLKOUT+	O
F4	TxIN12	I	A2	TxOUT0-	O
F5	TxIN17	I	A3	TxOUT0+	O
F6	NC		C4	TxOUT1-	O
F7	TxIN22	I	D4	TxOUT1+	O
F8	TxIN25	I	B5	TxOUT2-	O
G1	GND	G	C5	TxOUT2+	O
G2	TxIN8	I	B6	TxOUT3-	O
G3	TxIN10	I	A8	TxOUT3+	O
G4	TxIN13	I	A4	LVDS VCC	P
G5	VCC	P	A5	LVDS VCC	P
G6	GND	G	C7	PLL VCC	P
G7	TxIN21	I	E1	VCC	P
G8	TxIN23	I	E6	VCC	P
H1	TxIN9	I	G5	VCC	P
H2	VCC	P	H2	VCC	P
H3	TxIN11	I	B8	NC	
H4	TxIN14	I	C2	NC	
H5	TxIN15	I	C3	NC	
H6	TxIN18	I	F2	NC	
H7	TxIN19	I	F3	NC	
H8	TxIN20	I	F6	NC	

G : Ground  
I : Input  
O : Output  
P : Power  
NC : No Connect

**DS90CR286 MTD56 (TSSOP) Package Pin Description — Channel Link Receiver**

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN-	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs.
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN-	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe. Pin name RxCLK OUT.
PWR DWN	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V <sub>CC</sub>	I	4	Power supply pins for TTL outputs.

## Pin Descriptions (Continued)

### DS90CR286 MTD56 (TSSOP) Package Pin Description — Channel Link Receiver (Continued)

Pin Name	I/O	No.	Description
GND	I	5	Ground pins for TTL outputs.
PLL $V_{CC}$	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS $V_{CC}$	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

## Applications Information

The Channel Link devices are intended to be used in a wide variety of data transmission applications. Depending upon the application the interconnecting media may vary. For example, for lower data rate (clock rate) and shorter cable lengths (< 2m), the media electrical performance is less critical. For higher speed/long distance applications the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). Twin-coax for example, has been demonstrated at distances as great as 5 meters and with the maximum data transfer of 1.848 Gbit/s. Additional applications information can be found in the following National Interface Application Notes:

AN = ####	Topic
AN-1041	Introduction to Channel Link
AN-1108	Channel Link PCB and Interconnect Design-In Guidelines
AN-806	Transmission Line Theory
AN-905	Transmission Line Calculations and Differential Impedance
AN-916	Cable Information

**CABLES:** A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The 21-bit CHANNEL LINK chipset (DS90CR215/216) requires four pairs of signal wires and the 28-bit CHANNEL LINK chipset (DS90CR285/286) requires five pairs of signal wires. The ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is also recommended that cable skew remain below 150 ps (66 MHz clock rate) to maintain a sufficient data sampling window at the receiver.

In addition to the four or five cable pairs that carry data and clock, it is recommended to provide at least one additional conductor (or pair) which connects ground between the transmitter and receiver. This low impedance ground provides a common mode return path for the two devices. Some of the more commonly used cable types for point-to-point applications include flat ribbon, flex, twisted pair and Twin-Coax. All are available in a variety of configurations and options. Flat ribbon cable, flex and twisted pair generally perform well in short point-to-point applications while Twin-Coax is good for short and long applications. When using ribbon cable, it is recommended to place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs. For Twin-Coax cable applications, it is recommended to utilize a shield on each cable pair. All extended point-to-point applications should also employ an overall shield surrounding all cable pairs

regardless of the cable type. This overall shield results in improved transmission parameters such as faster attainable speeds, longer distances between transmitter and receiver and reduced problems associated with EMS or EMI.

The high-speed transport of LVDS signals has been demonstrated on several types of cables with excellent results. However, the best overall performance has been seen when using Twin-Coax cable. Twin-Coax has very low cable skew and EMI due to its construction and double shielding. All of the design considerations discussed here and listed in the supplemental application notes provide the subsystem communications designer with many useful guidelines. It is recommended that the designer assess the tradeoffs of each application thoroughly to arrive at a reliable and economical cable solution.

**BOARD LAYOUT:** To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer should also try to maintain equal length on signal traces for a given differential pair. As with any high speed design, the impedance discontinuities should be limited (reduce the numbers of vias and no 90 degree angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. Care should be taken to ensure that the differential trace impedance match the differential impedance of the selected physical media (this impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input). Finally, the location of the CHANNEL LINK TxOUT/RxIN pins should be as close as possible to the board edge so as to eliminate excessive pcb runs. All of these considerations will limit reflections and crosstalk which adversely effect high frequency performance and EMI.

**UNUSED INPUTS:** All unused inputs at the TxIN inputs of the transmitter must be tied to ground. All unused outputs at the RxOUT outputs of the receiver must then be left floating.

**INPUTS:** The TxIN and control inputs are compatible with LVCMOS and LVTTTL levels. These pins are not 5V tolerant.

**TERMINATION:** Use of current mode drivers requires a terminating resistor across the receiver inputs. The CHANNEL LINK chipset will normally require a single 100Ω resistor between the true and complement lines on each differential pair of the receiver input. The actual value of the termination resistor should be selected to match the differential mode characteristic impedance (90Ω to 120Ω typical) of the cable. *Figure 19* shows an example. No additional pull-up or pull-down resistors are necessary as with some other differential

## Applications Information (Continued)

technologies such as PECL. Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.

**DECOUPLING CAPACITORS:** Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three

parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each  $V_{CC}$  and the ground plane(s) are recommended. The three capacitor values are 0.1  $\mu\text{F}$ , 0.01  $\mu\text{F}$  and 0.001  $\mu\text{F}$ . An example is shown in *Figure 20*. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL  $V_{CC}$  should receive the most filtering/bypassing. Next would be the LVDS  $V_{CC}$  pins and finally the logic  $V_{CC}$  pins.

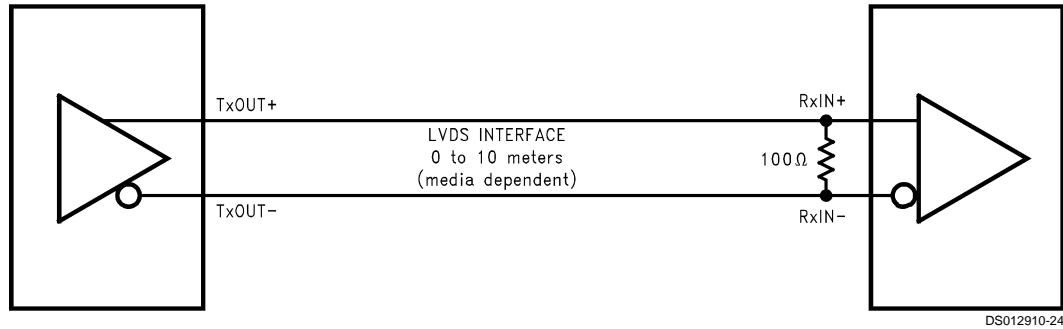


FIGURE 19. LVDS Serialized Link Termination

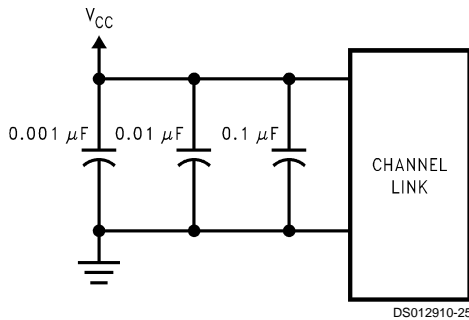


FIGURE 20. CHANNEL LINK Decoupling Configuration

**CLOCK JITTER:** The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 66 MHz clock has a period of 15 ns which results in a data bit width of 2.16 ns. Differential skew ( $\Delta t$  within one differential pair), interconnect skew ( $\Delta t$  of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal. Individual bypassing of each  $V_{CC}$  to ground will minimize the noise passed on to the PLL, thus creating a

low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

**COMMON MODE vs. DIFFERENTIAL MODE NOISE MARGIN:** The typical signal swing for LVDS is 300 mV centered at +1.2V. The CHANNEL LINK receiver supports a 100 mV threshold therefore providing approximately 200 mV of differential noise margin. Common mode protection is of more importance to the system's operation due to the differential data transmission. LVDS supports an input voltage range of Ground to +2.4V. This allows for a  $\pm 1.0\text{V}$  shifting of the center point due to ground potential differences and common mode noise.

**POWER SEQUENCING AND POWERDOWN MODE:** Outputs of the CHANNEL LINK transmitter remain in TRI-STATE<sup>®</sup> until the power supply reaches 2V. Clock and data outputs will begin to toggle 10 ms after  $V_{CC}$  has reached 3V and the Powerdown pin is above 1.5V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to 5  $\mu\text{W}$  (typical).

The CHANNEL LINK chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to  $V_{CC}$  through an internal diode. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.



Applications Information (Continued)

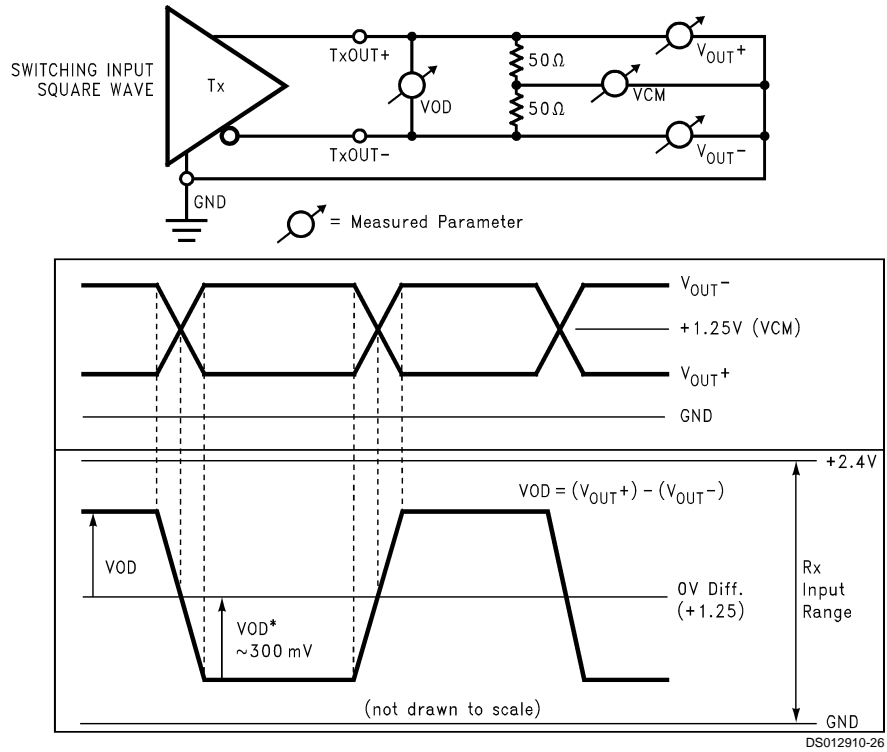
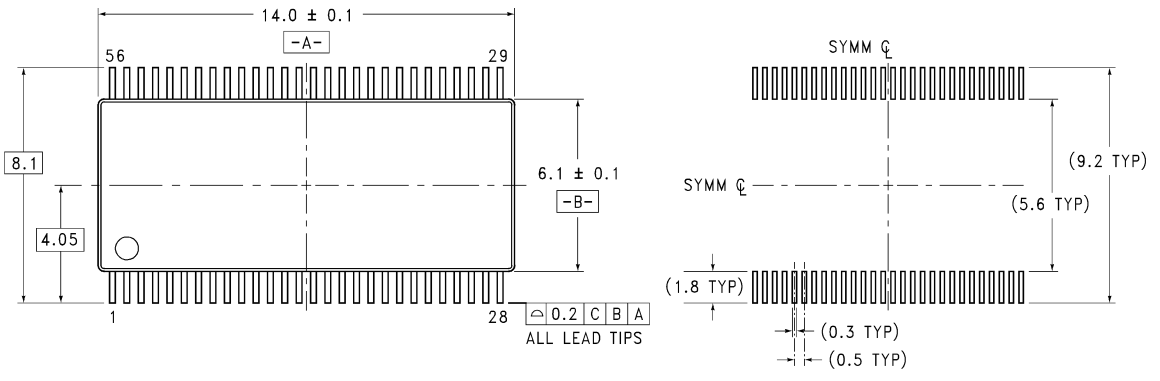
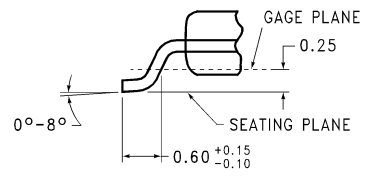
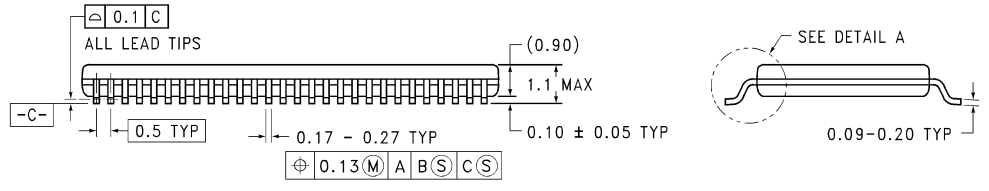


FIGURE 21. Single-Ended and Differential Waveforms

**Physical Dimensions** inches (millimeters) unless otherwise noted



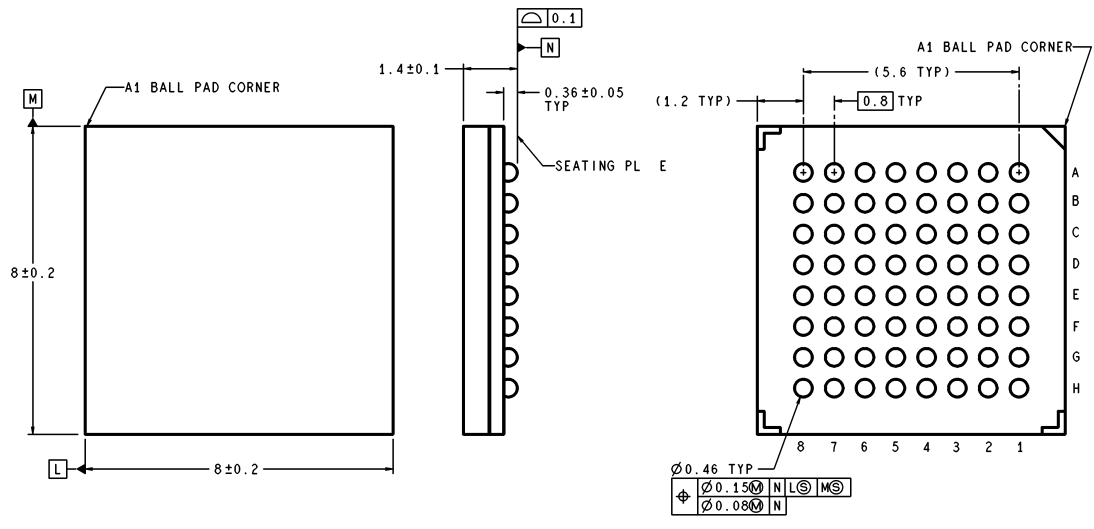
**LAND PATTERN RECOMMENDATION**



**DETAIL A**  
TYPICAL

MTD56 (REV B)

**Order Number DS90CR285MTD or DS90CR286MTD  
NS Package Number MTD56**



DIMENSIONS ARE IN MILLIMETERS

SLC64A (Rev B)

**64 ball, 0.8mm fine pitch ball grid array (FBGA) package  
Dimensions shown in millimeters only  
Order Number DS90CR285SLC  
NS Package Number SLC64A**

## Notes

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