

**Vertical Clock Driver for CCD Image sensor**

**Description**

CXD1250M/N is a clock driver developed for the vertical register drive of CCD Image sensor.

**Features**

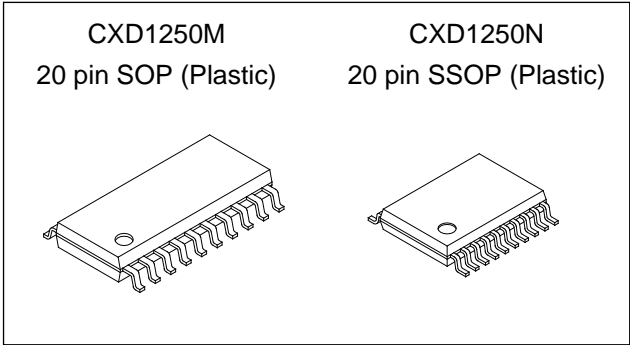
4-channel vertical clock driver and 1 channel substrate driver are built-in.

**Application**

CCD camera

**Structure**

CMOS



**Absolute Maximum Ratings** (Ta = 25°C)

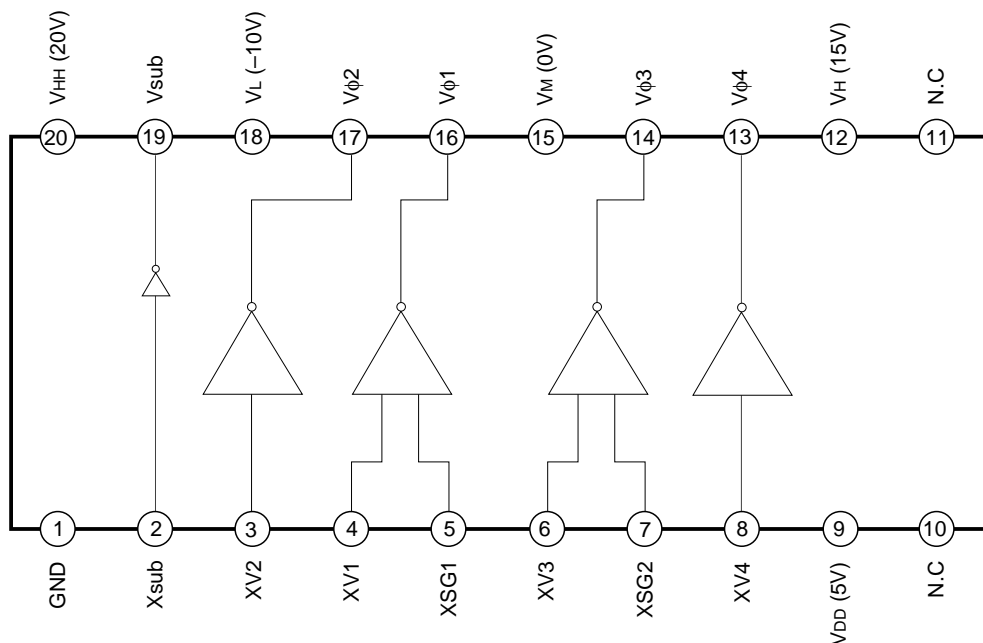
|                         |                               |   |    |
|-------------------------|-------------------------------|---|----|
| • Supply voltage        | V <sub>DD</sub>               | V <sub>L</sub> - 0.3 to V <sub>L</sub> + 35.0 | V  |
|                         | V <sub>M</sub>                | V <sub>L</sub> - 0.3 to V <sub>L</sub> + 35.0 | V  |
|                         | V <sub>H</sub>                | V <sub>L</sub> - 0.3 to V <sub>L</sub> + 35.0 | V  |
|                         | V <sub>HH</sub>               | V <sub>L</sub> - 0.3 to V <sub>L</sub> + 35.0 | V  |
| • Input voltage         | V <sub>i</sub>                | V <sub>L</sub> - 0.3 to V <sub>DD</sub> + 0.3 | V  |
| • Output voltage        | MV <sub>φ</sub> (pins 13, 17) | V <sub>L</sub> - 0.3 to V <sub>M</sub> + 0.3  | V  |
| • Output voltage        | HV <sub>φ</sub> (pins 14, 16) | V <sub>L</sub> - 0.3 to V <sub>H</sub> + 0.3  | V  |
| • Output voltage        | HHV <sub>φ</sub> (pin 19)     | V <sub>L</sub> - 0.3 to V <sub>HH</sub> + 0.3 | V  |
| • Operating temperature | T <sub>opr</sub>              | -25 to +85                                    | °C |
| • Storage temperature   | T <sub>stg</sub>              | -40 to +125                                   | °C |

**Recommended Operating Conditions**

|                         |                  |                       |    |
|-------------------------|------------------|-----------------------|----|
| • Supply voltage        | V <sub>DD</sub>  | 5.0 ± 0.5             | V  |
|                         | V <sub>M</sub>   | V <sub>L</sub> + 10.0 | V  |
|                         | V <sub>H</sub>   | V <sub>L</sub> + 25.0 | V  |
|                         | V <sub>HH</sub>  | V <sub>L</sub> + 30.0 | V  |
|                         | V <sub>L</sub>   | -10.0                 | V  |
| • Operating temperature | T <sub>opr</sub> | -20 to +75            | °C |

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Block Diagram and Pin Configuration (Top View)



Pin Description

| No. | Symbol | I/O | Description                   |
|-----|--------|-----|-------------------------------|
| 1   | GND    | —   | GND                           |
| 2   | Xsub   | I   | Output control (Vsub)         |
| 3   | XV2    | I   | Output control (Vφ2)          |
| 4   | XV1    | I   | Output control (Vφ1)          |
| 5   | XSG1   | I   | Output control (Vφ1)          |
| 6   | XV3    | I   | Output control (Vφ3)          |
| 7   | XSG2   | I   | Output control (Vφ3)          |
| 8   | XV4    | I   | Output control (Vφ4)          |
| 9   | VDD    | —   | Power supply (5V)             |
| 10  | NC     | —   |                               |
| 11  | NC     | —   |                               |
| 12  | VH     | —   | Power supply (15V)            |
| 13  | Vφ4    | O   | Output (2 level : VM, VL)     |
| 14  | Vφ3    | O   | Output (3 level : VH, VM, VL) |
| 15  | VM     | —   | Power supply (0V)             |
| 16  | Vφ1    | O   | Output (3 level : VH, VM, VL) |
| 17  | Vφ2    | O   | Output (2 level : VM, VL)     |
| 18  | VL     | —   | Power supply (-10V)           |
| 19  | Vsub   | O   | Output (2 level : VHH, VL)    |
| 20  | VHH    | —   | Power supply (20V)            |

Truth Table

| Input   |          |         |      | Output         |                |                 |
|---------|----------|---------|------|----------------|----------------|-----------------|
| XV1 · 3 | XSG1 · 2 | XV2 · 4 | Xsub | V $\phi$ 1 · 3 | V $\phi$ 2 · 4 | Vsub            |
| L       | H        | X       | X    | V <sub>M</sub> | X              | X               |
| H       | H        | X       | X    | V <sub>L</sub> | X              | X               |
| X       | X        | L       | X    | X              | V <sub>M</sub> | X               |
| X       | X        | H       | X    | X              | V <sub>L</sub> | X               |
| X       | X        | X       | L    | X              | X              | V <sub>HH</sub> |
| X       | X        | X       | H    | X              | X              | V <sub>L</sub>  |
| L       | L        | X       | X    | V <sub>H</sub> | X              | X               |
| H       | L        | X       | X    | Z              | X              | X               |

X : Don't care  
Z : High impedance

DC Characteristics (Ta = 25°C)

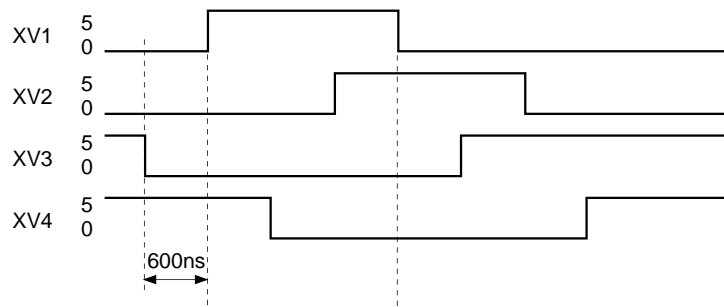
| Item                      | Symbol                 | Test condition                       |              | Min. | Typ. | Max. | Unit    |
|---------------------------|------------------------|--------------------------------------|--------------|------|------|------|---------|
|                           |                        |                                      | Power supply |      |      |      |         |
| "H" level input voltage   | V <sub>IH</sub>        |                                      |              | 3.5  | —    | —    | V       |
| "L" level input voltage   | V <sub>IL</sub>        |                                      |              | —    | —    | 1.5  | V       |
| "L" level output voltage  | V $\phi$ <sub>L</sub>  | I $\phi$ <sub>L</sub> = 20 $\mu$ A   |              | —    | -10  | -9.9 | V       |
| "M" level output voltage  | V $\phi$ <sub>M</sub>  | I $\phi$ <sub>M</sub> = -20 $\mu$ A  |              | —    | 0.0  | 0.1  | V       |
| "M" level output voltage  | V $\phi$ <sub>M</sub>  | I $\phi$ <sub>M</sub> = 20 $\mu$ A   |              | -0.1 | 0.0  | —    | V       |
| "H" level output voltage  | V $\phi$ <sub>H</sub>  | I $\phi$ <sub>H</sub> = -20 $\mu$ A  |              | 14.9 | 15   | —    | V       |
| "HH" level output voltage | V $\phi$ <sub>HH</sub> | I $\phi$ <sub>HH</sub> = -20 $\mu$ A |              | 19.9 | 20   | —    | V       |
| Input current             | I <sub>i</sub>         |                                      |              | —    | 1.0  | —    | $\mu$ A |
| Power supply current *    | I <sub>M</sub>         |                                      |              | —    | 4.5  | 5.0  | mA      |
| Power supply current *    | I <sub>DD</sub>        |                                      |              | —    | 0.3  | 0.5  | mA      |
| Power supply current *    | I <sub>H</sub>         |                                      |              | —    | 0.1  | 0.2  | mA      |
| Power supply current *    | I <sub>HH</sub>        |                                      |              | —    | 0.05 | 0.1  | mA      |

\* Supply current at operation (See the Test Circuit)

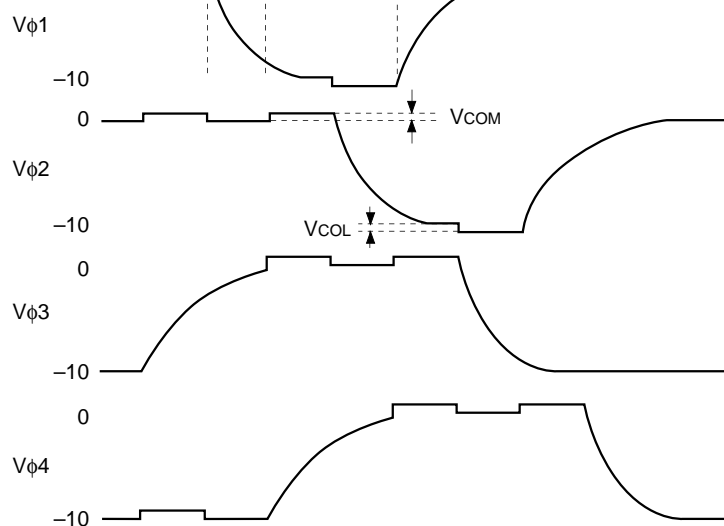
**Switching Characteristics** (See the Test Circuit  $T_a = 25^\circ\text{C}$ ,  $V_{HH} = 20\text{V}$ ,  $V_H = 15\text{V}$ ,  $V_M = 0\text{V}$ ,  $V_L = -10\text{V}$ ,  $V_{DD} = 5\text{V}$ )

| Item                               | Symbol           | Conditions  | Max. | Min. | Unit |
|------------------------------------|------------------|---|------|------|------|
| Output current                     | $I_L$            | $V_{\phi 1 \text{ to } 4} = -9.5\text{V}$                       | -25  |      | mA   |
| Output current                     | $I_{M1}$         | $V_{\phi 1 \text{ to } 4} = -0.5\text{V}$                       |      | 10   | mA   |
| Output current                     | $I_{M2}$         | $V_{\phi 1, 3} = 0.5\text{V}$                                   | -9   |      | mA   |
| Output current                     | $I_H$            | $V_{\phi 1, 3} = 14.5\text{V}$                                  |      | 12   | mA   |
| Output current                     | $I_{SL}$         | $V_{\text{sub}} = -9.5\text{V}$                                 | -12  |      | mA   |
| Output current                     | $I_{SH}$         | $V_{\text{sub}} = -19.5\text{V}$                                |      | 7    | mA   |
| Rise time $V_L \rightarrow V_M$    | $T_{TLM}$        | $V_{\phi 1 \text{ to } 4} = -0.5\text{V}$ After input transient | 1000 |      | ns   |
| Fall time $V_M \rightarrow V_L$    | $T_{TML}$        | $V_{\phi 1 \text{ to } 4} = -9.5\text{V}$ After input transient | 500  |      | ns   |
| Rise time $V_M \rightarrow V_H$    | $T_{TMH}$        | $V_{\phi 1, 3} = 14\text{V}$ After input transient              | 1000 |      | ns   |
| Fall time $V_H \rightarrow V_M$    | $T_{THM}$        | $V_{\phi 1, 3} = 1\text{V}$ After input transient               | 1000 |      | ns   |
| Rise time $V_L \rightarrow V_{HH}$ | $T_{TLHH}$       | $V_{\text{sub}} = 17\text{V}$ After input transient             | 200  |      | ns   |
| Fall time $V_{HH} \rightarrow V_L$ | $T_{THHL}$       | $V_{\text{sub}} = -7\text{V}$ After input transient             | 200  |      | ns   |
| Coupling amplitude (middle level)  | $V_{\text{COM}}$ | $V_{\phi 1 \text{ to } 4}$                                      | 0.5  |      | V    |
| Coupling amplitude (low level)     | $V_{\text{COL}}$ | $V_{\phi 1 \text{ to } 4}$                                      | 0.5  |      | V    |

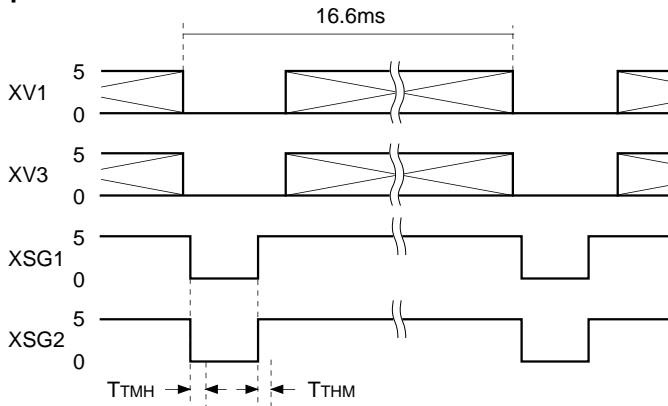
**Input Waveform** (Repeat Cycle 15.7kHz)



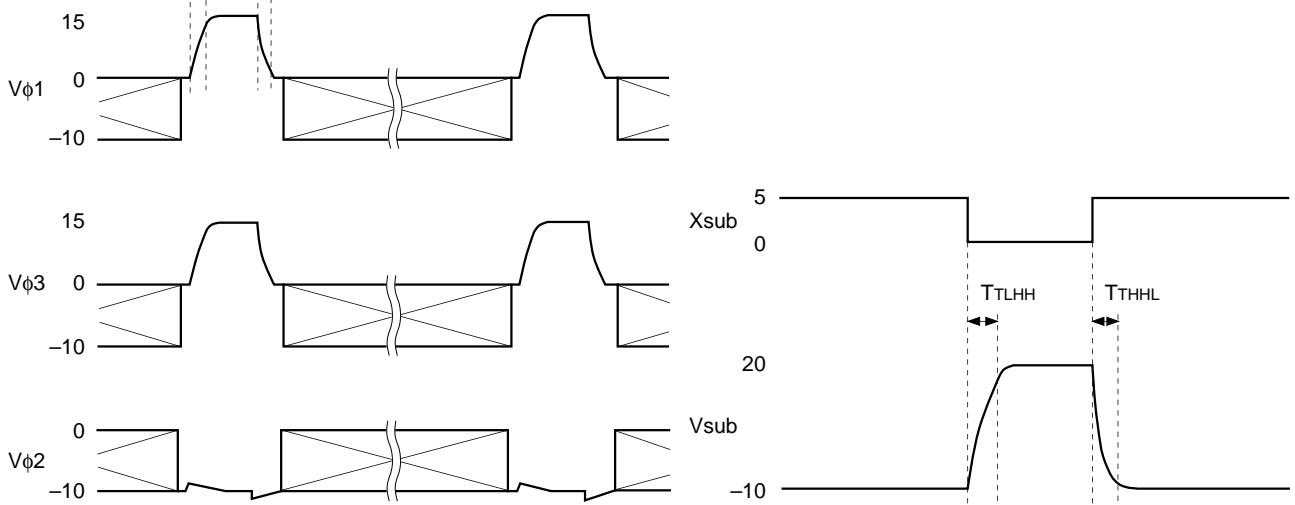
**Output Waveform**



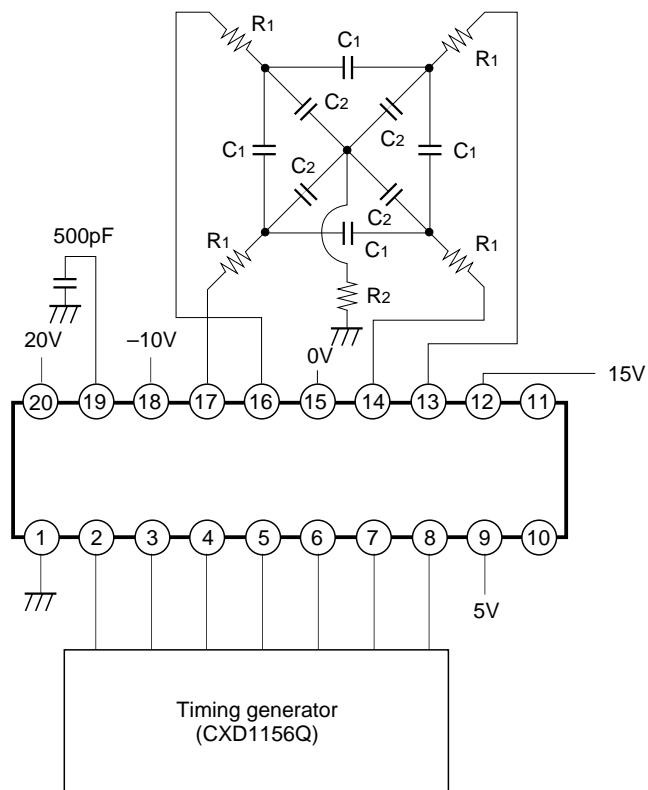
**Switching Waveform  
Input Waveform**



**Output Waveform**

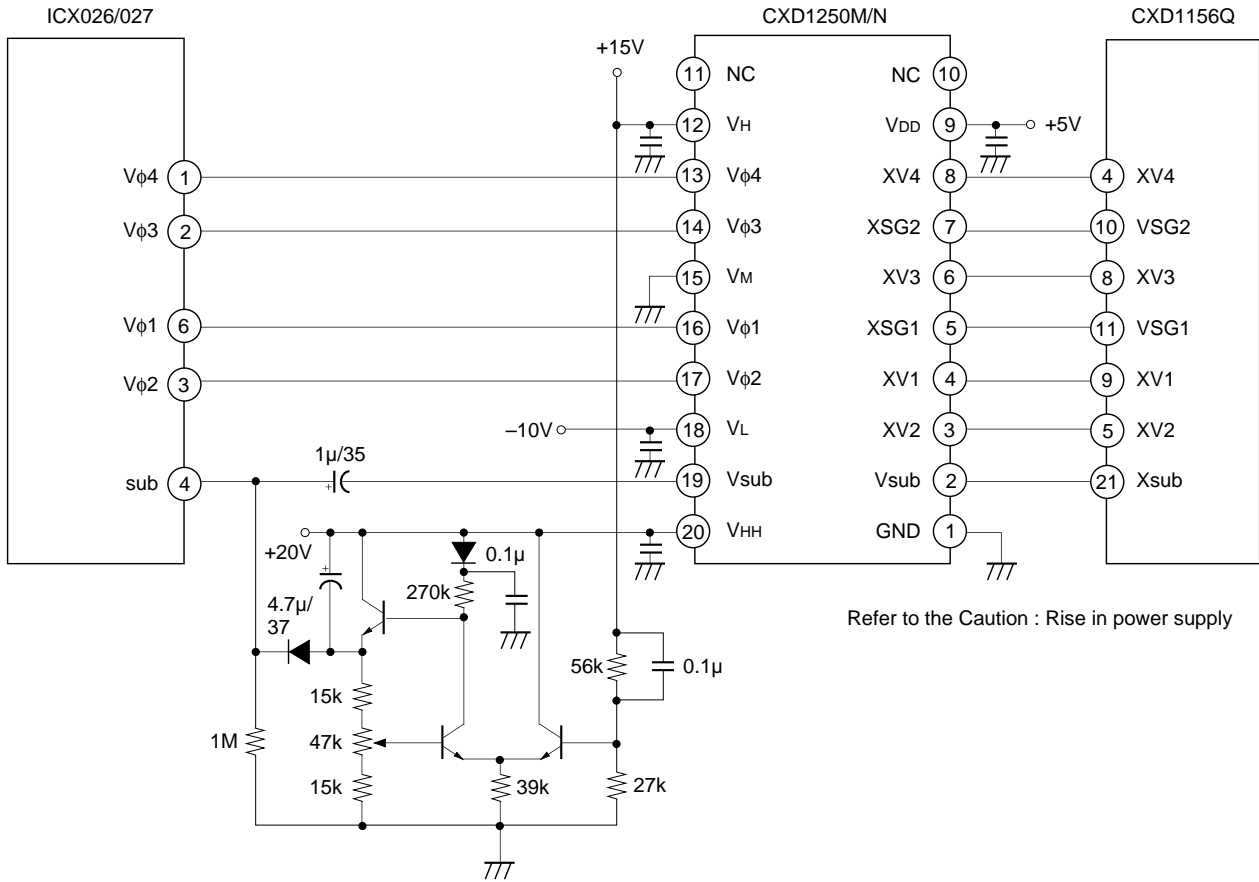


**Test Circuit**



- R1; 27Ω
- R2; 5Ω
- C1; 1500pF
- C2; 3300pF

Application Circuit



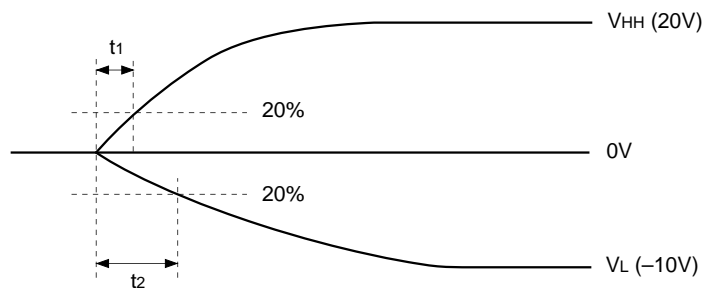
Refer to the Caution : Rise in power supply

Note:  
The capacitor more than 0.1μF should be connected between the ground and each pin of VDD, VH, VHH and VL .

Caution : Rise in Power Supply

When the substrate driver is in use, be careful not to let the CCD imagesensors Sub (pin 4) turn into negative voltage.

To this end, raise VL and VHH at the application circuit under the following conditions.



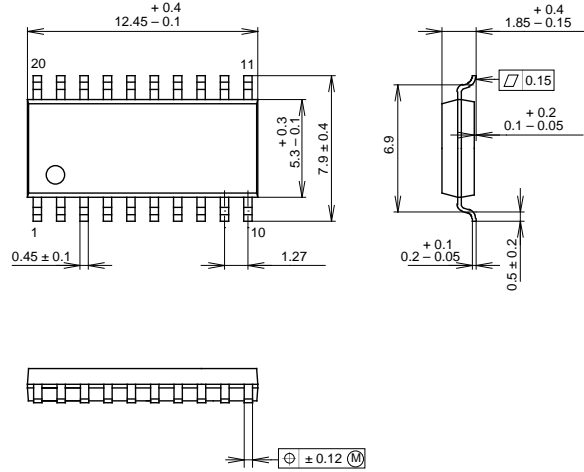
$$t_2 \geq t_1 \geq 10\text{msec}$$

Package Outline

Unit: mm

CXD1250M

20PIN SOP (PLASTIC) 300mil



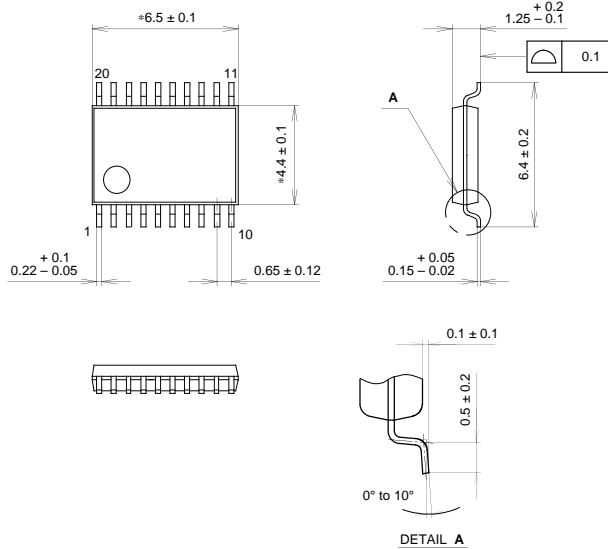
PACKAGE STRUCTURE

|            |                  |
|------------|------------------|
| SONY CODE  | SOP-20P-L01      |
| EIAJ CODE  | +SOP020-P-0300-A |
| JEDEC CODE |                  |

|                  |                      |
|------------------|----------------------|
| PACKAGE MATERIAL | EPOXY / PHENOL RESIN |
| LEAD TREATMENT   | SOLDER PLATING       |
| LEAD MATERIAL    | COPPER ALLOY         |
| PACKAGE WEIGHT   | 0.3g                 |

CXD1250N

20PIN SSOP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

|            |                |
|------------|----------------|
| SONY CODE  | SSOP-20P-L01   |
| EIAJ CODE  | SSOP020-P-0044 |
| JEDEC CODE |                |

|                  |                            |
|------------------|----------------------------|
| PACKAGE MATERIAL | EPOXY RESIN                |
| LEAD TREATMENT   | SOLDER / PALLADIUM PLATING |
| LEAD MATERIAL    | COPPER / 42 ALLOY          |
| PACKAGE WEIGHT   | 0.1g                       |