SONY

CXA1645P/M

RGB Encoder

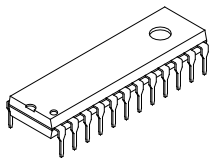
For the availability of this product, please contact the sales office.

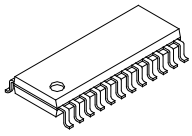
Description

The CXA1645P/M is an encoder IC that converts analog RGB signals to a composite video signal. This IC has various pulse generators necessary for encoding. Composite video outputs and Y/C outputs for the S terminal are obtained just by inputting composite sync, subcarrier and analog RGB signals.

It is best suited to image processing of personal computers and video games.

24 pin DIP (Plastic) 24 pin SOP (Plastic)





Features

- Single 5V power supply
- Compatible with both NTSC and PAL systems
- Built-in 75Ω drivers
  (RGB output, composite video output, Y output, C output)
- Both sine wave and pulse can be input as a subcarrier.
- Built-in band pass filter for the C signal and delay line for the Y signal
- Built-in R-Y and B-Y modulator circuits
- Built-in PAL alternate circuit
- Burst flag generator circuit
- Half H killer circuit

Applications

Image processing of video games and personal computers

Structure

Bipolar silicon monolithic IC

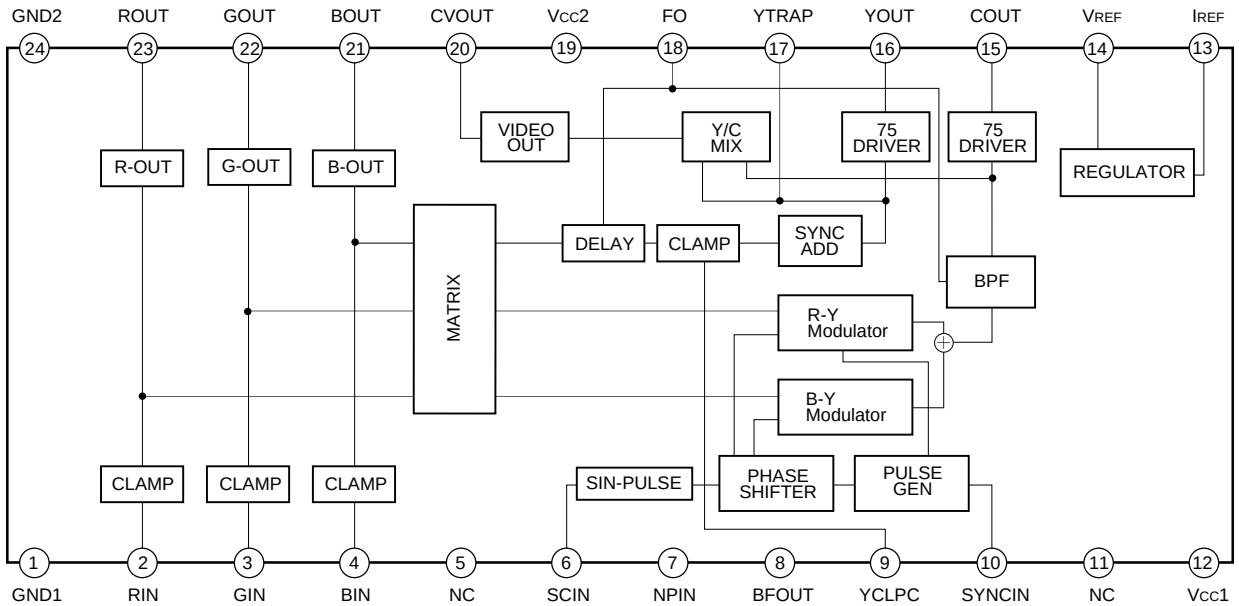
Absolute Maximum Ratings

• Supply voltage	V_{CC}	14	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	CXA1645P 1250	mW
		CXA1645M 780	mW

Recommended Operating Condition

Supply voltage	V_{CC}1, 2	5.0 ± 0.25 V

Block Diagram and Pin Configuration



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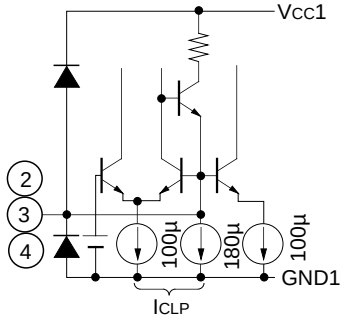
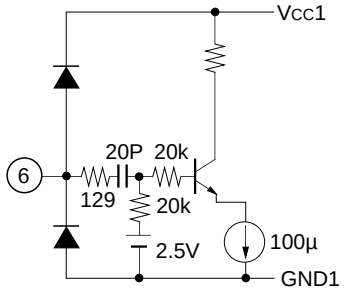
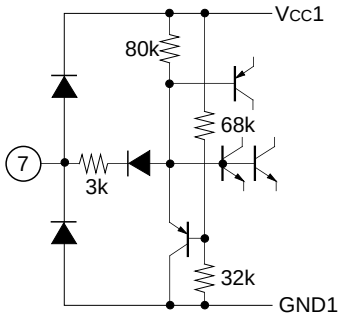
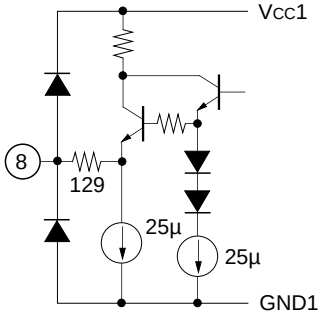
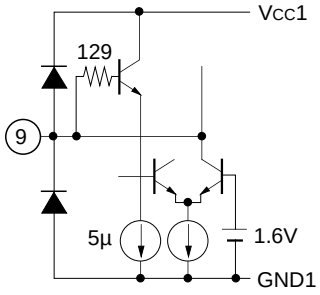
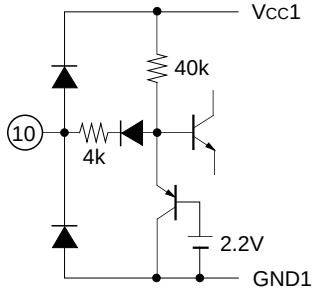
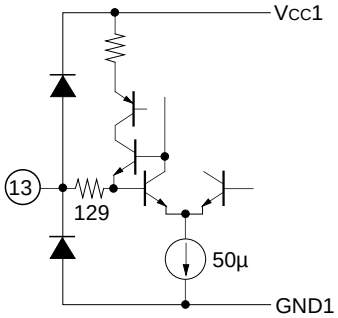
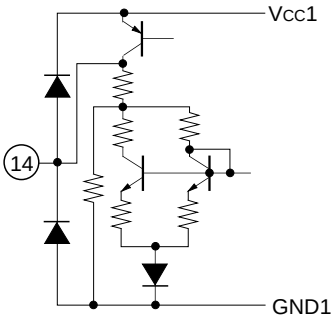
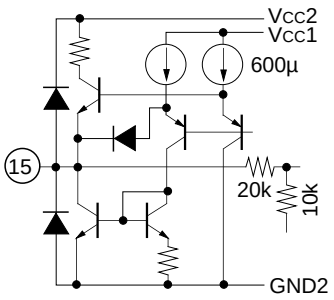
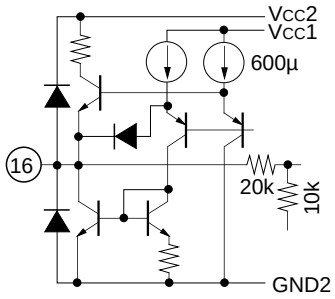
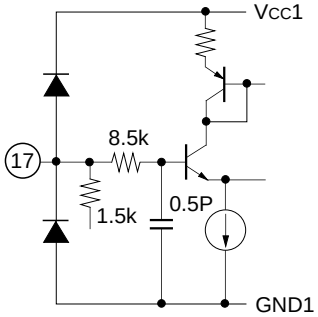
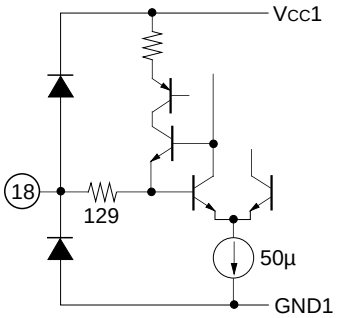
E93411A41-ST

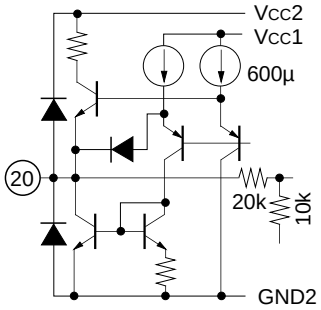
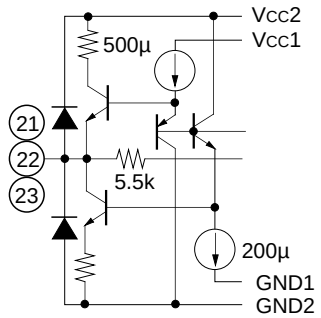
Pin Description

* Externally applied voltage

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	GND1	0V*		Ground for all circuits other than RGB, composite video and Y/C output circuits. The leads to GND2 should be as short and wide as possible.
2 3 4	RIN GIN BIN	Black level when clamped 2.0V		Analog RGB signal inputs. Input 100%, = 1Vp-p (max.). To minimize clamp error, input at as low impedance as possible. ICLP turns ON only in the burst flag period.
5	NC			NO CONNECTION
6	SCIN	—		Subcarrier input. Input 0.4 to 0.5Vp-p sine wave or pulse. Refer to Notes on Operation, Nos. 3 and 5.
7	NPIN	1.7V		Pin for switching between NTSC and PAL modes NTSC: Vcc, PAL: GND
8	BFOUT	H : 3.6V L : 3.2V		BF pulse monitoring output. Incapable of driving a 75Ω load.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9	YCLPC	2.5V		Pin to determine the Y signal clamp time constant. Connect to GND via a 0.1µF capacitor.
10	SYNC IN	2.2V		Composite sync signal input. Input TTL-level voltages. L (≤ 0.8V): SYNC period H (≥ 2.0V)
12	Vcc1	5.0V*		Power supply for all circuits other than RGB, composite video and Y/C output circuits. Refer to Notes on Operation. Nos. 4 and 10.
13	IREF	2.0V		Pin to determine the internal reference current. Connect to GND via a 47kΩ resistor.
14	VREF	4.0V		Internal reference voltage. Connect a decoupling capacitor of approximately 10µF. Refer to Notes on Operation, Nos. 4 and 7.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15	COUT	2.2V		Chroma signal output. Capable of driving a 75Ω load. Refer to Notes on Operation, Nos. 6 and 9.
16	YOUT	Black level 1.3V		Y signal output. Capable of driving a 75Ω load. Refer to Notes on Operation, Nos. 6 and 9.
17	YTRAP	Black level 1.6V	 Input resistance 1.5kΩ	Pin for reducing cross color caused by the subcarrier frequency component of the Y signal. When the CVOUT pin is in use, connect a capacitor or a capacitor and an inductor in series between YTRAP and GND. Decide capacitance and inductance, giving consideration to cross color and the required resolution. No influence on the YOUT pin. Refer to Notes on Operation, No. 8.
18	FO	2.0V		Internal filter fo adjustment pin. Connect to GND via the following resistor according to the NTSC or PAL mode. NTSC: 20kΩ (±1%) PAL : 16kΩ (±1%)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
19	$V_{CC}2$	5.0V*		Power supply for RGB, composite video and Y/C output circuits. Decouple this pin with a large capacitor of 10µF or above as a high current flows. Refer to Notes on Operation, Nos. 4 and 10.
20	CVOUT	Black level 1.2V		Composite video signal output. Capable of driving a 75Ω load. Refer to Notes on Operation, Nos. 6 and 9.
21 22 23	BOUT GOUT ROUT	Black level 1.7V		Analog RGB signal outputs. Capable of driving a 75Ω load. Refer to Notes on Operation, Nos. 6 and 9.
24	GND2	0V*		Ground for RGB, composite video and Y/C output circuits. The leads to GND1 should be as short and wide as possible.

Electrical Characteristics (Ta = 25°C, V_{CC} = 5V, See the Electrical Characteristics Measurement Circuit.)

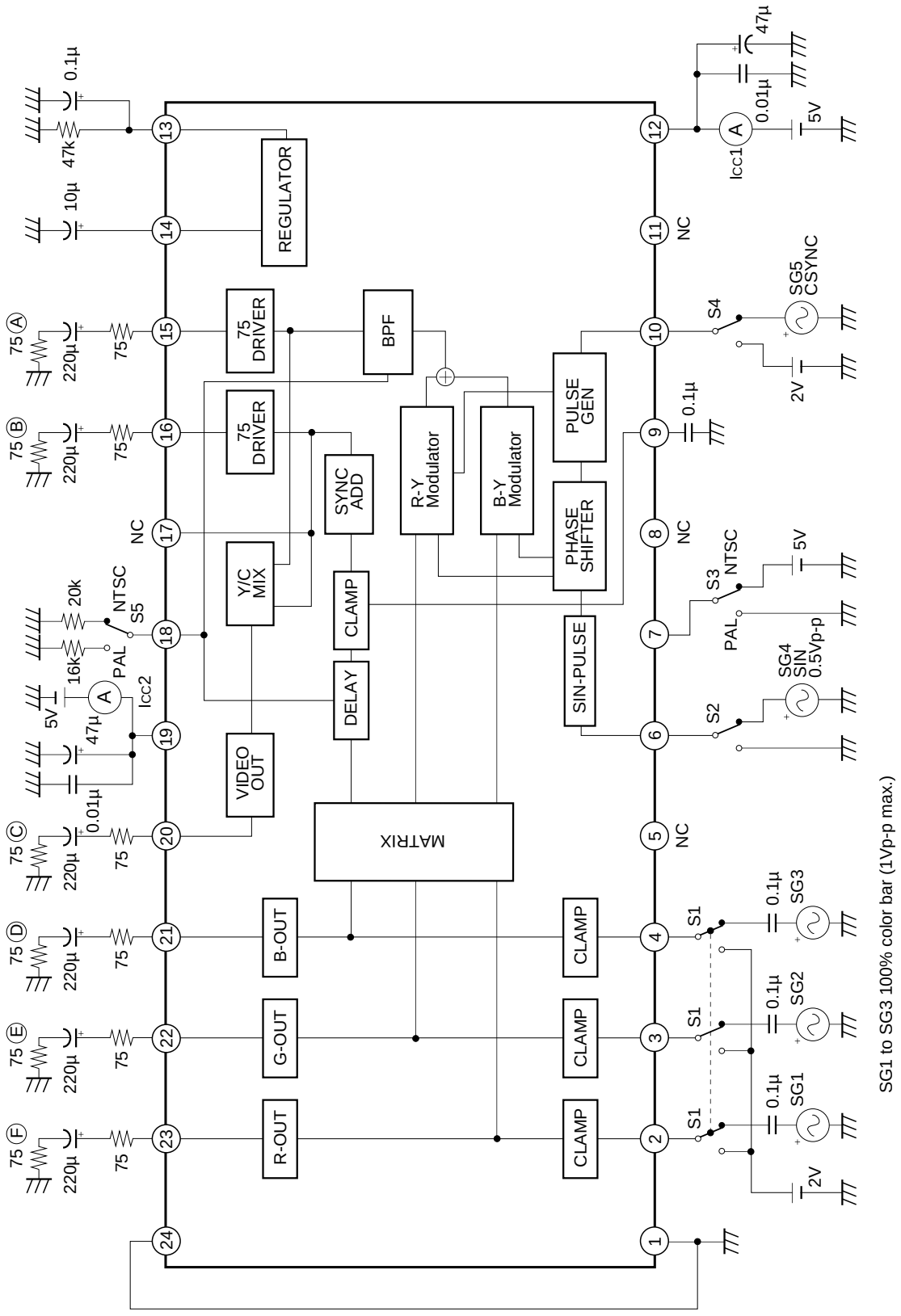
Item	Symbol	S1 RIN GIN BIN	S2 SCIN	S3 NPIN	S4 SYNC IN	S5 FO	Measurement point	Measurement Conditions	Min.	Typ.	Max.	Unit
Current consumption 1	$I_{CC}1$	2V	SG4	5V	SG5	20k	$I_{CC}1$	No input signal, SG5: CSYNC TTL level, SG4: SIN wave 3.58MHz 0.5Vp-p Fig. 1		31		mA
Current consumption 2	$I_{CC}2$						$I_{CC}2$			12		
(R, G, BOUT)												
RGB output voltage	V_O (R)	SG1			2V		D	SG1 to SG3: DC direct coupling 2.5V_{DC}, 1.0Vp-p f = 200kHz Pin 9 = Clamp voltage Fig. 2	0.64	0.71	0.78	Vp-p
	V_O (G)	SG2					E					
	V_O (B)	SG3					F					
RGB output frequency characteristics	f_C (R)	SG1			2V		D	SG1 to SG3: DC direct coupling 2.5V_{DC}, 1.0Vp-p f = 200kHz/5MHz Pin 9 = Clamp voltage Fig. 3	–3.0			dB
	f_C (G)	SG2					E					
	f_C (B)	SG3					F					
(YOUT & CVOUT)												
Output sync level	V_O (YS1/2)	SG1 to SG3	0V	5V	SG5	20k	B/C	SG1 to SG3: 100% color bar input, 1.0Vp-p (Max.) SG5: CSYNC TTL level Fig. 4	0.26	0.29	0.33	Vp-p
R100%: Y level	V_O (YR1/2)								0.17	0.21	0.26	V
G100%: Y level	V_O (YG1/2)								0.35	0.42	0.49	V
B100%: Y level	V_O (YB1/2)								0.065	0.08	0.095	V
White 100%: Y level	V_O (YW1/2)								0.6	0.71	0.82	V
Output frequency characteristics	f_C (Y1/2)	SG1 to SG3	0V	5V	2V	20k		SG1 to SG3: DC direct coupling 2.5V_{DC}, 1.0Vp-p f = 200kHz/5MHz Pin 9 = Clamp voltage Fig. 3	–3.0			dB

* Clamp voltage: voltage appearing at Pin 9 when CSYNC is input.

Item	Symbol	S1 RIN GIN BIN	S2 SCIN	S3 NPIN	S4 SYNC IN	S5 FO	Measurement point	Measurement Conditions	Min.	Typ.	Max.	Unit
(COUT & CVOUT)												
Burst level	V_O (BN1/2)	SG1 to SG3	SG4	5V	SG5	20k	A/C	SG1 to SG3: 100% color bar input, 1.0Vp-p (Max.) SG4: SIN wave, 3.58MHz 0.5Vp-p SG5: CSYNC TTL level Fig. 5	0.2	0.25	0.3	Vp-p
R chroma ratio	R/BN1/2								2.84	3.16	3.48	
R phase	$\theta_{R1/2}$								94	104	114	deg
G chroma ratio	G/BN1/2								2.65	2.95	3.25	
G phase	$\theta_{G1/2}$								231	241	251	deg
B chroma ratio	B/BN1/2								2.01	2.24	2.47	
B phase	$\theta_{B1/2}$								337	347	357	deg
Burst width	t_W (B) 1/2								2.5	2.75	3.2	µs
Burst position	t_D (B) 1/2								0.4	0.6	0.75	µs
Carrier leak	$V_{L1/2}$	SG1 to SG3	SG4	5V	SG5	20k		SG1 to SG3: No signal, SG4: SIN wave, 3.58MHz 0.5Vp-p SG5: CSYNC TTL level 3.58MHz component measured. Fig. 6			20	mVp-p
PAL burst level ratio	K (BP1/2)	SG1 to SG3	SG4	GND	SG5	16k		SG1 to SG3: No signal, SG4: SIN wave, 4.43MHz 0.5Vp-p SG5: CSYNC TTL level Fig. 6	0.9	1.0	1.1	
PAL burst phase	$\theta_{PAL1/2}$								125	135	145	deg
	$\theta_{\overline{PAL1/2}}$								215	225	235	

* Clamp voltage: voltage appearing at Pin 9 when CSYNC is input.

Electrical Characteristics Measurement Circuit



Measuring Signals and Output Waveforms

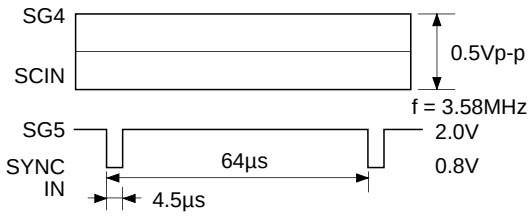


Fig. 1

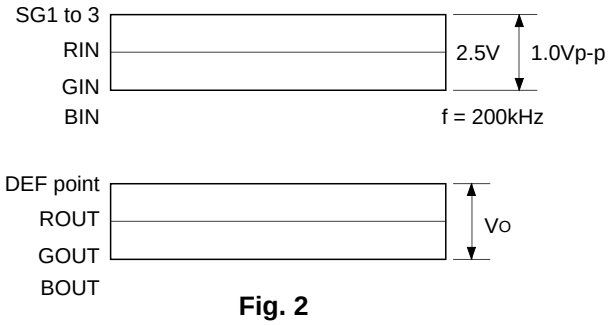


Fig. 2

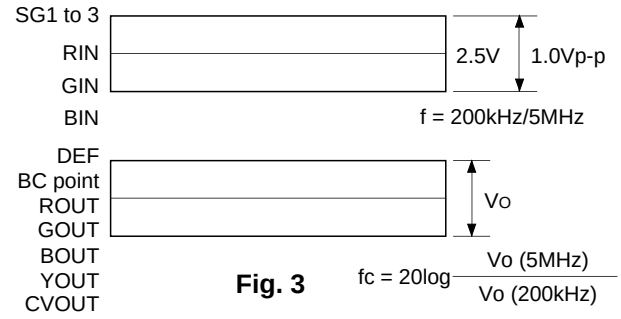


Fig. 3

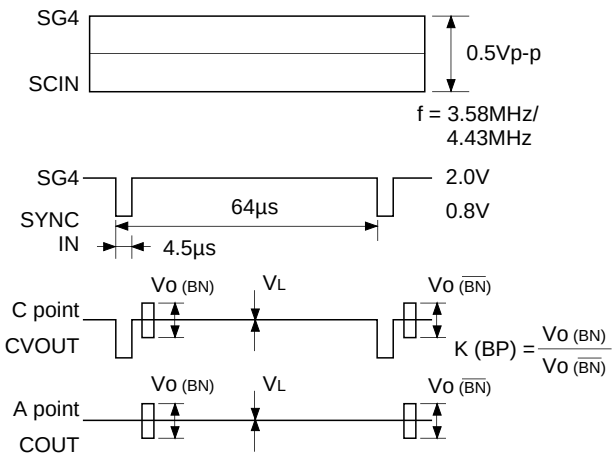


Fig. 6

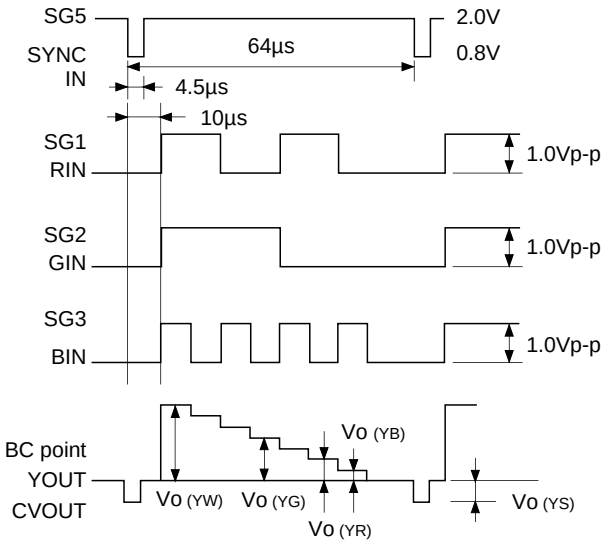


Fig. 4

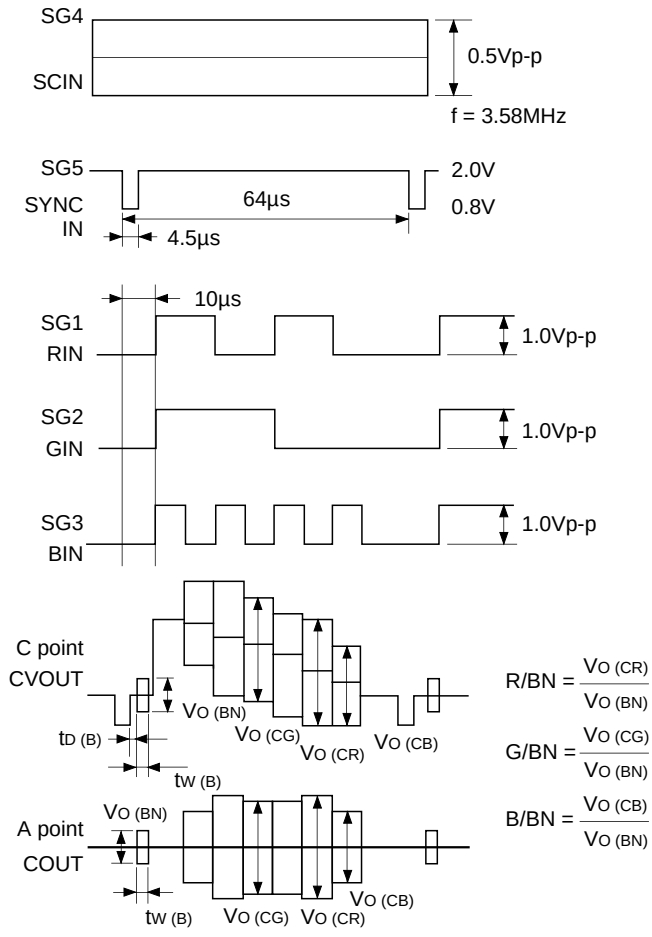
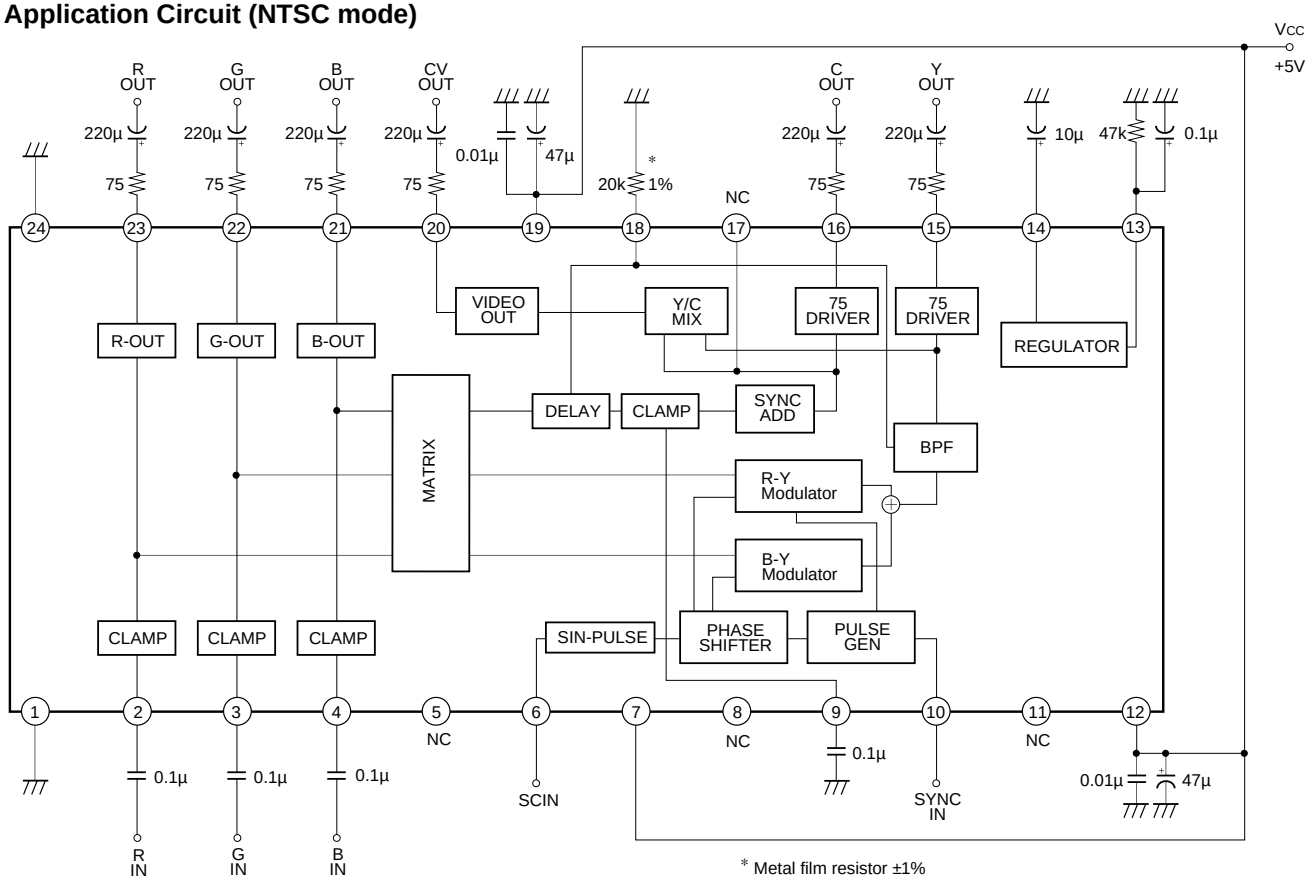


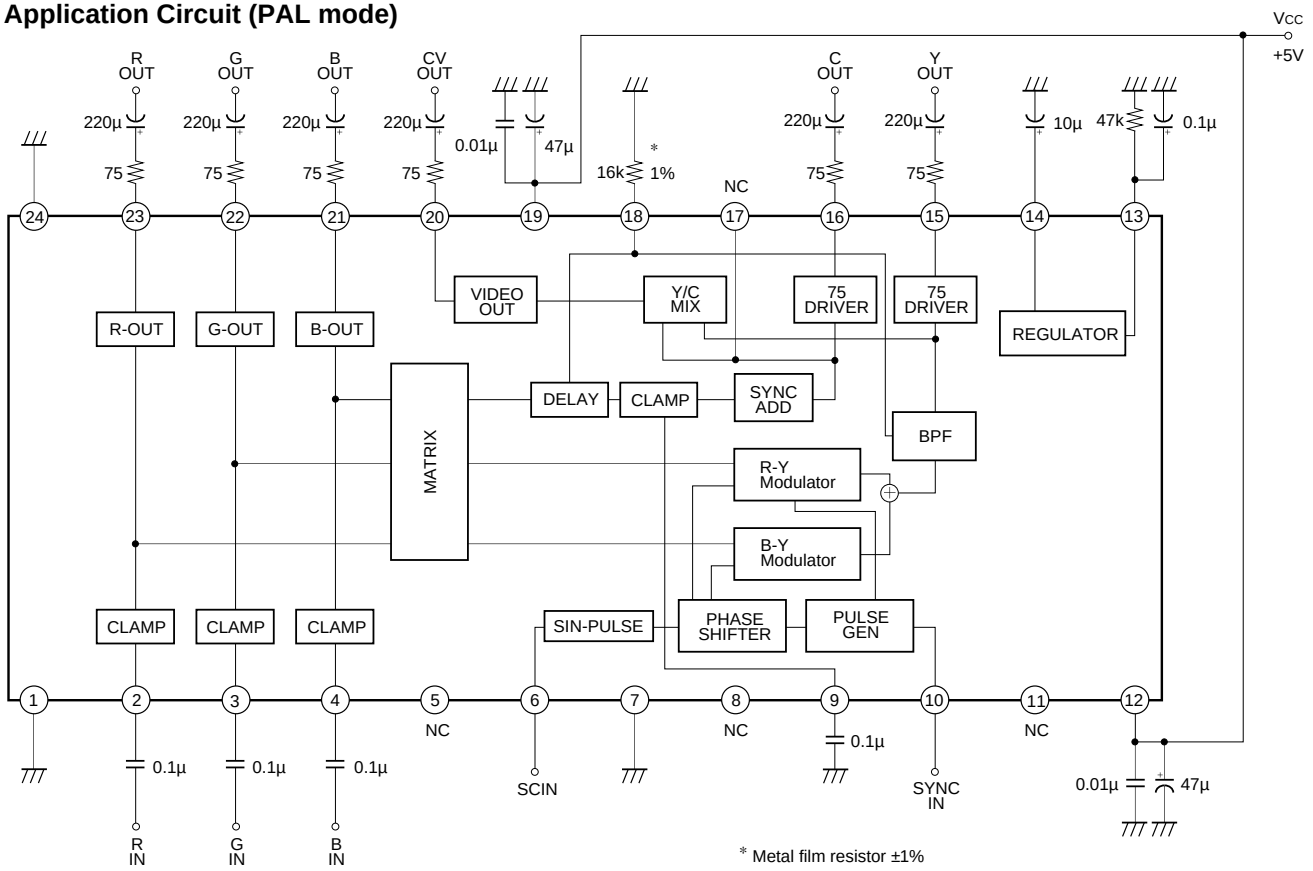
Fig. 5

Application Circuit (NTSC mode)



* Metal film resistor ±1%

Application Circuit (PAL mode)



* Metal film resistor ±1%

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

Analog RGB signals input from Pins 2, 3 and 4 are clamped in the clamping circuit and output from Pins 23, 22 and 21, respectively.

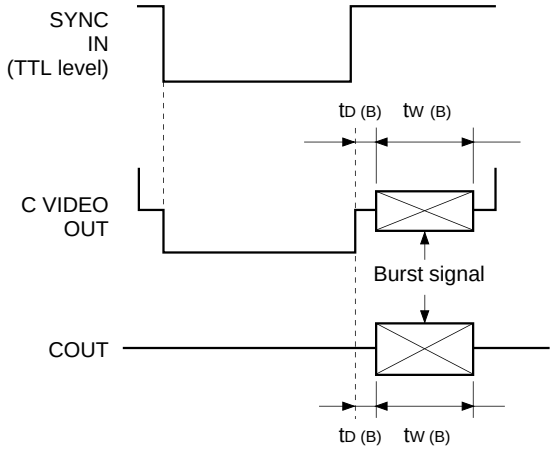
The matrix circuit performs operations on each input signal, generating luminance signal Y and color difference signals R-Y and B-Y. The Y signal enters the delay line to adjust delay time with the color signal C. Then, after addition of the CSYNC signal input from Pin 10, the Y signal is output from Pin 16.

A subcarrier input from Pin 6 is input to the phase shifter, where its phase is sfited 90°. Then, the subcarrier is input to the modulators and modulated by the R-Y signal and the B-Y signal. Modulated subcarriers are mixed, sent to the band pass filter to eliminate higher harmonic components and finally output from Pin 15 as the C signal. At the same time, Y and C signals are mixed and output from Pin 20 as the composite video signal.

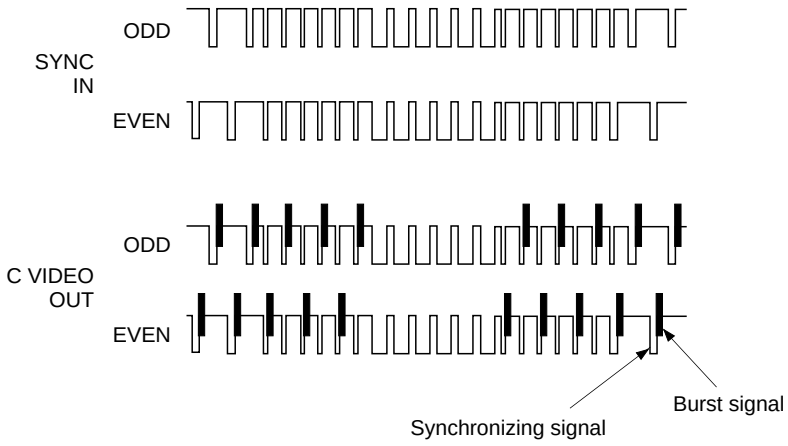
Burst Signal

The CXA1645P/M generates burst signals at the timing shown below according to the composite sync signal input.

H synchronization



V synchronization



Notes on Operation

Be careful of the following when using the CXA1645P/M.

1. This IC is designed for image processing of personal computers and video games. When using the IC in other video devices, make thorough investigations on image quality.

2. Be sure that analog RGB signals are input at 1.0Vp-p maximum and have low enough impedance. High impedance may affect color saturation, hue, etc. Inputting RGB signals in excess of 1.3Vp-p may disable the clamp operation.

3. The SC input (Pin 6) can be either a sine wave or a pulse in the range from 0.4 to 5.0Vp-p.
   However, when a pulse is input, its phase may be shifted several degrees from that of the sine wave input. In the IC, the SC input is biased to 1/2 V_{CC}. Accordingly, when a 5.0Vp-p pulse is input and the duty factor deviates from 50%, High- and Low-level pulse voltages may exceed V_{CC} and GND in the IC, which causes subcarrier distortion. In such a case, be very careful that the duty factor keeps to 50%.

4. When designing a printed circuit board pattern, pay careful attention to the routing of the V_{CC} and GND leads. To decouple the V_{CC} and V_{REF} pins, use tantalum, ceramic or other capacitors with good frequency characteristics. Ground the capacitors by connections shown below as closely to each IC pin as possible. Try to design the leads as short and wide as possible.

$V_{CC}1$, V_{REF}	... GND1
$V_{CC}2$	... GND2

   Design the pattern so that V_{CC} (or V_{REF}) is connected to GND via a capacitor at the shortest distance.

5. SC and SYNC input pulses
   Attach a resistor and a capacitor to eliminate high-frequency components of SC (Figure A) and SYNC (Figure B) before input.

Fig. A

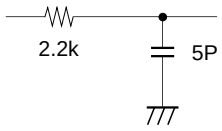
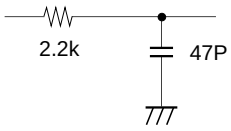


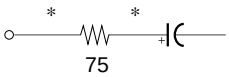
Fig. B



   Be careful not to input pulses containing high-frequency components. Otherwise, high-frequency components may flow into V_{CC}, GND and peripheral parts, resulting in malfunctions.

6. Connecting an external resistor to the 75Ω driver output pin
   A capacitance of several dozen picofarads at each pin may start oscillation. To prevent oscillation, design the pattern so that a 75Ω resistor is mounted near the pin (see Figure C).

Fig. C



* Make these leads short.

   When any of the 75Ω driver output pins is not in use, leave it unconnected and design the pattern so that no parasitic capacitance is generated on the printed circuit board.

7. V_{REF} pin (Pin 14)

   Do not connect this pin to an external load that might cause AC signals to flow, which will cause IC malfunctions. When connecting a DC load, make sure that the current flowing from this pin is kept below 2mA.

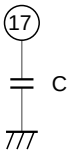
8. YTRAP pin (Pin 17)

   There are the following two means of reducing cross color generated by subcarrier frequency components contained in the Y signal.

(1) Install a capacitor of 30 to 68pF between YTRAP and GND. Decide the capacitance by conducting image evaluation, etc., giving consideration to both cross color and resolution.

Relations between capacitance and image quality are as follows:

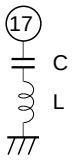
Capacitance	30pF ⟷ 68pF
Cross color Resolution	Large ⟷ Small High ⟷ Low



(2) Connect a capacitor C and an inductor L in series between YTRAP and GND. When the subcarrier frequency is fo, the values C and L are determined by the equation $fo = \frac{1}{2\pi\sqrt{LC}}$. Decide the values in image evaluation, etc., giving consideration to both cross color and resolution.

Relations between inductor values and image quality are as follows:

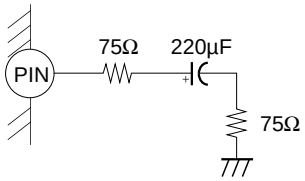
Inductor value	Small ⟷ Large
Cross color Resolution	Large ⟷ Small High ⟷ Low



For instance, L = 68µH and C = 28pF are recommended for NTSC. It is necessary to select an inductor L with a sufficiently small DC resistance. Method (2) is more useful for achieving a higher resoluation than method (1). When an even higher resolution is necessary, use of the S terminal (YOUT and COUT) is recommended.

9. Driving COUT (Pin 15), YOUT (Pin 16), CVOUT (Pin 20), and B.G.R OUT (Pins 21, 22 and 23) outputs

   In Pin Description, "Capable of driving a 75Ω load" means that the pin can drive a capacitor +75Ω +75Ω load shown in the figure below. In other words, the pin is capable of driving a 150Ω load in AC.



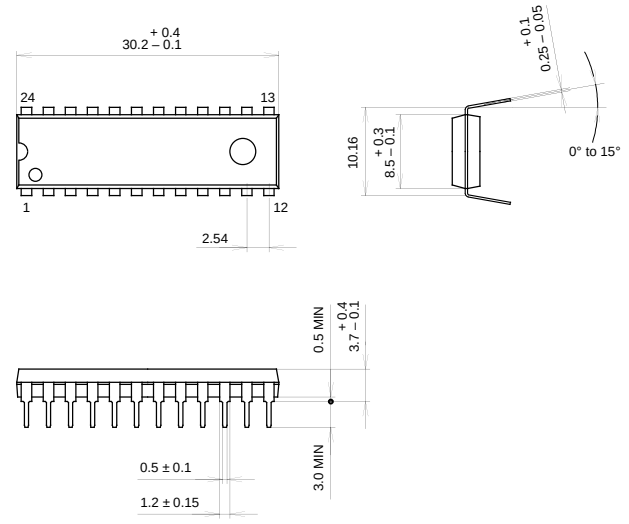
   Keep in mind that the pin is incapable of driving a 150Ω load in DC load in DC direct coupling.

10. This IC employs a number of 75Ω driver pins, so oscillation is likely to occur when measures described in Nos. 4 and 6 are not taken thoroughly. Be very careful of oscillation in printed circuit board design and carry out thorough investigations in the actual driving condition.

Package Outline Unit: mm

CXA1645P

24PIN DIP (PLASTIC) 400mil



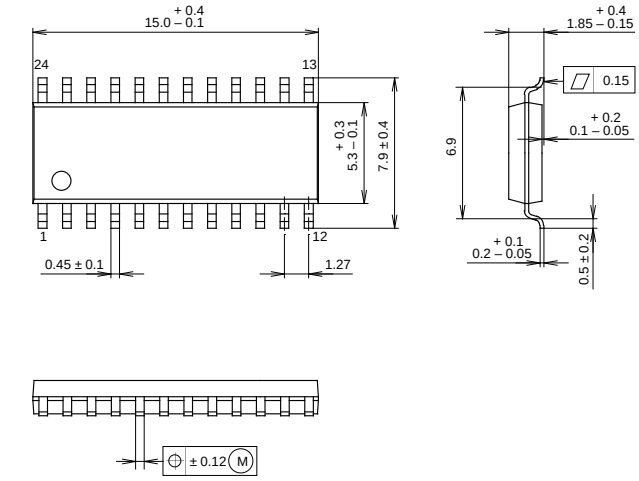
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	2.0g

SONY CODE	DIP-24P-01
EIAJ CODE	*DIP024-P-0400-A
JEDEC CODE	

CXA1645M

24PIN SOP (PLASTIC)



PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY / 42ALLOY
PACKAGE WEIGHT	0.3g

SONY CODE	SOP-24P-L01
EIAJ CODE	*SOP024-P-0300-A
JEDEC CODE	