CIRRUS LOGIC®

CS8416

192 kHz Digital Audio Interface Receiver

Features

- Complete EIAJ CP1201, IEC-60958, AES3, S/PDIF compatible receiver
- +3.3V Analog Supply (VA)
- +3.3V Digital Supply (VD)
- +3.3V to +5.0V Digital Interface Supply (VL)
- 8:2 S/PDIF Input MUX
- AES/SPDIF input pins selectable in hardware mode
- 3 General Purpose Outputs (GPO) allow signal routing
- Selectable signal routing to GPO pins
- S/PDIF to TX inputs selectable in hardware mode
- Flexible 3-wire serial digital output port
- 32 kHz to 192 kHz sample frequency range
- Low jitter clock recovery
- Pin and microcontroller read access to Channel Status and User data
- SPI or I^2C control port Software Mode and standalone Hardware Mode
- Differential cable receiver
- On-chip Channel Status data buffer memories
- Auto-detection of compressed audio input streams
- Decodes CD Q sub-code
- OMCK System Clock Mode

General Description

The CS8416 is a monolithic CMOS device which receives and decodes one of 8 channels of audio data according to the IEC60958, S/PDIF, EIAJ CP1201, or AES3 interface standards. The CS8416 has a serial digital audio output port and comprehensive control ability through a selectable control port in Software Mode or through selectable pins in Hardware Mode. Channel status data are assembled in buffers, making read access easy. GPO pins may be assigned to route a variety of signals to output pins

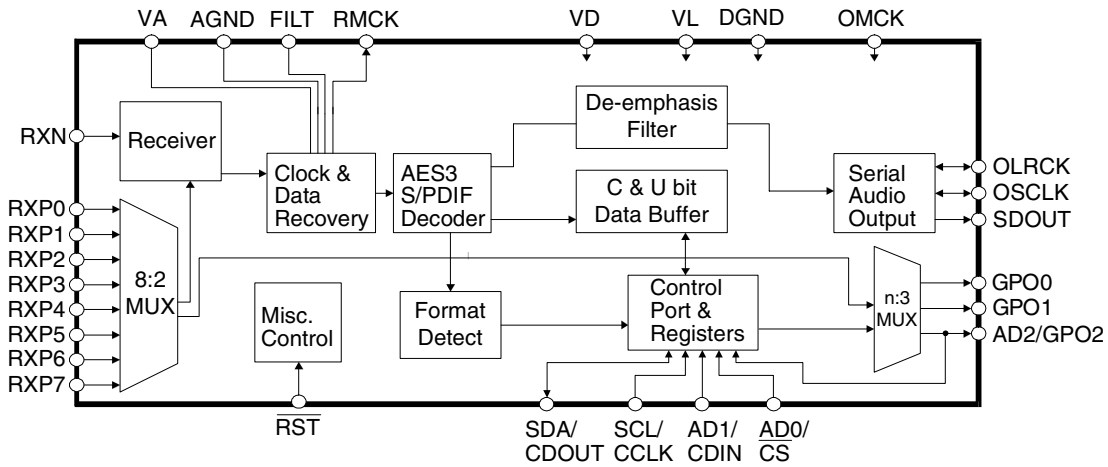
A low jitter clock recovery mechanism yields a very clean recovered clock from the incoming AES3 stream.

Stand-alone operation allows systems with no microcontroller to operate the CS8416 with dedicated output pins for channel status data.

Target applications include A/V receivers, CD-R, DVD receivers, multimedia speakers, digital mixing consoles, effects processors, set-top boxes, and computer and automotive audio systems.

ORDERING INFORMATION

CS8416-CS	28-pin SOIC	-10 to +70°C
CS8416-CZ	28-pin TSSOP	-10 to +70°C
CS8416-IS	28-pin SOIC	-40 to +85°C
CS8416-IZ	28-pin TSSOP	-40 to +85°C
CDB8416	Evaluation Board	



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find one nearest you go to www.cirrus.com

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1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V)

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Voltage		VA VD VL	3.13 3.13 3.13	3.3 3.3 3.3 or 5.0	3.46 3.46 5.25	V V V
Ambient Operating Temperature:	'-CS' & '-CZ' '-IS' & '-IZ'	T_A	-10 -40	- -	+70 +85	°C

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V; all voltages with respect to 0V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameter		Symbol	Min	Max	Units
Power Supply Voltage		VA, VD,VL	-	6.0	V
Input Current, Any Pin Except Supplies	(Note 1)	I_{in}	-	±10	mA
Input Voltage		V_{in}	-0.3	(VL) + 0.3	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

DC ELECTRICAL CHARACTERISTICS (AGND = DGND = 0 V; all voltages with respect to 0 V.)

Parameters		Symbol	Min	Typ	Max	Units
Power-down Mode (Note 2), (Note 4)						
Supply Current in power down	VA	IA	-	10	-	µA
	VD	ID	-	70	-	µA
	VL = 3.3 V	IL	-	10	-	µA
	VL = 5.0 V	IL	-	12	-	µA
Normal Operation (Note 3), (Note 4)						
Supply Current at 48 kHz frame rate	VA	IA	-	5.7	-	mA
	VD	ID	-	5.9	-	mA
	VL = 3.3 V	IL	-	2.8	-	mA
	VL = 5.0 V	IL	-	4.2	-	mA
Supply Current at 192 kHz frame rate	VA	IA	-	9.4	-	mA
	VD	ID	-	23	-	mA
	VL = 3.3 V	IL	-	7.8	-	mA
	VL = 5.0 V	IL	-	11.8	-	mA

Notes: 2. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

3. Normal operation is defined as $\overline{RST}$ = HI.

4. Assumes that no digital inputs are left floating. It is recommended that all digital inputs be driven high or low at all times.

DIGITAL INPUT CHARACTERISTICS (AGND = DGND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{IN}	-	-	±0.5	µA
Differential Input Sensitivity, RXP[7:0] to RXN	V_{TH}	-	150	200	mVpp
Input Hysteresis	V_H	0.15	-	1.0	V

DIGITAL INTERFACE SPECIFICATIONS (AGND = DGND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Max	Units
High-Level Output Voltage (I_{OH} = -3.2 mA)	V_{OH}	(VL) - 1.0	-	V
Low-Level Output Voltage (I_{OL} = 3.2 mA)	V_{OL}	-	0.5	V
High-Level Input Voltage, except RXP[7:0], RXN	V_{IH}	2.0	(VL) + 0.3	V
Low-Level Input Voltage, except RXP[7:0], RXN	V_{IL}	-0.3	0.8	V

SWITCHING CHARACTERISTICS (Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{RST}$ Pin Low Pulse Width		200	-	-	µS
PLL Clock Recovery Sample Rate Range		30	-	200	kHz
RMCK Output Jitter (Note 5)		-	200	-	ps RMS
RMCK Output Duty-Cycle		45	50	55	%

Notes: 5. Typical RMS cycle-to-cycle jitter.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORTS

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
OSCLK/OLRCK Active Edge to SDOUT Output Valid	(Note 6)	t_{dpd}	-	-	23	ns
Master Mode						
RMCK to OSCLK active edge delay	(Note 6)	t_{smd}	0	-	12	ns
RMCK to OLRCK delay	(Note 7)	t_{lmd}	0	-	12	ns
OSCLK and OLRCK Duty Cycle			-	50	-	%
Slave Mode						
OSCLK Period		t_{sckw}	36	-	-	ns
OSCLK Input Low Width		t_{sckl}	14	-	-	ns
OSCLK Input High Width		t_{sckh}	14	-	-	ns
OSCLK Active Edge to OLRCK Edge	(Notes 6,7,8)	t_{lrckd}	10	-	-	ns
OSCLK Edge Setup Before OSCLK Active-Edge	(Notes 6,7,9)	t_{lrcks}	10	-	-	ns

Notes: 6. In Software mode the active edges of OSCLK are programmable.

7. In Software mode the polarity of OLRCK is programmable.

8. This delay is to prevent the previous OSCLK edge from being interpreted as the first one after OLRCK has changed.

9. This setup time ensures that this OSCLK edge is interpreted as the first one after OLRCK has changed.

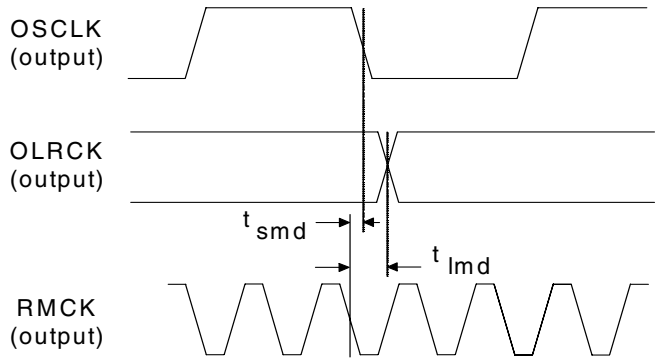


Figure 1. Audio Port Master Mode Timing

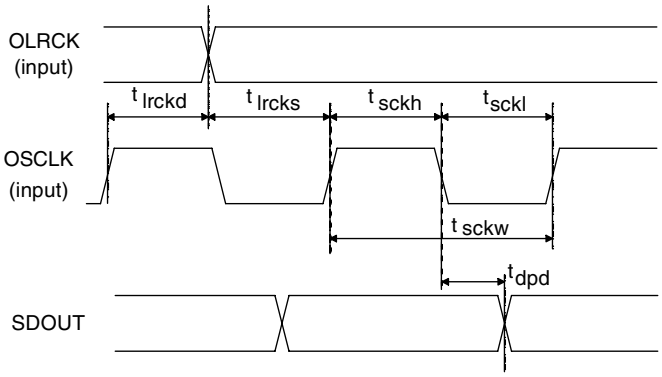


Figure 2. Audio Port Slave Mode and Data Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency	(Note 10)	f_{sck}	0	6.0	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 11)	t_{dh}	15	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	50	ns
Rise Time of CDOUT		t_{r1}	-	25	ns
Fall Time of CDOUT		t_{f1}	-	25	ns
Rise Time of CCLK and CDIN	(Note 12)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 12)	t_{r2}	-	100	ns

Notes: 10. If Fs is lower than 46.875 kHz, the maximum CCLK frequency should be less than 128 Fs. This is dictated by the timing requirements necessary to access the Channel Status memory. Access to the control register file can be carried out at the full 6 MHz rate. The minimum allowable input sample rate is 32 kHz, so choosing CCLK to be less than or equal to 4.1 MHz should be safe for all possible conditions.

11. Data must be held for sufficient time to bridge the transition time of CCLK.

12. For f_{sck} <1 MHz.

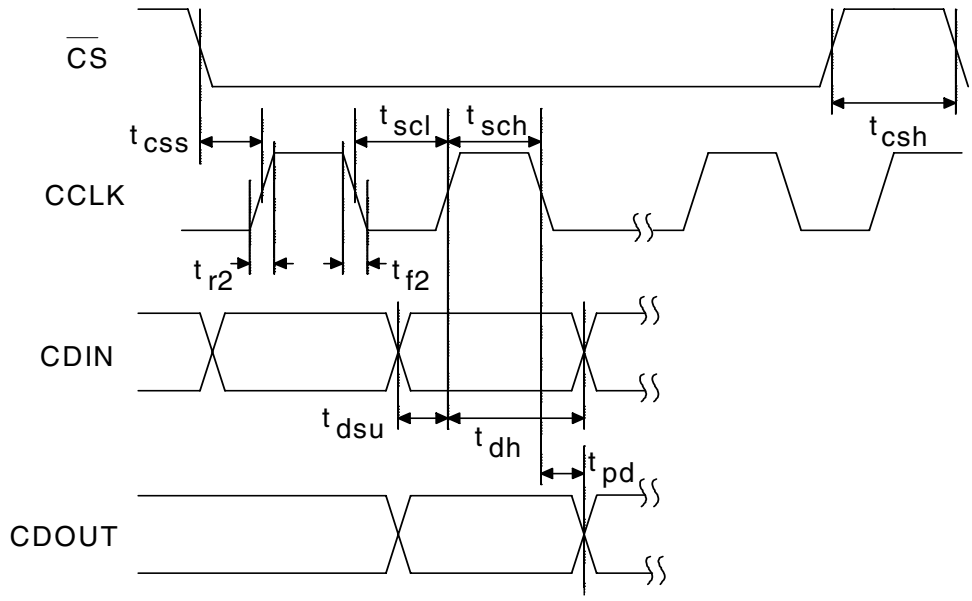


Figure 3. SPI Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT- I²C FORMAT

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 13)	t_{hdd}	10	-	ns
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_r	-	25	ns
Fall Time SCL and SDA	t_f	-	25	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

Notes: 13. Data must be held for sufficient time to bridge the 25 ns transition time of SCL.

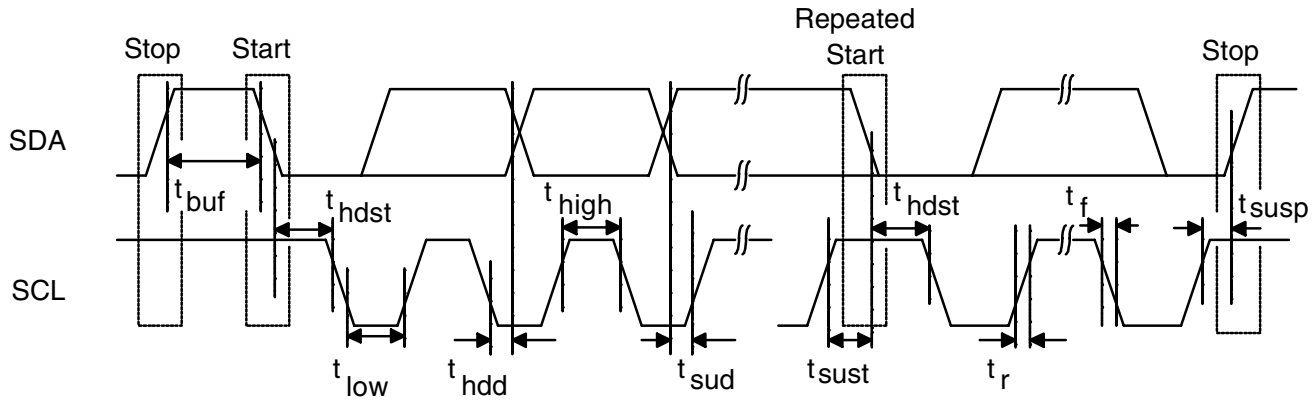
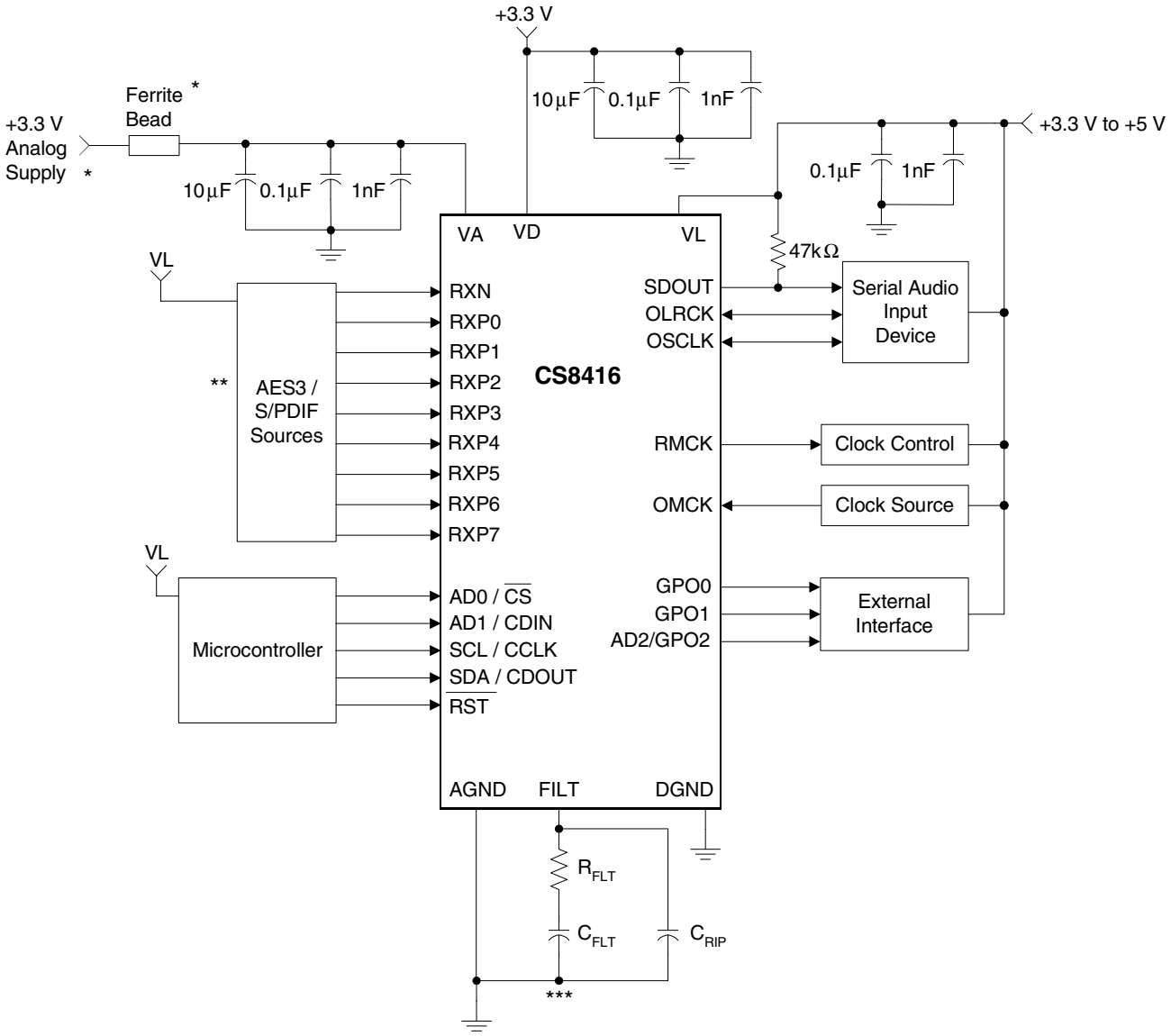


Figure 4. I²C Mode Timing

2. TYPICAL CONNECTION DIAGRAMS

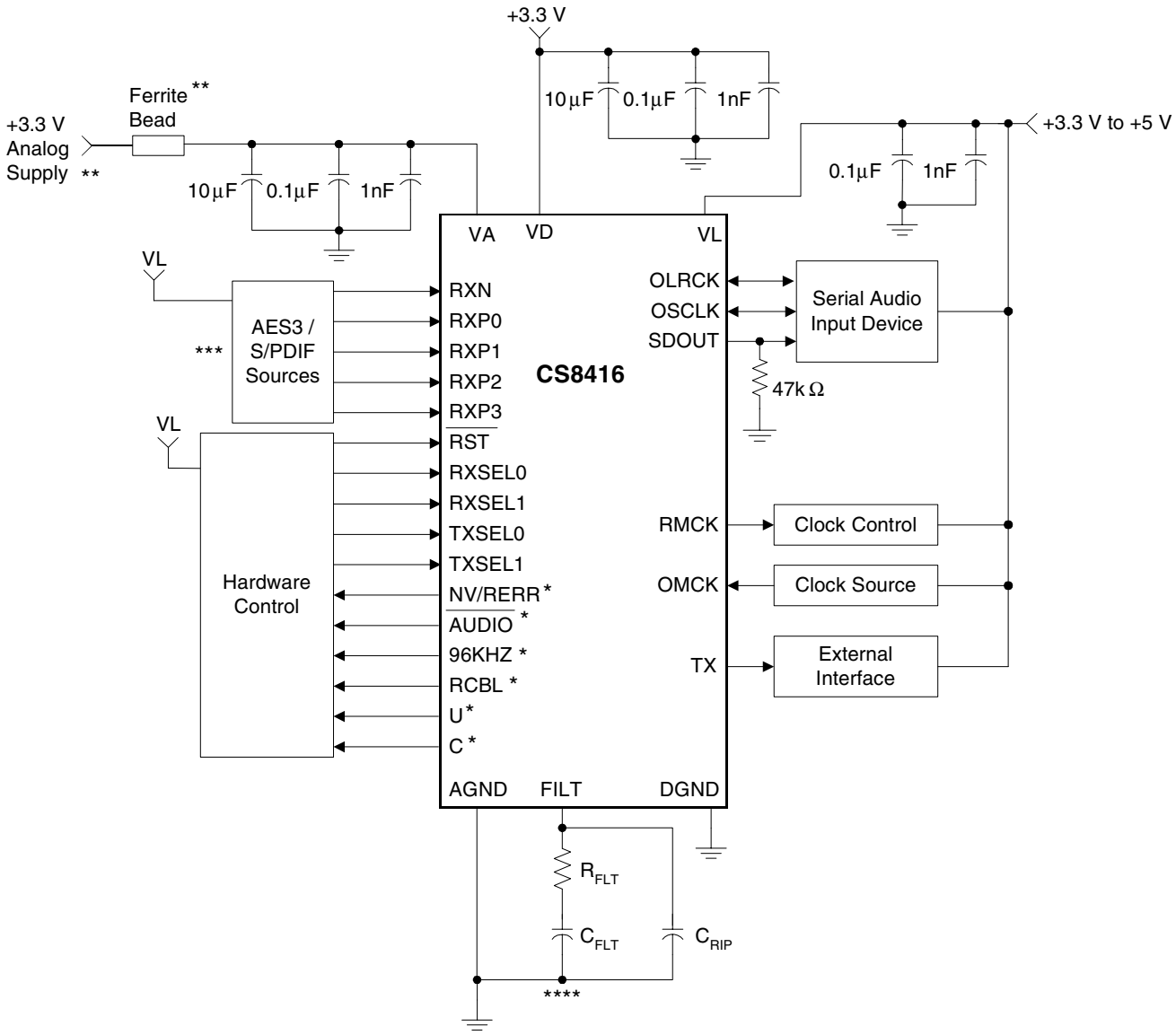


*** A separate analog supply is only necessary in applications where RMCK is used for a jitter sensitive task. For applications where RMCK is not used for a jitter sensitive task, connect VA to VD via a ferrite bead. Keep decoupling capacitors between VA and AGND.**

**** See "S/PDIF Receiver" on page 17 and "Appendix A: External AES3/SPDIF/IEC60958 Receiver Components" on page 47 for typical input configurations and recommended input circuits.**

***** For best jitter performance connect the filter ground directly to the AGND pin. See Table 6 on page 52 for PLL filter values.**

Figure 5. Typical Connection Diagram - Software Mode



*** These pins must be pulled high to VL or low to DGND through a 47 kΩ resistor.**

**** A separate analog supply is only necessary in applications where RMCK is used for a jitter sensitive task. For applications where RMCK is not used for a jitter sensitive task, connect VA to VD via a ferrite bead. Keep de-coupling capacitors between VA and AGND.**

***** See "S/PDIF Receiver" on page 17 and "Appendix A: External AES3/SPDIF/IEC60958 Receiver Components" on page 47 for typical input configurations and recommended input circuits.**

****** For best jitter performance connect the filter ground directly to the AGND pin. See Table 6 on page 52 for PLL filter values.**

Figure 6. Typical Connection Diagram - Hardware Mode

3. GENERAL DESCRIPTION

The CS8416 is a monolithic CMOS device which receives and decodes audio data according to the AES3, IEC60958, S/PDIF, and EIAJ CP1201 interface standards.

The CS8416 utilizes an 8:2 multiplexer to select between eight inputs for decoding and to allow an input signal to be routed to an output of the CS8416. Input data is either differential or single-ended. A low jitter clock is recovered from the incoming data using a PLL. The decoded audio data is output through a configurable, 3-wire serial audio output port. The channel status and Q-channel subcode portion of the user data are assembled in registers and may be accessed through an SPI or I^2C port.

Three General Purpose Output (GPO) pins are provided to allow a variety of signals to be accessed under software control. In hardware mode, dedicated pins are used to select audio stream inputs for decoding and transmission to a dedicated TX pin. Hardware mode also allows direct access to channel status and user data output pins.

Figure 5 and Figure 6 show the power supply and external connections to the CS8416 when configured for software and hardware modes. Please note that all I/O pins, including RXN and RXP[7:0], operate at the VL voltage.

3.1. AES3 and S/PDIF Standards Documents

This document assumes that the user is familiar with the AES3 and S/PDIF data formats. It is advisable to have current copies of the AES3, IEC60958, and IEC61937 specifications on hand for easy reference.

The latest AES3 standard is available from the Audio Engineering Society or ANSI at www.aes.org or at www.ansi.org. Obtain a copy of the latest IEC60958/61937 standard from ANSI or from the International Electrotechnical Commission at www.iec.ch. The latest EIAJ CP-1201 standard is available from the Japanese Electronics Bureau.

Application Note 22: *Overview of Digital Audio Interface Data Structures* contains a useful tutorial on digital audio specifications, but it should not be considered a substitute for the standards.

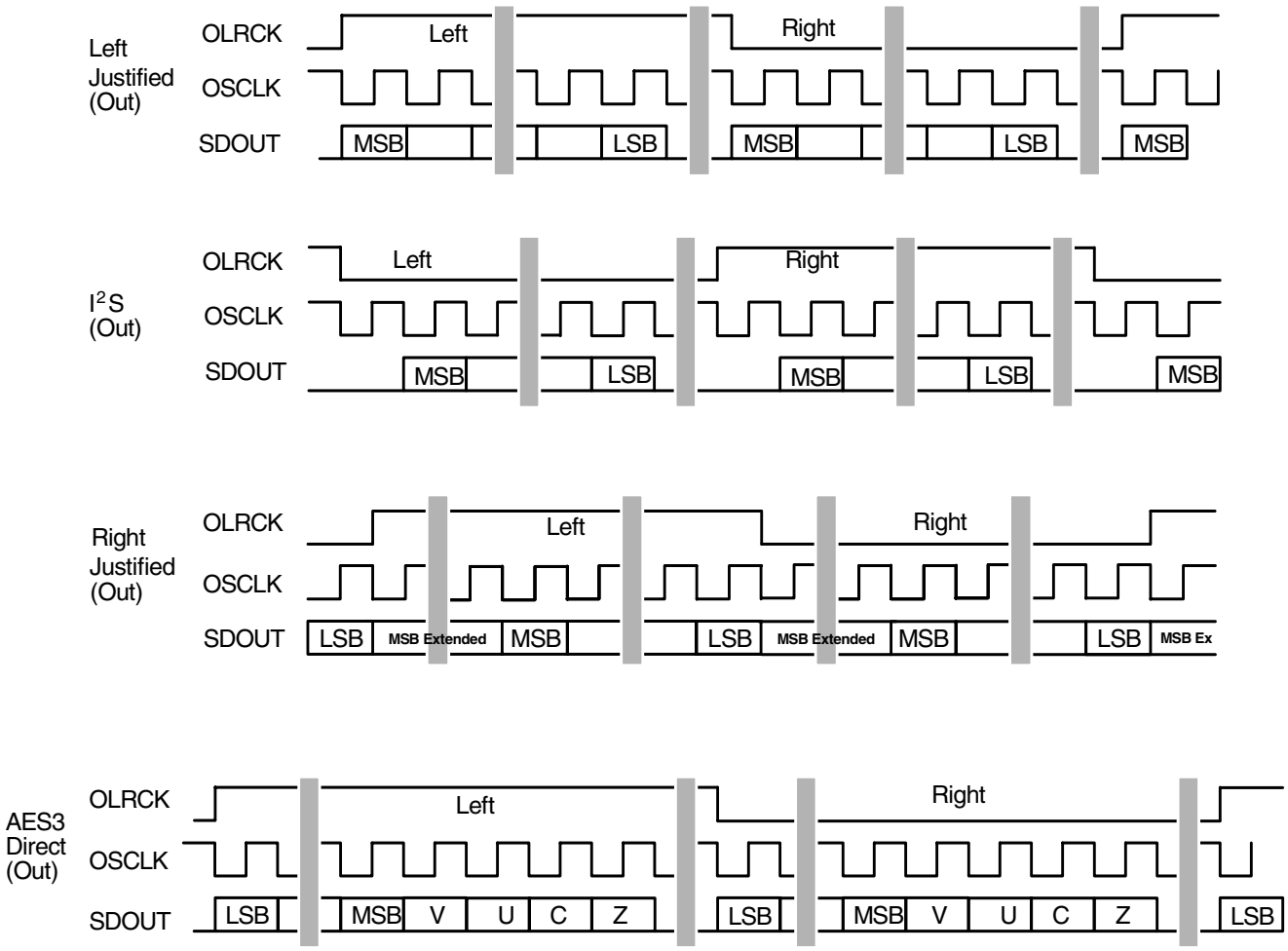
The paper *An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission*, by Clifton Sanchez, is an excellent tutorial on SCMS. It is available from the AES as reprint 3518.

4. SERIAL AUDIO OUTPUT PORT

A 3-wire serial audio output port is provided. The port can be adjusted to suit the attached device setting the control registers. The following parameters are adjustable: master or slave, serial clock frequency, audio data resolution, left or right justification of the data relative to left/right clock, optional one-bit cell delay of the first data bit, the polarity of the bit clock, and the polarity of the left/right clock. By setting the appropriate control bits, many formats are possible.

Figure 7 shows a selection of common output formats, along with the control bit settings. A special AES3 direct output format is included, which allows the serial output port access to the V, U, and C bits embedded in the serial audio data stream. The P bit, which would normally be a parity bit, is replaced by a Z bit, which is used to indicate the start of each block. The received channel status block start signal is also available as the RCBL pin in hardware mode and through a GPO pin in software mode.

In master mode, the left/right clock (OLRCK) and the serial bit clock (OSCLK) are outputs, derived from the recovered RMCK clock. In slave mode, OLRCK and OSCLK are inputs. OLRCK is normally synchronous to the appropriate master clock, but OSCLK can be asynchronous and discontinuous if required. By appropriate phasing of OLRCK and control of the serial clocks, multiple CS8416's can share one serial port. OLRCK should be continuous, but the duty cycle can be less than the specified typical value of 50% if enough serial clocks are present in each phase to clock all the data bits. When in slave mode, the serial audio output port cannot be set for right-justified data. The CS8416 allows immediate mute of the serial audio output port audio data by the MUTESAO bit of Control Register 1.



	SOMS*	SOSF*	SORES[1:0]*	SOJUST*	SODEL*	SOSPOL*	SOLRPOL*
Left Justified	X	X	XX	0	0	0	0
I^2S	X	X	XX	0	1	0	1
Right Justified	1	X	XX	1	0	0	0
AES3 Direct	X	X	11	0	0	0	0

X = don't care to match format, but does need to be set to the desired setting

* See Serial Output Data Format Register Bit Descriptions for an explanation of the meaning of each bit

Figure 7. Serial Audio Output Example Formats

4.1. Slip/Repeat Behavior

When using the serial audio output port in slave mode with an OLRCK input that is asynchronous to the incoming AES3 data, the interrupt bit OSLIP (bit 5 in the Interrupt 1 Status register, 0Dh) is provided to indicate when repeated or dropped samples occur. Refer to Figure 8 for the AES3 data format diagram.

When the serial output port is configured as slave, depending on the relative frequency of OLRCK to the input AES3 data (Z/X) preamble frequency, the data will be slipped or repeated at the output of the CS8416.

After a fixed delay from the Z/X preamble (a few periods of the internal clock, which is running at 256Fs), the circuit will look back in time until the previous Z/X preamble and check which of the following conditions occurred:

1) If during that time, the internal data buffer was not updated, then a slip has occurred. Data from the previous frame will be output and OSLIP will be set to 1. Due to the OSLIP bit being “sticky,” it will remain 1 until the register is read. It will then be reset until another slip/repeat condition occurs.
2) If during that time the internal data buffer did not update between two positive or negative edges (depending on OLRPOL) of OLRCK, then a repeat has occurred. In this case the buffer data was updated twice, so the part has lost one frame of data. This event will also trigger OSLIP to be set to 1. Due to the OSLIP bit being “sticky,” it will remain 1 until the register is read. It will then be reset until another slip/repeat condition occurs.
3) If during that time, it did see a positive edge on OLRCK (or negative edge if the SOLRPOL is set to 1) then no slip or repeat has happened. Due to the OSLIP bit being “sticky,” it will remain in its previous state until either the register is read or a slip/repeat condition occurs.

If the user reads OSLIP as soon as the event triggers, over a long period of time the rate of occurring INT will be equal to the difference in frequency between the input AES data and the slave serial output LRCK. The CS8416 uses a hysteresis window when a slip/repeat event occurs. The slip/repeat is triggered when an edge of OLRCK passes a window size from the beginning of the Z/X preamble. Without the hysteresis window, jitter on OLRCK with a frequency very close to Fs could slip back and forth, causing multiple slip/repeat events. The CS8416 uses a hysteresis window to ensure that only one slip/repeat happens even with jitter on OLRCK.

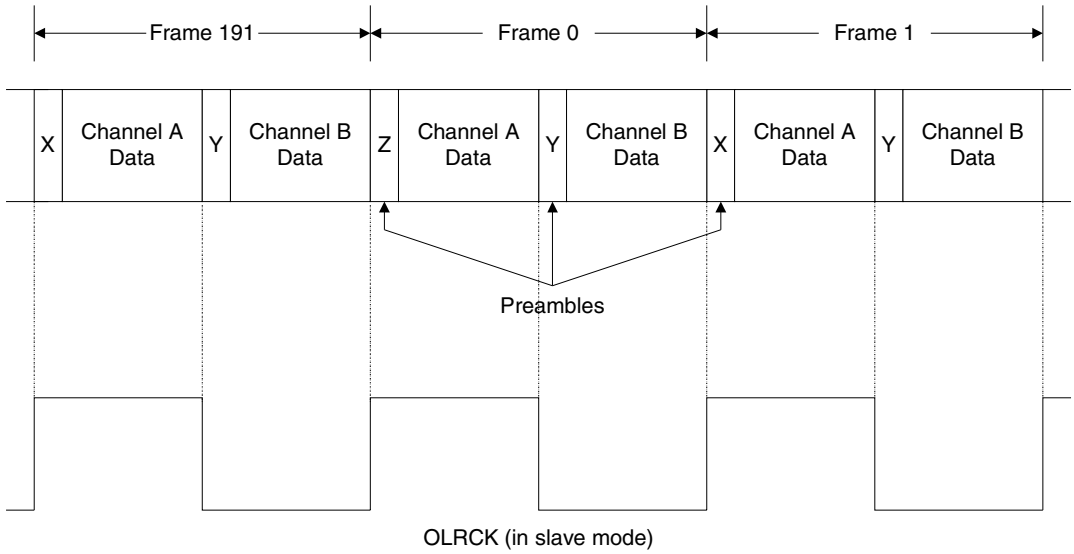


Figure 8. AES3 Data Format

4.2. AES11 Behavior

When OLRCK is configured as a master, the positive or negative edge of OLRCK (depending on the setting of SOLRPOL in register 05h) will be within -1.0%(1/Fs) to 1.1%(1/Fs) from the start of the preamble X/Z. In master mode, the latency through the part is dependent on the input sample frequency. The delay through the part from the beginning of the preamble to the active edge of OLRCK for the various sample frequencies is given in Table 1 In master mode without the de-emphasis filter engaged, the latency of the audio data will be 3 frames.

Fs (kHz)	Delay (ns)
32	96.6
44.1	78.6
48	74.6
64	60.6
96	50.6
192	TBD

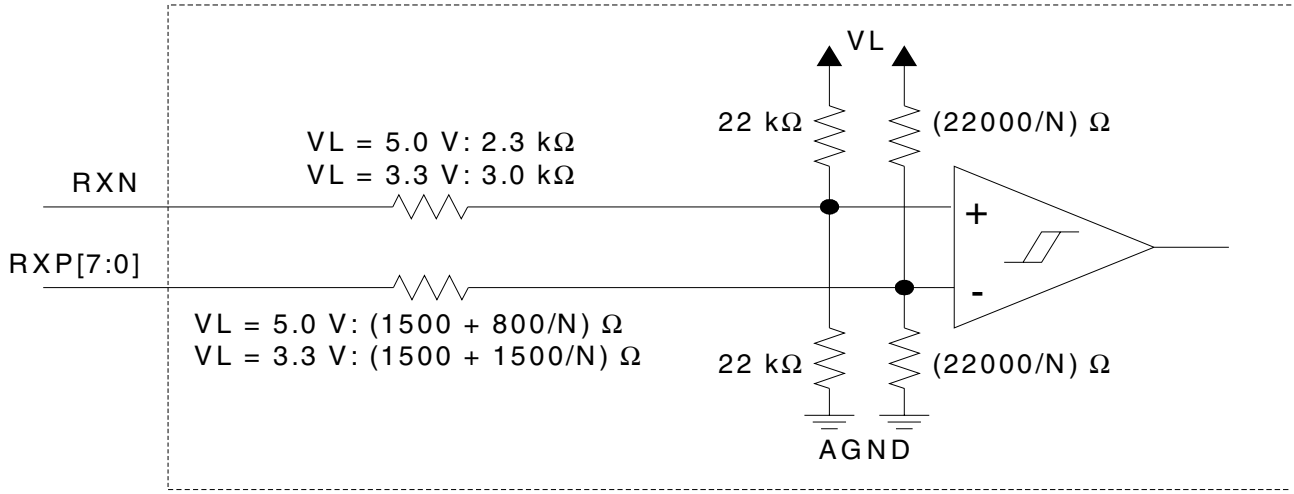
Table 1. Delays by Frequency Values

When OLRCK is configured as a slave any synchronized input within +/-28%(1/Fs) from the positive or negative edge of OLRCK (depending on the setting of SOLRPOL in register 05h) will be treated as being sampled at the same time. Since the CS8416 has no control of the OLRCK in slave mode, the latency of the data through the part will be a multiple of 1/Fs plus the delay between OLRCK and the preambles.

Both of these conditions are within the tolerance range set forth in the AES11 standard.

5. S/PDIF RECEIVER

The CS8416 includes an AES3/SPDIF digital audio receiver. The receiver accepts and decodes bi-phase encoded audio and digital data according to the AES3, IEC60958 (S/PDIF), and EIAJ CP-1201 interface standards. The receiver consists of an analog differential input stage, driven through analog input pins RXP0 to RXP7 and a common RXN, a PLL based clock recovery circuit, and a decoder which separates the audio data from the channel status and user data. External components are used to terminate the incoming data cables and isolate the CS8416. These components are detailed in "Appendix A: External AES3/SPDIF/IEC60958 Receiver Components" on page 47. Figure 9 shows the input structure of the receiver.



If RXP[7:0] is selected by either the receiver MUX or the TX passthrough MUX, N=1.
If RXP[7:0] is selected by both the receiver MUX and the TX passthrough MUX, N=2.
If RXP[7:0] is not selected at all, N=0 (i.e. high impedance).

Figure 9. Receiver Input Structure

5.1. 8:2 S/PDIF Input Multiplexer

5.1.1. General

The CS8416 employs a 8:2 S/PDIF input multiplexer to accommodate up to eight channels of input digital audio data. Digital audio data may be single-ended or differential. Differential inputs utilize RXP[7:0] and a shared RXN. Single ended signals are accommodated by using the RXP[7:0] inputs and AC coupling RXN to ground.

All active inputs to the CS8416 8:2 input multiplexer should be coupled through a capacitor as these inputs are biased at VL/2 when selected. These inputs are floating when not selected. Unused multiplexer inputs should be left floating or tied to AGND. The recommended capacitor value is 0.01 µF to 0.1 µF. The recommended dielectrics for the AC coupling capacitors are C0G or X7R.

The input voltage range for the input multiplexer is set by the I/O power supply pin, VL. The input voltage of the RXP[7:0] and RXN pins is also set by the level of VL. Input signals with voltage levels above VL or below DGND may degrade performance or damage the part.

5.1.2. Software Mode

The multiplexer select line control is accessed through bits RXSEL[2:0] in control port register 04h. The multiplexer defaults to RXP0.

The second output of the input multiplexer is used to provide the selected input as a source to be output on a GPO pin. This pass through signal is selected by TXSEL[2:0] in control port register 04h. This single-ended signal is resolved to full-rail, but is not de-jittered before it is output.

5.1.3. Hardware Mode

In hardware mode the input to the decoder is selected by dedicated pins, RXSEL[1:0].

The pass through signal is selected by dedicated pins, TXSEL[1:0] for output on the dedicated TX pin. This single-ended signal is resolved to full-rail, but is not de-jittered before it is output.

Selectable inputs are restricted to RXP0 to RXP3 for both the receiver and the TX output pin. These inputs are selected by RXSEL[1:0] and TXSEL[1:0] respectively.

5.2. OMCK System Clock Mode

A special clock switching mode is available that allows the OMCK clock input to automatically replace RMCK when the PLL becomes unlocked. This is accomplished without spurious transitions or glitches on RMCK. In Hardware mode this feature is enabled by a transition (rising edge active) on the OMCK pin after reset. Therefore to not enable the clock switching feature in Hardware mode, OMCK should be tied to DGND or VL. However, in Hardware mode, once the clock switching feature has been enabled, it can only be disabled by resetting the part. In Software mode the automatic clock switching feature is enabled by setting SWCLK bit in Control1 register to a “1”. Additionally in Software mode, OMCK can be manually set to output on RMCK by using the FSWCLK bit in the Control0 register.

When the clock switching feature is enabled, OSCLK and OLRCK are derived from the OMCK input when the clock has been switched and the serial port is in master mode. When clock switching is enabled and the PLL is not locked, OLRCK will be OMCK/256 and OSCLK will be OMCK/4. When the PLL loses lock, the frequency of the VCO drops to ~500 kHz. When this system clock mode is not enabled, the OSCLK and OLRCK will be based on the VCO when the PLL is not locked. Table 2 shows an example of output clocks based on clock switching being enabled or disabled.

Clock Switching Enabled/Disabled	PLL Locked/Unlocked	RMCK Clock Ratio	RMCK	OSCLK	OLRCK
Disabled	Locked	128*F_s	6.144 MHz	3.072 MHz	48 kHz
Enabled	Locked	128*F_s	6.144 MHz	3.072 MHz	48 kHz
Disabled	Unlocked	128*F_s	~250 kHz	~125 kHz	~1.95 kHz
Enabled	Unlocked	128*F_s	11.2896 MHz	2.8224 MHz	44.1 kHz
Disabled	Locked	256*F_s	12.288 MHz	3.072 MHz	48 kHz
Enabled	Locked	256*F_s	12.288 MHz	3.072 MHz	48 kHz
Disabled	Unlocked	256*F_s	~500 kHz	~125 kHz	~1.95 kHz
Enabled	Unlocked	256*F_s	11.2896 MHz	2.8224 MHz	44.1 kHz

Example with OMCK = 11.2896 MHz, the receiver input sample rate = 48 kHz, OSLCK = 64*F_s, and FSWCLK (Software mode only) = ‘0’.

Table 2. Clock Switching Output Clock Rates

5.3. PLL, Jitter Attenuation, and Clock Switching

Please see “Appendix C: PLL Filter” on page 50 for a general description of the PLL, selection of recommended PLL filter components, and layout considerations. Figure 5 and Figure 6 shows the recommended configuration of the two capacitors and one resistor that comprise the PLL filter.

6. GENERAL PURPOSE OUTPUTS

Three General Purpose Outputs (GPO) are provided to allow the equipment designer flexibility in configuring the CS8416. Fourteen signals are available to be routed to any of the GPO pins. The outputs of the GPO pins are set through the GPOxSEL[3:0] bits in the Control2 (02h) and Control3 (03h) registers. All GPO pins default to GND after reset.

GPO pins may be configured to provide the following data:

Function	Code	Definition
GND	0000	Fixed low level
$\overline{\text{EMPH}}$	0001	State of $\overline{\text{EMPH}}$ bit in the incoming data stream.
INT	0010	CS8416 interrupt output
C	0011	Channel status bit
U	0100	User data bit
RERR	0101	Receiver Error
NVERR	0110	Non-Validity Receiver Error
RCBL	0111	Receiver Channel Status Block
96KHZ	1000	If the input sample rate is ≤ 48 kHz, outputs a “0”. Outputs a “1” if the sample rate is ≥ 88.1 kHz. Otherwise the output is indeterminate.
$\overline{\text{AUDIO}}$	1001	Non-audio indicator for decoded input stream
VLRCK	1010	Virtual LRCK. Can be used to frame the C and U output data.
TX	1011	Pass through of AES/SPDIF input selected by TXSEL[2:0] in the Control 4 register (04h)
VDD	1100	VDD fixed high level
HRMCK	1101	F_S X 512 (Note 14)

Codes 1110 to 1111 - Reserved

Table 3. GPO Pin Configurations

Notes: 14. Frequency = 25 MHz Max, duty cycle not guaranteed, target duty cycle = 50% @ F_S = 48 kHz.

7. ERROR AND STATUS REPORTING

7.1. General

While decoding the incoming bi-phase encoded data stream, the CS8416 has the ability to identify various error conditions.

7.1.1. Software Mode

Software mode allows the most flexibility in reading errors. When unmasked, bits in the Receiver Error register (0Ch) indicate the following errors:

1) QCRC – CRC error in Q subcode data.
2) CCRC – CRC error in channel status data.
3) UNLOCK – PLL is not locked to incoming data stream.
4) V – Data Validity bit is set.
5) CONF – The logical OR of UNLOCK and BIP. The input data stream may be near error condition due to jitter degradation.
6) BIP – Biphase encoding error.
7) PAR – Parity error in incoming data.

The error bits are “sticky”, meaning that they are set on the first occurrence of the associated error and will remain set until the user reads the register through the control port. This enables the register to log all unmasked errors that occurred since the last time the register was read.

As a result of the bits “stickiness”, it is necessary to perform two reads on these registers to see if the error condition still exists.

The Receiver Error Mask register (06h) allows masking of individual errors. The bits in this register default to 00h and serve as masks for the corresponding bits of the Receiver Error register. If a mask bit is set to 1, the error is unmasked, which implies the following: its occurrence will be reported in the receiver error register, induce a pulse on RERR, invoke the occurrence of a RERR interrupt, and affect the current audio sample according to the status of the HOLD bits. The exceptions are the QCRC and CCRC errors, which do not affect the current audio sample, even if unmasked.

The HOLD bits allow a choice of:

- Holding the previous sample
- Replacing the current sample with zero (mute)

OR

- Not changing the current audio sample

7.1.2. Hardware Mode

In Hardware mode the user may only choose between Non-Validity Receiver Error (NVERR) or Receiver Error (RERR) by pulling the NV/RERR pin low or high respectively. The pull-up/pull-down condition will be sensed on startup and the appropriate error reporting will be set.

RERR – The previous audio sample is held and passed to the serial audio output port if the validity bit is high, or a parity, bi-phase, confidence or PLL lock error occurs during the current sample.

NVERR – The previous audio sample is held and passed to the serial audio output port if a parity, bi-phase, confidence or PLL lock error occurs during the current sample.

7.2. Non-Audio Detection

An AES3 data stream may be used to convey non-audio data, thus it is important to know whether the incoming AES3 data stream is digital audio or not. This information is typically conveyed in channel status bit 1, which is extracted automatically by the CS8416. However, certain non-audio sources, such as AC-3 or MPEG encoders, may not adhere to this convention, and the bit may not be properly set. The CS8416 AES3 receiver can detect such non-audio data through the use of an autodetect module. The autodetect module is similar to autodetect software used in Cirrus Logic DSPs. If the AES3 stream contains sync codes in the proper format for IEC61937 or DTS data transmission, an internal AUTODETECT signal will be asserted. If the sync codes no longer appear after a certain amount of time, autodetection will time-out and AUTODETECT will be de-asserted until another format is detected. The AUDIO signal is the logical OR of AUTODETECT and the received channel status bit 1 (as decoded according to the CHS bit in the Control1 register). In Hardware Mode, AUDIO is output on pin 15. In Software mode AUDIO is available through the GPO pins. If non-audio data is detected, the data is still processed exactly as if it were normal audio. The exception is the use of de-emphasis auto-select feature which will bypass the de-emphasis filter if the input stream is detected to be non-audio. It is up to the user to mute the outputs as required.

7.2.1. Format Detection

In Software Mode, the CS8416 can automatically detect various serial audio input formats. The Format Detect Status register (0Bh) is used to indicate a detected format. The register will indicate if uncompressed PCM data, IEC61937 data, DTS_LD data, DTS_CD data, or digital silence was detected. Additionally, the IEC61937 Pc/Pd burst preambles are available in registers 23h-26h. See the register descriptions for more information.

7.3. Interrupts

The CS8416 has a comprehensive interrupt capability. The INT signal, available in Software mode, indicates when an interrupt condition has occurred and may be output on one of the GPOs. It can also be set through bits INT[1:0] in the Control1 register (01h) to be active low, active high or active low with no active pull-up transistor. This last mode is used for active low, wired-OR hook- ups, with multiple peripherals connected to the microcontroller interrupt input pin.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. Each source may be masked off through mask register bits. In addition, each source may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer. Refer to the register descriptions for the Interrupt Mast (07h), Interrupt Mode MSB (08h), Interrupt Mode LSB (09h), and Interrupt 1 Status (0Dh) registers.

8. CHANNEL STATUS AND USER DATA HANDLING

"Appendix B: Channel Status Buffer Management" on page 49 describes the overall handling of Channel Status and User data.

8.1. Software Mode

In Software Mode several options are available for accessing the Channel Status and User data that is encoded in the received AES3/SPDIF stream.

The first option allows access directly through registers. The first 5 bytes of the Channel Status block are decoded into the Receiver Channel Status Registers 19h - 22h. Registers 19h - 1Dh contain the A channel status data. Registers 1Eh - 22h contain the B channel status data.

Received Channel Status (C), User (U), and $\overline{\text{EMPH}}$ bits may also be output to the GPO pins by appropriately setting the GPOxSEL bits in control port registers 02h and 03h. In serial port master mode, OLRCK and RCBL can be made available to qualify the U data output. In serial port slave mode, VLRCK and RCBL can be made available to qualify the U data output. VLRCK is a virtual word clock, equal to the receiver recovered sample rate, that can be used to frame the C/U output. VLRCK and RCBL are available through the GPO pins. Figure 10 illustrates timing of the C and U data and their related signals.

The user may also access all of the C and U bits directly from the output data stream (SDOUT) by setting bits SORES[1:0]=11 (AES3 Direct mode) in the Serial Audio Data Format register (05h). The appropriate bits can be stripped from the SDOUT signal by external control logic such as a DSP or microcontroller.

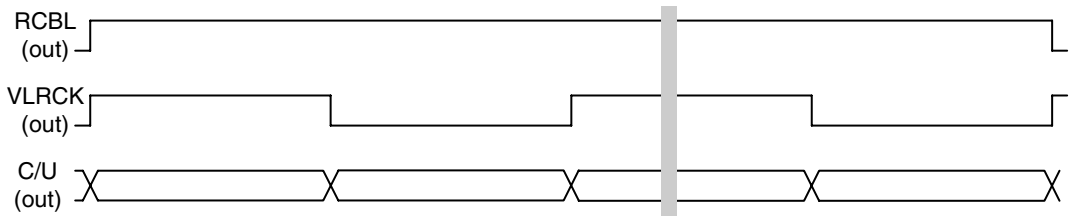
If the incoming User data bits have been encoded as Q-channel subcode, the data is decoded, buffered, and presented in 10 consecutive register locations (0Eh-17h). An interrupt may be enabled to indicate the decoding of a new Q-channel block, which may be read through the control port.

The encoded Channel Status bits which indicate sample word length are decoded according to AES3-1992 or IEC 60958. The number of auxiliary bits are reported in bits 7 to 4 of the Receiver Channel Status register (0Ah).

8.2. Hardware Mode

In Hardware Mode, Received Channel Status (C), and User (U) bits are output on pins 19 and 20. In serial port master mode, OLRCK and RCBL are made available to qualify the C and U data output. Figure 10 illustrates timing of the C and U data and their related signals.

The user may also access all of the C and U bits directly from the output data stream (SDOUT) by pulling the $\overline{\text{AUDIO}}$ and C pins high through 47 kΩ resistors to VL (AES3 Direct mode). The appropriate bits can be stripped from the SDOUT signal by external control logic such as a DSP or microcontroller. Only OL-CK in master mode is available to qualify the U output. See "Hardware Mode Function Selection" on page 40 and "Hardware Mode Equivalent Register Settings" on page 40 to configure these pins.



- **RCBL goes high 2 frames after receipt of a Z preamble and is high for 16 frames.**
- **VLRCK is a virtual work clock, available through the GPO pins, that can be used to frame the C/U output.**
- **VLRCK duty cycle is 50%. VLRCK frequency is always equal to the incoming frame rate.**
- **If the serial audio output port is in master mode, VLRCK = OLRCK.**
- **C/U transitions are aligned within ±1% of VLRCK period to VLRCK edges**

Figure 10. C/U data outputs

9. CONTROL PORT INTERFACE

The Control Port is used to load all the internal settings. In addition, Channel Status and User data may be read through the control port. The operation of the Control Port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the Control Port pins should remain static if no operation is required.

9.1. Memory Address Pointer (MAP)

9.1.1. Memory Address Pointer (MAP) Register Detail

7	6	5	4	3	2	1	0
INCR	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0

9.1.2. INCR (Auto Map Increment Enable)

Default = '0'

0 - Disabled, the MAP will stay constant for successive writes

1 - Enabled, the MAP will auto increment after each byte is written, allowing block reads or writes of successive registers

9.1.3. MAP6-0 (Memory Address Pointer)

Default = '0000000'

9.2. Format Selection

The Control Port has 2 formats: SPI and I^2C, with the CS8416 operating as a slave device.

If I^2C operation is desired, AD0/$\overline{CS}$ should be tied to VL or DGND. If the CS8416 ever detects a high to low transition on AD0/$\overline{CS}$ after reset, SPI format will automatically be selected.

9.3. I^2C Format

In I^2C Format, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with a clock to data relationship as shown in Figure 12. Pins AD0 and AD1 form the two least significant bits of the chip address and should be connected to VL or DGND as desired. The GPO2 pin is used to set the AD2 bit by connecting a 47 kΩ resistor from the GPO2 pin to VL or to DGND. The state of the pin is sensed while the CS8416 is being reset. The upper 4 bits of the 7-bit address field are fixed at 0010.

9.3.1. Writing in I^2C Format

To communicate with the CS8416, initiate a START condition of the bus (see Figure 11). Next, send the chip address. The eighth bit of the address byte is the R/$\overline{W}$ bit (low for a write). The next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. To write multiple registers, continue providing a clock and data, waiting for the CS8416 to acknowledge between each byte. To end the transaction, send a STOP condition.

9.3.2. Reading in I^2C Format

To communicate with the CS8416, initiate a START condition of the bus (see Figure 11). Next, send the chip address. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read). The contents of the register pointed to by the MAP will be output after the chip address. To read multiple registers, continue providing a clock and issue an ACK after each byte. To end the transaction, send a STOP condition.

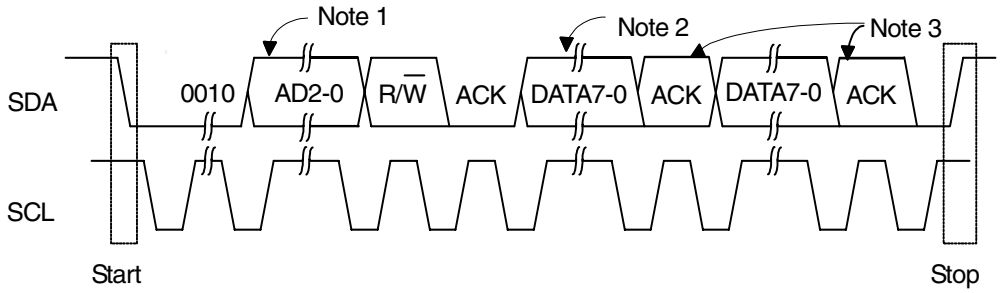


Figure 11. Control Port Timing in I²C Mode

Notes: 1. AD2 is derived from a resistor attached to the GPO2 pin.
AD1 and AD0 are determined by the state of the corresponding pins.
2. If operation is a write, this byte contains the Memory Address Pointer, MAP.
3. If operation is a read, the last bit of the read should be NACK (high).

9.4. SPI Format

In SPI format, $\overline{CS}$ is the CS8416 chip select signal, CCLK is the Control Port bit clock, CDIN is the input data line from the microcontroller, CDOUT is the output data line and the chip address is 0010000. $\overline{CS}$, CCLK and CDIN are all inputs and data is clocked in on the rising edge of CCLK. CDOUT is an output and is high impedance when not actively outputting data.

9.4.1. Writing in SPI

Figure 12 shows the operation of the Control Port in SPI format. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into register designated by the MAP. To write multiple registers, keep $\overline{CS}$ low and continue providing clocks on CCLK. End the read transaction by setting $\overline{CS}$ high.

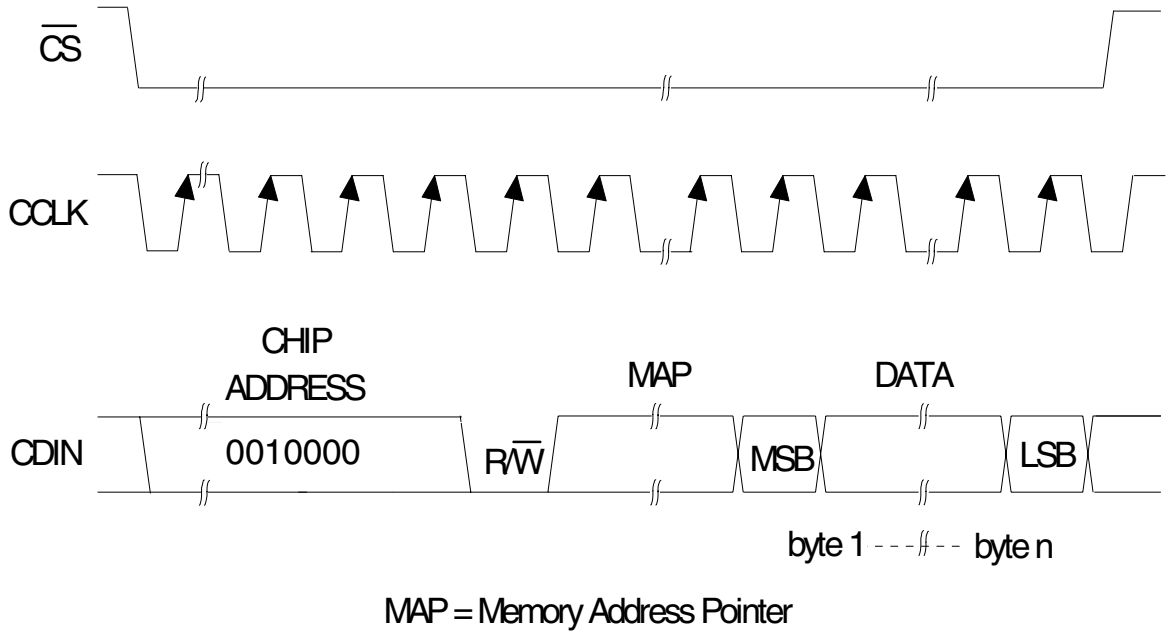


Figure 12. Control Port Timing, SPI Format (Write)

9.4.2. Reading in SPI

Figure 13 shows the operation of the Control Port in SPI format. To read to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address and must be 0010000. The eighth bit is a read/write control (R/$\overline{W}$), which must be high to read. The CDOUT line will then output the data from the register designated by the MAP. To read multiple registers, keep $\overline{CS}$ low and continue providing clocks on CCLK. End the read transaction by setting $\overline{CS}$ high. The CDOUT line will go to a high impedance state once $\overline{CS}$ goes high.

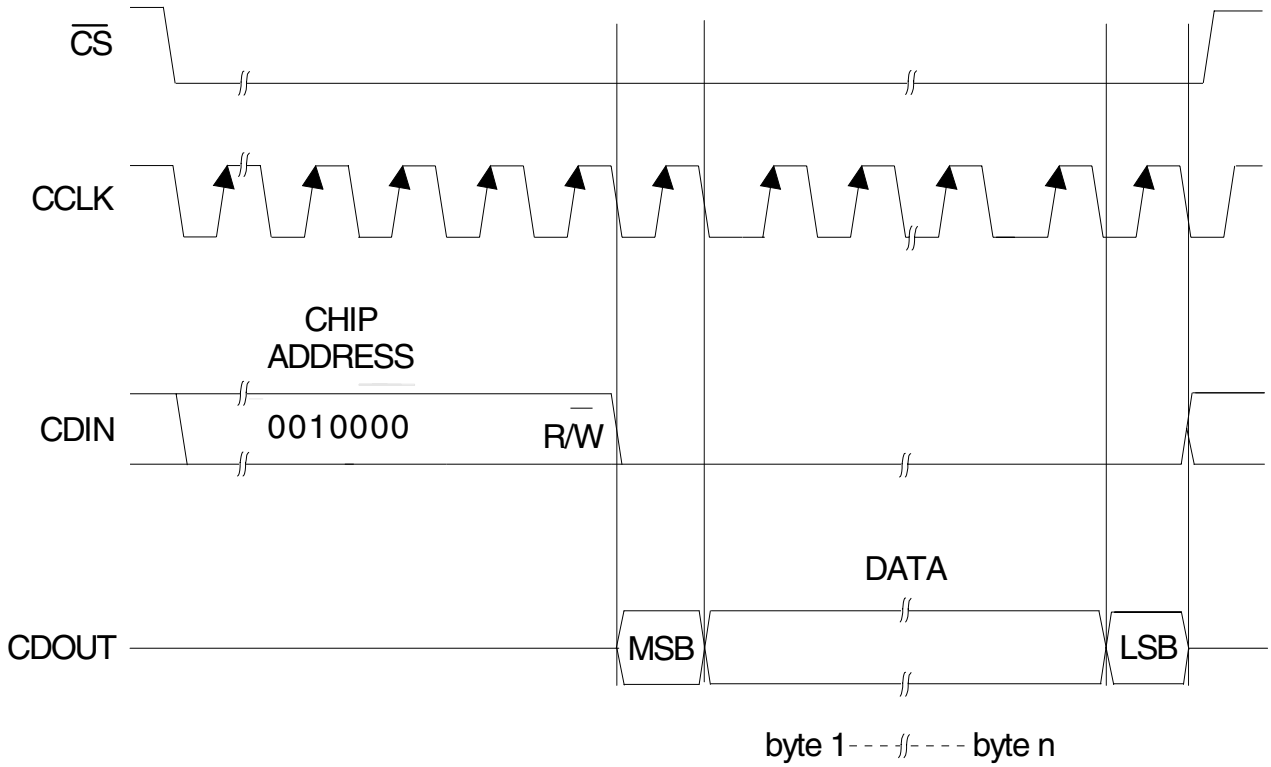


Figure 13. Control Port Timing, SPI Format (Read)

10. CONTROL PORT REGISTER SUMMARY

Addr (HEX)	R/W	Function	7	6	5	4	3	2	1	0
00	R/W	Control0	0	FSWCLK	0	0	0	TRUNC	Reserved	Reserved
01	R/W	Control1	SWCLK	MUTSAO	INT1	INT0	HOLD1	HOLD0	RMCKF	CHS
02	R/W	Control2	DETCI	EMPH_CNTL2	EMPH_CNTL1	EMPH_CNTL0	GPO0SEL3	GPO0SEL2	GPO0SEL1	GPO0SEL0
03	R/W	Control3	GPO1SEL3	GPO1SEL2	GPO1SEL1	GPO1SEL0	GPO2SEL3	GPO2SEL2	GPO2SEL1	GPO2SEL0
04	R/W	Control4	RUN	RXD	RXSEL2	RXSEL1	RXSEL0	TXSEL2	TXSEL1	TXSEL0
05	R/W	Serial Audio Data Format	SOMS	SOSF	SORES1	SORES0	SOJUST	SODEL	SOSPOL	SOLRPOL
06	R/W	Receiver Error Mask	0	QCRCM	CCRCM	UNLOCKM	VM	CONFM	BIPM	PARM
07	R/W	Interrupt Mask	0	PCCHM	OSLIPM	DETCM	CCHM	RERRM	QCHM	FCHM
08	R/W	Interrupt Mode MSB	0	PCCH1	OSLIP1	DETC1	CCH1	RERR1	QCH1	FCH1
09	R/W	Interrupt Mode LSB	0	PCCH0	OSLIP0	DETC0	CCH0	RERR0	QCH0	FCH0
0A	R	Receiver Channel Status	AUX3	AUX2	AUX1	AUX0	PRO	COPY	ORIG	EMPH
0B	R	Audio Format Detect	0	PCM	IEC61937	DTS_LD	DTS_CD	Reserved	DGTL_SIL	96KHZ
0C	R	Receiver Error	0	QCRC	CCRC	UNLOCK	V	CONF	BIP	PAR
0D	R	Interrupt Status	0	PCCH	OSLIP	DETC	CCH	RERR	QCH	FCH
0E	R	Q-Channel Subcode [0:7]	CONTROL	CONTROL	CONTROL	CONTROL	ADDRESS	ADDRESS	ADDRESS	ADDRESS
0F	R	Q-Channel Subcode [8:15]	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK
10	R	Q-Channel Subcode [16:23]	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX
11	R	Q-Channel Subcode [24:31]	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE
12	R	Q-Channel Subcode [32:39]	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND
13	R	Q-Channel Subcode [40:47]	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME
14	R	Q-Channel Subcode [48:55]	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO
15	R	Q-Channel Subcode [56:63]	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE
16	R	[Q-Channel Subcode 64:71]	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND
17	R	Q-Channel Subcode [72:79]	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME
18	R	OMCK_RMCK Ratio	ORR7	ORR6	ORR5	ORR4	ORR3	ORR2	ORR1	ORR0
19	R	Channel A Status	AC0[7]	AC0[6]	AC0[5]	AC0[4]	AC0[3]	AC0[2]	AC0[1]	AC0[0]
1A	R	Channel A Status	AC1[7]	AC1[6]	AC1[5]	AC1[4]	AC1[3]	AC1[2]	AC1[1]	AC1[0]
1B	R	Channel A Status	AC2[7]	AC2[6]	AC2[5]	AC2[4]	AC2[3]	AC2[2]	AC2[1]	AC2[0]
1C	R	Channel A Status	AC3[7]	AC3[6]	AC3[5]	AC3[4]	AC3[3]	AC3[2]	AC3[1]	AC3[0]

Addr (HEX)	R/W	Function	7	6	5	4	3	2	1	0
1D	R	Channel A Status	AC4[7]	AC4[6]	AC4[5]	AC4[4]	AC4[3]	AC4[2]	AC4[1]	AC4[0]
1E	R	Channel B Status	BC0[7]	BC0[6]	BC0[5]	BC0[4]	BC0[3]	BC0[2]	BC0[1]	BC0[0]
1F	R	Channel B Status	BC1[7]	BC1[6]	BC1[5]	BC1[4]	BC1[3]	BC1[2]	BC1[1]	BC1[0]
20	R	Channel B Status	BC2[7]	BC2[6]	BC2[5]	BC2[4]	BC2[3]	BC2[2]	BC2[1]	BC2[0]
21	R	Channel B Status	BC3[7]	BC3[6]	BC3[5]	BC3[4]	BC3[3]	BC3[2]	BC3[1]	BC3[0]
22	R	Channel B Status	BC4[7]	BC4[6]	BC4[5]	BC4[4]	BC4[3]	BC4[2]	BC4[1]	BC4[0]
23	R	Burst Preamble PC Byte 0	PC0[7]	PC0[6]	PC0[5]	PC0[4]	PC0[3]	PC0[2]	PC0[1]	PC0[0]
24	R	Burst Preamble PC Byte 1	PC1[7]	PC1[6]	PC1[5]	PC1[4]	PC1[3]	PC1[2]	PC1[1]	PC1[0]
25	R	Burst Preamble PD Byte 0	PD0[7]	PD0[6]	PD0[5]	PD0[4]	PD0[3]	PD0[2]	PD0[1]	PD0[0]
26	R	Burst Preamble PD Byte 1	PD1[7]	PD1[6]	PD1[5]	PD1[4]	PD1[3]	PD1[2]	PD1[1]	PD1[0]
7F	R	ID & Version	ID3	ID2	ID1	ID0	VER3	VER2	VER1	VER0

11. CONTROL PORT REGISTER BIT DEFINITIONS

11.1. Control0 (00h)

7	6	5	4	3	2	1	0
0	FSWCLK	0	0	0	TRUNC	Reserved	Reserved

FSWCLK – Forces the clock signal on OMCK to be output on RMCK regardless of the SWCLK (Control1 register bit 6) bit functionality or PLL lock.

Default = '0'

0 – Clock signal on OMCK is output on RMCK according to the SWCLK bit functionality.

1 – Forces the clock signal on OMCK to be output on RMCK regardless of the SWCLK bit functionality.

TRUNC – Determines if the audio word length is set according to the incoming channel status data as decoded by the AUX[3:0] bits. The resulting word length in bits is 24-AUX[3:0].

Default = '0'

0 – incoming data is not truncated.

1 – incoming data is truncated according to the length specified in the channel status data.

Truncation occurs before the de-emphasis filter. TRUNC has no effect on output data if de-emphasis filter is not used.

Reserved – These bits may change state depending on the input audio data.

11.2. Control1 (01h)

7	6	5	4	3	2	1	0
SWCLK	MUTESAO	INT1	INT0	HOLD1	HOLD0	RMCKF	CHS

SWCLK - Lets OMCK determine RMCK, OSCLK, OLRCK when PLL loses lock

Default = '0'

0 - Enable automatic clock switching on PLL unlock. OMCK clock input is automatically output on RMCK on PLL Unlock.
1 - Disable automatic clock switching. RMCK runs at the VCO frequency (~500kHz) on PLL Unlock.

MUTESAO - Mute control for the serial audio output port

Default = '0'

0 - SDOUT not muted.
1 – SDOUT muted.

INT[1:0] - Interrupt output pin (INT) control

Default = '00'

00 - Active high; high output indicates interrupt condition has occurred.
01 - Active low, low output indicates an interrupt condition has occurred.
10 - Open drain, active low. Requires an external pull-up resistor on the INT pin. Thus it is not recommended to multiplex INT onto GPO2 in I^2C control port mode since an external resistor is required on GPO2 to specify the AD2 bit of the chip address.
11 – Reserved.

HOLD[1:0] – Determine how received audio sample is affected when a receive error occurs

Default = '00'

00 – hold last audio sample.

01 – replace the current audio sample with all zeros (mute).

10- do not change the received audio sample.

11 - reserved

RMCKF – Recovered Master Clock Frequency

Default = '0'

0 – RMCK output frequency is 256*F_S.

1 – RMCK output frequency is 128*F_S.

CHS – Sets which channel's C data is decoded in the Receiver Channel Status register (0Ah).

Default = '0'

0 – A channel.

1 – B channel.

If CHS = 0 and TRUNC = 1, both channels' audio data will be truncated by the AUX[3:0] bits indicated in the channel A Channel Status data. If CHS = 1 and TRUNC = 1, both channels' audio data will be truncated by the AUX[3:0] bits indicated in the channel B Channel Status data. This will occur even if the AUX[3:0] bits indicated in the channel A Channel Status data are not equal to the AUX[3:0] bits indicated in the channel B Channel Status data.

11.3. Control2 (02h)

7	6	5	4	3	2	1	0
DETCI	EMPH_CNTL2	EMPH_CNTL1	EMPH_CNTL0	GPO0SEL3	GPO0SEL2	GPO0SEL1	GPO0SEL0

DETCI – D to E status transfer inhibit

Default = '0'

0 – Allow update.

1 – Inhibit update.

EMPH_CNTL[2:0] – De-emphasis filter control. See Figure 14 for De-emphasis filter response.

Default = '000'

000 – De-emphasis filter off.

001 – 32 kHz setting.

010 – 44.1 kHz setting.

011 – 48 kHz setting.

100 – 50 µs/15 µs de-emphasis filter auto-select on. Coefficients (32, 44.1 or 48 kHz or no de-emphasis filter at all) match the pre-emphasis and sample frequency indicators in the channel status bits of Channel A. Thus it is impossible to have de-emphasis applied to one channel but not the other. The de-emphasis filter is turned off if the audio data is detected to be non-audio data.

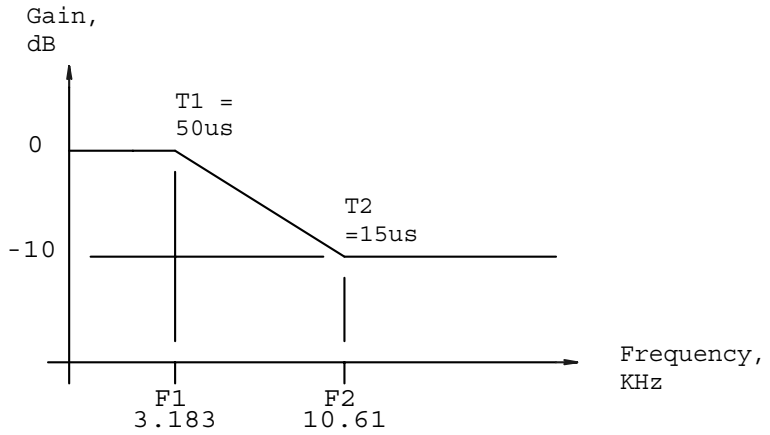


Figure 14. De-emphasis filter response

GPO0SEL[3:0] – GPO0 Source select. See "General Purpose Outputs" on page 19.

Default = '0000'

11.4. Control3 (03h)

7	6	5	4	3	2	1	0
GPO1SEL3	GPO1SEL2	GPO1SEL1	GPO1SEL0	GPO2SEL3	GPO2SEL2	GPO2SEL1	GPO2SEL0

GPO1SEL[3:0] – GPO1 Source select. See "General Purpose Outputs" on page 19.

Default = '0000'

GPO2SEL[3:0] – GPO2 Source select. See "General Purpose Outputs" on page 19.

Default = '0000'

11.5. Control4 (04h)

7	6	5	4	3	2	1	0
RUN	RXD	RXSEL2	RXSEL1	RXSEL0	TXSEL2	TXSEL1	TXSEL0

RUN - Controls the internal clocks, allowing the CS8416 to be placed in a "powered down", low current consumption, state.

Default = '0'

0 - Internal clocks are stopped. Internal state machines are reset. The fully static control port is operational, allowing registers to be read or changed. Power consumption is low.

1 - Normal part operation. This bit must be written to the 1 state to allow the CS8416 to begin operation. All input clocks should be stable in frequency and phase when RUN is set to 1.

RXD – RMCK Control

Default = '0'

0 -RMCK is an output, Clock is derived from input frame rate.

1 – RMCK becomes high impedance. The output of OSCLK, OLRCK, and SDOUT are indeterminate.

RX_SEL[2:0] – Selects RXP0 to RXP7 for input to the receiver

Default ='000'

000 – RXP0

001 – RXP1, etc

TX_SEL[2:0] – Selects RXP0 to RXP7 as the input for GPO TX source

Default ='000'

000 – RXP0

001 – RXP1, etc

11.6. Serial Audio Data Format (05h)

7	6	5	4	3	2	1	0
SOMS	SOSF	SORES1	SORES0	SOJUST	SODEL	SOSPOL	SOLRPOL

SOMS - Master/Slave Mode Selector

Default = '0'

0 - Serial audio output port is in slave mode. OSCLK and OLRCK are inputs.
1 - Serial audio output port is in master mode. OSCLK and OLRCK are outputs.

SOSF - OSCLK frequency (for master mode)

Default = '0'

0 - OSCLK output frequency is $64*F_s$.
1 - OSCLK output frequency is $128*F_s$.

SORES[1:0] - Resolution of the output data on SDOUT

Default = '00'

00 - 24-bit resolution.

01 - 20-bit resolution.

10 - 16-bit resolution.

11 - Direct copy of the received NRZ data from the AES3 receiver including C, U, and V bits. The time slot occupied by the Z bit is used to indicate the location of the block start. This setting forces the SOJUST bit to be "0".

SOJUST - Justification of SDOUT data relative to OLRCK

Default = '0'

0 - Left-justified.
1 - Right-justified (master mode only and SORES ≠11).

SODEL - Delay of SDOUT data relative to OLRCK, for left-justified data formats

(This control is only valid in left justified mode)

Default = '0'

0 - MSB of SDOUT data occurs in the first OSCLK period after the OLRCK edge.
1 - MSB of SDOUT data occurs in the second OSCLK period after the OLRCK edge.

SOSPOL - OSCLK clock polarity

Default = '0'

0 - SDOUT is sampled on rising edges of OSCLK.
1 - SDOUT is sampled on falling edges of OSCLK.

SOLRPOL - OLRCK clock polarity

Default = '0'

0 - SDOUT data is valid for the left channel when OLRCK is high.
1 - SDOUT data is valid for the right channel when OLRCK is high.

11.7. Receiver Error Mask (06h)

7	6	5	4	3	2	1	0
0	QCRCM	CCRCM	UNLOCKM	VM	CONFM	BIPM	PARM

The bits in this register serve as masks for the corresponding bits of the Receiver Error Register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will appear in the receiver error register, will affect RERR, will affect the RERR interrupt, and will affect the current audio sample according to the status of the HOLD bit. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not appear in the receiver error register, will not affect the RERR pin, will not affect the RERR interrupt, and will not affect the current audio sample. The CCRC and QCRC bits behave differently from the other bits: they do not affect the current audio sample even when unmasked. This register defaults to 00h.

11.8. Interrupt Mask (07h)

7	6	5	4	3	2	1	0
0	PCCHM	OSLIPM	DETCM	CCHM	RERRM	QCHM	FCHM

The bits of this register serve as a mask for the Interrupt Status register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the internal INT signal or the status register. The bit positions align with the corresponding bits in Interrupt Status register. This register defaults to 00h.

The INT signal may be selected to appear on the GPO pins. *See "General Purpose Outputs" on page 19.*

11.9. Interrupt Mode MSB (08h) and Interrupt Mode LSB(09h)

7	6	5	4	3	2	1	0
0	PCCH1	OSLIP1	DETC1	CCH1	RERR1	QCH1	FCH1
0	PCCH0	OSLIP0	DETC0	CCH0	RERR0	QCH0	FCH0

The two Interrupt Mode registers form a 2-bit code for each Interrupt Status register function. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT interrupt pin becomes active during the interrupt condition. Be aware that the active level (Active High or Low) only depends on the INT[1:0] bits. These registers default to 00h.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

11.10. Receiver Channel Status (0Ah)

7	6	5	4	3	2	1	0
AUX3	AUX2	AUX1	AUX0	PRO	COPY	ORIG	$\overline{\text{EMPH}}$

The bits in this register can be associated with either channel A or B of the received data. The desired channel is selected with the CHS bit of the Control1 register.

AUX3:0 - Incoming auxiliary data field width, as indicated by the incoming channel status bits, decoded according to IEC60958 and AES3.

0000 - Auxiliary data is not present.
0001 - Auxiliary data is 1 bit long.
0010 - Auxiliary data is 2 bits long.
0011 - Auxiliary data is 3 bits long.
0100 - Auxiliary data is 4 bits long.
0101 - Auxiliary data is 5 bits long.
0110 - Auxiliary data is 6 bits long.
0111 - Auxiliary data is 7 bits long.
1000 - Auxiliary data is 8 bits long.
1001 - 1111 Reserved

PRO - Channel status block format indicator

0 - Received channel status block is in the consumer format.
1 - Received channel status block is in the professional format.

COPY - SCMS copyright indicator

0 - Copyright asserted.
1 - Copyright not asserted. If the category code is set to General in the incoming AES3 stream, copyright will always be indicated by COPY, even when the stream indicates no copyright.

ORIG - SCMS generation indicator, decoded from the category code and the L bit.

0 - Received data is 1st generation or higher.
1 - Received data is original.
Note: COPY and ORIG will both be set to 1 if incoming data is flagged as professional or if the receiver is not in use.

$\overline{\text{EMPH}}$ – Indicates whether the input audio data has been pre-emphasized. Also indicates turning on of the de-emphasis filter during de-emphasis auto-select mode.

0 – 50 µs/15 µs pre-emphasis indicated.
1 – 50 µs/15 µs pre-emphasis not indicated.

11.11. Format Detect Status (0Bh)

7	6	5	4	3	2	1	0
0	PCM	IEC61937	DTS_LD	DTS_CD	Reserved	DGTL_SIL	96KHZ

Note: PCM, DTS_LD, DTS_CD and IEC61937 are mutually exclusive. A ‘1’ indicated the condition was detected.

PCM – Uncompressed PCM data was detected.

IEC61937 – IEC61937 data was detected.

DTS_LD – DTS_LD data was detected.

DTS_CD – DTS_CD data was detected.

Reserved – This bit may change state depending on the input audio data.

DGTL_SIL – Digital Silence was detected: at least 2047 consecutive constant samples of the same 24-bit audio data on both channels.

96KHZ – If the input sample rate is ≤ 48 kHz, outputs a "0". Outputs a "1" if the sample rate is ≥ 88.1 kHz. Otherwise the output is indeterminate.

11.12. Receiver Error (0Ch)

7	6	5	4	3	2	1	0
0	QCRC	CCRC	UNLOCK	V	CONF	BIP	PAR

This register contains the AES3 receiver and PLL status bits. Unmasked bits will go high on occurrence of the error, and will stay high until the register is read. Reading the register resets all bits to 0, unless the error source is still true. Bits that are masked off in the receiver error mask register will always be 0 in this register.

QCRC - Q-subcode data CRC error indicator. Updated on Q-subcode block boundaries

0 - No error.
1 - Error.

CCRC - Channel Status Block Cyclic Redundancy Check bit. Updated on CS block boundaries, valid in Pro mode

0 - No error.
1 - Error.

UNLOCK - PLL lock status bit. Updated on CS block boundaries.

0 - PLL locked.
1 - PLL out of lock.

V - Received AES3 Validity bit status. Updated on sub-frame boundaries.

0 - Data is valid and is normally linear coded PCM audio.
1 - Data is invalid, or may be valid compressed audio.

CONF - Confidence bit. Updated on sub-frame boundaries.

0 - No error.
1 - Confidence error. The logical OR of UNLOCK and BIP. The input data stream may be near error condition due to jitter degradation.

BIP - Bi-phase error bit. Updated on sub-frame boundaries.

0 - No error.
1 - Bi-phase error. This indicates an error in the received bi-phase coding.

PAR - Parity bit. Updated on sub-frame boundaries.

0 - No error.
1 - Parity error.

11.13. Interrupt 1 Status (0Dh)

7	6	5	4	3	2	1	0
0	PCCH	OSLIP	DETC	CCH	RERR	QCH	FCH

For all bits in this register, a "1" means the associated interrupt condition has occurred at least once since the register was last read. A "0" means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0, unless the interrupt mode is set to level and the interrupt source is still true. Status bits that are masked off in the associated mask register will always be "0" in this register.

PCCH – PC burst preamble change.

Indicates that the PC byte has changed from its previous value. If the IEC61937 bit in the Format Detect Status register goes high, it will cause a PCCH interrupt even if the PC byte hasn't changed since the last time the IEC61937 bit went high.

OSLIP - Serial audio output port data slip interrupt

When the serial audio output port is in slave mode, and OLRCK is asynchronous to the port data source, this bit will go high every time a data sample is dropped or repeated. See Slip/Repeat Behavior for more information.

DETC - D to E C-buffer transfer interrupt.

The source for this bit is true during the D to E buffer transfer in the C bit buffer management process.

C_CHANGE -Indicates that the current 10 bytes of channel status is different from the previous 10 bytes. (5 bytes per channel)

RERR - A receiver error has occurred.

The Receiver Error register may be read to determine the nature of the error which caused the interrupt.

QCH – A new block of Q-subcode is available for reading. The data must be read within 588 AES3 frames after the interrupt occurs to avoid corruption of the data by the next block.

FCH – Format Change: Goes high when the PCM, IEC61937, DTS_LD, DTS_CD, or DGTL_SIL bits in the Format Detect Status register transition from 0 to 1. When these bits in the Format Detect Status register transition from 1 to 0, an interrupt will not be generated.

11.14. Q-Channel Subcode (0Eh - 17h)

7	6	5	4	3	2	1	0
CONTROL	CONTROL	CONTROL	CONTROL	ADDRESS	ADDRESS	ADDRESS	ADDRESS
TRACK	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK	TRACK
INDEX	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX	INDEX
MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE	MINUTE
SECOND	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND	SECOND
FRAME	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME	FRAME
ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO
ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE	ABS MINUTE
ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND	ABS SECOND
ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME	ABS FRAME

Each byte is LSB first with respect to the 80 Q-subcode bits Q[79:0]. Thus bit 7 of address 0Eh is Q[0] while bit 0 of address 0Eh is Q[7]. Similarly bit 0 of address 17h corresponds to Q[79].

11.15. OMCK/RMCK Ratio (18h)

7	6	5	4	3	2	1	0
ORR7	ORR6	ORR5	ORR4	ORR3	ORR2	ORR1	ORR0

This register allows the calculation of the incoming sample rate by the host microcontroller from the equation ORR=Fso/Fsi. The Fso is determined by OMCK, whose frequency is assumed to be 256*Fso. ORR is represented as an unsigned 2-bit integer and a 6-bit fractional part. The value is meaningful only after the PLL has reached lock. For example, if the OMCK is 12.288 MHz, Fso would be 48 kHz (48 kHz = 12.288 MHz/256). Then if the input sample rate is also 48 kHz, you would get 1.0 from the ORR register (The value from the ORR register is hexadecimal, so the actual value you will get is 40h).
If $F_{SO}/F_{SI} > 3\ ^{63}/_{64}$, ORR will saturate at the value FFh. Also, there is no hysteresis on ORR. Therefore a small amount of jitter on either clock can cause the LSB ORR[0] to oscillate.

ORR[7:6] - Integer part of the ratio (Integer value=Integer(SRR[7:6])).

ORR[5:0] - Fractional part of the ratio (Fraction value=Integer(SRR[5:0])/64).

11.16. Channel Status Registers (19h - 22h)

19h	Channel A Status Byte 0	AC0[7]	AC0[6]	AC0[5]	AC0[4]	AC0[3]	AC0[2]	AC0[1]	AC0[0]
1Ah	Channel A Status Byte 1	AC1[7]	AC1[6]	AC1[5]	AC1[4]	AC1[3]	AC1[2]	AC1[1]	AC1[0]
1Bh	Channel A Status Byte 2	AC2[7]	AC2[6]	AC2[5]	AC2[4]	AC2[3]	AC2[2]	AC2[1]	AC2[0]
1Ch	Channel A Status Byte 3	AC3[7]	AC3[6]	AC3[5]	AC3[4]	AC3[3]	AC3[2]	AC3[1]	AC3[0]
1Dh	Channel A Status Byte 4	AC4[7]	AC4[6]	AC4[5]	AC4[4]	AC4[3]	AC4[2]	AC4[1]	AC4[0]
1Eh	Channel B Status Byte 0	BC0[7]	BC0[6]	BC0[5]	BC0[4]	BC0[3]	BC0[2]	BC0[1]	BC0[0]
1Fh	Channel B Status Byte 1	BC1[7]	BC1[6]	BC1[5]	BC1[4]	BC1[3]	BC1[2]	BC1[1]	BC1[0]
20h	Channel B Status Byte 2	BC2[7]	BC2[6]	BC2[5]	BC2[4]	BC2[3]	BC2[2]	BC2[1]	BC2[0]
21h	Channel B Status Byte 3	BC3[7]	BC3[6]	BC3[5]	BC3[4]	BC3[3]	BC3[2]	BC3[1]	BC3[0]
22h	Channel B Status Byte 4	BC4[7]	BC4[6]	BC4[5]	BC4[4]	BC4[3]	BC4[2]	BC4[1]	BC4[0]

11.17. IEC61937 PC/PD Burst preamble (23h - 26h)

23h	Burst Preamble PC Byte 0	PC0[7]	PC0[6]	PC0[5]	PC0[4]	PC0[3]	PC0[2]	PC0[1]	PC0[0]
24h	Burst Preamble PC Byte 1	PC1[7]	PC1[6]	PC1[5]	PC0[4]	PC1[3]	PC1[2]	PC1[1]	PC1[0]
25h	Burst Preamble PD Byte 0	PD0[7]	PD0[6]	PD0[5]	PC0[4]	PD0[3]	PD0[2]	PD0[1]	PD0[0]
26h	Burst Preamble PD Byte 1	PD1[7]	PD1[6]	PD1[5]	PD1[4]	PD1[3]	PD1[2]	PD1[1]	PD1[0]

11.18. CS8416 I.D. and Version Register (7Fh)

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	VER3	VER2	VER1	VER0

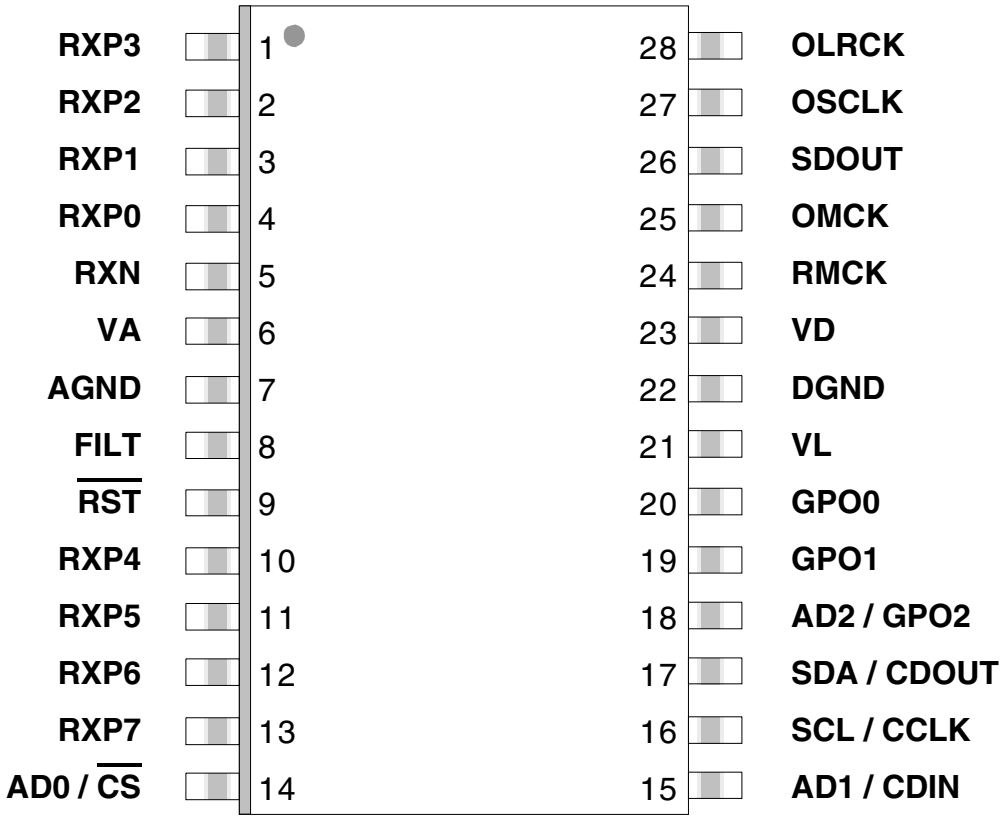
ID[3:0] - ID code for the CS8416. Permanently set to 0010

VER[3:0] = 0001 (revision A)

VER[3:0] = 0010 (revision B)

VER[3:0] = 0011 (revision C)

12. PIN DESCRIPTION - SOFTWARE MODE



VA	6	**Analog Power** (*Input*) - Analog power supply. Nominally +3.3 V. This supply should have as little noise as possible since noise on this pin will directly affect the jitter performance of the recovered clock
VD	23	**Digital Power** (*Input*) – Digital core power supply. Nominally +3.3 V
VL	21	**Logic Power** (*Input*) – Input/Output power supply. Nominally +3.3 V or +5.0 V
AGND	7	**Analog Ground** (*Input*) - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
DGND	22	**Digital & I/O Ground** (*Input*) - Ground for the I/O and core logic. AGND and DGND should be connected to a common ground area under the chip.
$\overline{\text{RST}}$	9	**Reset** (*Input*) - When $\overline{\text{RST}}$ is low, the CS8416 enters a low power mode and all internal states are reset. On initial power up, $\overline{\text{RST}}$ must be held low until the power supply is stable, and all input clocks are stable in frequency and phase.
FILT	8	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and analog ground. For minimum PLL jitter, return the ground end of the filter network directly to AGND. See “Appendix C: PLL Filter” on page 50 for more information on the PLL and the external components.

RXP0 **RXP1** **RXP2** **RXP3** **RXP4** **RXP5** **RXP6** **RXP7**	4 3 2 1 10 11 12 13	**Positive AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver inputs carrying AES3 or S/PDIF encoded digital data. The RXP[7:0] inputs comprise the 8:2 S/PDIF Input Multiplexer. The select line control is accessed using the Control 4 register (04h). Unused multiplexer inputs should be left floating or tied to AGND. See "Appendix A: External AES3/SPDIF/IEC60958 Receiver Components" on page 47 for recommended input circuits.
RXN	5	**Negative AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver input carrying AES3 or S/PDIF encoded digital data. Used along with RXP[7:0] to form an AES3 differential input. In single-ended operation this should be AC coupled to ground through a capacitor. See "Appendix A: External AES3/SPDIF/IEC60958 Receiver Components" on page 47 for recommended input circuits.
OMCK	25	**System Clock** (*Input*) - When the OMCK System Clock Mode is enabled using the SWCLK bit in the Control 1 register, the clock signal input on this pin is automatically output through RMCK on PLL unlock. OMCK serves as the reference signal for OMCK/RMCK ratio expressed in register 18h. See "OMCK System Clock Mode" on page 18.
RMCK	24	**Input Section Recovered Master Clock** (*Output*) - Input section recovered master clock output from the PLL. Frequency defaults to 256x the sample rate (F_s) and may be set to 128x through the RMCKF bit in the Control 1 register (01h). RMCK may also be set to high impedance by the RXD bit in the Control 4 register (04h).
OSCLK	27	**Serial Audio Output Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDOUT pin
OLRCK	28	**Serial Audio Output Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT pin. Frequency will be the output sample rate (Fs)
SDOUT	26	**Serial Audio Output Data** (*Output*) - Audio data serial output pin. This pin must be pulled high to VL through a 47 kΩ resistor to place the part in Software Mode.
SDA/CDOUT	17	**Serial Control Data I/O (I^2C) / Data Out (SPI)** (*Input/Output*) - In I^2C mode, SDA is the control I/O data line. SDA is open drain and requires an external pull-up resistor to VL. In SPI mode, CDOUT is the output data from the control port interface on the CS8416. See section 6. Control Port Interface.
SCL/CCLK	16	**Control Port Clock** (*Input*) - Serial control interface clock and is used to clock control data bits into and out of the CS8416. CCLK isan open drain ouput and requires an external pull-up resistor to VL. See section 6. Control Port Interface.
AD0/$\overline{CS}$	14	**Address Bit 0 (I^2C) / Control Port Chip Select (SPI)** (*Input)* - A falling edge on this pin puts the CS8416 into SPI control port mode. With no falling edge, the CS8416 defaults to I^2C mode. In I^2C mode, AD0 is a chip address pin. In SPI mode, $\overline{CS}$ is used to enable the control port interface on the CS8416. See Section 6. Control Port Interface.
AD1/CDIN	15	**Address Bit 1 (I^2C) / Serial Control Data in (SPI)** (*Input*) - In I^2C mode, AD1 is a chip address pin. In SPI mode, CDIN is the input data line for the control port interface. See section 6. Control Port Interface.
AD2/GPO2	18	**General Purpose Output 2** *(Output)* - If using the I^2C control port, this pin must be pulled high or low through a 47 kΩ resistor. See "General Purpose Outputs" on page 19 for GPO functions.
GPO1	19	**General Purpose Output 1** *(Output)* - See "General Purpose Outputs" on page 19 for GPO functions.
GPO0	20	**General Purpose Output 0** *(Output)* - See "General Purpose Outputs" on page 19 for GPO functions.

13. HARDWARE MODE

The CS8416 has a hardware mode which allows the device to operate without a microcontroller. Hardware mode is selected by connecting the 47 kΩ pull-up/down resistor on the SDOUT pin to ground. Various pins change function in hardware mode, described in the Hardware Mode Function Selection.

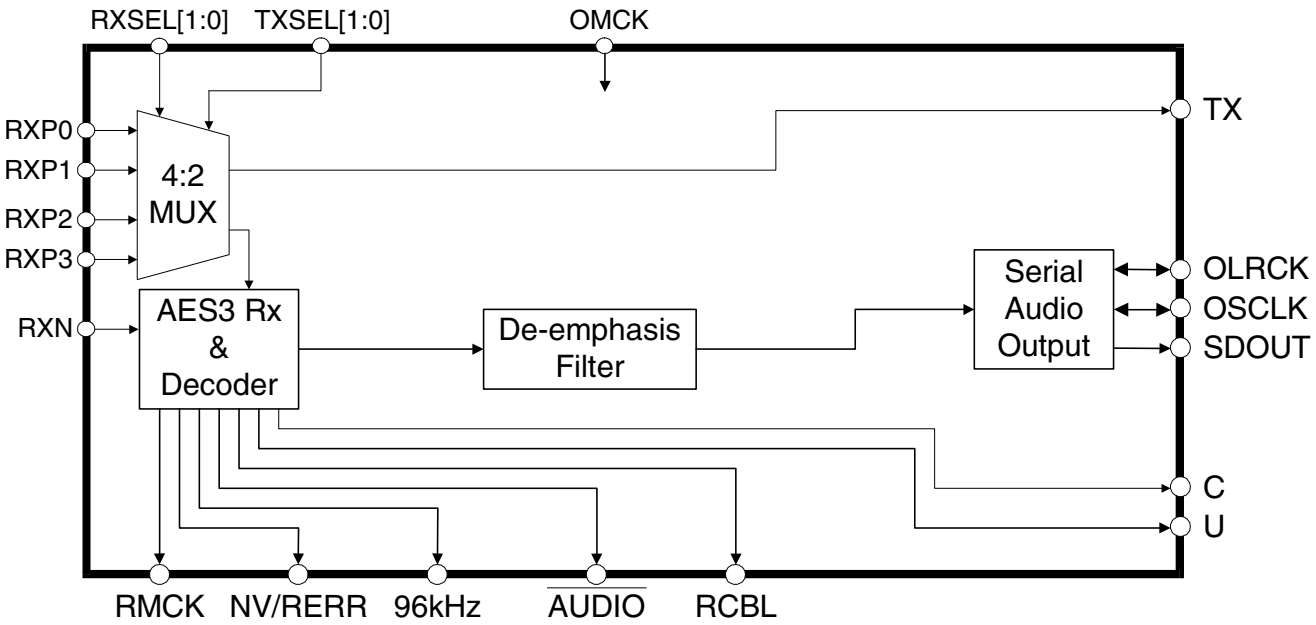
Hardware mode data flow is shown in Figure 15. Audio data is input through the AES3/SPDIF receiver, and routed to the serial audio output port. The decoded C and U bits are also output, clocked at both edges of OLRCK (master mode only, see Figure 10).

An error in the incoming audio stream will be indicated on the NV/RERR pin. This pin can be configured in one of two ways. If RERR is chosen by pulling NV/RERR to VL, the previous audio sample is held and passed to the serial audio output port if the validity bit is high, or a parity, bi-phase, confidence or PLL lock error occurs during the current sample. If NVERR is chosen by pulling NV/RERR to DGND, only parity, bi-phase, confidence or PLL lock error cause the previous audio sample to be held.

13.1. Serial Audio Port Formats

In hardware mode, only a limited number of alternative serial audio port formats are available. Table 5 defines the equivalent software mode bit settings for each format.

The start-up options, shown in Table 4, allow choice of the serial audio output port as a master or slave, and the serial audio port format.



Power supply pins (VA, VD, and VL), AGND, DGND, the reset pin ($\overline{RST}$) and the PLL filter pin (FILT) are omitted from the diagram. Please refer to the Typical Connection Diagram for connection details.

Figure 15. Hardware Mode Data Flow

13.2. Hardware Mode Function Selection

Hardware Mode and several options for Hardware Mode are selected by pulling CS8416 pins up to VL or down to DGND through a 47 kΩ resistor immediately after $\overline{RST}$ is released. For each mode, every start-up option select pin MUST have an external pull-up or pull-down resistor as there are no internal pull-up or pull-down resistors for these startup conditions (set after reset).

Pin Number	Pin Name	Pull Down to DGND Function	Pull Up to VL Function
26	SDOUT	Hardware Mode	Software Mode
17	RCBL	Serial Port Slave Mode	Serial Port Master Mode
14	NV/RERR	NVERR Selected	RERR Selected
15	AUDIO	Serial Format Select 1 (SFSEL1)=0	Serial Format Select 1 (SFSEL1)=1
19	C	Serial Format Select 0 (SFSEL0)=0	Serial Format Select 0 (SFSEL0)=1
18	U	RMCK Frequency=256*F_s	RMCK Frequency=128*F_s
16	96KHZ	Emphasis Audio Match Off	Emphasis Audio Match On

Table 4. Hardware Mode Start Up Pin Conditions

13.3. Hardware Mode Equivalent Register Settings

Listed below are the equivalent values that the registers are set to in Hardware Mode.

Control0 register (00h)

FSWCLK = 0

TRUNC = 0

Control1 register (01h)

SWCLK = Set to 1 if there a transition on OMCK after reset. Otherwise set to 0.
MUTSAO = 0
INT[1:0] = N/A, there is no interrupt pin in hardware mode.
HOLD[1:0] = 00
RMCKF = Set by U pin pull-up/down at startup.
CHS = 0

Control2 register (02h)

DETCI = N/A
EMPH_CNTL[2] = set by 96KHZ pull-up/down at startup. See Figure 14 on page 30 for the de-emphasis filter response.
EMPH_CNTL[1:0] = 00
GPO0SEL[3:0] = N/A

Control3 register (03h)

GPO1SEL[3:0] = N/A
GPO2SEL[3:0] = N/A

Control4 register (04h)

RUN = 1
RXD = 0

RX_SEL[2] = 0
RX_SEL[1:0] = RX_SEL[1:0] pins.
TX_SEL[2] = 0
TX_SEL[1:0] = TX_SEL[1:0] pins.

Serial Audio Data Format register (05h)

SOMS = set by RCBL pullup/pulldown at startup.

bits[6:0] = Set by startup pull up/pull down on $\overline{\text{AUDIO}}$ & C at startup. See Table 5 for bit settings.

Serial Format Select [1:0]	SOSF	SORES[1:0]	SOJUST	SODEL	SOSPOL	SOLRPOL
00 (Left Justified 24 bit)	0	00	0	0	0	0
01(I^2S 24 bit)	0	00	0	1	0	1
10 (Right Justified 24 bit)	0	00	1	0	0	0
11 (Direct AES3)	0	11	0	0	0	0

Table 5. Hardware Mode Serial Audio Format Select

Receiver Error Mask register (06h)

QCRCM = 0

CRCM = 0

UNLOCKM = 1

CONFM = 1

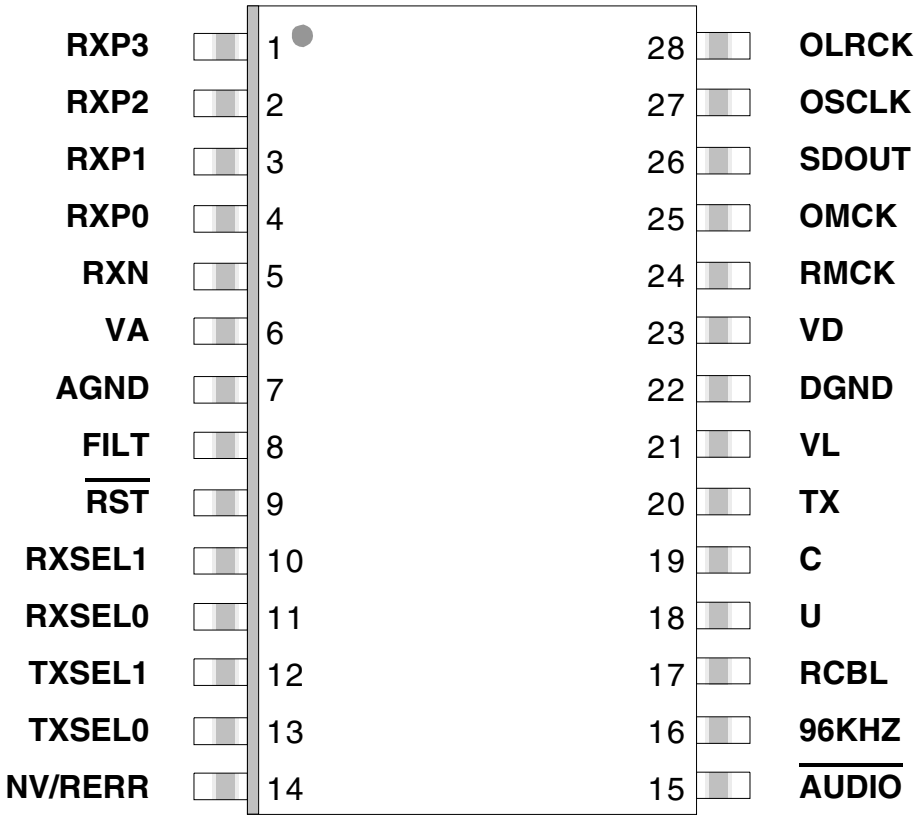
BIPM = 1

PARM = 1

VM = set by NV/RERR pull-down/up at startup.

Registers 07h through 7Fh do not have Hardware Mode equivalent settings.

14. PIN DESCRIPTION - HARDWARE MODE



VA	6	**Analog Power** (*Input*) - Analog power supply. Nominally +3.3 V. This supply should have as little noise as possible since noise on this pin will directly affect the jitter performance of the recovered clock
VD	23	**Digital Power** (*Input*) – Digital core power supply. Nominally +3.3 V
VL	21	**Logic Power** (*Input*) – Input/Output power supply. Nominally +3.3 V or +5.0 V
AGND	7	**Analog Ground** (*Input*) - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
DGND	22	**Digital & I/O Ground** (*Input*) - Ground for the I/O and core logic. AGND and DGND should be connected to a common ground area under the chip.
$\overline{\text{RST}}$	9	**Reset** (*Input*) - When $\overline{\text{RST}}$ is low, the CS8416 enters a low power mode and all internal states are reset. On initial power up, $\overline{\text{RST}}$ must be held low until the power supply is stable, and all input clocks are stable in frequency and phase.
FILT	8	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and analog ground. For minimum PLL jitter, return the ground end of the filter network directly to AGND. See “Appendix C: PLL Filter” on page 50 for more information on the PLL and the external components.
RXP0 **RXP1** **RXP2** **RXP3**	4 3 2 1	**Positive AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver inputs carrying AES3 or S/PDIF encoded digital data. The RXP[3:0] inputs comprise the 4:2 S/PDIF Input Multiplexer. The select line control is accessed using the RXPSEL[1:0] pins. Unused multiplexer inputs should be left floating or tied to AGND. See “Appendix A: External AES3/SPDIF/IEC60958 Receiver Components” on page 47 for recommended input circuits.

RXN	5	**Negative AES3/SPDIF Input** (*Input*) - Single-ended or differential receiver input carrying AES3 or S/PDIF encoded digital data. Used along with RXP[3:0] to form an AES3 differential input. In single-ended operation this should be AC coupled to ground through a capacitor. See "Appendix A: External AES3/SPDIF/IEC60958 Receiver Components" on page 47 for recommended input circuits.
OMCK	25	**System Clock** (*Input*) - OMCK System Clock Mode is enabled by a transition (rising edge actived) on OMCK after reset. When enabled, the clock signal input on this pin is automatically output through RMCK on PLL unlock. See "OMCK System Clock Mode" on page 18.
RMCK	24	**Input Section Recovered Master Clock** (*Output*) - Input section recovered master clock output from the PLL. Frequency is 256x the sample rate (F_s) when the U pin is pulled down by a 47 kΩ resistor to DGND. Frequency is 128x the sample rate (F_s) when the U pin is pulled up by a 47 kΩ resistor to DGND.
OSCLK	27	**Serial Audio Output Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDOUT pin
OLRCK	28	**Serial Audio Output Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT pin. Frequency will be the output sample rate (Fs)
SDOUT	26	**Serial Audio Output Data** (*Output*) - Audio data serial output pin. This pin must be pulled high to DGND through a 47 kΩ resistor to place the part in Hardware Mode.
RXSEL1 **RXSEL0**	10 11	**Receiver_MUX Selector** *(Input)* - Used to select which pin, RXP[3:0], is used for the receiver input.
TXSEL1 **TXSEL0**	12 13	**TX Pin MUX SELECTION** *(Input)* - Used to select which pin, RXP[3:0], is passed to the TX pin output.
TX	20	**S/PDIF MUX Pass through** (*Output)* - Single-ended signal is resolved to full-rail, but is not de-jittered before it is output. Output is set by TXSEL[1:0]. If TX is not used, the user should set it to output one of the unused receiver inputs or use a 47 kΩ pulldown resistor to minimize noise.
NV/RERR	14	**Non-Validity Receiver Error/Receiver Error** *(Output)* - Receiver error indicator. NVERR is selected by a 47 kΩ resistor to DGND. RERR is selected by a 47 kΩ resistor to VL.
$\overline{\text{AUDIO}}$	15	**Audio Channel Status Bit** *(Output)* **–** When low, a valid linear PCM audio stream is indicated. See "Non-Audio Detection" on page 21. This pin is also used to select the serial port format (SFSEL1) at reset.
96KHZ	16	**96 kHz Sample Rate Detect** *(Output)* - If the input sample rate is ≤ 48 kHz, ouputs a "0". Outputs a "1" if the sample rate is ≥ 88.1 kHz. Otherwise the output is indeterminate. Also used to set the Emphasis Audio Match feature at reset.
RCBL	17	**Receiver Channel Status Block** *(Output)* -Indicates the beginning of a received channel status block. RCBL goes high two frames after the reception of a Z preamble, remains high for 16 frames and then returns low for the remainder of the block. RCBL changes on rising edges of RMCK. Also used to set the serial audio port to master or slave at reset.
C	19	**Channel Status Data** (*Output*) - Outputs channel status data from the AES3 receiver, clocked by the rising and falling edges of OLRCK. Also used to select the serial port format (SFSEL0) at reset.
U	18	**User Data** (*Output*) - Outputs user data from the AES3 receiver, clocked by the rising and falling edges of OLRCK. Also used to select the frequency of RMCK to either 256*F_s or 128*F_s at reset.

15. APPLICATIONS

15.1. Reset, Power Down and Start-up

When $\overline{\text{RST}}$ is low, the CS8416 enters a low power mode and all internal states are reset, including the control port and registers, and the outputs are muted. In Software Mode, when $\overline{\text{RST}}$ is high, the control port becomes operational and the desired settings should be loaded into the control registers. Writing a 1 to the RUN bit will then cause the part to leave the low power state and begin operation. After the PLL has settled, the serial audio outputs will be enabled.

Some options within the CS8416 are controlled by a start-up mechanism. During the reset state, some of the pins are reconfigured internally to be inputs. Immediately upon exiting the reset state, the level of these pins is sensed. The pins are then switched to be outputs. This mechanism allows output pins to be used to set alternative modes in the CS8416 by connecting a 47 kΩ resistor to between the pin and either VL (HI) or DGND (LO). For each mode, every start-up option select pin MUST have an external pull-up or pull-down resistor as there are no internal pull-up or pull-down resistors for these startup conditions. In software mode, the only start-up option pins are GPO2, which are used to set a chip address bit for the control port in I^2C mode, and SDOUT, which selects between Hardware and Software Modes. The hardware mode uses many start-up options, which are detailed in “Hardware Mode Function Selection” on page 40

15.2. ID Code and Revision Code

The CS8416 has a register that contains a 4-bit code to indicate that the addressed device is a CS8416. This is useful when other CS84XX family members are resident in the same system, allowing common software modules.

The CS8416 4-bit revision code is also available. This allows the software driver for the CS8416 to identify which revision of the device is in a particular system, and modify its behavior accordingly. To allow for future revisions, it is strongly recommend that the revision code is read into a variable area within the microcontroller, and used wherever appropriate as revision details become known.

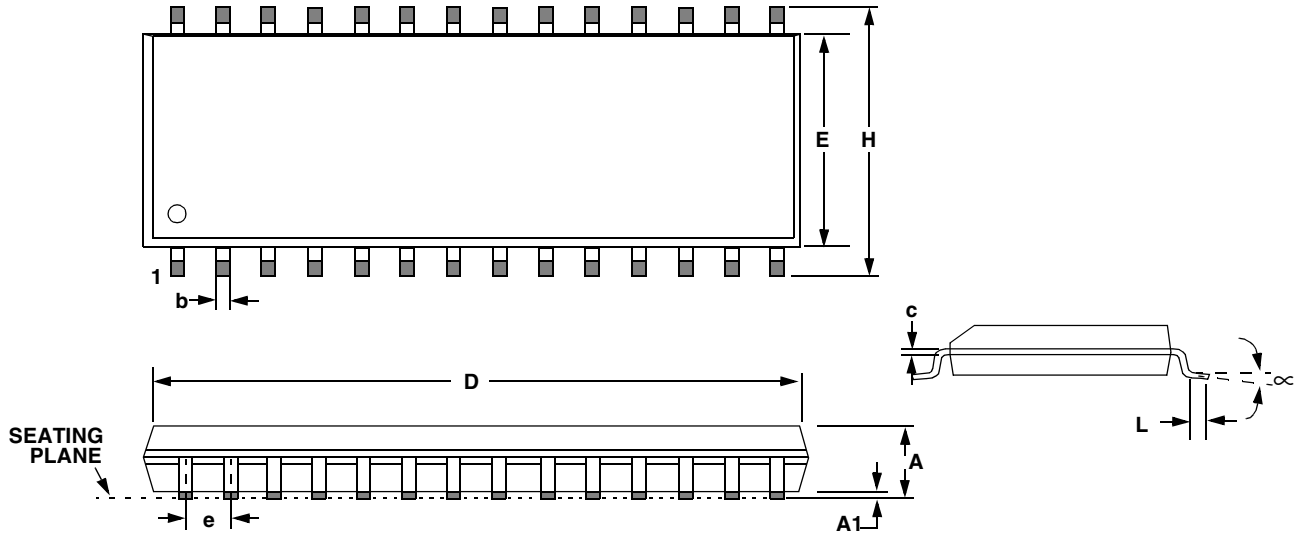
15.3. Power Supply, Grounding, and PCB layout

For most applications, the CS8416 can be operated from a single +3.3 V supply, following normal supply decoupling practices. (See Table 5 and Table 6). For applications where the recovered input clock, output on the RMCK pin, is required to be low jitter, then use a separate, quiet, analog +3.3 V supply for VA, decoupled to AGND. In addition, a separate region of analog ground plane around the FILT, AGND, VA, RXP[0:7] and RXN pins is recommended. VL sets the level for the digital inputs and outputs, as well as the AES/SPDIF receiver inputs.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be mounted on the same side of the board as the CS8416 to minimize inductance effects, and all decoupling capacitors should be as close to the CS8416 as possible. See “Appendix C: PLL Filter” on page 50 for layout recommendations for the PLL.

16. PACKAGE DIMENSIONS

28L SOIC (300 MIL BODY) PACKAGE DRAWING

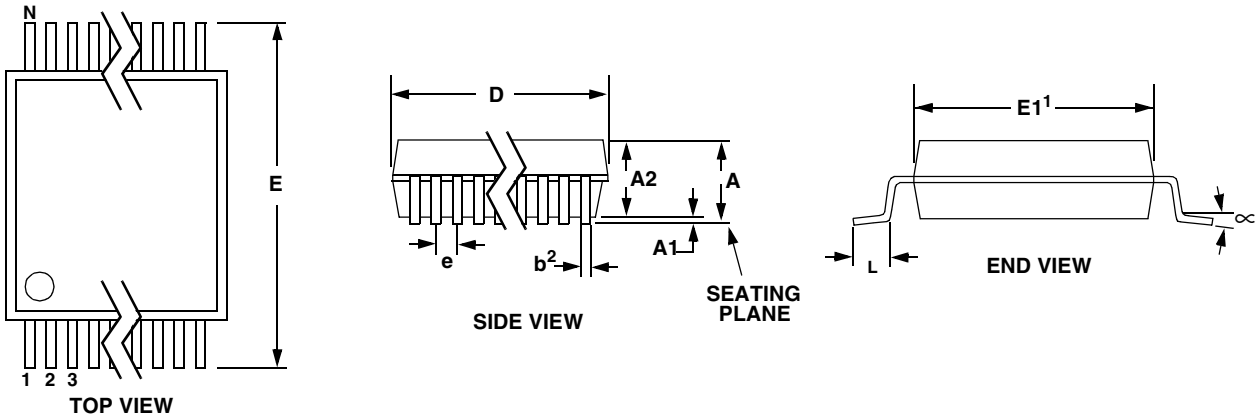


	INCHES			MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.093	0.098	0.104	2.35	2.50	2.65
A1	0.004	0.008	0.012	0.10	0.20	0.30
b	0.013	0.017	0.020	0.33	0.42	0.51
C	0.009	0.011	0.013	0.23	0.28	0.32
D	0.697	0.705	0.713	17.70	17.90	18.10
E	0.291	0.295	0.299	7.40	7.50	7.60
e	0.040	0.050	0.060	1.02	1.27	1.52
H	0.394	0.407	0.419	10.00	10.34	10.65
L	0.016	0.026	0.050	0.40	0.65	1.27
∝	0°	4°	8°	0°	4°	8°

JEDEC #: MS-013

Controlling Dimension is Millimeters

28L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.47	--	--	1.20	
A1	0.002	0.004	0.006	0.05	0.10	0.15	
A2	0.03150	0.035	0.04	0.80	0.90	1.00	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.378 BSC	0.382 BSC	0.386 BSC	9.60 BSC	9.70 BSC	9.80 BSC	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.029	0.50	0.60	0.75	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

17. APPENDIX A: EXTERNAL AES3/SPDIF/IEC60958 RECEIVER COMPONENTS

17.1. AES3 Receiver External Components

The CS8416 AES3 receiver is designed to accept both the professional and consumer interfaces. The digital audio specifications for professional use call for a balanced receiver, using XLR connectors, with 110 Ω ± 20% impedance. The XLR connector on the receiver should have female pins with a male shell. Since the receiver has a very high input impedance, a 110 Ω resistor should be placed across the receiver terminals to match the line impedance, as shown in Figure 16 and Figure 17. Although transformers are not required by the AES, they are, however, strongly recommended.

If some isolation is desired without the use of transformers, a 0.01 µF capacitor should be placed in series with each input pin (RXP[7:0] and RXN) as shown in Figure 17. However, if a transformer is not used, high frequency energy could be coupled into the receiver, causing degradation in analog performance.

Figure 16 and Figure 17 show an optional (recommended) DC blocking capacitor (0.1 µF to 0.47 µF) in series with the cable input. This improves the robustness of the receiver, preventing the saturation of the transformer, or any DC current flow, if a DC voltage is present on the cable.

In the configuration of systems, it is important to avoid ground loops and DC current flowing down the shield of the cable that could result when boxes with different ground potentials are connected. Generally, it is good practice to ground the shield to the chassis of the transmitting unit, and connect the shield through a capacitor to chassis ground at the receiver. However, in some cases it is advantageous to have the ground of two boxes held to the same potential, and the cable shield might be depended upon to make that electrical connection. Generally, it may be a good idea to provide the option of grounding or capacitively coupling the shield to the chassis.

In the case of the consumer interface, the standards call for an unbalanced circuit having a receiver impedance of 75 Ω ±5%. The connector for the consumer interface is an RCA phono socket. The receiver circuit for the consumer interface is shown in Figure 18. Figure 19 shows an implementation of the Input S/PDIF Multiplexer using the consumer interface.

The circuit shown in Figure 20 may be used when external RS422 receivers, optical receivers or other TTL/CMOS logic outputs drive the CS8416 receiver section.

17.2. Isolating Transformer Requirements

Please refer to the application note AN134: *AES and SPDIF Recommended Transformers* for resources on transformer selection.

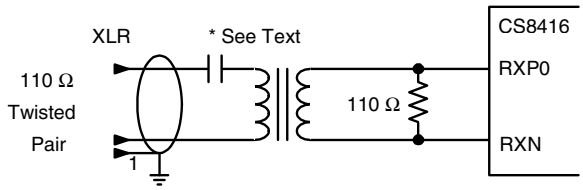


Figure 16. Professional Input Circuit

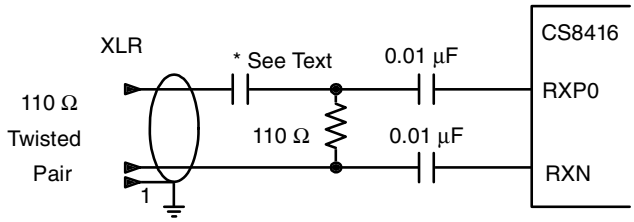


Figure 17. Transformerless Professional Input Circuit

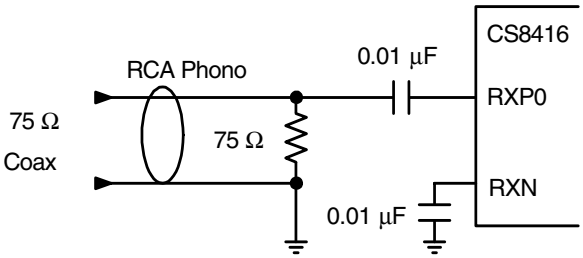


Figure 18. Consumer Input Circuit

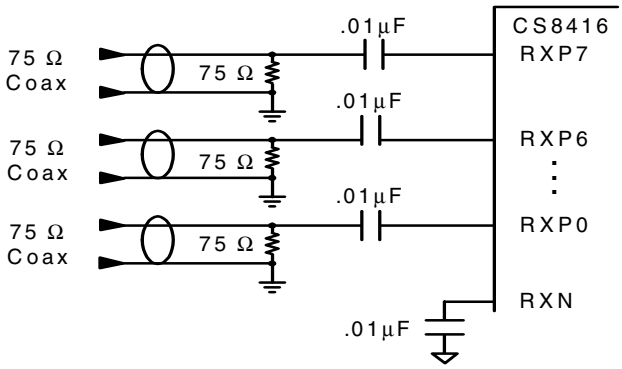


Figure 19. S/PDIF MUX Input Circuit

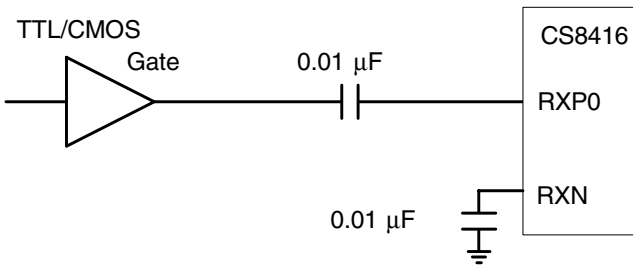


Figure 20. TTL/CMOS Input Circuit

18. APPENDIX B: CHANNEL STATUS BUFFER MANAGEMENT

18.1. AES3 Channel Status (C) Bit Management

The CS8416 contains sufficient RAM to store the first 5 bytes of C data for both A and B channels (5 x 2 x 8 = 80 bits). The user may read from this buffer's RAM through the control port.

The buffering scheme involves 2 80-bit buffers, named D and E, as shown in Figure 21. The MSB of each byte represents the first bit in the serial C data stream. For example, the MSB of byte 0 (which is at control port address 32) is the consumer/professional bit for channel status block A.

The first buffer (D) accepts incoming C data from the AES receiver. The 2nd buffer (E) accepts entire blocks of data from the D buffer. The E buffer is also accessible from the control port, allowing reading of the C data.

18.2. Accessing the E buffer

The user can monitor the incoming data by reading the E buffer, which is mapped into the register space of the CS8416, through the control port.

The user can configure the interrupt enable register to cause interrupts to occur whenever D to E buffer transfers occur. This allows determination of the allowable time periods to interact with the E buffer.

Also provided is a D to E inhibit bit in the Control2 register (02h). This may be used whenever "long" control port interactions are occurring or for debugging purposes.

A flowchart for reading the E buffer is shown in Figure 22. Since a D to E interrupt occurs just after reading, there is a substantial time interval until the next D to E transfer (approximately 192 frames worth of time). This is usually plenty of time to access the E data without having to inhibit the next transfer.

18.2.1. Serial Copy Management System (SCMS)

In software mode, the CS8416 allows read access to all the channel status bits. For consumer mode SCMS compliance, the host microcontroller needs to read and interpret the Category Code, Copy bit and L bit appropriately.

In hardware mode, the SCMS protocol can be followed by either using the COPY and ORIG output pins, or by using the C bit serial output pin. These options are documented in the hardware mode section of this data sheet.

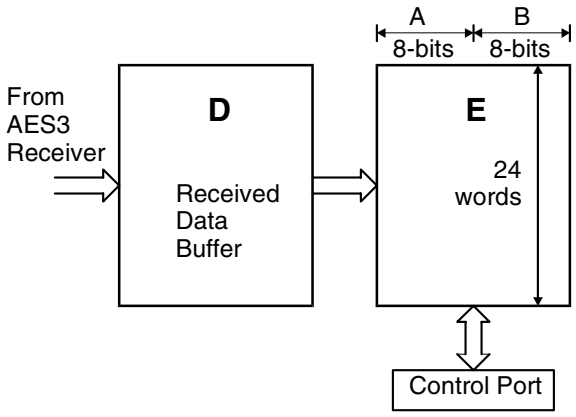


Figure 21. Channel Status Data Buffer Structure

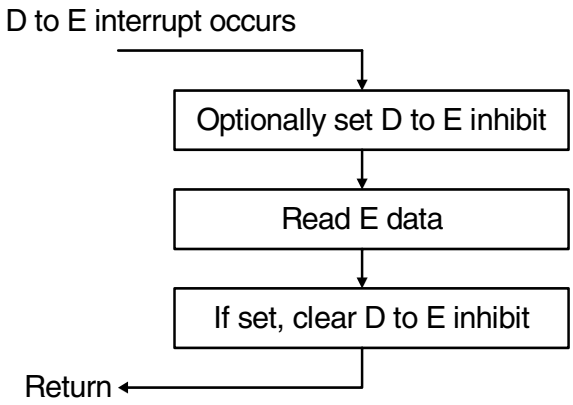


Figure 22. Flowchart for Reading the E Buffer

19. APPENDIX C: PLL FILTER

19.1. General

An on-chip Phase Locked Loop (PLL) is used to recover the clock from the incoming data stream. Figure 23 is a simplified diagram of the PLL in these parts. When the PLL is locked to an bi-phase encoded input stream, it is updated at each preamble in the bi-phase encoded stream. This occurs at twice the sampling frequency, F_S.

There are some applications where low jitter in the recovered clock, presented on the RMCK pin, is important. For this reason, the PLL has been designed to have good jitter attenuation characteristics, as shown in Figure 25. In addition, the PLL has been designed to only use the preambles of the bi-phase encoded stream to provide lock update information to the PLL. This results in the PLL being immune to data dependent jitter affects because the preambles do not vary with the data.

The PLL has the ability to lock onto a wide range of input sample rates with no external component changes. If the sample rate of the input subsequently changes, for example in a varispeed application, the PLL will only track up to ±12.5% from the nominal center sample rate. The nominal center sample rate is the sample rate that the PLL first locks onto upon application of an bi-phase encoded data stream or after enabling the CS8416 clocks by setting the RUN control bit. If the 12.5% sample rate limit is exceeded, the PLL will return to its wide lock range mode and re-acquire a new nominal center sample rate.

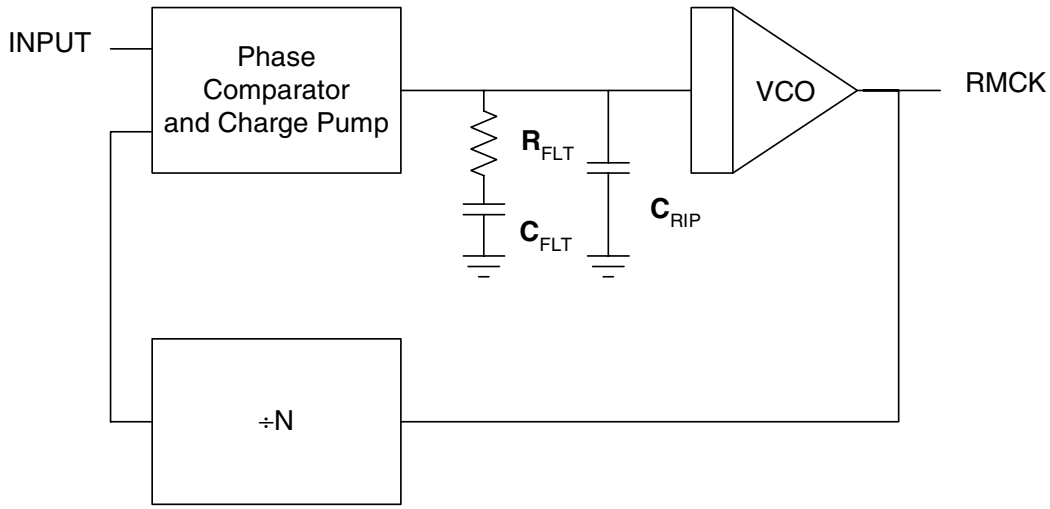


Figure 23. PLL Block Diagram

19.2. External Filter Components

19.2.1. General

The PLL behavior is affected by the external filter component values. Figure 5 and Figure 6 shows the recommended configuration of the two capacitors and one resistor that comprise the PLL filter. In Table 6, the component values shown have a high corner frequency jitter attenuation curve, take a short time to lock, and offer good output jitter performance. Lock times are worst case for an Fsi transition of 192 kHz.

It is important to treat the PLL FLT pin as a low level analog input. It is suggested that the ground end of the PLL filter be returned directly to the AGND pin independently of the digital ground plane.

19.2.2. Capacitor Selection

The type of capacitors used for the PLL filter can have a significant effect on receiver performance. Large or exotic film capacitors are not necessary as their leads and the required longer circuit board traces add undesirable inductance to the circuit. Surface mount ceramic capacitors are a good choice because their own inductance is low, and they can be mounted close to the FILT pin to minimize trace inductance. For C_{RIP}, a C0G or NPO dielectric is recommended, and for C_{FLT}, an X7R dielectric is preferred. Avoid capacitors with large temperature co-coefficient, or capacitors with high dielectric constants, that are sensitive to shock and vibration. These include the Z5U and Y5V dielectrics.

19.2.3. Circuit Board Layout

Board layout and capacitor choice affect each other and determine the performance of the PLL. Figure 24 contains a suggested layout for the PLL filter components and for bypassing the analog supply voltage. The 0.1 µF bypass capacitor is in a 1206 form factor. R_{FLT}, C_{FLT}, C_{RIP}, and the 1000 pF decoupling capacitor are in an 0805 form factor. The traces are on the top surface of the board with the IC so that there is no via inductance. The traces themselves are short to minimize the inductance in the filter path. The VA and AGND traces extend back to their origin and are shown only in truncated form in the drawing.

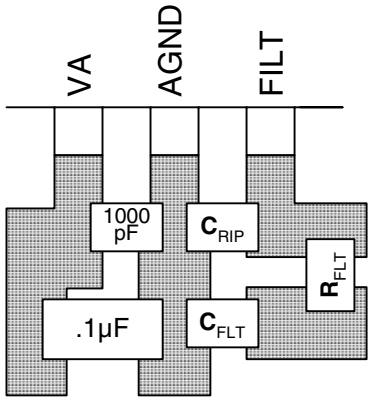


Figure 24. Recommended Layout Example

19.2.4. Component Value Selection

The external PLL component values are listed in Table 6.

Range (kHz)	R_{FLT}	C_{FLT}	C_{RIP}	Settling Time
32 - 192	3 kΩ	22 nF	1 nF	4 ms

Table 6. External PLL Component Values

19.2.5. Jitter Attenuation

Shown in Figure 25 is the jitter attenuation plot. The AES3 and IEC60958-4 specifications state a maximum of 2 dB jitter gain or peaking.

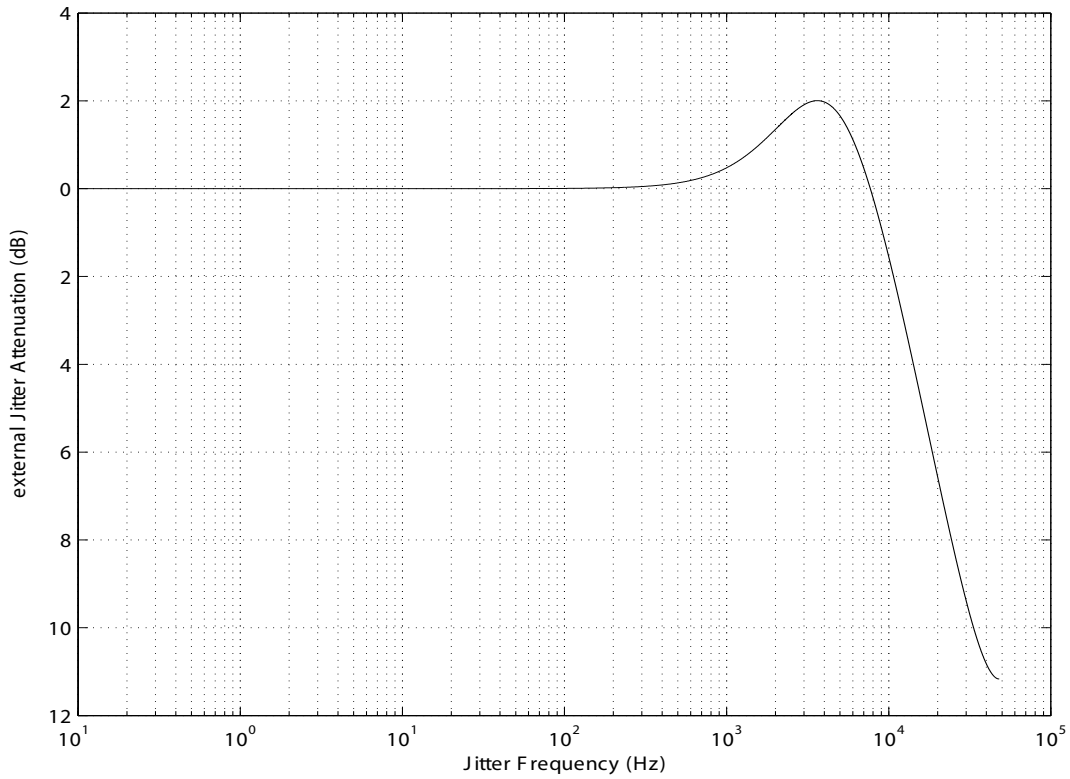


Figure 25. Jitter Attenuation Characteristics of PLL

• Notes •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