Application Note **MSAN-141**

Implementation Details of the MT8930B/31BS/T Interface

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Contents

Introduction

The Integrated Services Digital Network is being developed to provide a full range of telecommunication services over an all digital network. The key element to this fully digital network is to provide service integration using a global standardized set of user access interface points. These standardized interfaces are revealed in the ISDN User Access Reference Model explained in detail in Application Note MSAN-128, *"Implementing an ISDN Architecture Using the ST-BUS"*.

An essential element to the ISDN evolution is to provide service to all end users while keeping the cost affordable. To minimize the cost, ISDN must utilize the existing network to its fullest and choose the most economical set of digital interfaces. As these interfaces become standardized, Zarlink Semiconductor is committed to supply silicon for every interface point in the ISDN model.

The Subscriber Network Interface Circuit (SNIC) is a four wire interface which terminates the on premise subscriber loop. As such, it finds applications in digital telephone sets, digital PABX line cards, low rate multiplexer and in the NT1/NT2 functional block of the ISDN reference model. This application note deals with the functional details of the MT8930B/31B as well as the network specification at the Subscriber Network Interface. In order to take full advantage of the contents of this note, reference must be made to the MT8930B/31B data sheets.

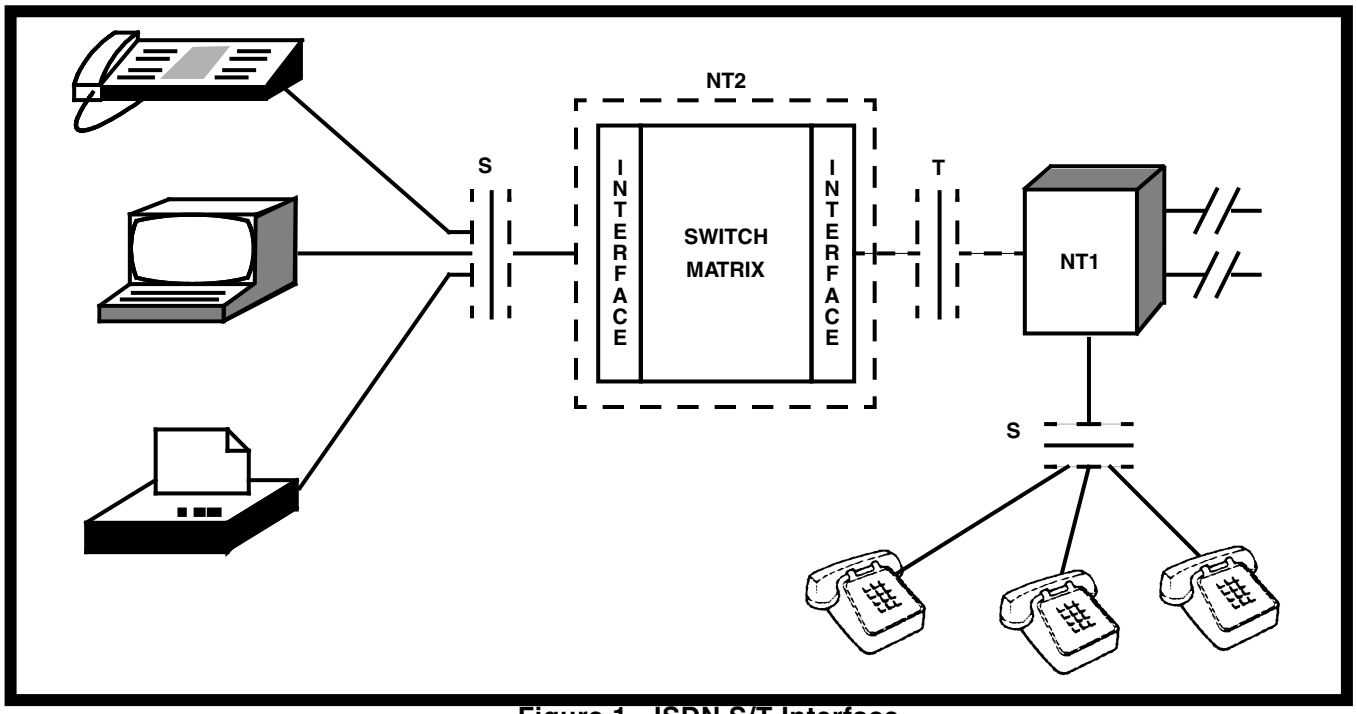


Figure 1 - ISDN S/T Interface

TABLE OF CONTENTS

1.0 MT8930B/31B S/T-Interface Transceiver

The MT8930B/31B Subscriber Network Interface Circuit (SNIC) is a multifunction transceiver providing a complete interface to the S/T Reference Point as specified in CCITT Recommendation I.430 and ANSI T1.605. Implementing both point-to-point and point-to- multipoint voice/data transmission, the SNIC may be used at either end of the digital subscriber loop. A programmable digital interface allows the MT8930B/31B to be configured as a Network Termination (NT) or as a Terminal Equipment (TE) device.

The physical medium for the S-interface is a balanced line for each direction of transmission capable of supporting 192 kbit/s which will now be referred to as the S-Bus. This transmission facility is time division multiplexed in order to carry 2 x 64 kbit/s B-channels and 1 x 16 kbit/s D-channel. Transmission capability for both B and D channels, as well as related timing and synchronization functions, are provided on chip. The signalling capability and procedures necessary to enable customer terminals (TEs) to be activated and deactivated form part of the MT8930B/31B's functionality. The SNIC handles D-channel resource allocation and prioritization for access contention resolution and signalling requirements in passive bus line configurations. Control and status information allows implementation of maintenance functions and monitoring of the device and the subscriber loop.

An HDLC transceiver is included on the SNIC for link access protocol handling via the D-channel. Depacketized data is passed to and from the transceiver via the microprocessor port. Two 19 byte deep FIFOs, one for transmit and one for receive, are provided to buffer the data. The HDLC block can be set up to transmit or receive to/from either the S-interface port or the ST-BUS port. Further, the transmit destination and receive source can be independently selected, e.g., transmit to S-interface while receiving from ST-BUS. The transmit and receive paths can be separately enabled or disabled. Both one and two byte address recognition is supported by the SNIC. A transparent mode allows data to be passed directly to the D-channel without being packetized.

The MT8930B provides a controllerless mode which eliminates the need for a microprocessor. The TE mode in the MT8930B is selected by tying pin 8 to ground, or to a 4.096 MHz clock. On the other hand, the MT8931B doesn't offer a controllerless mode, but its TE mode is selected by either tying pin 8 to a 4.096 MHz clock or to a crystal connected between pin 8 and pin 7.

The MT8930B is recommended as a replacement for the MT8930 in existing systems, or for new proprietary applications where CCITT and ANSI standards don't have to be fully met. In such cases, customers may operate the MT8930B in TE mode without the use of an external clock, therefore, saving the added cost of an external oscillator.

The MT8931B, on the other hand, is recommended for new designs requiring full compatibility with CCITT and ANSI standards. The MT8931B will operate in TE mode with just a crystal, as compared to an oscillator for the MT8930B.

2.0 Access Considerations at the S-Interface

2.1 Line Code

The line code used on the S-interface is a pseudo ternary code with 100% pulse width as shown in Figure 2 below. Binary zeros are represented as marks on the line and successive marks will alternate in polarity. A mark which does not adhere to the alternating polarity is known as a bipolar violation.

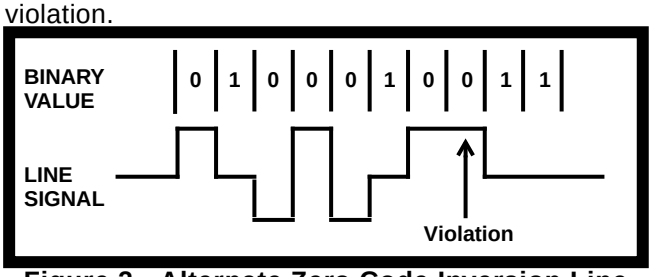


Figure 2 - Alternate Zero Code Inversion Line

2.2 Frame Structure

A valid S-Bus frame consists of 48 bits transmitted at the nominal bit rate of 192 kbit/s. This gives a 4 kHz S-Bus frame of which each B- or D-channel will consume two valid timeslots. The frame is structured using various bits which are used as follows:

F-bit: The F-bit is used to delimit the S-Bus frame boundary. The F-bit is positioned at the beginning of the frame and it can be identified very quickly because it will always be a mark which will violate the alternate line code sequence. (i.e., F-bit is a violation).

Fa-bit: The Fa-bit is the auxiliary framing bit. It is used to secure the frame position in the presence of an idle B- and D-channel following the F-bit. The Fa and N bits can

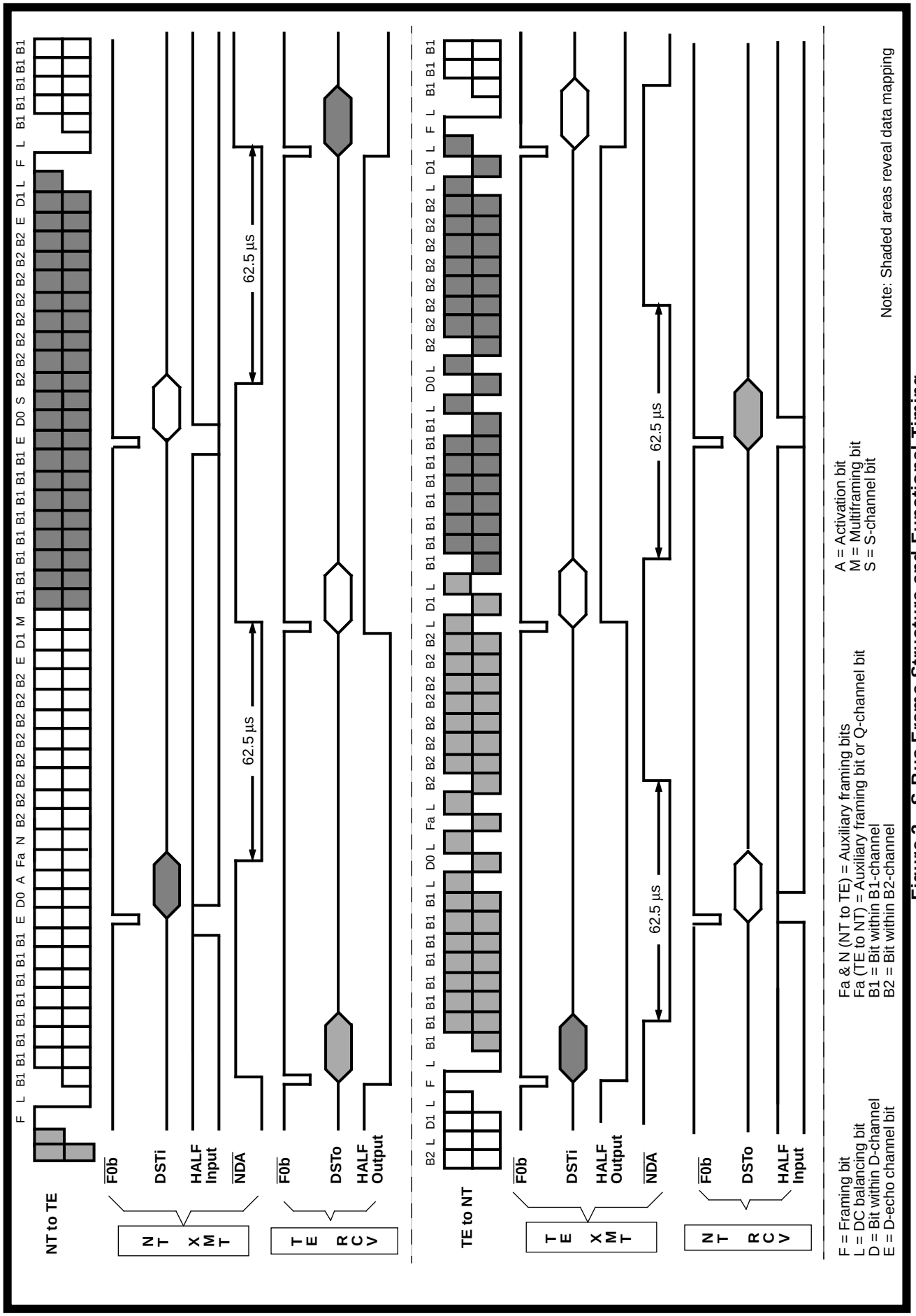


Figure 3 - S-Bus Frame Structure and Functional Timing

also be used to identify a multiframe structure which will make provisions for a low speed signalling channel to be used in the TE to NT (Q-channel) or NT to TE (S-channel).

N-bit: The N-bit is always set to complement the auxiliary framing bit. It is used in conjunction with the Fa-bit to identify a valid Q-bit.

L-bit: The L-bit is the DC balancing bit. It is used to compensate for DC content on the line. The balancing bit will be a mark if the preceding number of marks up to the previous balancing bit is odd. The L-bit in the TE to NT frame structure will also maintain a consistent pulse polarity for the first mark of every B- or D-channel.

A-bit: The A-bit is used by the NT during line activation procedures (refer to Figure 5). The state of the A-bit will advise the TE if the NT has achieved synchronization. The A-bit will be a binary zero (INFO2) if the NT is not synchronized to the TE and it will bea binary one (INFO4) if the NT is synchronized

E-bit: The E-bit is the D-echo channel. The NT will reflect the binary value of the received D-channel into the transmitted E-bit. The TEs can thus monitor the D-echo channel to establish the access contention resolution in a point-to-multipoint configuration. This is described in more detail in the section of the D-channel priority mechanism.

M-bit: The M-bit establishes the framing pattern for the second level of multiframing which is used to structure the Q and S bits. The frame with M-bit=1 identifies frame #1 in the twenty frame multiframe.

These bits are collated with the two 64 kbit B-channels and the 16 kbit D-channel as shown in Figure 3. This identifies the valid frame structure for both the NT and the TE.

2.2.1 Terminal Framing

The framing mechanism on the S-interface makes uses of line code violations to identify frame boundaries. The F-bit violates the alternating line code sequence to allow for quick identification of the frame boundaries. To secure the frame alignment, another violation of the line code sequence must occur within 14 bits after the F-bit (refer Figure 4). The next mark following the frame balancing bit (L-bit) produces this line code violation which will secure the framing pattern. If the data following the balancing bit is all binary ones, the zero in the auxiliary framing bit (Fa) will provide successive violations to assure that the 14 bit criterion specified in Recommendation I.430 and ANSI T1.605 are satisfied.

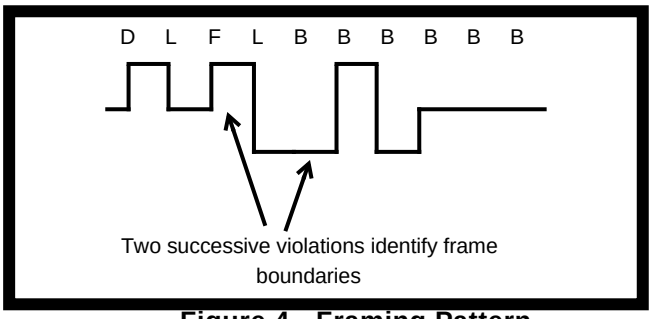


Figure 4 - Framing Pattern

The state machine used by the SNIC to establish frame synchronization is as follows. In the power-up state or in an out-of-sync condition, the terminal frame synchronization pattern (i.e., violations) must be received without error for three consecutive frames. If an invalid framing pattern is received during the frame search, it will reset the terminal framer state machine. Upon detection of the third valid framing pattern, the device will go into a synchronized state. Once in sync, it will only go out of sync if three consecutive framing patterns are received in error. The CCITT I.430 and ANSI T1.605 specifications recommend at least two invalid framing structures before declaring an out-of-sync condition. But since the NT can miss a framing pattern during a multiframe sequence (i.e., idle B1-channel, Idle D-channel with Q-bit=1), two framing patterns in error provides very little noise margin.

In a noisy environment, the out-of-sync criteria can be disabled by selecting the ”force sync” option (B5 of C-channel Control Register). With the force sync option enabled, the SNIC will lock on to the boundaries of the received frame thus maintaining a synchronized state as long as this option is selected. This function essentially locks the receive counters, thus the device will not synchronize if the Force Sync option is enabled during an out-of-sync condition.

2.2.2 Multiframing

The SNIC has provisions for the detection and generation of the multiframing pattern. This same multiframe will provide a layer 1 signalling capability using the S-bit, from NT to TE, and the Q-bit, from TE to NT.

The multiframe consists of a five S-Bus frame multiframe. Upon detection of the multiframe signal,

the TE will replace the next Fa-bit to be transmitted with the Q-bit, while the NT will insert the S-channel into the S-bit.

The multiframing structure consists of five S-Bus frames which can be identified by the binary inversion of the Fa and N-bit on the first frame of the multiframe in the NT to TE frame structure, i.e., Fa = binary 1 (Space) with N = binary 0 (Mark). This is activated by setting bit B1 of the NT C-channel Control Register to a binary one once every five S-Bus frames. (Note that the TxMFR bit must be set to binary 0 for four of the five frames in order for the multiframing of the SNIC to function normally.) Upon activation of the multiframe signal, the NT can use the S-bit to forward the S-channel towards the TE.

Upon detection of the multiframe structure, the TE will replace its transmitted Fa-bit with the transmit maintenance channel (Q-bit) found in the TE mode C-channel Control Register. (The TxMCH bit must be updated every five S-Bus frames to maintain continuity in the Q-channel.)

Structuring the Q-channel is achieved with a second level of multiframing using the M-bit found in the NT to TE frame structure. These bits are defined in Table 1. Below is an explanation on how the MT8930B/31B handles multiframing. Note that all write and read cycles to the device must be done when the $\overline{NDA}$ signal is low.

1) Multiframing procedure on the NT side.

Before activation of the S-Bus, the HALF bit in the C-channel Control Register should be set to '1'. In successive ST-BUS frames, this bit should alternate between '1' and '0' in every other ST-BUS frame. The microprocessor must keep track of when HALF is '1' or HALF is '0'. This task is needed because the device makes use of the state of the HALF bit to transmit the multiframe bits.

To start a multiframe, the TxMFR bit should be set to '1' in the same $\overline{NDA}$ window when '0' is to be written to the HALF bit. The device will then set the Fa and N bits on the line to '1' and '0' respectively. This action will alert the TE to be ready to receive a multiframe. The M/S bit in the C-channel control Register should be used to complete the structuring of the multiframe as shown in Table 1 by transmitting M and S bits. The M/S bit transmits the M bit on the S-Bus when HALF is '0', and the S bit when HALF is '1'.

The received Q-channel from the TE is presented in the RxMCH bit of the C-channel Status Register. It

FRAME #	NT→TE F_a-bit	NT→TE M-bit	NT→TE S-bit	TE→NT F_a-bit
1	1	1	SC11	Q1
2	0	0	SC21	0
3	0	0	SC31	0
4	0	0	SC41	0
5	0	0	SC51	0
6	1	0	SC12	Q2
7	0	0	SC22	0
8	0	0	SC32	0
9	0	0	SC42	0
10	0	0	SC52	0
11	1	0	SC13	Q3
12	0	0	SC23	0
13	0	0	SC33	0
14	0	0	SC43	0
15	0	0	SC53	0
16	1	0	SC14	Q4
17	0	0	SC24	0
18	0	0	SC34	0
19	0	0	SC44	0
20	0	0	SC54	0
1	1	1	SC11	Q1
2	0	0	SC21	0
:	:	:	:	:

Table 1. Multiframe Structure

should be read in the same $\overline{NDA}$ window when '0' is to be written to the HALF bit. Please note that data written to the TxMFR and M/S bits are latched internally and will be repeated in every S-Bus frame unless they are rewritten by the microprocessor. It is the responsibility of the microprocessor to structure the multiframe bits (setting and resetting the TxMFR and M/S bits in corresponding frames) to conform to the format shown in Table 1.

2) Multiframing procedure on the TE side.

In TE mode, the HALF bit in the C-channel Status Register is an output. The microprocessor needs only to monitor the RxMFR bit in the Status Register for the start of the multiframe. The M and S bits from the NT will be received in the M/S bit of the status register. The state of the HALF bit is used to indicate when the M/S bit presents the M bit or when it presents the S bit. The TxMCH bit in the C-channel Control Register is used to transmit the Q-channel bit to the NT. Note that the TE SNIC will automatically replace the TxMCH bit with the Fa bit on the S-Bus frame when the start of a multiframe is received from the NT (when RxMFR bit is set to '1', while HALF bit is '0').

2.3 State Activation Machine

CCITT Recommendation I.430 and ANSI T1.605 have defined the activation protocol required on the S/T interface. This protocol is defined in the form of information signals termed INFO0 through INFO4. These signals are defined in Figure 5.

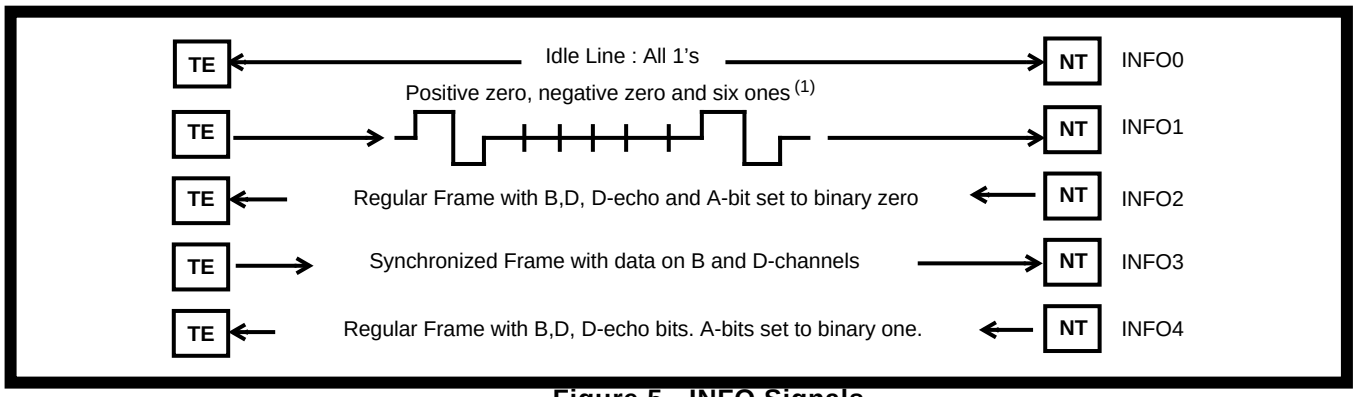


Figure 5 - INFO Signals

Note (1): For MT8930B, the frequency of the INFO1 signal may deviate by up to 50% of the nominal frequency if pin CK is connected to ground as opposed to a 4.096 MHz clock.

2.3.1 State Machine

In the NT mode, asserting the Activation Request (AR=1) bit will result in the transmission of the INFO2 signal after the first occurrence of the system frame pulse ($\overline{F0i}$). As long as the Deactivation Request bit is not asserted (DR=0) on the TE, the remote terminal will synchronize to INFO2 and respond with INFO3. If the TE fails to synchronize to the incoming signal after a timeout period determined by the user, the DR bit of the NT should be set to 0 in order to respond with INFO0.

In the TE mode, AR=1 established from the management entity, will result in the transmission of the INFO1 signal after the first occurrence of the system frame pulse ($\overline{F0i}$). If DR =0 on the NT side of the loop, the Network Terminator will detect the presence of Bus Activity (BA) and respond with INFO2. (Note that the NT need not synchronize to the incoming INFO1 signal.) This will allow the activation of the line even if a collision occurred during multiple INFO1 signals. If the NT does not respond to the INFO1 before a software defined timeout period (30 seconds worst case value), the DR on the TE should be set in order to return to sending INFO0.

When the NT responds to INFO1 with the INFO2 signal, the TEs will synchronize to the line signal and respond with INFO3. At this point, the activation state machine responds in the same way as though the NT had initiated the activation.

During fault conditions, the state machine responds as follows. If the NT loses sync with the incoming data signal, it will return to sending INFO2. If the TE loses synchronization with the incoming data, it immediately stops sending INFO3 and sends INFO0.

The progression through the state machine can be monitored using the binary encoded state sequence for the respective mode of operation.

In the NT mode, the binary encoded states (see Table 2) are as follows:

IS0	IS1	
0	0	- deactivated (G1)
0	1	- pending deactivation (G4)
1	0	- pending activation (G2)
1	1	- activated (G3)

When NT is in a deactivated state it is receiving and transmitting the INFO0 signal. In pending activation state the NT transmits the INFO2 signal while trying to sync to INFO3. This state is only active if the DR=0. In activated state the device is synchronized to the remote TEs. This implies that it is transmitting INFO4 while receiving INFO3. This state can only be entered if the DR=0. If the DR =1, the state machine will enter the pending deactivation state (if not already in the deactivated state). This implies that the NT will be transmitting INFO0 while receiving INFO3 until the TE can recognize the DR. The device will remain in this state until it receives INFO0 from the TE or the 32 ms timer expires. If after 32 msec., the TE has not responded to the DR the NT will go into the deactivation state. The NT must enter the deactivated state before activation can be reinitiated.

State	G1	G2	G3	G4
INFO Sent	I0	I2	I4	I0
Act. Req.	G2	/	/	G2
Deact. Req.	/	T2;G4	T2;G4	/
T2 Expiry	--	--	--	G1
Rcv. INFO0	--	--	G2	G1
Rcv. INFO1	G2	--	/	--
Rcv. INFO3	/	G3	--	--
Lost Sync	/	/	G2	--

Table 2. NT State Machine

Note: -- = No change
/ = Not applicable
T2 = Start Timer 2

State	F3	F4/5	F6/8	F7
INFO Sent	I0	I1 or I0 if BA	I0 or I3 if SYNC	I3
Act. Req.	F4/5	/	/	G2
Deact. Req.	/	F3	F3	F3
Rcv. INFO0	--	--	F3	F3
Rcv. any signal	--	F5	--	/
Rcv. INFO2	F6/8	F6/8	--	F6/8
Rcv. INFO4	F6/8	F6/8	F7	--
Lost Sync	/	/	--	F6/8

Table 3. TE State Machine

Note: -- = No change
/ = Not applicable
BA = Bus Activity
Sync = Synchronization
Any signal = reception of three zeros in any 48-bit interval

In the TE mode, the binary encoded states (see Table 3) are as follows:

IS0	IS1	
0	0	- deactivated (F3)
0	1	- synchronized (F6/8)
1	0	- activation request (F4/5)
1	1	- activated (F7)

When the TE is in the deactivated state it is sending INFO0. This can occur when NT and TE are in the power down mode and there is no activity on the line. As well, the TE will enter a deactivated state when DR=1. This causes the NT to send INFO2 until the management entity completes the deactivation procedure. In activation request state, the TE is transmitting INFO1. If this state is maintained it implies that the NT has raised the DR and is therefore not ready to receive information. In the synchronized state, the TE is receiving INFO2 from the NT and has achieved frame synchronization. If the TE remains in the synchronized state it implies that the NT has not synchronized to the INFO3 signal or that the NT is not transmitting the A-bit. Finally, in the activated state the TE transmits INFO3 while the NT transmits INFO4 and normal data transfer can take place.

The Diagnostic Register of a TE SNIC should be cleared as long as the device has not achieved full activation (state F7). This action is required to avoid placing the device accidently in one of the test modes that will prevent it from completing the activation procedure. The Diagnostic Register can be kept cleared by setting the ClrDia bit in the Control Register to 1, and keeping this bit set until full activation is declared by the device (IS0, IS1=1,1).

The preceding protocol defines all ideal conditions during activation of the line. The full state machine incorporated on the SNIC is defined in Tables 2 and 3. Note that the letters identifying the states correspond to those of I.430 and T1.605 specifications. The activation need only be initiated by the line or the user at either end (i.e., NT or TE). Progression through the state machine will be performed by the device without user intervention. (Progression will take place only if DR=0.) Activation or deactivation of the bus is granted through bits 6 and 7 of the C-channel Control Register.

Note that for the TE state machine, distinction between states F6 and F8 when IS0, IS1=0,1 can be done in two ways. By reading Sync bit (Sync=1 for F6, Sync=0 for F8), or by reading INFO0 bit (INFO0=0 for F6, INFO0=1 for F8). Similarly, distinction between F4 and F5 when IS0, IS1=1,0 can be done by reading BA bit (BA=1 for F5, BA=0 for F4), or by reading INFO0 bit (INFO0=1 for F5, INFO0=0 for F4).

2.3.2 Activation Times and Timers

In the ISDN, the NT and TE will require various timing parameters to avoid tying up the network by the overhead introduced from the various protocols. Some of these restrictions are in the form of timers while others will be realized in software. These limits consist of the following:

1. A TE in the deactivated state will respond to the receipt of INFO2 or INFO4 (in absence of errors) within a 100 ms time interval. However, a TE in the synchronized state will respond to the receipt of INFO4 within 500 µs time interval (2 frames).

2. An NT in the deactivated state must respond to the INFO1 signal within a 1 s time interval under normal conditions. Likewise, the NT will respond to the INFO3 with the transmission of INFO4 within 500 ms under normal conditions.

3. A TE in the activated state will respond to the reception of INFO0 by the transmission of INFO0 within 25 ms.
4. An NT in the activated state will respond to the reception of INFO0 or an out-of-sync condition with the transmission of INFO2 within 25 ms. The NT will not start sending INFO0 without a request from the management entity.

5. One last timing parameter exists within the NT to prevent an unintentional reactivation during a deactivation request. With reference to the state diagram, the NT will only go to the pending deactivation state upon expiry of timer 2 which must be between 25 and 100 ms.

All the time intervals mentioned above are inherent in the SNIC silicon. The response time to the INFO signals are relevant to the detection algorithms for each signals. (These algorithms are detailed in the following section.) The timer (timer 2) implemented on the SNIC, (to avoid unintentional reactivation of the NT) has been set to 32 ms which is well in the range of 25 to 100 ms specified above.

2.3.3 INFO Detection Algorithms

The activation times for the TE and the NT, are determined by the detection algorithms for the INFO0 through INFO4 signals. The detection scheme used for the INFO signals will identify the worst case detection time under no-fault conditions.

The MT8930B/31B uses a combination of an energy detection circuit in conjunction with a timer in order to detect the INFO1 signal. The detection of INFO2 relies on the convergence of the PLL as well as the framer of the MT8930B/31B. Once activity occurs on the line, the PLL will train the clocks to the correct frequency before sampling the received data. The INFO2 signal is detected upon the occurrence of a synchronized state with the AR bit set to binary"0". Therefore, under normal conditions (no errors), the worst case synchronization time is two frames following the convergence of the PLL.

The NT detects the reception of INFO3 upon the synchronization of the incoming signal. Since the PLL need not be trained, the detection of INFO3 is directly related to the synchronization algorithm.

The INFO4 signal is identified by the status of the A-bit. If the TE is synchronized to the received line signal, it will identify INFO4 on the first occurrence of the A-bit = 1_B. Therefore, the detection and reporting of the A-bit will occur within two ST-BUS frames or 250 µs.

The SNIC provides an internal signal labelled "Bus Activity". This signal will go high when three zeros are received in a time period equivalent to 48 bits or 250 µs. Receiving 128 consecutive ONEs resets this signal. This scheme allows the detection of INFO0 in about 667 µs. Bit 7 of the Mode Status Register reflects the binary value of this signal.

2.4 D-Channel Access

In a multidrop configuration, a systematic approach is required to allow competing TEs access to the single 16 kbit/s D-channel. A layer 1 priority scheme has been implemented to allocate terminal priority as well as provide contention resolution.

A TE gains access to the D-channel when it reaches its priority count. This is accomplished by monitoring the received D-echo channel (E-bit) transmitted from the NT and counting the number of consecutive binary ones. Any zero received on the E-bit will restart the counting process. The priority mechanism is based on this counting process, such that, a TE can only start transmitting once the counter is equal to, or exceeds the value of its priority class.

Any TE which is not using the on-chip HDLC, (using ST-BUS D-Channel) must request access to the D-channel by raising the DReq bit (B3 of the TE mode C-channel Control Register). The user must wait until the D-channel acknowledgment bit (Dack) (B0 of the TE mode C-channel Status Register) is received before forwarding the packet. If the TE fails to respond to the Dack within an eight bit interval, access to the D-channel may be lost as the priority count on another TE may be attained.

The priority mechanism circuitry is activated once the HDLC transmitter is enabled and data is written to the TxFIFO.

2.4.1 Priority Classes

Using the counting algorithm mentioned above, the MT8930B/31B can establish four levels of priority. These priority levels are split into two classes, which are subdivided into two levels (refer to Table 4). Only the class of priority is accessible to the user through B4 of the TE mode C-channel control register.

Class	Level	Count
High	High	8
High	Low	9
Low	High	10
Low	Low	11

Table 4. Priority Classes

The level of priority is strictly internal to the device and cannot be accessed by the user. In a priority class, the level of priority is changed from high to low when the TE has successfully completed its transmission. The level of priority is reinstated only after the priority count for the respective TE has been attained.

2.4.2 Collision Detection

The D-echo channel is also used to detect contention on the D-channel. The TEs which are trying to access the D-channel will monitor the E-bit

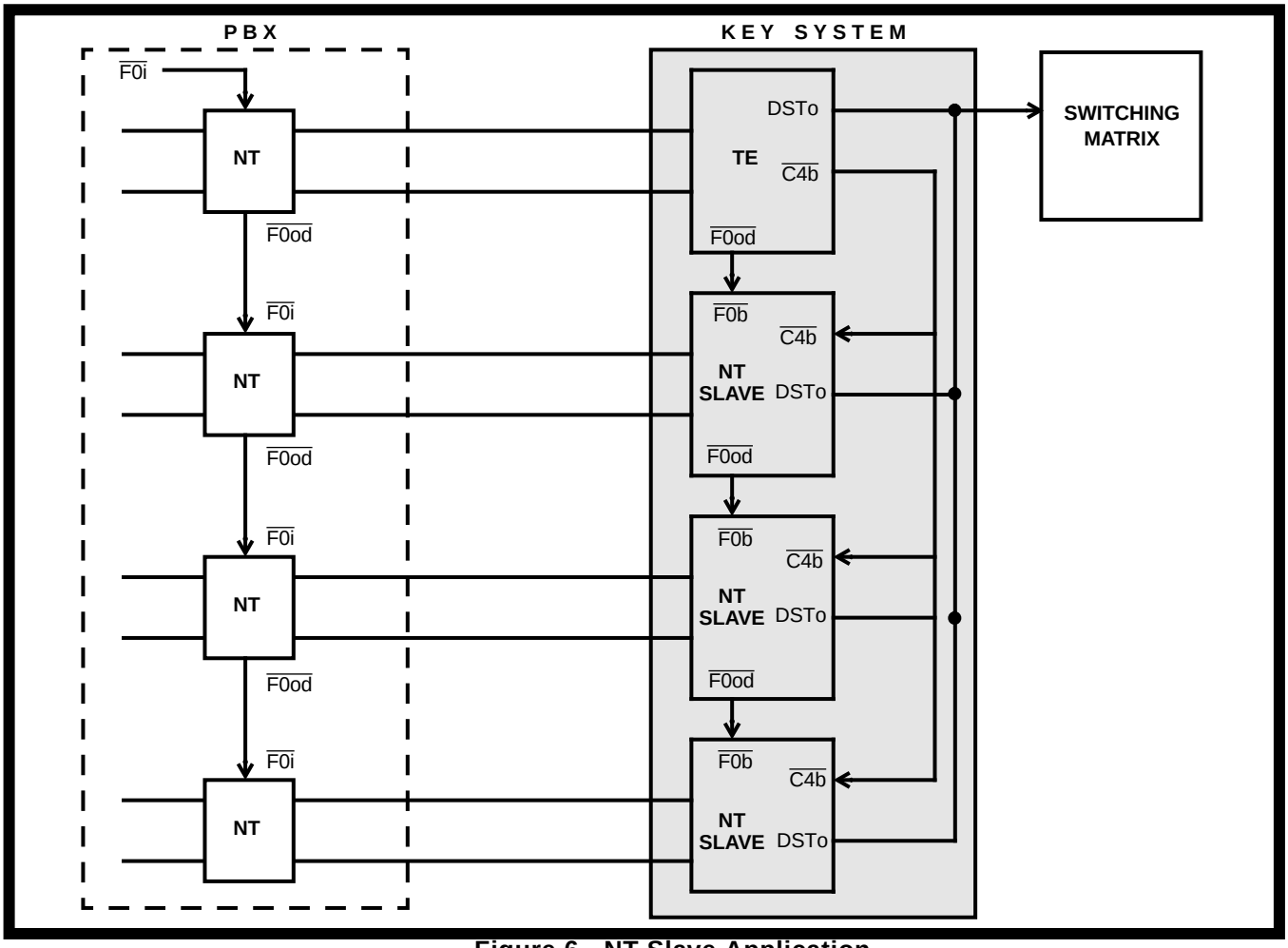


Figure 6 - NT Slave Application

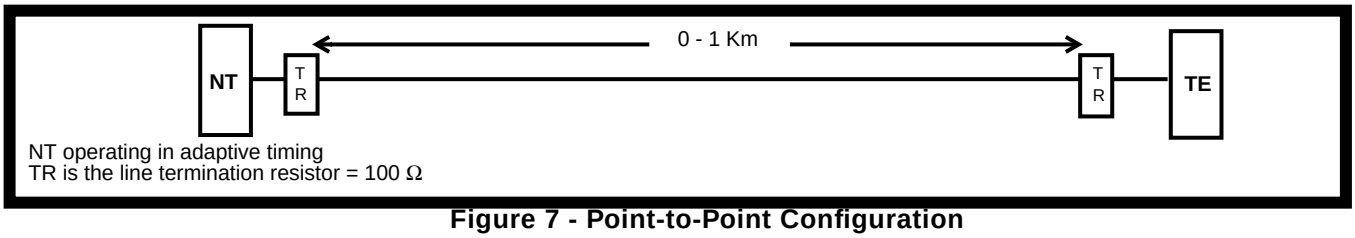


Figure 7 - Point-to-Point Configuration

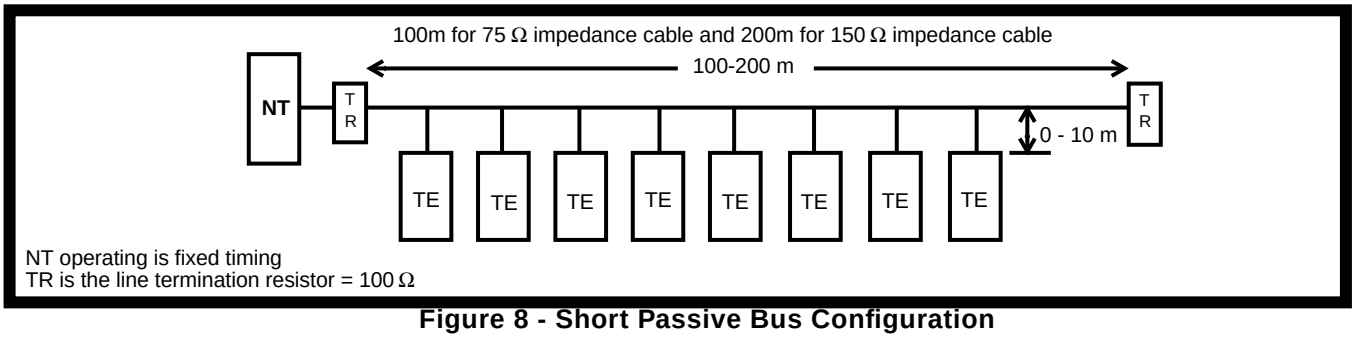


Figure 8 - Short Passive Bus Configuration

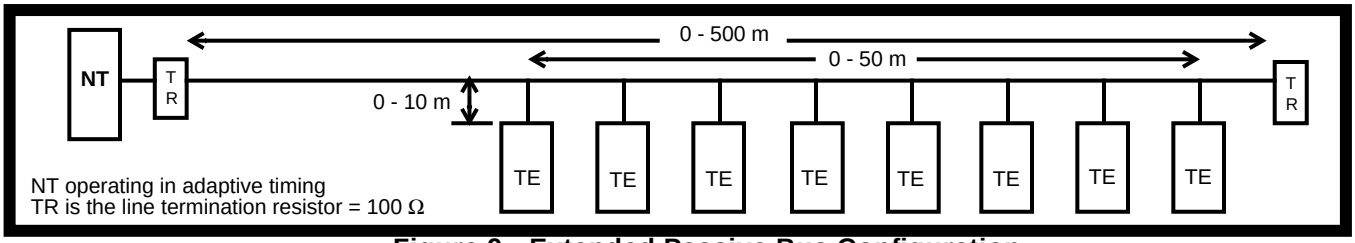


Figure 9 - Extended Passive Bus Configuration

and compare this bit with the last bit transmitted on the D-channel. If the bits are the same, the TE will continue transmitting. If the comparison differs, a collision has occurred and the TE will immediately stop transmitting on the D-channel, generate an interrupt through the Dcoll bit, reset the DCack bit on the next frame pulse, and restart the counting process. If the D-channel is sourced from the on-chip HDLC, the packet will be depleted from the FIFO without being transmitted on the S or ST-BUS.

2.5 Clocking

The subscriber loop, (S/T interface), is a fully synchronized carrier where the transmitted frame from the NT is phase aligned to the transmitted TE frame. The transmitted F-bit of each TE frame is delayed by two bits with respect to the received F-bit of the NT frame (refer to Figure 3).

In a typical application, the NT will derive its timing source directly from the network clock. A TE, on the other hand, will derive its timing from the received line signal. Certain applications, such as key systems and small PBXs, will require multiple TEs to have a phase related clock in order to make use of a common backplane. Such an option is provided in the SNIC and is called the NT slave mode.

2.5.1 NT Slave

As mentioned above, some applications require a common system clock for multiple TEs. Setting bit B1 in the NT C-channel Diagnostics Register will allow the SNIC to operate in a TE mode using external timing source. A typical configuration is described in Figure 6. The NT slaves would derive their clocks from an SNIC which is in a TE mode. The timing signals generated from the TE (i.e., $\overline{C4b}$ and $\overline{F0b}$) will be used as the system clocks for the remaining NT slaves. This allows the ST-BUS outputs to be daisy chained using $\overline{F0od}$ pulse, allowing the ST-BUS to be used as a backplane. NT slaves can tolerate up to ±2.5 µs differential delay between the receive frame at the TE providing the timebase and their own receive signal.

2.6 Loop Configurations

The wiring configuration of the subscriber loop is assumed to be one continuous cable consisting of a point-to-point or point-to-multipoint loop which will be terminated at both ends with an appropriate termination resistor (100 ohms). For a point-to-point or extended passive bus wiring configurations, the NT must be placed in the adaptive timing mode (B3 of NT C-channel control register to logic 1). This will allow the timing recovery circuit to track the phase impairment introduced by the transmission medium. In a short passive bus loop configuration this adaptive timing is an undesired effect as the line signal from the various sources will have different phase impairments. Therefore, the timing recovery circuit must not try to track the phase impairment as the phase of each bit received may vary up to 4 µsec. Therefore, in the short passive bus, the NT must be placed in a fixed timing mode. This is accomplished by setting B4 of NT C-channel Control Register to logic 0. Further descriptions of each loop configuration follows.

2.6.1 Point-to-Point

In the point-to-point wiring configuration only one NT and one TE are active at any one time for either direction of transmission (refer to Figure 7). The SNIC is placed in the point-to-point mode by setting the Timing bit (B4) of the NT mode C-channel Control Register to a binary 1. This bit will enable the adaptive timing circuit which will allow the SNIC to operate with 10 to 42 microseconds of loop delay. The maximum line length for the point-to-point bus is limited by the attenuation of the signal as well as the round trip delay introduced from the line (i.e., delay on the E-echo).

2.6.2 Short Passive Bus

The short passive bus is a point-to-multipoint wiring configuration which allows more then one TE to communicate with a single NT (refer to Figure 8). The positioning of the TEs on the short passive bus is not restricted along the full length of the cable.

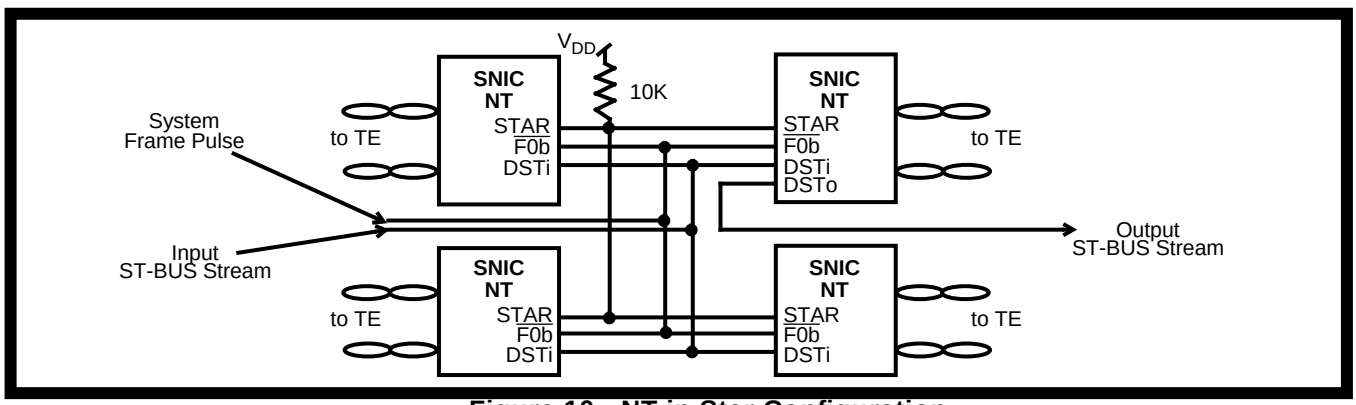


Figure 10 - NT in Star Configuration

This implies that the NT must be capable of extracting data from different sources arriving with variable delays. For this reason, the adaptive timing circuit mentioned above, must be disabled so that the receiver will not try to track the differential delays. (The adaptive timing circuit can be disabled by setting the Timing bit (B4) of the NT C-channel Control Register to a binary 0). The variable delay introduced from the various sources must not exceed a single bit period (in the presence of jitter). This delay, coupled with the built-in offset of two bits, sets the maximum round trip delay at 10 to 14 µsec. This restriction sets the maximum operational distance from the NT in the order of 100 to 200 meters depending upon cable characteristics.

2.6.3 Extended Passive Bus

A third wiring configuration is a compromise between the point-to-point and the short passive bus (refer to Fig. 9). This wiring configuration, known as the extended passive bus, is a multidrop line which can extend up to 500 meters in length. The concept behind the extended bus is to limit the differential round trip delays between the TEs to 2µs. This restricts the positioning of the TEs to a cluster or grouping of terminals at the far end of the cable having differential distance of 0-50 meters.

2.6.4 Star

For applications which require a multidrop bus expanded over an extended range, a star configuration can be implemented to increase the line length of the extended passive bus. The core of the star configuration (refer to Figure 10) is a cluster of NTs all tied together via the star pin. This will allow the NT to operate any loop configuration except the information present on the S-Bus will be reflected to all other NTs. This implies that the information transmitted by the TE on any branch of the STAR will be received by all the NTs as if they were all on the same physical S-Bus. All activation and access contention will operate normally.

3.0 SYSTEM INTERFACE

The system interface to the MT8930B/31B is the “Serial Telecom” Bus or better known as the ST-BUS. The ST-BUS is a synchronous time division multiplexed serial bussing scheme with data streams operating at 2048 kbit/s configured as 32 X 64 kbit/s channels (refer to Figure 11).

3.1 ST-BUS Timing

Synchronization of the data transfer on the ST-BUS is provided from a frame pulse which identifies the frame boundaries and repeats at an 8 kHz rate. (Figure 12 shows how the frame pulse ($\overline{F0b}$) defines the ST-BUS frame boundaries.) All data is clocked into the device on the rising edge of the 4096 kHz clock ($\overline{C4b}$) three quarters of the way into the bit cell, while data is clocked out on the falling edge of the 4096 kHz clock at the start of the bit cell.

All timing signals (i.e., $\overline{F0b}$ & $\overline{C4b}$) are bidirectional denoted by the terminating b). The I/O configuration of these pins is controlled by the mode of operation (NT or TE). In the NT mode, all synchronized signals are supplied from an external source and the SNIC uses this timing to transfer

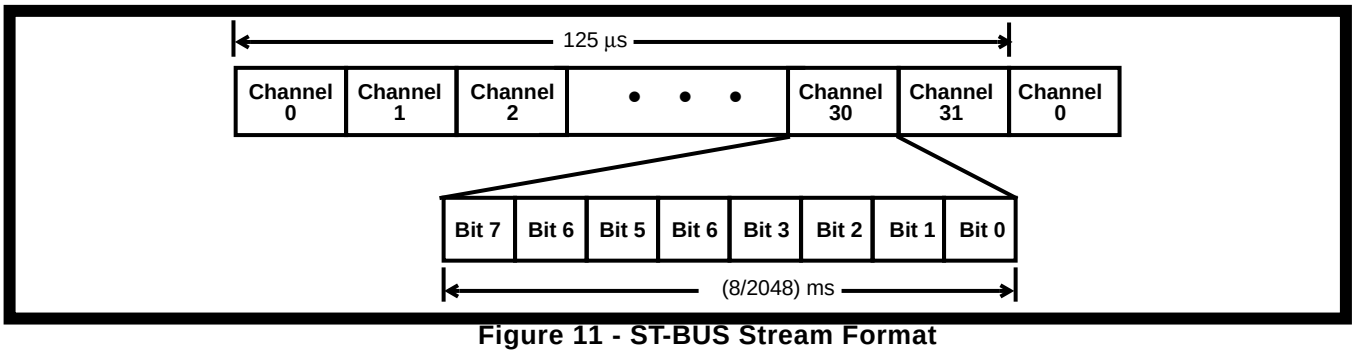


Figure 11 - ST-BUS Stream Format

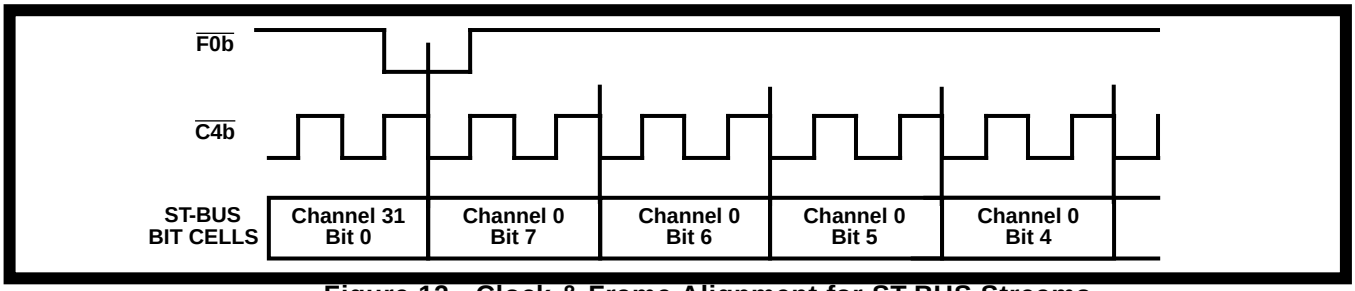


Figure 12 - Clock & Frame Alignment for ST-BUS Streams

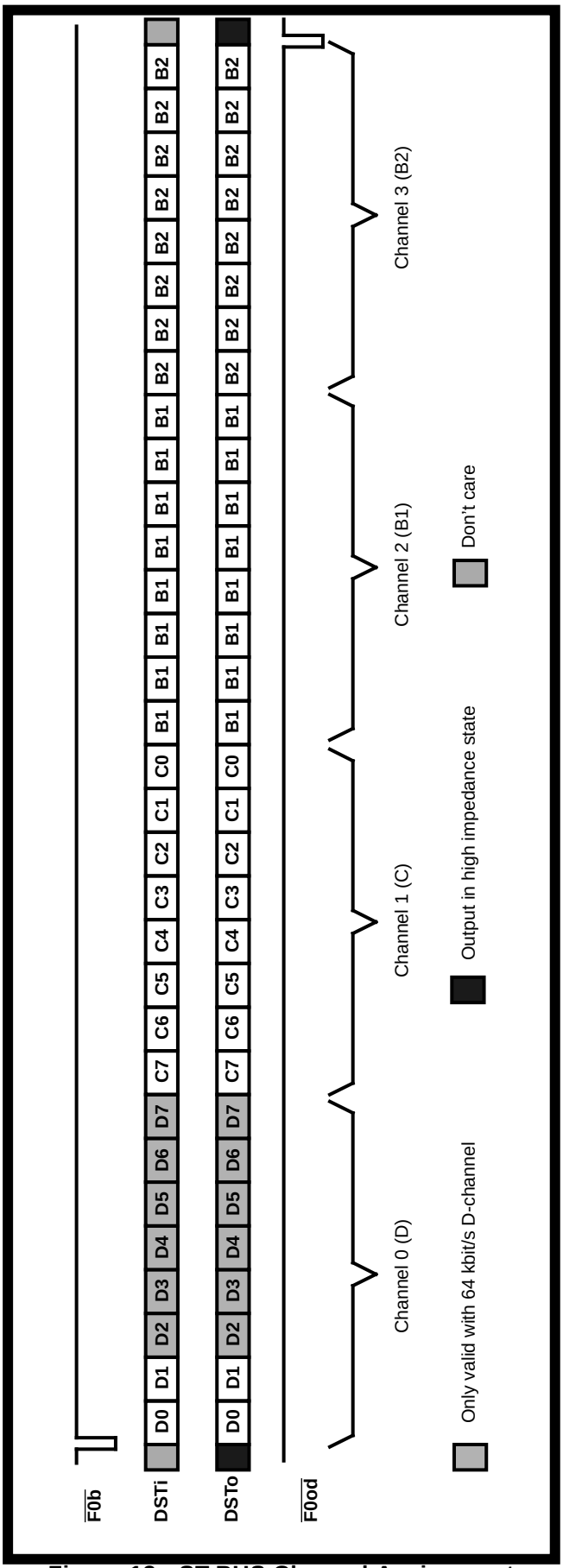


Figure 13 - ST-BUS Channel Assignment

information to and from the S or ST-BUS. In the TE mode, timing is generated from an on-board analog phase-locked loop which extracts timing from the received data on the S-Bus and generates the system 4096 kHz ($\overline{C4b}$) and frame pulse ($\overline{F0b}$). The analog phase-locked loop also maintains proper phase relation between the timing signals as well as filtering out jitter which may be present on the received line signal. Please refer to section 5.3 “PLL and Jitter” for more details.

3.2 Channel Assignment

The SNIC makes use of three types of channels to transmit and receive data and control/status to and from the S-interface port. These are the B, D and C-channels.

The B1 and B2 channels each have a bandwidth of 64 kbit/s and are used to carry PCM voice or data across the network.

The D-channel is primarily intended to carry signalling information for circuit switching through the ISDN network. The SNIC provides the capability of having a 16 kbit/s or full 64 kbit/s D-channel by allocating the B1-channel timeslot on the S-Bus to the D-channel.

The C-channel provides a means for the system to control and monitor the functions of the SNIC. This control/status channel is accessed by the system through the ST-BUS or microprocessor port. The C-channel provides access to two registers which provide complete control over the state activation machine, the D-channel priority mechanism as well as the various maintenance functions. These channels are transferred to the SNIC using the first four channels on the DSTi and DSTo lines of the ST-BUS interface (refer to Figure 13). To simplify the channel assignment of a full ST-BUS stream, the SNIC supplies a delayed frame pulse ($\overline{F0od}$) which can be used in a daisy chain configuration. The first SNIC in the chain will receive the system frame pulse with the following devices receiving its predecessor’s delayed output frame pulse ($\overline{F0od}$).

3.3 System to Line Mapping

In order for system designers to get a better understanding of the inherent delays introduced by the S/T interface, a detailed explanation of the throughput delays of the MT8930B/31B are required. Figure 3 is divided into two sections with each section having the respective line signal, transmitter timing signals and remote receiver timing signals. Since the S-Bus has a 4 kHz frame, the valid

channels on the ST-BUS can be mapped into either half of the S-Bus frame. For this reason, a HALF signal is required to identify the source or destination of the ST-BUS channels on the S-Bus frame. Figure 3 reveals the frame mapping between the ST-BUS system interface and the S-Bus line port for both the NT and TE simultaneously under zero line length condition.

3.3.1 Frame Mapping

Figure 3 reveals the functional timing diagram which uses shading to identify the ST-BUS frame mapping into the S-Bus for both the transmission of NT and TE frames (at zero line length). Although the diagram is split into separate sections, the phase relationship between NT and TE frames cannot be ignored.

For the NT transmit S-Bus frame, the ST-BUS mapping is dependent on the state of the HALF signal as input during frame pulse. If HALF=1, the ST-BUS frame being received on DSTi is transmitted on the second half of the current S-Bus frame. (This implies that the M/S-bit of the C-channel control register will be mapped into the S-bit). If HALF=0, the ST-BUS frame being received on DSTi is transmitted in the first half of the next S-Bus frame. (This implies that the M/S-bit of the C-channel control register will be mapped into the M-bit). If the HALF pin is tied to V_{DD} or V_{SS}, an internal HALF signal will establish the mapping of the ST-BUS on to the S-Bus frame. A transition on the HALF pin will overrule the internal signal and cause the S-Bus frame to be repositioned accordingly. (This HALF signal can also be accessed using B2 of the NT mode C-channel Control Register.)

The information being transmitted from the NT, is received by the TE and is output to the ST-BUS with a delay of a little more than a couple of bits. This can be seen in the diagram where the received B- and D-channels are output on the ST-BUS frame following the reception of this data on the S-Bus port. Any delay introduced from the transmission line will be added to this throughput delay.

For the TE transmit S-Bus frame, data mapping of the ST-BUS to S-Bus frame is again relevant to the state of the output on the HALF pin (sampled on the falling edge of the $\overline{C4b}$ clock within the frame pulse low window), or the HALF bit in the Status Register. When HALF=1, information on DSTi will be routed to the second half of the S-Bus frame. (Since the $\overline{F0b}$ pulse occurs at the S-Bus frame boundary, the transmit throughput delay is a minimum of 125 µs.) Conversely, if HALF=0, the information on DSTi will be routed to the first half of the S-Bus frame.

With zero line length, the transmission delay for the TE transmit S-Bus frame will have a nominal delay of two 192 kbit/s bit periods relative to the NT transmit S-Bus frame. (This is seen by lining up the NT transmit and TE transmit S-Bus frames relative to the TE ST-BUS frame pulse.) The S-Bus frame is received on the NT and is output on the ST-BUS (DSTo) with the delay shown in Figure 3.

Using Figure 3, the end-to-end delay introduced by the interfaces (at zero line length) can be calculated as follows:

1. From the NT, a channel under test will experience delay from the NT DSTi to the TE DSTo of approximately 208.33 µs, (i.e., 1 X 125 µs + 16 X 1/192kbit/s).

2. The delay from the TE DSTi to the NT DSTo of approximately 292 µs, (i.e., 2 X 125 µs + 8 X 1/192kbit/s).

This yields a total end-to-end throughput delay with zero line length of 500 µs.

3.3.2 Channel Mapping

As mentioned earlier, the SNIC uses the first four ST-BUS channels following the framing pulse to carry the D, C and two B-channels. Under normal operation, the two B-channels from the ST-BUS will be transmitted and received on the S-Bus while the D-channel will be transmitted/received from the FIFOs of the HDLC formatter. If the D-channel is to be sourced externally, the HDLC formatter can be bypassed which will provide a 16 kbit/s data path (two least significant bits of the 64 kbit/s channel) from the ST-BUS to S-Bus and vice-versa. The HDLC formatter is bypassed by disabling both the HDLC transmitter and receiver (B6 and B7 and the HDLC Control Register 1 are set to”0”).

If the D-channel requires more bandwidth, the DinB feature can be set in the SNIC (B5 of C-channel Control Register) which will place the 64 kbit/s D-channel in the B1 timeslot. This has the effect of replacing the B1-channel on the S-Bus with the active 64 kbit/s D-channel received on the ST-BUS input. With the DinB option active, the 16 kbit/s D-channel on the S-Bus will be placed in an idle mode and cannot be accessed until the function is disabled.

4.0 CONTROL INTERFACE PORT

Both the MT8930B and MT8931B have a microprocessor port. However, the parallel port on the MT8930B operates as either a general purpose microprocessor interface or as a hardwired control/ status port.

4.1 Microprocessor Port

An 8 bit microprocessor port with multiplexed address and data bus provides a secondary system interface to the SNIC. Full access is granted to all I/O channels of the S-Bus or ST-BUS. The data received on the S-Bus is stored in a temporary register before being shifted out onto the ST-BUS. It is this register which is accessed through the microport, thus explaining the timing restriction on the “synchronous registers”. The same configuration is used for data received on the ST-BUS directed to the S-Bus. This implies that the data will default from S-Bus to ST-BUS and vice-versa unless the processor intervenes. The microprocessor also has unique access to the on-board HDLC formatter.

4.1.1 Motel Bus

In microprocessor control mode, the parallel port is compatible with either the Motorola or Intel multiplexed bus signals and timing. The MOTEL circuit (**MO**torola and In**TEL** compatible bus) on the SNIC converts the external parallel bus to a consistent internal time base regardless of the type of processor being used.

The MOTEL circuit uses the level of the DS/$\overline{RD}$ pin at the rising edge of AS/ALE to select the appropriate bus timing. If DS/$\overline{RD}$ is low at the rising edge of AS/ALE then Motorola bus timing is selected. Conversely, if DS/$\overline{RD}$ is high at the rising edge of AS/ALE, then Intel bus timing is selected. This has the effect of redefining the microprocessor port transparently to the user.

4.1.2 Memory Map

As mentioned above, the SNIC has multiple registers which are used to monitor and control the various functions of the SNIC as well as provide access to the multiple data channels directed at either the S-Bus or the ST-BUS ports. These registers are located in specific address locations as shown in Table 5. This memory map shows two types of registers, one being the synchronous access (registers which are accessible from a serial port) and the second being the asynchronous access registers (relevant to the HDLC and Master Control).

4.1.2.1 Synchronous Access

The synchronous registers have constraints with respect to the reading and writing to the registers.

	Address Lines					Write	Read
	A4	A3	A2	A1	A0		
	0	0	0	0	0	Master Control Register	verify
A	0	0	0	0	1	ST-BUS Control Register	verify
S	0	0	0	1	0	HDLC Control Register 1	verify
Y	0	0	0	1	1	HDLC Control Register 2	HDLC Status Register
N	0	0	1	0	0	HDLC Interrupt Mask Register	HDLC Interrupt Status Register
C	0	0	1	0	1	HDLC Tx FIFO	HDLC Rx FIFO
	0	0	1	1	0	HDLC Address Byte #1 Register	verify
	0	0	1	1	1	HDLC Address Byte #2 Register	verify
	0	1	0	0	0	C-channel Control Register	
	0	1	0	0	1		C-channel Status Register
	1	0	0	0	0	Control Register 1	Not available
	1	0	0	1	0	Not Available	Master Status Register
	0	1	0	0	0		DSTi C-channel
	0	1	0	0	1	DSTo C-channel	
S	0	1	0	1	0	S-Bus Tx D-channel	DSTi D-channel
Y	0	1	0	1	1	DSTo D-channel	S-Bus Rx D-channel
N	0	1	1	0	0	S-Bus Tx B1-channel	DSTi B1-channel
C	0	1	1	0	1	DSTo B1-channel	S-Bus Rx B1-channel
	0	1	1	1	0	S-Bus Tx B2-channel	DSTi B2-channel
	0	1	1	1	1	DSTo B2-channel	S-Bus Rx B2-channel

Table 5. SNIC Address Map

Since the same physical register is used to receive data from the ST-BUS and transmit this information to the S-Bus, the register can not be accessed while the information of the register is being shifted in or out of the line or system ports. Therefore, the New Data Available ($\overline{NDA}$) signal is generated from the MT8930B/31B which will guarantee access to all synchronous registers. The $\overline{NDA}$ signal is output on the $\overline{IRQ}$, $\overline{NDA}$ pin only if this feature is enabled through B2 of the master control register (B2=1). In certain applications, the timing constraint placed on the microprocessor access to the various registers may leave insufficient time to access all relevant registers. In this situation, specific registers can be accessed outside the $\overline{NDA}$ window. The timing for these registers is provided in Figure 14.

4.1.2.2 Asynchronous Access

The asynchronous registers, on the other hand, are those registers which may be accessed at any time. These registers are mainly used to establish the mode of the microport or to manipulate the HDLC formatter.

4.1.3 Bit Orders

When using the B-channels for PCM voice, the first bit to be transmitted on the S-Bus should be the sign bit. This complies with the existing telecom standards which transmit PCM voice as most significant bit first. However, if the B-channels are to carry data, the bit ordering must be reversed to comply with the existing datacom standards (i.e., least significant bit first).

These contradicting standards place a restriction on all information input and output through the serial and parallel ports. Information transferred through the serial ports, will maintain the integrity of the bit order. Data sent to either serial port from the parallel port, will transmit the least significant bit first. Therefore, a PCM byte input through the microprocessor port must be reordered to have the sign bit as the least significant bit.

The D-channel received on DSTi must be ordered with the least significant bit first as shown in Figure 13. This also applies to the D-channel directed to DSTo from the microprocessor port.

The C-channel bit mapping from the parallel port to the ST-BUS is organized such that the most significant bit is transmitted or received first.

4.2 Controllerless Mode

This option is available only in the MT8930B. It allows the SNIC to function without the need of a controlling processor. The C_{mode} pin is used as the select input to the multiplexer. When C_{mode} is high, the micro port reverts to the 8 bit multiplexed bus microprocessor port with all relevant timing inputs. When C_{mode} is low, the controllerless mode is selected and the parallel port reverts to a hardwired control/status port.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Synchronous Access Type A	t_{SAA}		124.75		µs	
2	Synchronous Access Type B	t_{SAB}		62.5		µs	
3	Synchronous Access Type C	t_{SAC}		109.3		µs	

Note: Type A: includes writing to DSTo, D, C, B1, and B2; and reading from the S-Bus RxD, B1, and B2.
Type B: includes writing to the S-Bus Tx B1 channel.
Type C: includes writing to the S-Bus Tx B2, and D; and reading from DSTi D, C, B1, and B2.

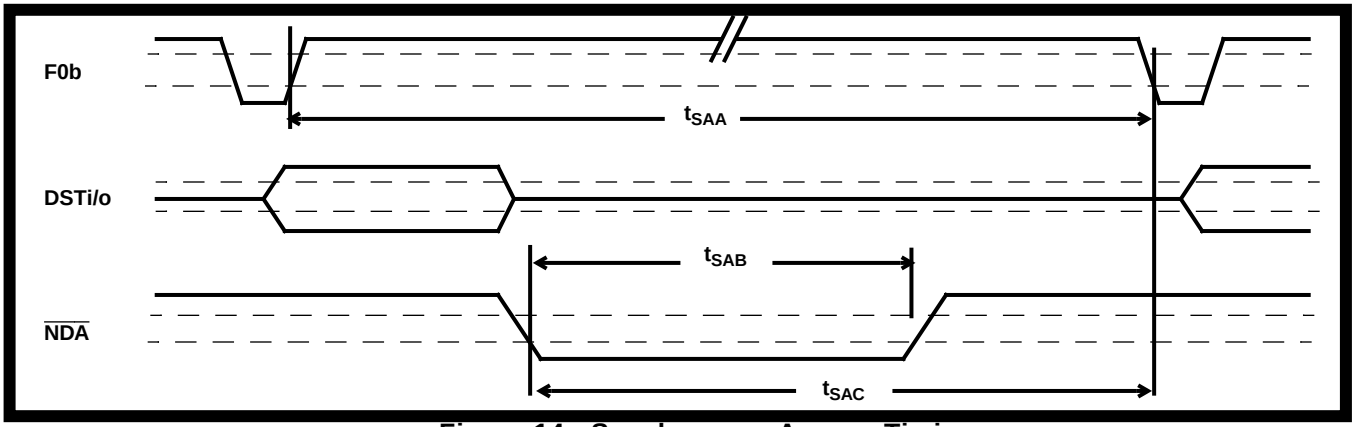


Figure 14 - Synchronous Access Timing

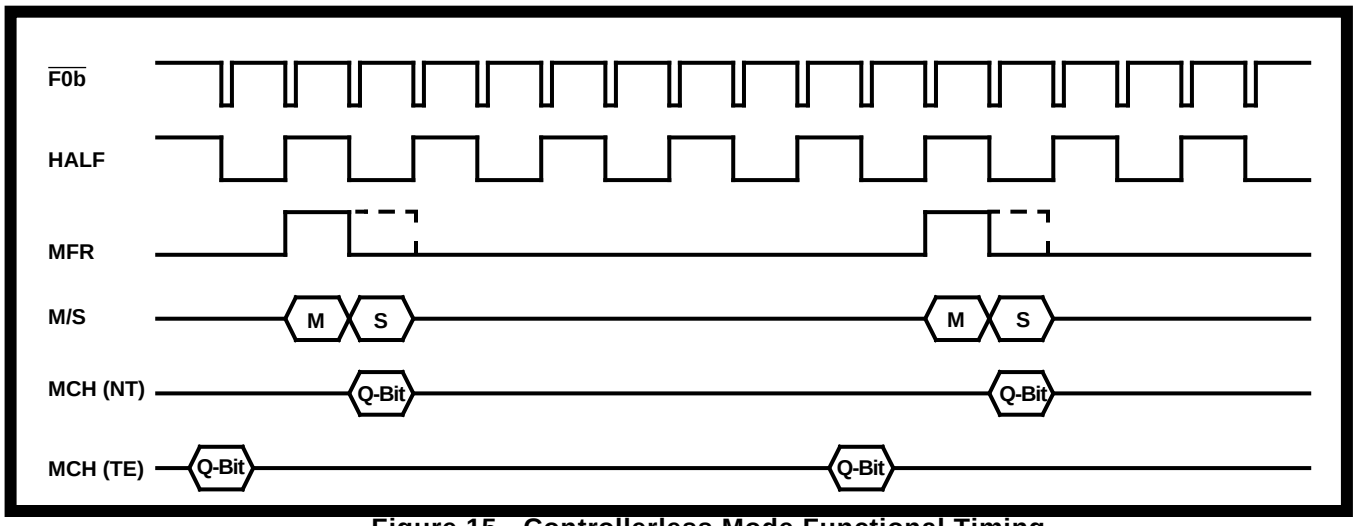


Figure 15 - Controllerless Mode Functional Timing

Note: - — - as output

In the controllerless mode, the parallel bus has direct connection to the C-channel control and status registers for either the TE or NT device. These control/status pins allow the SNIC to be configured using a discrete state machine or with manual switches. All inputs/outputs to the control port will be latched/refreshed by the SNIC on the falling edge of the $\overline{C4b}$ clock midway through the system frame pulse ($\overline{F0b}$). Figure 15 shows the timing diagram surrounding the structuring of the S- and Q-channels in the NT controllerless mode.

In the controllerless mode, the SNIC can still be controlled through the input C-channel on the system (ST-BUS) interface. The structuring of the serial control requires the P/$\overline{SC}$ pin to be tied to V_{SS}, thus rendering the remaining control pins as ”don’t cares”. The option of disabling the ST-BUS channels is not supported in the controllerless mode, therefore, all input and output channels will be enabled.

5.0 TRANSMISSION PERFORMANCE

The transmission medium for the subscriber loop is a four conductor configured as two twisted pairs.

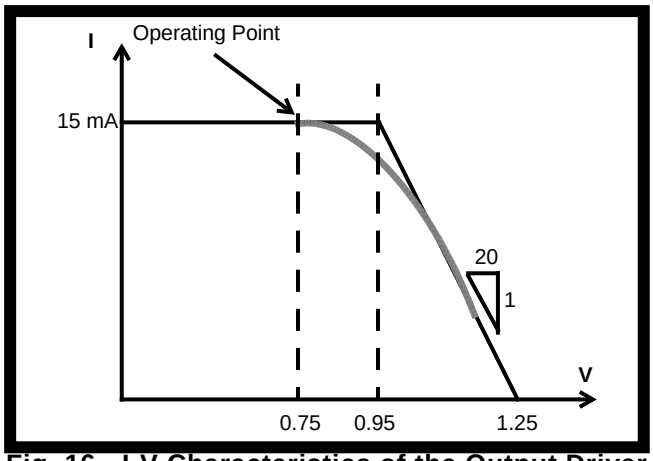


Fig. 16 - I-V Characteristics of the Output Driver

To minimize the reflection of a propagating signal, a 100 ohm termination resistor is required in order to match the characteristic impedance of the twisted pair cable.

This terminating resistor is relevant to the transmission line and is thus placed at both ends of the transmit and receive pair (refer to Figures 7 to 9). With the TE presenting a high impedance on both

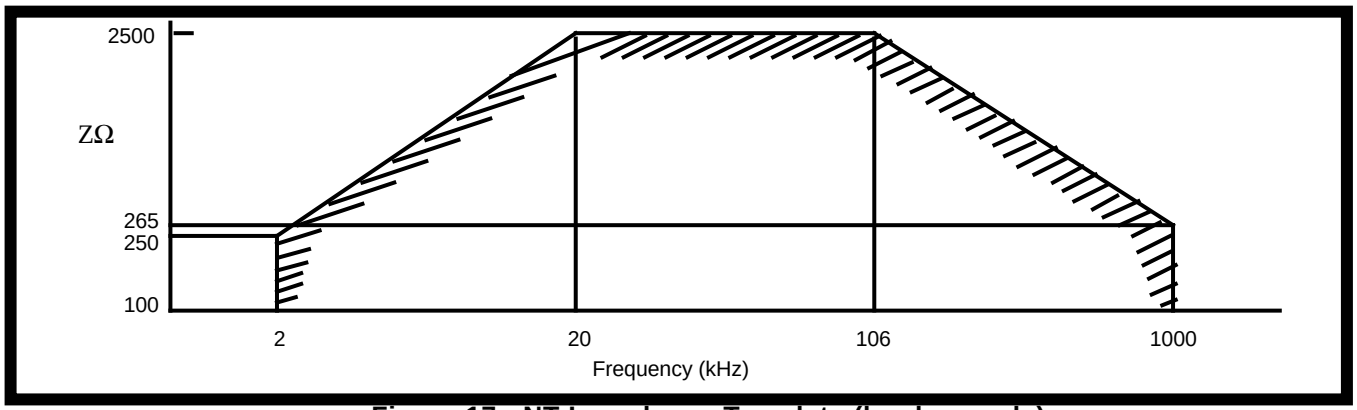


Figure 17 - NT Impedance Template (log-log scale)

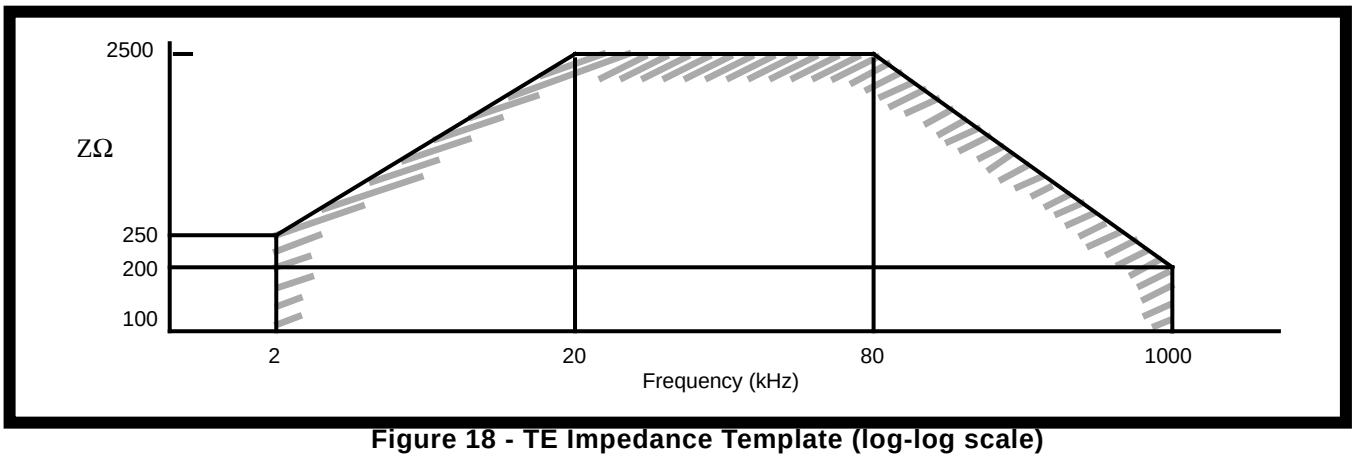


Figure 18 - TE Impedance Template (log-log scale)

the Rx and Tx lines, multiple TEs can be connected without altering the characteristics impedance of the line.

5.1 Transmitter Characteristics

The line driver incorporated on the SNIC is a temperature compensated, voltage limited current source having a typical I-V characteristics as shown in Figure 16. This I-V curve reveals that when the transmitter is active (transmitting a binary 0), the output impedance will be greater than or equal to the minimum specified impedance of 20 ohms when driving the 50 ohm load (i.e., the combination of the two 100 ohm terminating resistors). When the transmitter is inactive, the output impedance of the line driver will exceed the impedance template shown in Figure 17 for the NT and Figure 18 for the TE.

The transmitter is configured as a single-ended driver with a minimum 50 ohm series resistor (refer to Figure 19).

An external resistor of 40 ohms is used to present more than 20 ohm load impedance to the transmission line through a 2:1 transformer (assuming a DC resistance of the transformer as specified in Table 6). This single-ended drive will have the effect of reducing the power consumption by half relative to a differential drive while still producing a nominal pulse amplitude of 750 mV. The pulse shape produced by the driver (using appropriate transformer) will comply to the pulse template shown in Figure 20. (Figure 20 reveals the nominal pulse template for a transmit output pulse with overshoot limited as follows. Any overshoot on the leading edge of a pulse is permitted up to 5% of pulse amplitude where this amplitude is defined at the middle of the signal element. The overshoot must have 0.5 of its amplitude within 0.25µsec.)

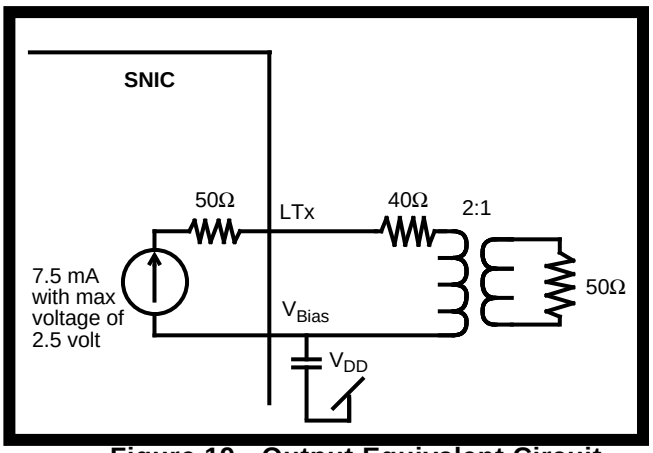


Figure 19 - Output Equivalent Circuit

5.2 Receiver Characteristics

The MT8930B/31B requires the S-Bus signal to pass through a 1:2 transformer before being applied to the bipolar line receiver. The signal from the transformer is passed through various filters and peak detectors before the data is recovered (see Figure 21).

The lowpass filter removes any pulse overshoot and noise which could effect the performance of the peak detectors. The highpass filter removes low frequency noise which may be generated by the alternate mark inversion line code. This highpass filter will also perform limited post equalization which will improve the effects of intersymbol interference over long loop lengths.

Two peak detectors, one for the positive pulses and the second for negative pulses, are used to establish an internal reference voltage which, in turn, will be used as the thresholds for the input recovery circuit. In the fixed timing mode (i.e., short passive bus) the filters and peak detectors are bypassed with an input threshold set to 30% of the nominal pulse amplitude with no line attenuation. In the adaptive timing mode the threshold for the data recovery circuit is set to 40% of the output from the peak detectors with a

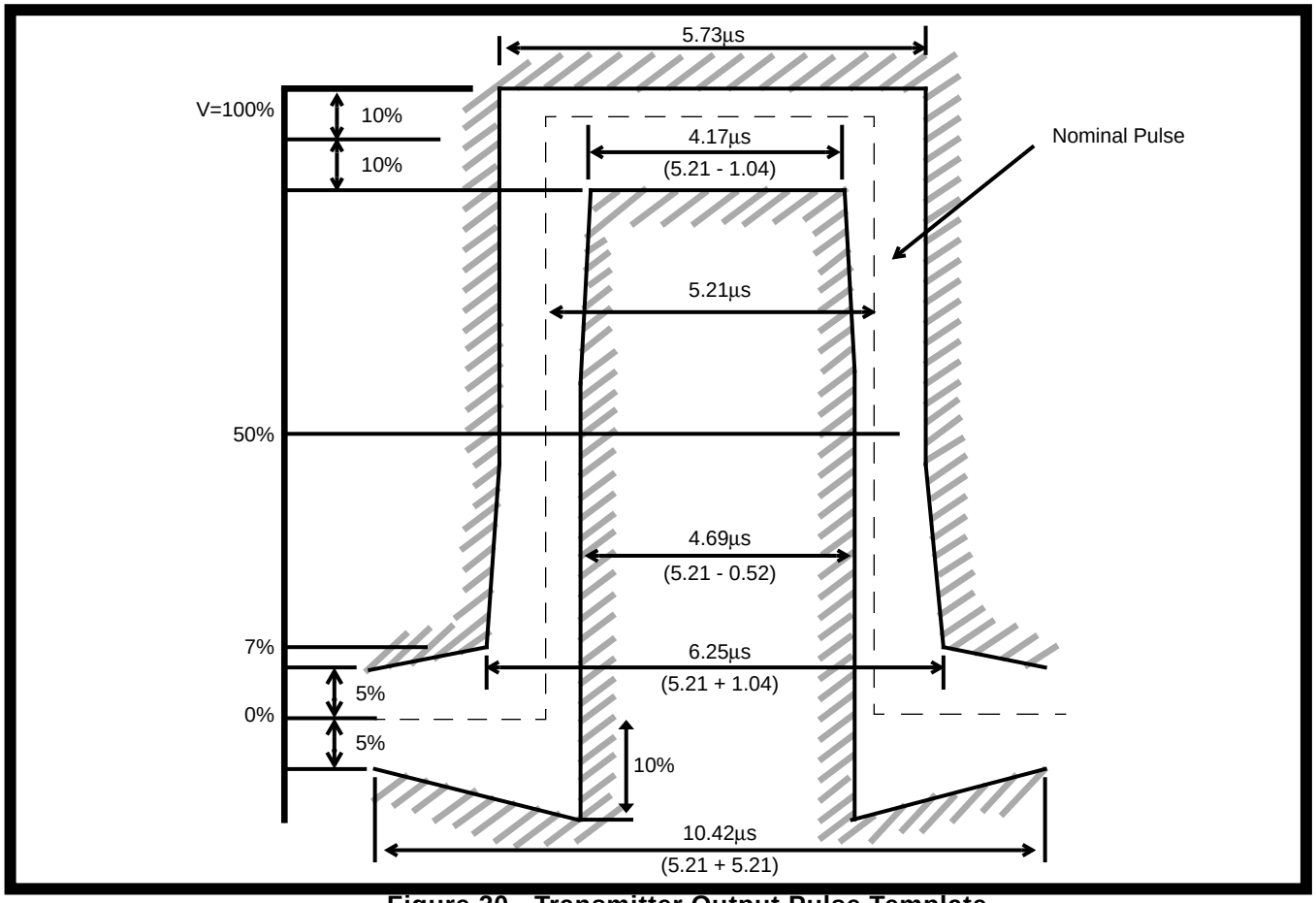


Figure 20 - Transmitter Output Pulse Template

minimum threshold set to 16 dB below nominal pulse amplitude. This minimum threshold on the input circuit is required to maintain the active region of the input signal well above the noise and crosstalk levels.

5.3 PLL and Jitter

The SNIC has self-contained clock recovery using an on chip analog phase-locked loop. Incorporated in the Phase-Locked Loop (PLL) is a voltage controlled oscillator which allows the SNIC to function without an external crystal. The PLL has both a phase and frequency detection circuit which accelerates phase acquisition. The extracted clock is presented on the $\overline{C4b}$ pin with a nominal frequency of 4.096 MHz. If the TE mode of the MT8930B is selected by tying pin CK/NT low, then the frequency of the VCO will deviate from its nominal value in the absence of a line signal. For TE applications requiring a stable and constant VCO frequency at all times, the CK/NT pin of the MT8930B should be connected to a 4.096 MHz clock. This clock input will still configure the device in TE mode while serving to train the PLL in the absence of a line signal on the S/T bus. Note that the MT8931B, on the other hand, requires a clock input or a crystal to be connected to pin XTAL1/NT in order to select TE mode. Therefore, the VCO frequency is always centered at the proper value. Under all conditions the TE will phase-lock to the INFO2 signal within 50 ms. An inherent advantage of

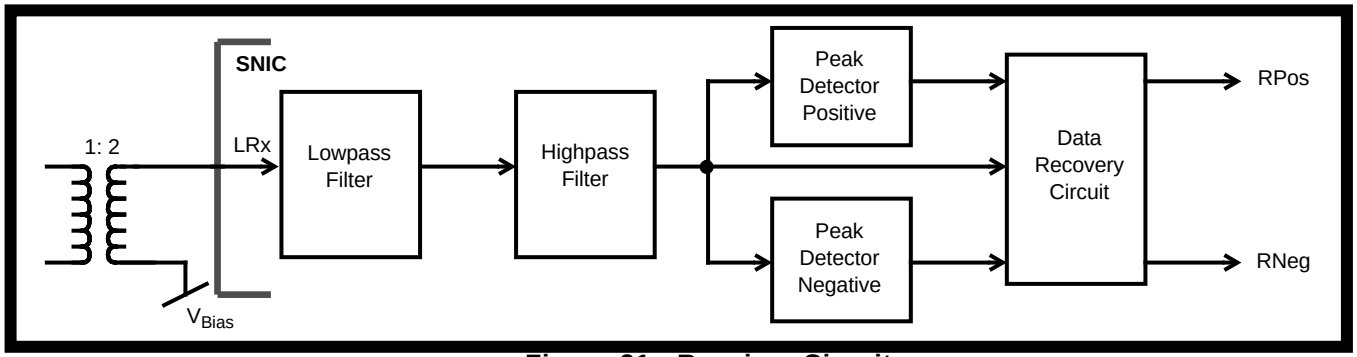


Figure 21 - Receiver Circuit

the analog PLL is its capability to reject input jitter. The PLL has a second order jitter transfer function with a 3 dB cutoff point situated at 1kHz as shown in Figure 22.

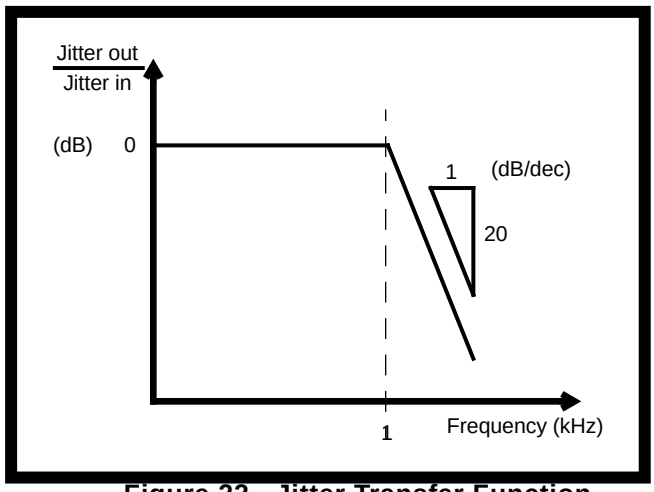


Figure 22 - Jitter Transfer Function

In the NT mode, the SNIC will produce a 192 kHz baud rate clock by dividing the 4096 kHz system clock. In the TE mode, the 192 kbit/s line data will generate the 4096 kHz system clock as well as the system frame pulse.

6.0 TRANSFORMER SPECIFICATION

The SNIC interfaces to the line port through 2:1 transformers whose typical schematic is shown in Figure 23. To meet all the CCITT I.430 and ANSI T1.605 Specifications on the S interface, the specifications of the transformers used with the SNIC must comply with the values listed in Table 6. Figure 25 shows the test circuit used to measure the longitudinal conversion loss parameter given in Table 6.

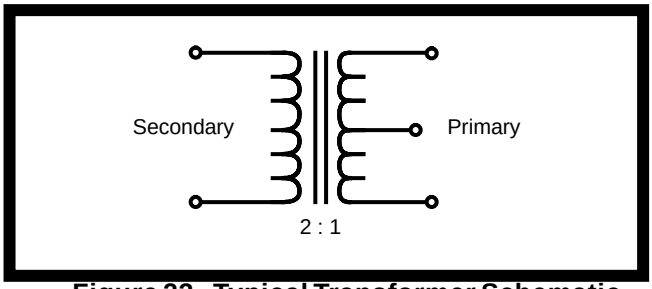


Figure 23 - Typical Transformer Schematic

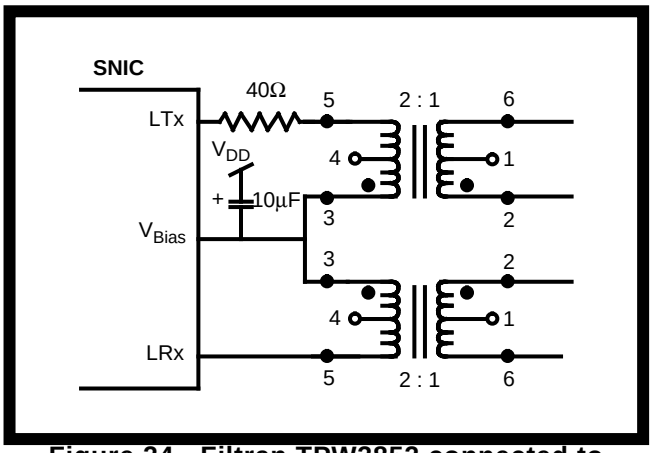


Figure 24 - Filtran TPW3852 connected to MT8930B/31B (Protection Circuitry not shown)

Transformer Parameter		Min.	Typ.	Max.	Units	Test Conditions
1. DC Resistance	Primary Secondary		2.0 3.0		Ohm Ohm	
2. DCR Match Between Split Windings		5			%	
3. Turns Ratio Primary:Secondary			1:2			
4. Inductance	Primary (L_P) Secondary (L_S)	22 88	30	41 164	mH mH	10kHz @ $1V_{rms}$
5. Leakage Inductance	Primary (L_{LP}) Secondary (L_{LS})			6 24	µH µH	Secondary Short Circuited,10kHz @ $1V_{rms}$ Primary Short Circuited,10kHz @ $1V_{rms}$
6. Distributed Capacitance	Primary (C_P) Secondary (C_S)			152 38	pF pF	Secondary Open Circuit, 1 MHz @ $1V_{rms}$ Primary Open Circuit, 1 MHz @ $1V_{rms}$
7. Interwinding Capacitance				30	pF	1 MHz @ $1V_{rms}$
8. Dielectric Strength Primary to Secondary		1500			V_{rms}	
9. Volt-Microsecond Prod.		100	1000		V-µS	
10. Longitudinal Conversion Loss		30 43			dB dB	Termination 1, f=1.2 MHz. See Test Cct. Fig.3 Termination 2, f=1.2 MHz. See Test Cct. Fig.3

Table 6. MT8930B/31B Transformer Specification

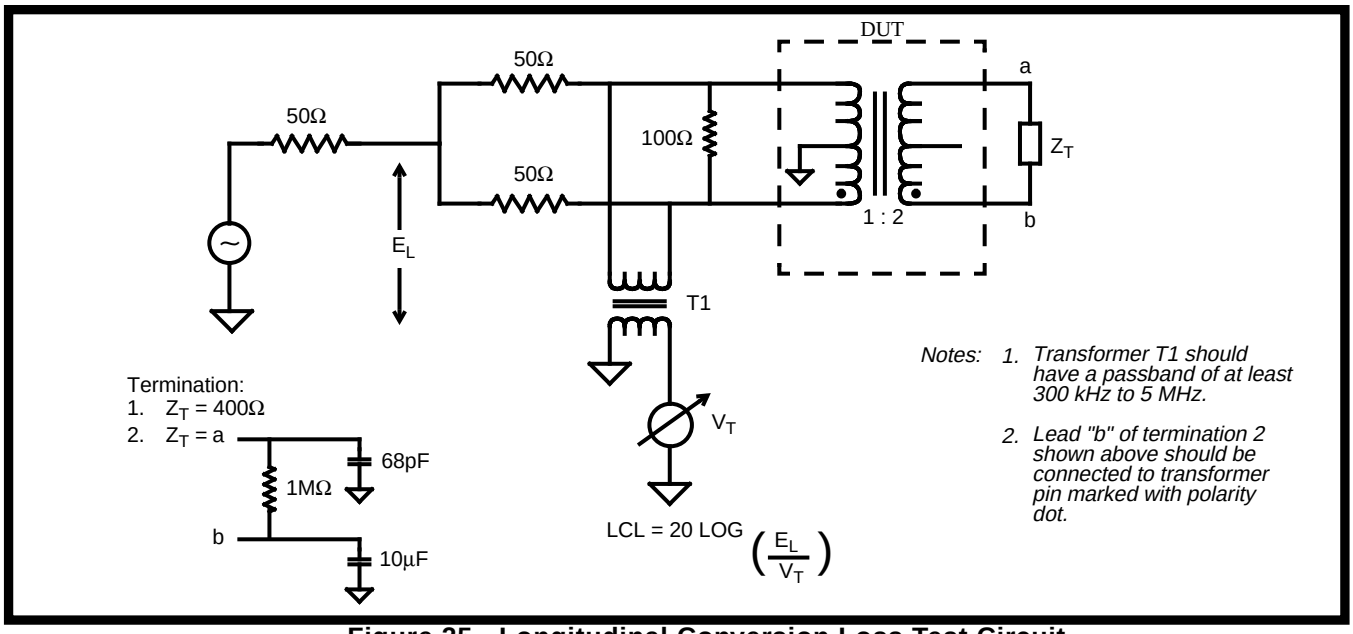


Figure 25 - Longitudinal Conversion Loss Test Circuit

7.0 PROTECTION CIRCUITRY

In compliance with ANSI T1.605 Specification, the following power fault conditions should not damage either the NT or the TE:

1. DC voltage: a) Amplitude: 56.5 V
   b) Current limit: 0.5A
   c) Duration: continuous for 5 minutes

2. AC voltage: a) Amplitude: 200 V peak
   b) Source resistance: 1500Ω
   c) Duration: 2 sec on, 4 sec off, continuous for 5 minutes

3. Voltage surge: a) Amplitude: 1000 V peak
   b) Rise time: 1 µs
   c) Fall time: 50 µs
   d) Source capacitance: 15 nF

For part 1 and 2, voltages of each polarity should be applied between each of the 4-wire S interfaces, and each other of these wires and the ground reference of equipment power source. For part 3, fifty surges of each polarity should be applied between all 4 wires and the ground reference of the equipment power source. Each surge is to be simultaneously coupled to individual S interface wires, each through an impedance of 15 nF, balanced with respect to individual wires of the circuit pair.

The selection of the appropriate protection circuitry to meet these conditions is restricted by the value of the contributed total capacitance. This value must not exceed 80 pF when measured on the line side.

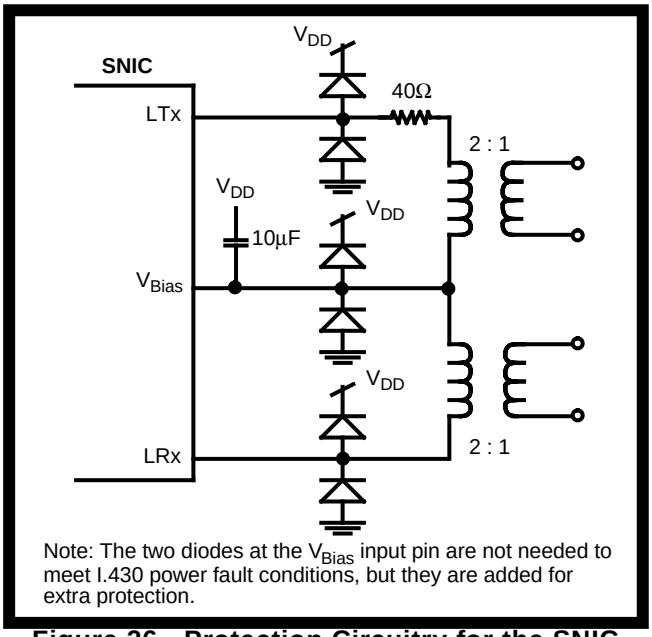


Figure 26 - Protection Circuitry for the SNIC

Otherwise, this added capacitance will prevent the device from complying with I.430 pulse and impedance templates.

One protection circuit which has been proved to meet all the stated power fault conditions on the line side, and provide added protection to the output and input drivers on the device side, is given in Figure 26. The total capacitance contributed by this circuit can be as low as 20 pF (when measured on the transmit pair of the line side) depending upon the type of diodes used. These diodes should have similar or better electrical characteristics than the ones stated below (typical diodes are the 1N916, 1N4149, 1N4448, 1N4449, 1N4150, 1N4450, 1N4148, 1N3600):

Breakdown Voltage	75 V
DC Forward Current	300 mA
Reverse Recovery Time	4 ns
Peak Forward Surge Current	
Pulse Width = 1 s	1 A
Pulse Width = 1 µs	4 A

However, to provide extra protection when the power fault conditions may exceed that of I.430 or when the interface wiring is exposed, gaz tubes can be used on the four-wire interface side. Gas tubes have very low capacitance (usually 1pF) and will not affect the performance of the device regarding pulse and impedance templates.

8.0 HDLC FORMATTER

The HDLC formatter incorporated on the SNIC handles the bit oriented protocol as per level 2 of the X.25 packet switching protocol defined by CCITT. In the ISDN environment, this Packet Assembly and Disassembly (PAD) function is fundamental to the structuring of the D-channel as per the LAPD signalling protocol, which will be the full layer two protocol used to route the voice and data channels through the ISDN network.

8.1 Packet Structure

By performing the PAD function the HDLC formatter will structure the packet as shown in Table 7. This implies that the HDLC formatter will automatically insert the opening and closing flags, it will assure data transparency by inserting and deleting a zero after five consecutive ones (in order to avoid duplicating the flag sequence). It will also generate and compare the cyclical redundancy check calculated for each packet using the generating polynomial: $G(X)=X^{16}+X^{12}+X^{5}+1$.

FLAG	DATA FIELD	FCS	FLAG
One Byte	n Bytes (n ≥ 2)	Two Bytes	One Byte

Table 7. Frame Format

The HDLC formatter can only be accessed through the microprocessor port in the form of internal registers or FIFOs. Asynchronous registers provide full control of all features as well as providing device status information. This structure consists of the following. On power up, the HDLC Control Register 1 must be initialized according to the specific application. This includes disabling the HDLC transmitter and receiver, enabling the address recognition (if desired), selecting the relevant port for both the receiver and transmitter, selecting the desired interframe time fill[1], and disabling the HDLC loopback. The user can then select the desired sources of interrupts using the HDLC Interrupt Mask Register and/or Master Control Register. (It is also a good practice to reset the receive and transmit FIFOs before beginning a communication session in the event that unwanted data has made its way into the FIFOs during the power up sequence.)

After the initialization process, the HDLC formatter can be used to transfer packetized D-channel over either serial port (i.e., S-Bus or ST-BUS). Structuring the packet is accomplished by building the message in the 19 byte deep TxFIFO using the relevant tags to identify the end of or an aborted packet. (Tagging a byte is achieved by setting the appropriate bit in the HDLC Control Register 2 then writing to the Tx FIFO.) If the packet exceeds 19 bytes, the transmitter must be enabled to deplete the FIFO before writing any further information to the packet. An algorithm for building a valid packet is provided in Figure 27.

If the transmission of the packet is directed to the S-Bus port in the TE mode and the HDLC transmitter is enabled, the SNIC will activate the priority mechanism circuitry to request the D channel as soon as data is written to the Tx FIFO. Once the D-channel acknowledgment signal is received the packet will be transmitted immediately following the opening flag. If a collision occurs during transmission, the remainder of the packet will be depleted from the Tx FIFO but will not be sent on to the D-channel of the S-Bus. Therefore, this packet must be reloaded into the Tx FIFO. When the SNIC is in NT mode or the packetized D-channel is directed to the ST-BUS port, the packet will be transmitted as soon as the transmitter is enabled.

During the reception of a packet, the 16 kbit/s D-channel is examined on a bit-by-bit basis with all inserted zeros removed, the CRC calculated and the bits organized into 8 bit bytes in the 19 deep RxFIFO. The control characters surrounding the packet structure such as the flags and the abort sequence will never make their way into the RxFIFO. If address recognition is enabled, the address field (one or two bytes) is compared to the byte in the Receive Address Registers. If a match does not occur, the received packet will be ignored and will not be loaded into the receive FIFO. Once an address match occurs, the packet, starting with the address field will be loaded into the RxFIFO for further processing.

[1] It must be noted that if the flag fill mode is enabled with the transmitter disabled, the HDLC formatter will not generate the opening flag once the transmitter is enabled. This will result in the first packet being lost.

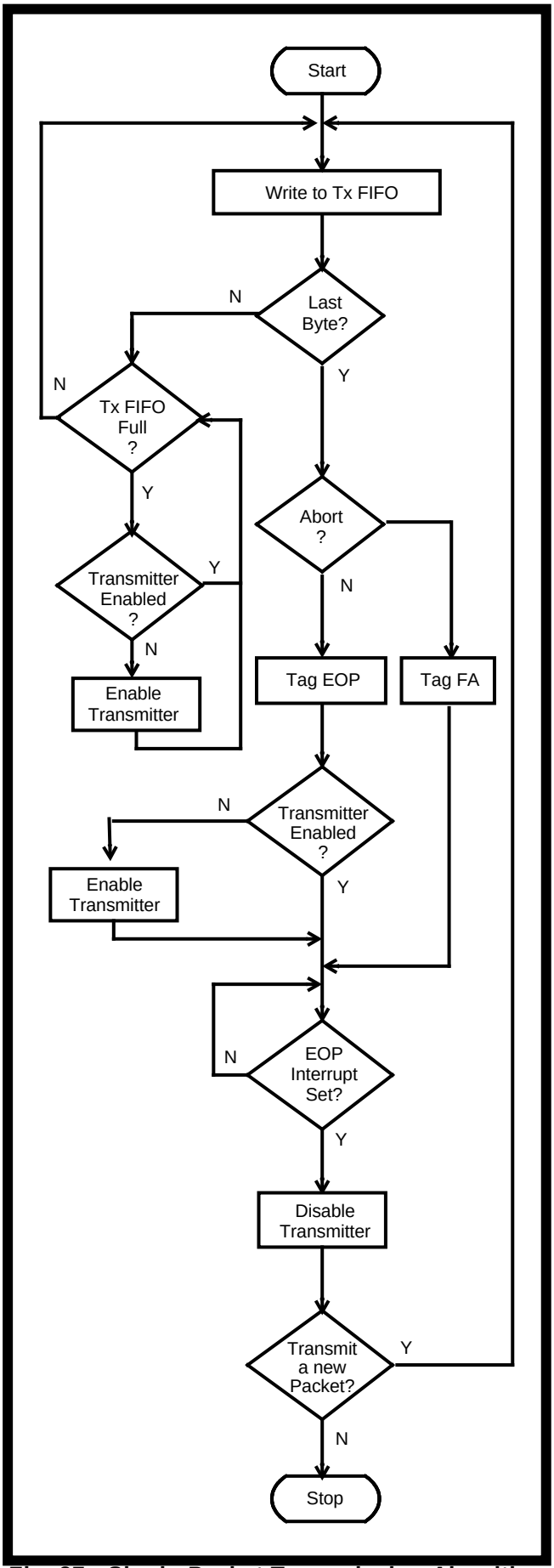


Fig. 27 - Single-Packet Transmission Algorithm

Structuring the received packet into a valid message is performed using the relevant status bits from the HDLC status register. All the bytes written to the receive FIFO are flagged with two status bits. The status bits are found in the HDLC status register and indicate whether the byte to be read from the FIFO is the first byte of the packet, the middle of the packet, the last byte of the packet with good FCS, or the last byte of the packet with bad FCS or an abort sequence. This status indication is valid for the byte which is to be read from the Receive FIFO. A simple algorithm for receiving a packet is provided in Figure 28.

8.2 FIFOs

As stated above, the SNIC has two 19 byte deep FIFOs for the reception and transmission of data over the D-channel. Associated with the FIFOs is an HDLC Status Register which carries the Rx and Tx FIFO status as revealed in Tables 8 and 9.

B5	B4	RxFIFO Status
0	0	RxFIFO Empty
0	1	≤ 14 Bytes
1	0	RxFIFO Overflow
1	1	≥ 15 Bytes

Table 8. RxFIFO Status

B3	B2	TxFIFO Status
0	0	TxFIFO Full
0	1	≥ 5 Bytes
1	0	TxFIFO Empty
1	1	≤ 4 Bytes

Table 9. TxFIFO Status

Critical status information, such as the RxFIFO overflow, RxFIFO full, TxFIFO full and TxFIFO underrun have related interrupt signals to avoid having to continuously poll the status register. These interrupt signals must be unmasked through the HDLC Interrupt Mask Register before they become active.

If the received FIFO overflows, any attempt to load more information to the full FIFO will be ignored until the RxFIFO is read. An RxFIFO overflow will introduce a corruption in the sequential flow in the packet which will result in a bad FCS. However, any attempt to write to a full TxFIFO will not overwrite the last byte in the FIFO and cause the byte to be lost. Conversely, if the transmit FIFO underruns, the HDLC transmitter will begin sending an abort sequence (01111111) followed by the selected interframe time fill.

8.3 Transparent Option

The Trans bit (B2) in the HDLC Control Register 1 can be set to provide transparent data transfer by disabling the protocol functions. The transmitter no longer generates the Flag, Abort and Idle sequences nor does it insert the zeros and calculate the FCS. The receiver section will also disable the protocol functions like Flag, Abort, Idle Detection, Zero Deletion, FCS Check and Address Comparison. This option allows the use of the FIFOs for raw data transfer without the associated overhead of the HDLC format. It should be noted that none of the protocol related status or interrupt bits are applicable

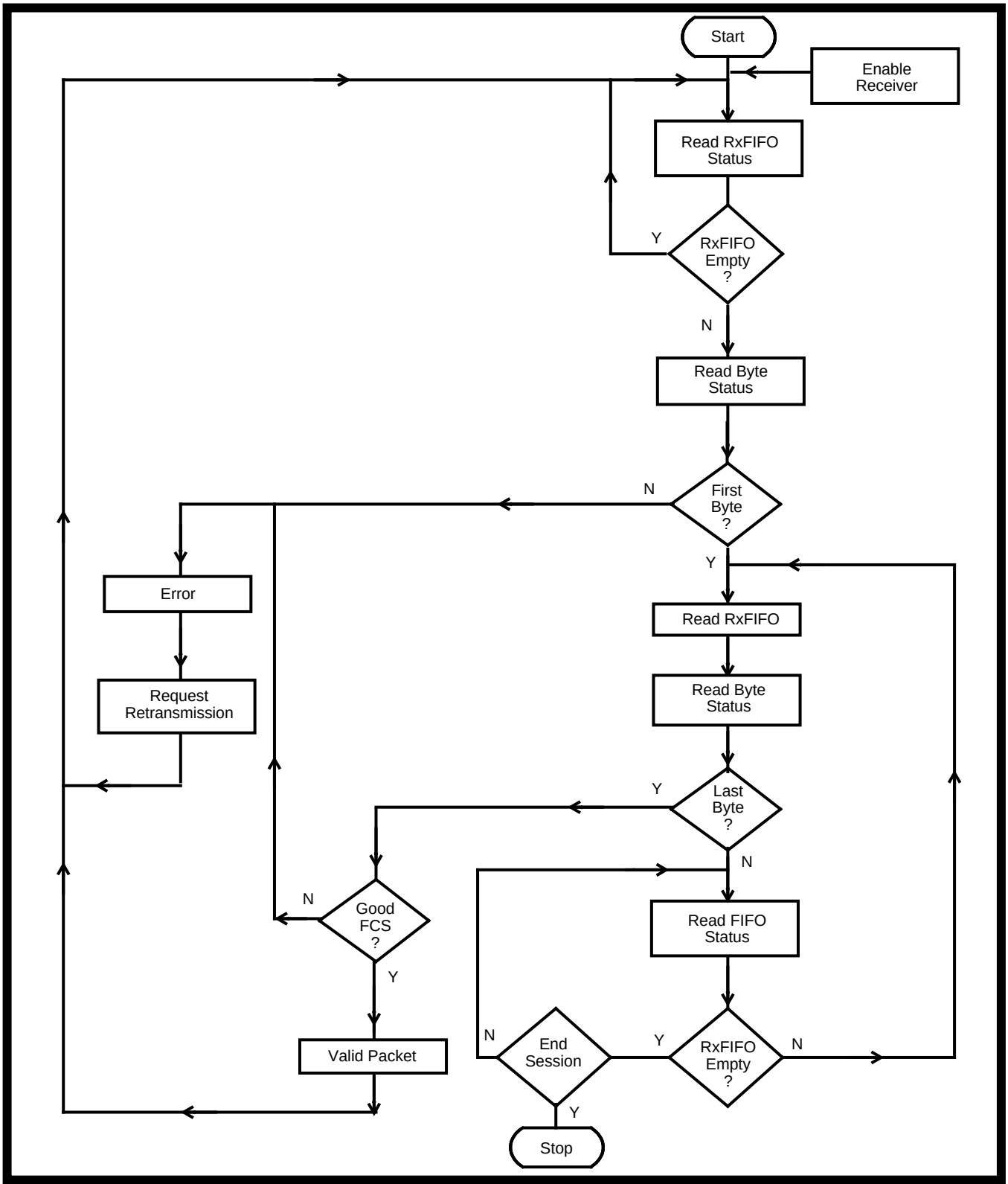


Figure 28 - Receive Packet Algorithm

in transparent data transfer state. However, the FIFO related status and interrupt bits are pertinent and carry the same meaning as they do while performing the protocol functions.

9.0 APPLICATION HINTS

9.1 Power-up Conditions

In controllerless mode, the transfer of data between the S-Bus and the ST-BUS is established on power up or after a reset. However, the ST-BUS ports and the HDLC transmitter and receiver are disabled on power up or after a reset if the microprocessor mode is selected. This prevents the transfer of data between the ST-BUS, the HDLC transceiver, and the S-Bus. To enable the transfer of data on the B1 and B2 channels of the two serial ports, the user has to set the corresponding bits in the ST-BUS Control Register. The D-channel data, however, is routed between the two serial ports and the HDLC transceiver in various configurations as indicated in section 9.3.

9.2 Controlling the SNIC

The C-channel on the ST-BUS DSTi stream can be used to control the SNIC. When controllerless mode is selected on the MT8930B, pin 11 (P/$\overline{SC}$) is used to indicate whether the microport pins or the DSTi C channel is the control source of the device. If the C channel is chosen, then the microport pins are ignored. In microprocessor controlled mode, however, bit 0 of the Master Control Register selects either the parallel port or the C channel to be the control source of the SNIC.

When the C channel is used to control the device, its data is loaded into the C-channel Control Register. When it is not used, the data on this channel is discarded. The contents of the NT or TE Mode Status Register (depending on the mode selected) is always sent out on the C channel of ST-BUS DSTo pin.

The microprocessor can overwrite any data transferred between the S-Bus and the ST-BUS by accessing the corresponding synchronous register.

9.3 D-Channel Switching

The D channel is routed between the HDLC transceiver, the S-Bus, and the ST-BUS in different ways. Figure 29 shows these possible configurations and the required condition to set each of them. An “x” mark in the diagram is a “don’t care” state meaning that the state of the corresponding bit has no effect on the setting of the communication path. Note that in all the configurations, the transfer of data to and from the ST-BUS on the D channel is enabled by setting respectively bits B4 and B0 of the ST-BUS Control Register to 1.

9.4 HDLC Operation

This section outlines a recommended procedure for transmitting, receiving, and monitoring the status of HDLC packets. The HDLC protocol on the D-channel of the S-Bus is enabled by initializing the SNIC as follows:

1) The TxEn, RxEn, TxPrtSel, and RxPrtSel bits in the HDLC Control Register 1 should be set to ONE.

2) The HDLC Interrupt Mask Register bits should be enabled so the device can issue interrupts indicating the status of the HDLC FIFOs and packets.

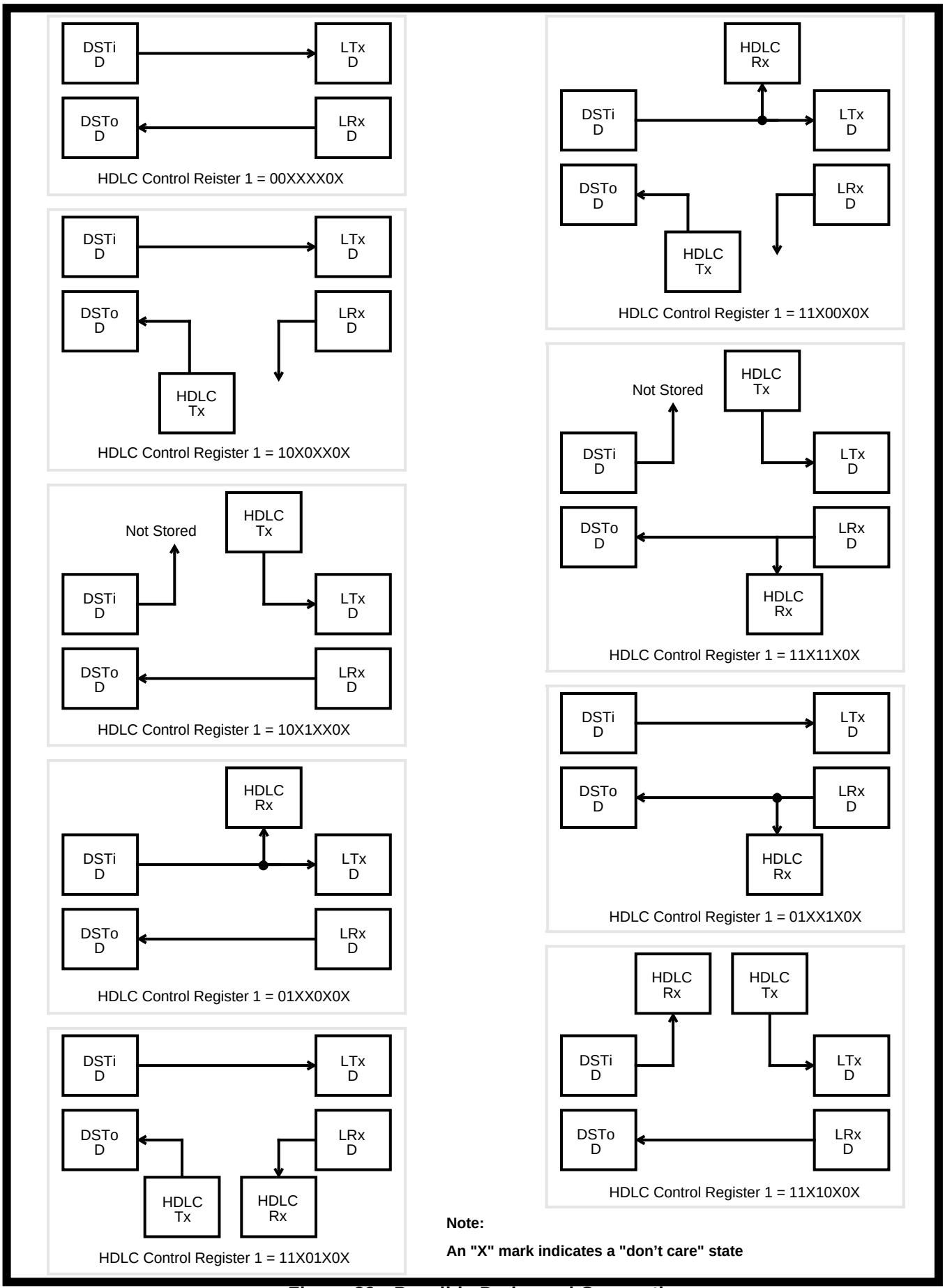
3) The IFTF bit in the HDLC Control Register 1 should be set to 0 for a TE SNIC in passive bus configuration. This will allow the device to transmit continuous ONEs between packets thus giving other TEs a chance to access the D-channel.

After initialization, the packets should be transmitted in the following sequence:

1) D-channel bytes are written to the Tx FIFO. Everytime a packet is to be closed, the EOP bit in the HDLC Control Register 2 should be set to ONE. This will tag the next byte written to the Tx FIFO with the end-of-packet sequence (CRC bits and the flag). A maximum of 19 bytes should be written to avoid an overflow condition.

   When the TxFIFO is loaded with more than one packet at a time, then the closing flag of the first transmitted packet will be used as the opening flag of the next packet. This will violate CCITT I.430 and ANSI T1.605 Recommendations which specifies that a TE must lower its priority level within the selected priority class after the successful transmission of a packet. The user can meet this requirement by loading the Tx FIFO with no more than one packet and then waiting for the DCack bit to go to zero, or for an HDLC interrupt caused by the TEOP bit in the HDLC Interrupt Status Register, before attempting to load a new packet.

2) When the device has only four remaining bytes in the Tx FIFO, an interrupt is issued through the TxFL bit in the HDLC Interrupt Status Register. This is a warning indicating that more data



Note:

An "X" mark indicates a "don't care" state

Figure 29 - Possible D-channel Connections

should be written to the Tx FIFO within 2 ms to avoid an underflow condition. Additional 15 bytes can be added to the Tx FIFO.

3) If an underflow condition occurs, then the device will abort the last packet automatically and an interrupt will be issued through the TxFun bit in the HDLC Interrupt Status Register. The packet should be retransmitted again.

4) A collision on the D-channel will cause a TE SNIC to generate an interrupt through the Dcoll bit and to ignore the remaining bytes of the packet. The user should then retransmit the packet.

5) Once the closing flag of the last packet in the Tx FIFO is transmitted, the SNIC issues an interrupt through the TEOP bit. The user may then repeat the procedure starting from step 1 if more packets are to be transmitted.

On the receiving side, packets should be processed in the following way:

1) An interrupt is issued through the RxFF bit in the HDLC Interrupt Status Register whenever 15 bytes have accumulated in the Rx FIFO. This is a warning indicating that the Rx FIFO should be read within 2.5 ms before it overflows.

2) If an interrupt indicating an overflow condition is detected (RxFov bit is set to 1), then the last packet that was not closed with a flag before the overflow occurred should be ignored.

3) The detection of a closing flag causes an interrupt through the EOPD bit of the HDLC Interrupt Status Register. The remaining bytes of the corresponding packet in the Rx FIFO should be read while monitoring the status of each byte by checking the two RxByte Status bits in the HDLC Status Register. These two bits indicate which byte is the last of the packet and whether the Frame Check Sequence (FCS) of this packet is good or bad.

4) Receiving a frame abort sets the EOPD and FA bits to 1 thus causing an interrupt. The SNIC will assign a bad FCS word to the aborted packet allowing the processing of this interrupt in the same manner as in step 3 above.

9.5 Hints on Passive Bus Configuration

In a passive bus configuration, there are certain procedures that all TEs on the line should follow to avoid contention and to provide fair access among all. Some of these procedures are listed as follows:

- When a TE has no layer 2 frames to transmit, it shall send binary ONEs on the D-channel. In other words, the interframe time fill on the D-channel in the TE-to-NT direction should be all binary ONEs. This can be done by setting the IFTF bit of HDLC Control Register 1 to logic 0. In this manner, other TEs will have an opportunity to access the D-channel using the priority mechanism circuitry.

- A TE should send binary ONEs in any B-channel which is not assigned to it. The user can put channels B1 or B2 in an all ONEs idle code by disabling the corresponding port of DSTi stream through the ST-BUS Control Register.

- When multiframing is declared, a TE which is not using the Q-bits should set them to binary ONE. Since the binary value of every Q-bit is determined by that of the TxMCH bit of the TE Mode C-channel Control Register, a TE which is not using the Q-bits should set the TxMCH bit to 1 while multiframing is active. A TE that does not follow this procedure will cause contention on the Q-channel with other TEs.

- For a point-to-multipoint wiring configuration, the user must maintain the wiring polarity integrity of the interchange circuit in the direction of TE-to-NT among all TEs. If this is not done, then collision will occur in bits common to all TEs such as the framing bit F.

10.0 CONCLUSION

As seen throughout this application note, the SNIC is a fully featured Subscriber Network Interface Circuit for the ISDN S/T interface. The objective of this note was to define some of the basic rate interface requirements as outlined in the CCITT I.430 and ANSI T1.605, and reveal how these functions were implemented on the SNIC.

The system interfaces to the SNIC were discussed to identify access procedures to the various internal registers using the ST-BUS and the microport. In addition, the internal timing used to transfer data within the silicon was discussed in order to calculate the throughput delay of the system to line, and line to system. This allows the system designer to determine the total delay introduced by the SNIC.

Finally, further explanation was given on the HDLC formatter. Packet structure and Tx and Rx FIFO were discussed to identify chip response during fault conditions.

Notes:

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