Application Note **MSAN-101**

Applications of the MT8804A 8 X 4 Analog Switch Array

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Introduction

The constant trend in electronic design is towards circuits which minimize power and space requirements while improving on the performance characteristics of the predecessors. The field of analog switching is no exception to this design strategy. The Zarlink MT8804A CMOS 8 x 4 Analog Switch Array is a micropower device which replaces several CMOS MSI packages and meets the stringent specifications required in analog switching systems. The 8 x 4 array configuration and minimal interchannel crosstalk make the MT8804A ideal for crosspoint switching applications. This application note provides both functional and parametric details of the device that would normally be required in designing the MT8804A into such systems. A series of application circuits and descriptions is presented to further illustrate the use and versatility of the MT8804A in communications and other more general areas.

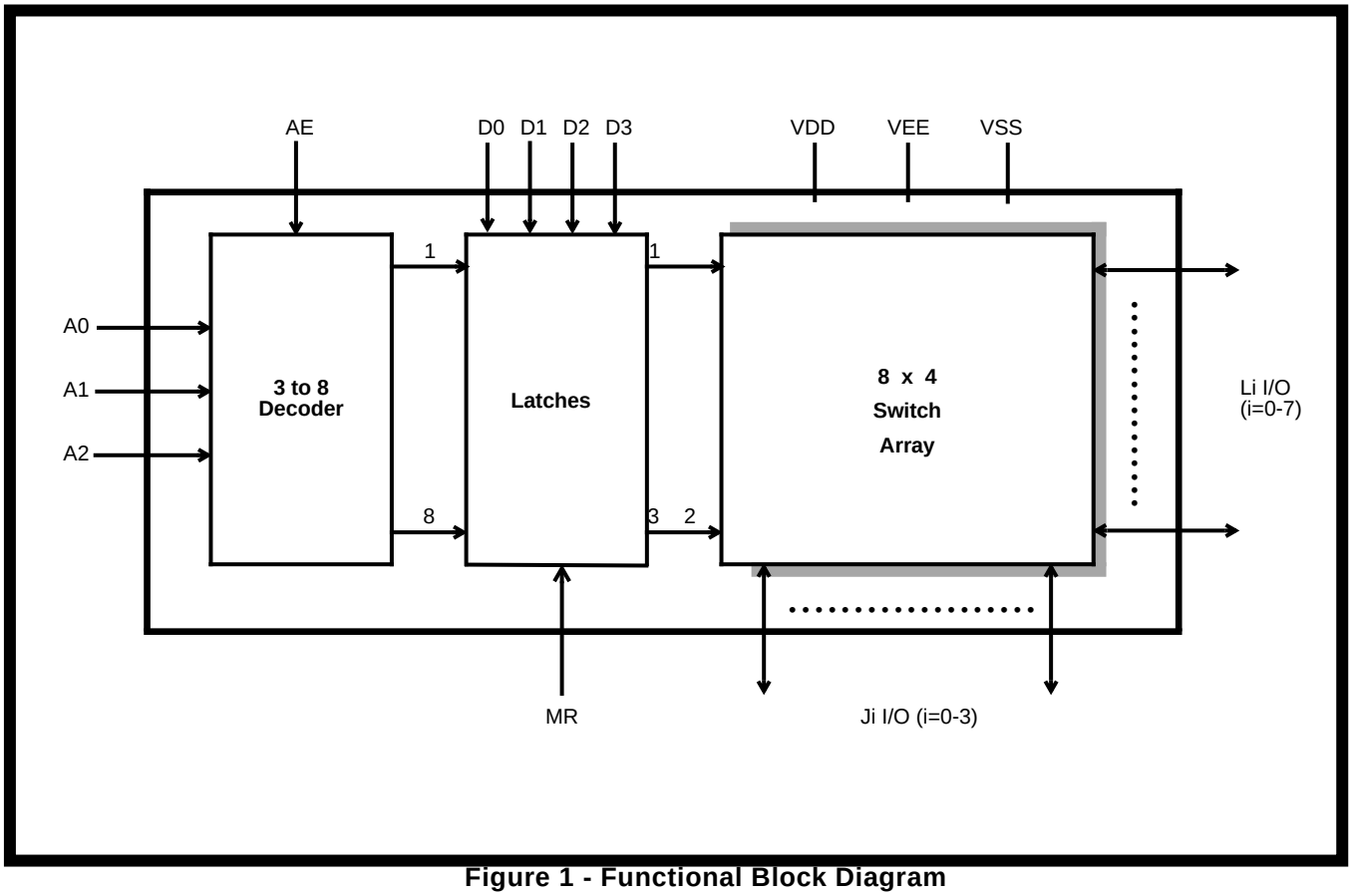

Figure 1 - Functional Block Diagram

The MT8804A in Detail

Configuration and Control

The 32 analog switches in the MT8804A are configured in an 8 x 4 array as shown in Figure 1. The eight switches in each column are connected to an input/output Junctor (J_0 - J_3), and similarly, the four switches of each row are connected to an input/output Line (L_0 - L_7). Each crosspoint switch provides either isolation or transmission between its associated line and junctor. The states of the switches are controlled by a set of 32 latches arranged in an 8 x 4 array corresponding to the analog switch matrix. A logical HIGH stored in a latch turns the corresponding switch ON, while a LOW level turns the switch OFF. Data is asynchronously written into the control latches whenever the Address Enable (AE) input is HIGH. The latch outputs are directly connected to the control inputs of the analog switches. This direct interconnection results in a “continuous read” of the control memory (latches) by the analog switches.

Writing data into the control memory is done the same as in a standard random access memory. However, since no read control signals are required, the control store can uniquely be treated as a write-only-memory. The eight rows are selected by the three Address (A_0 - A_2) inputs. The signals on these lines are decoded to a one-of-eight active high format. The Address Enable (AE) input gates the active output from the decoder to the enable inputs of the latches in the addressed row. Levels present on the Data (D_0 - D_3) inputs are asynchronously latched when the AE input is high. The data corresponds directly to the states of the switches in the addressed row; i.e. D_0 to J_0, D_1 to J_1, etc. For example, if junctor J_1 was to be connected to L_4, the control inputs would be set up as follows: D_3 D_2 D_1D_0 = 0010, and A_2 A_1 A_0 = 100. Pulsing the AE input HIGH would complete the connection. If instead, both J_1 and J_3 were to be connected to L_4 then the data inputs would be set to D_3 D_2 D_1 D_0 = 1010 and all else would remain the same. Similar connections can be programmed for each of the eight lines (L_0 - L_7). All of the latches in the control memory are asynchronously reset whenever the Master Reset (MR) input is HIGH. This results in all analog switches being turned OFF, isolating all junctors from all lines.

Power Supply Considerations

The MT8804A is equipped with on-chip logic level converters to simplify the interface to logic circuits in an analog switching system. The control inputs of the device are driven from signals between V_{DD} and V_{SS}. All of the control inputs are active HIGH with V_{DD} being a logical HIGH level and V_{SS} a logical LOW. The analog or digital signals switched through the array are allowed to swing between V_{DD} and V_{EE}.

The power supply input voltages are defined as follows:

$5V \le V_{DD}$ $V_{SS} \le 13V$ Digital
$5V \le V_{DD}$ $V_{EE} \le 13V$ Analog
$0V \le V_{SS}$ $V_{EE} \le 8V$ Level Converters

These voltages define the operating power supply ranges of the digital and analog inputs and the logic level converters. While the analog and digital power supplies have identical limits the levels may be different in a given application. For example, a valid power supply configuration is as follows:

V_{DD} = +5V, V_{SS} = 0V and V_{EE} = -6V. The control inputs are thus driven from a 5V CMOS logic system while the signals on the lines and junctors can swing from +5V to -6V. Caution must be used to meet all three power supply constraints when deciding upon a power supply configuration. The following is an example of invalid power supply voltages: V_{DD} = +5V, V_{SS} = 0V, and V_{EE} = -12V. In this case, V_{DD} - V_{EE} = 17V which exceeds the analog power supply range.

Analog Switch Characteristics

Like all monolithic analog switches, the MT8804A exhibits a resistive characteristic when turned on. This ‘ON’ resistance has two components, the actual resistance of the channels of the MOS transistors and the interconnect resistance between switches. The potential variation of the total resistance with temperature, power supply voltage and input signal voltage is illustrated in Figure 2 and 3. Most applications will not be adversely affected by the ON resistance or its variations with these parameters. However in some systems and applications with more stringent specifications, special considerations may be required. In cases such as driving through the MT8804A into low impedance loads, or using the device in a gain control circuit, it becomes necessary to consider the switch resistance in design equations.

Timing Measurements

Timing measurements such as propagation delays, set up and hold times, etc. on the control inputs of the MT8804A cannot be made directly as digital outputs are not available. For this reason, these

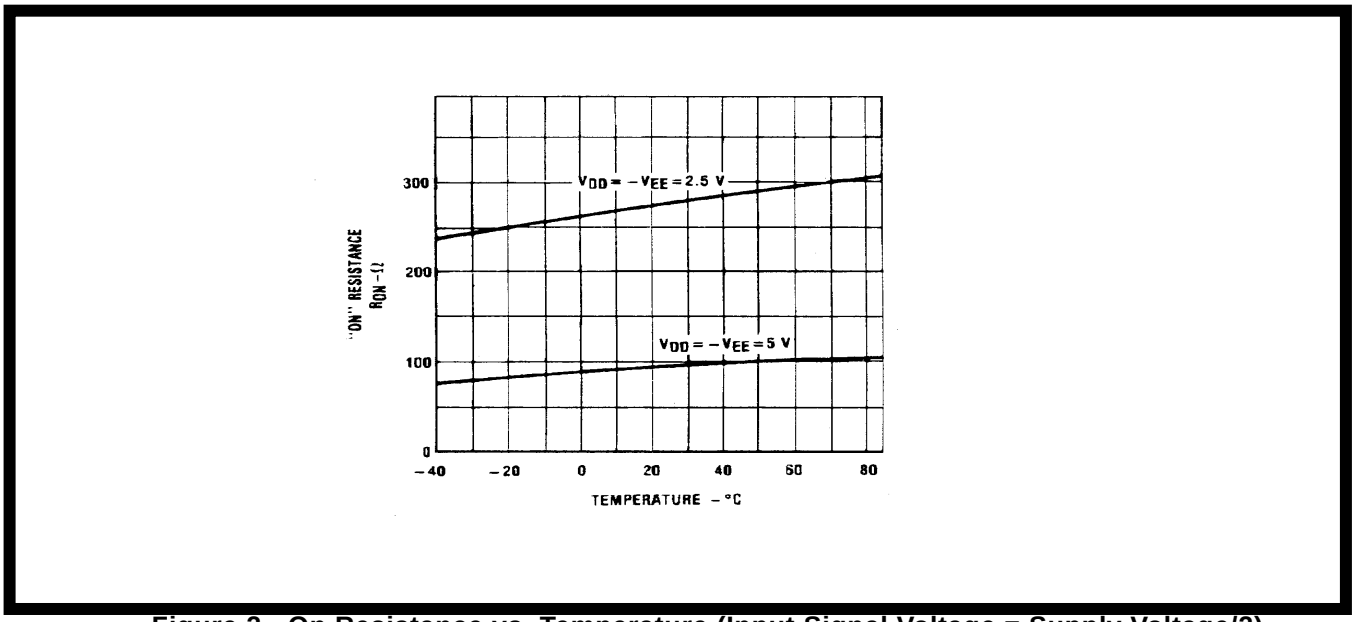

Figure 2 - On Resistance vs. Temperature (Input Signal Voltage = Supply Voltage/2)

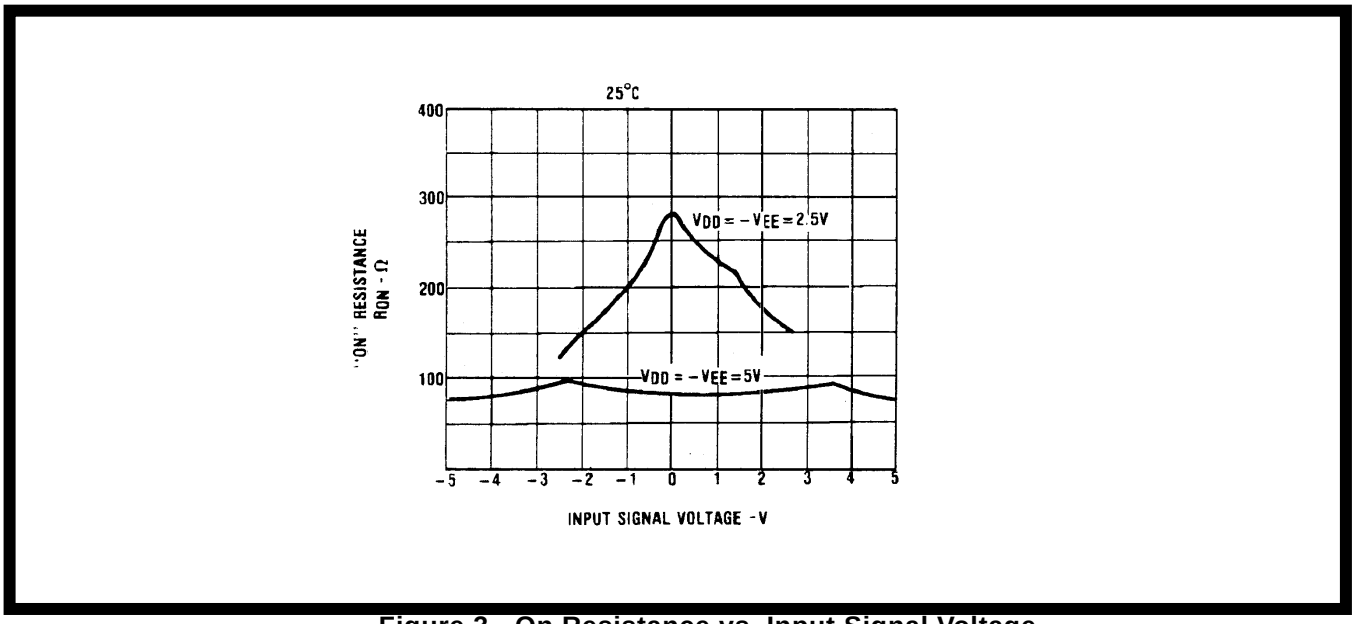

Figure 3 - On Resistance vs. Input Signal Voltage

measurements are made indirectly by observing the effects of changes in the control memory on the states of the analog switches. For example, to measure t_{PAE}, the propagation delay from the address enable (AE) input to the signal output, the following steps are taken. A load circuit (50pF in parallel with 10K) is connected from a given junctor to ground (V_{SS}). One of the lines (L_0 - L_7) is connected to V_{DD}. With all switches initially OFF, the control inputs are set up to connect the load circuit to V_{DD} through the appropriate switch. The AE input is pulsed HIGH and the propagation delay time is measured from the 50% voltage point of the resulting signal across the load. In both cases, time is measured from the leading edge of the signal. The actual time measured has three components.

1) The write time into the control latch

2) The turn on time of the analog switch

3) The propagation time through the channel of the switch

In digital switching applications of the MT8804A, it is this total time that is of concern. In general, however, the minimum time needed to write data into the latches is required. This is represented by the first of the three components listed above and is by far, the longest of the three. Therefore, basing system design on the actual measurements of total time will add a small safety margin without sacrificing significant device performance.

A special note is made in regards to the minimum address set up time (t_s). Due to internal capacitive loading on the AE input, the MT8804A requires more time to enable the control latches than is needed to enable and decode the address lines. For this reason, it is not necessary to provide any time for the address lines to settle prior to applying a pulse to the AE input. In other words, address changes are allowable up to and including the leading edge of the AE pulse.

Modular Line Interface Circuit

The MT8804A is shown in an eight channel line interface switching application in the circuit diagram of Figure 4. The Zarlink MH88610 Subscriber Line Interface Circuit (SLIC) interfaces the MT8804A to the telephone line. One of the functions of the SLIC is to provide 2-4 wire hybrid conversion. The 2-4 wire hybrid circuit separates the balanced full duplex signal at TIP and RING of the telephone line into receive and transmit ground referenced signals at VR (RECEIVE) and VX (TRANSMIT) of the SLIC. The receive inputs of the eight SLICs are connected to L0 to L7 of the MT8804A "C" device. The transmit outputs of the eight SLICs are connected to L0 to L7 of the MT8804A "A" device.

The MH88610 has a 2-wire to VX gain of 0.6dB, and a VR to 2-wire gain of -6.7dB. Therefore, a station-to-station call will have an overall gain of -6.1dB. This matches well with typical North American PBX on premise station-to-station loss plans which typically use a gain of -6dB.

Network Control

In general, to complete a telephone call with this system, it is necessary to connect the TRANSMIT output of a calling party to the RECEIVE input of a called party and vice versa. Thus, for each telephone conversation, two speech paths are required. In the configuration shown in Figure 4, four simultaneous conversations are possible. With all of the MT8804A's reset, the junctors (J_0 - J_3) are floating and not assigned to any particular telephone line. Thus, the junctor can be completely controlled by software in a microprocessor system, independent of the particular telephone line being switched. The software must maintain a record of which junctors are in use and which are free for completing calls. To better illustrate these points, all the steps required to complete a connection between two parties will be outlined.

The signal paths connecting the junctors of MT8804A's have been arbitrarily named S_0 to S_7 for reference. To connect a call from a given source party to a destination party, it is necessary to interconnect the respective TRANSMIT and RECEIVE leads. To accomplish this, addresses for the source and destination lines of the call must first be generated. The source address is derived from the off-hook conditions which are either encoded or scanned. The destination address is generated by reception of dial pulses or DTMF signals. Once these addresses have been established, the software can implement a control sequence to close the appropriate switches. This sequence is not unique as the order in which switches in the MT8804A are closed is not critical. The example which follows illustrates a possible control sequence that could be used.

If it is assumed that all the signal paths (S_0 - S_7) are free, then S_0 and S_1 would be used to complete the call. The source and destination addresses, once generated, are sequentially placed on the microprocessor data bus and hence onto the address inputs of the MT8804A's. Since S_0 and S_1 are being used, the data inputs (D_3 D_2 D_1 D_0) must be alternatively set to 0001 and 0010. With the source address on the address lines and D_3 D_2 D_1 D_0 = 0001, the ADDRESS ENABLE (AE) of chip 'A' is taken HIGH. The data lines are next set to D_3 D_2 D_1 D_0 = 0010 and the AE input of chip 'C' is taken HIGH. This completes the connections of the TRANSMIT and RECEIVE leads of the source party to S_0 and S_1 respectively. It remains only to connect the destination TRANSMIT lead to S_1 and RECEIVE lead to S_0 to complete the 2-way interconnection. To do this, the destination address is set on the address inputs of the MT8804A's. The data lines are again set to D_3 D_2 D_1 D_0 = 0010 and the AE input of chip 'A' is taken HIGH.

Lastly, with D_3 D_2 D_1 D_0 = 0001, the AE input of chip 'C' is pulsed high. This connects the TRANSMIT and RECEIVE leads of the destination line to S_1 and S_0 respectively as required. All necessary interconnections are thus complete and the processor become free to service other calls.

To disconnect a telephone call, the following steps are taken. Once a change in off-hook condition is detected, the address from the scanning circuitry is put onto the address lines and the data lines are all set to zero. The appropriate Address Enable pulses are applied to implement the disconnection. Once both parties have been scanned, the signal paths used for the conversation are freed and added to the list of available signal paths. The MASTER RESET, when taken high, will disconnect all interconnections, freeing all signal paths. This is useful for system initialization or testing.

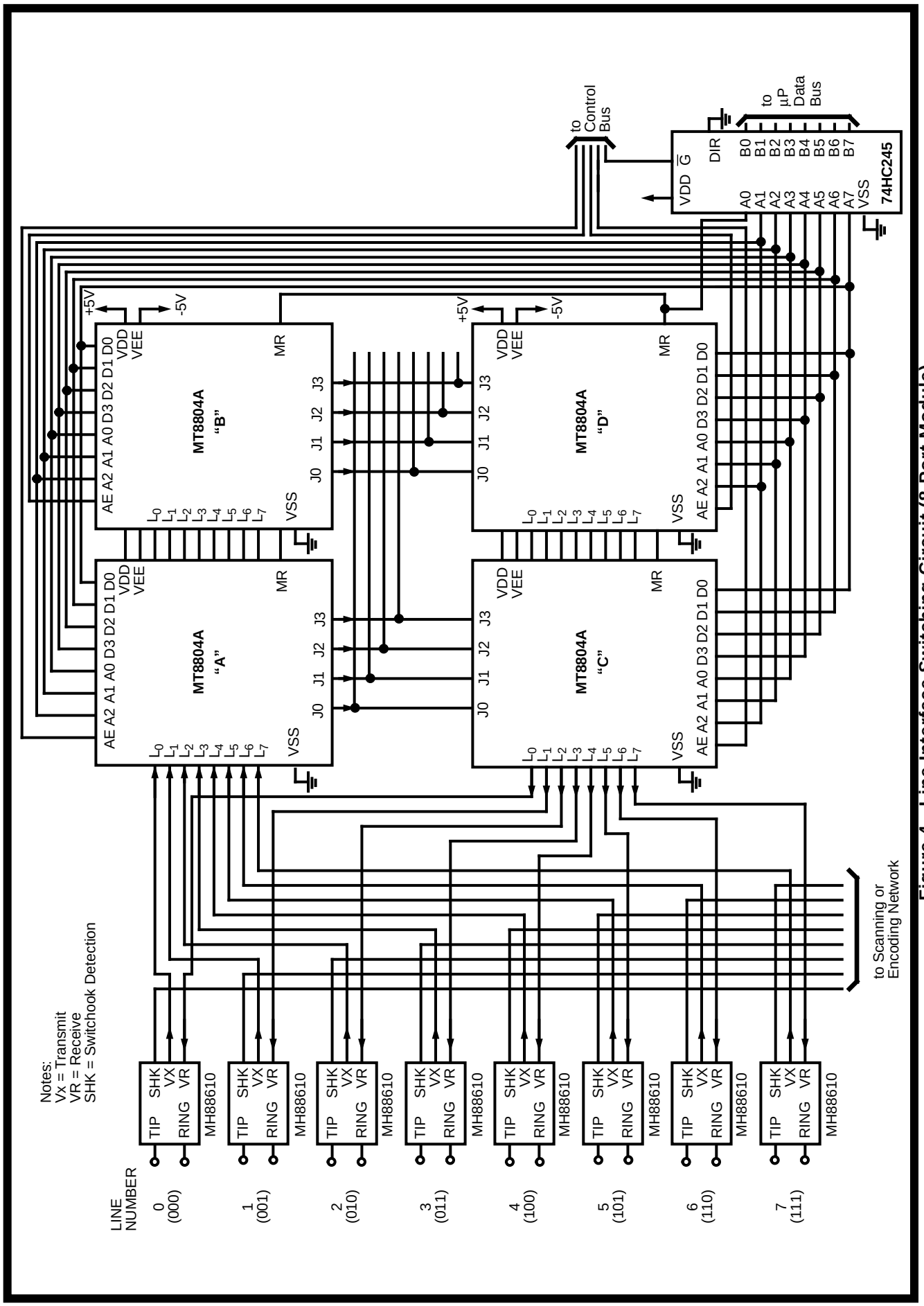

Figure 4 - Line Interface Switching Circuit (8-Port Module)

Switching Network Modularity and Expansion

The 8 port line interface switching module shown in Figure 4 would typically be used as the basis for larger systems such as a PBX. Expansion to a larger switching network involves two independent steps. The first involves increasing the maximum number of simultaneous conversations that can be conducted. This is referred to as traffic handling capacity, and is increased by adding MT8804A's in pairs to the basic module as shown in Figure 5. The lines (L_0 - L_7) are extended and connected to those of the new devices. The junctors (J_0 - J_3) of the two additional MT8804's are connected together to provide 4 additional signal paths. The network as shown has 12 signal paths and hence can carry 6 simultaneous telephone conversations.

The second expansion step is to increase the number of 8 port modules. Figure 6 shows the interconnection between two basic modules of Figure 4. The signal paths (S_0 - S_7) are extended to show how the two modules are connected. The control lines of each module (not shown) would be connected to the system data bus and appropriate enabling signals would have to be generated. That is, each module would also have a unique address. Combining both expansion steps is exemplified by a network comprised of two expanded switching modules of Figure 5. This would result in a system with 16 ports (telephone lines) capable of handling 6 simultaneous conversations.

The normal sequence in designing a switching network involves first establishing the maximum traffic handling capacity of the system. With this in hand, the 8 port modules can be designed with the appropriate number of MT8804A's. Modular system expansion would then only involve adding the required number of such modules. The number of MT8804A's required per module and total is shown in Table 1 as functions of the number of ports to the network and traffic handling capacity. From the table it can be seen that there is a one to one relationship between this traffic handling capacity and the number of MT8804A's required in the corresponding module. This can be used as a design aid in determining the amount of circuitry required to implement various sized systems. This information is expanded in the table of Table 2. Here, is shown the variation in the number of MT8804A's required as a function of traffic handling capacity only in a fixed 256 port system.

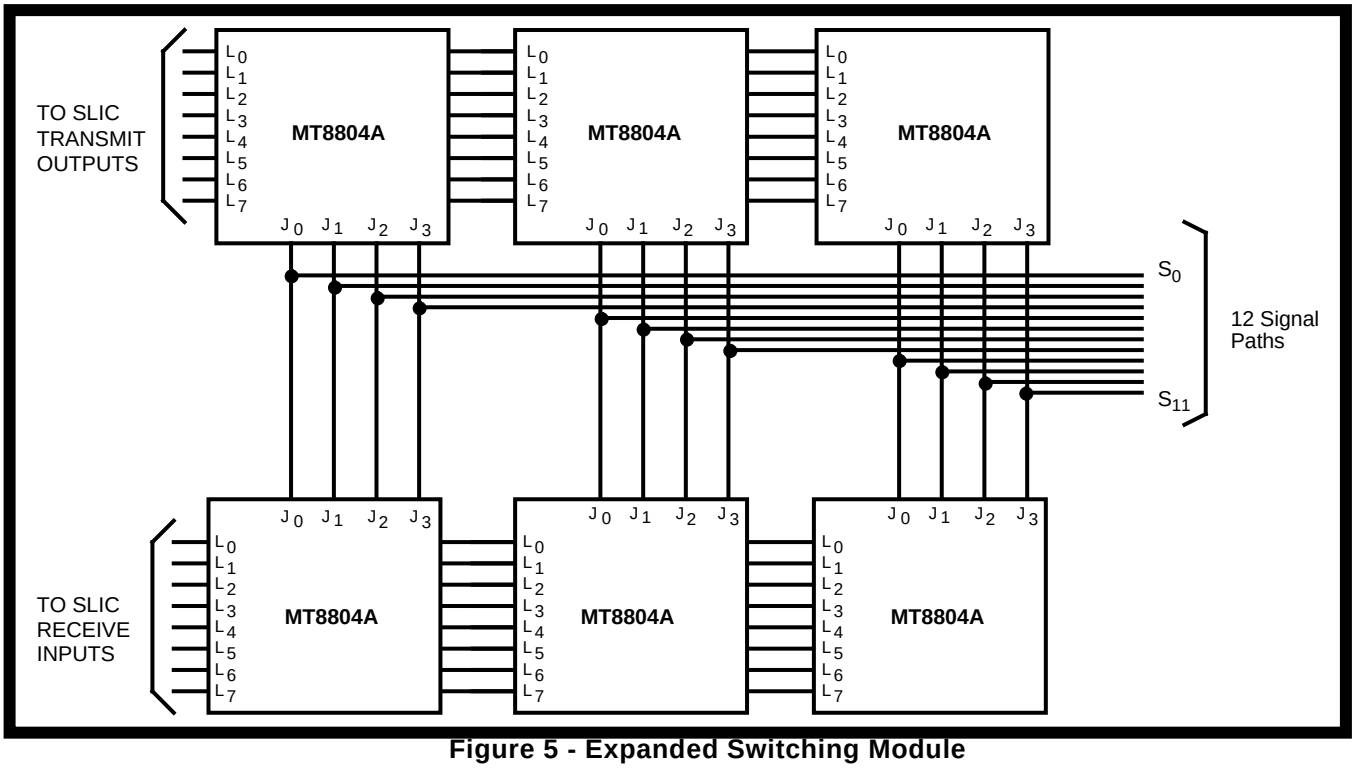

Figure 5 - Expanded Switching Module

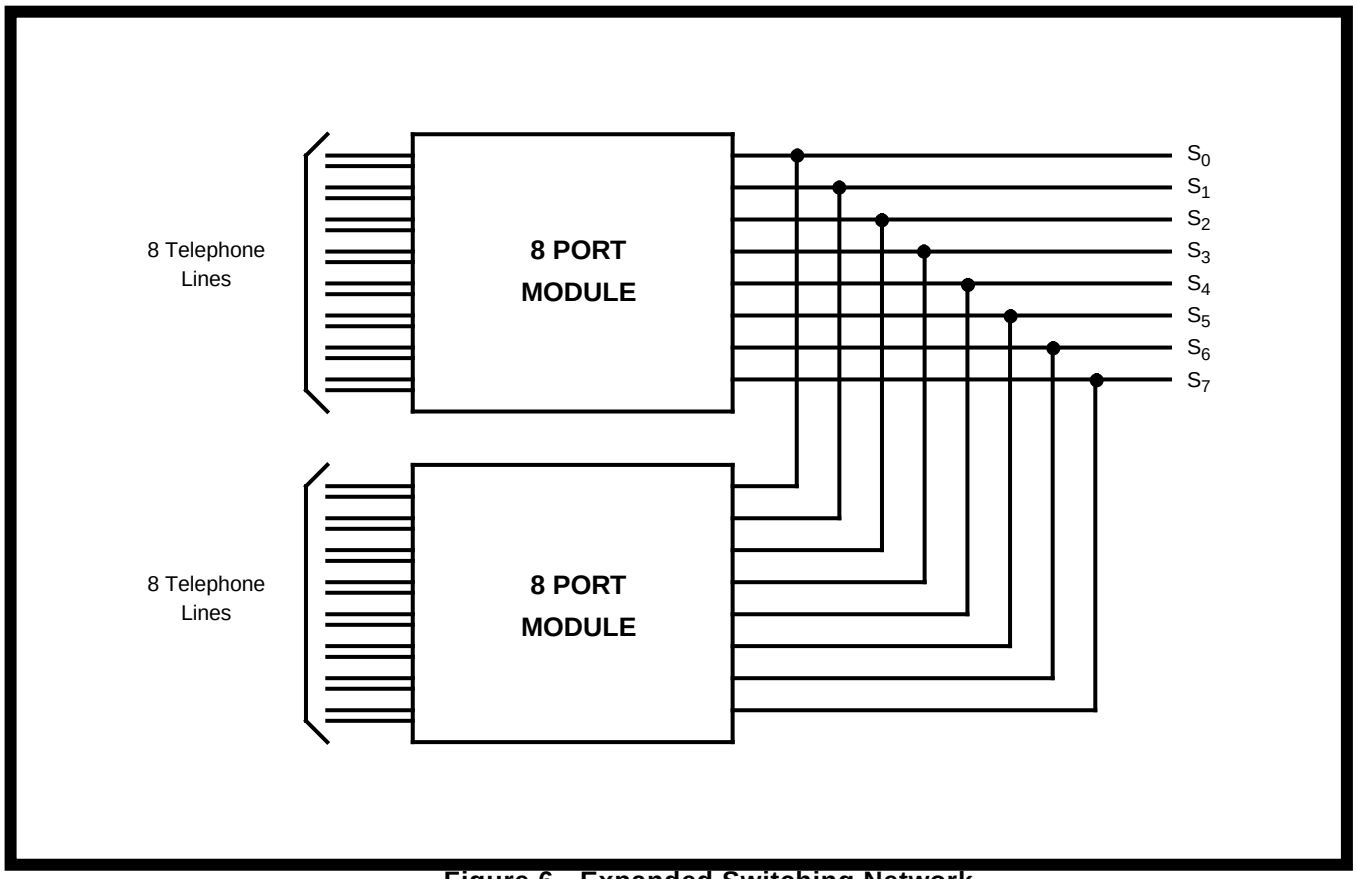

Figure 6 - Expanded Switching Network

NUMBER OF PORTS TO NETWORK	8	16	32	64	128	256
NUMBER OF 8 PORT MODULES	1	2	4	8	16	32
MAXIMUM NUMBER OF SIMULTANEOUS CONVERSATIONS	4	8	16	32	64	128
NUMBER OF SIGNAL PATHS REQUIRED	8	16	32	64	128	256
NUMBER OF MT8804A'S PER MODULE	4	8	16	32	64	128
NUMBER OF MT8804A'S TOTAL	4	16	64	256	1024	4096

Table 1. Number of MT8804A's as a Function of System Size

NUMBER OF PORTS TO NETWORK	256	256	256	256	256	256
NUMBER OF 8 PORT MODULES	32	32	32	32	32	32
MAXIMUM NUMBER OF SIMULTANEOUS CONVERSATIONS	4	8	16	32	64	128
NUMBER OF SIGNAL PATHS REQUIRED	8	16	32	64	128	256
NUMBER OF MT8804A'S PER MODULE	4	8	16	32	64	128
NUMBER OF MT8804A'S TOTAL	128	256	512	1024	2048	4096

Table 2. Number of MT8804A's as a Function of Traffic Density for a 256 Port Network

Summary

Using the MT8804A in line interface switching systems offers many advantages over conventional circuit elements. Replacing relays or smaller analog switch packages with this device results in great reductions in size and power consumption. Simultaneously, a low level of interchannel crosstalk is maintained. The on-chip control memory with microprocessor compatible inputs provides ease of

control and minimizes external circuit requirements. The 8 x 4 analog switch matrix configuration provides great flexibility in modular switching network design. All of these factors combine to make the MT8804A an ideal basis for PBX and key system networks.

Dual Tone Multifrequency Receiver Tester Control Circuit

The versatility of the MT8804A is shown in the Dual Tone Multifrequency (DTMF) receiver tester control circuit of Figure 7. The high and low tones may be mixed or a composite DTMF signal may be fed directly to the receiver under test. By mixing either f_L or f_H through the 200K resistor, plus or minus 6dB of twist may be added to the resulting DTMF signal. The amount of twist may be varied by adjusting resistor values. Dial tone rejection can be tested by switching in the CM7065, Zarlink Corporation's Precise Dial Tone Generator. The series resistor (R_S) and potentiometer are chosen to limit the voltage to the MT8804A to the supply limits. Sensitivity to 60Hz can be similarly tested.

If the receiver under test has the facility to accept dial pulses, these may be generated by switching the power supplies in and out at the required rates. A single pole double throw relay R1, is added to provide a switchable output impedance to simulate long line conditions. The relay drive is also switched by the MT8804A. The control of the MT8804A is provided by a stored test program in a microprocessor system or a hardwired controller which dictates the sequence of input signals presented to the receiver under test.

Test Equipment Switching System

Functional Description

The MT8804A is used as an analog coupling circuit in this test equipment switching system application. Various signal sources, voltmeters, a 2-channel oscilloscope and a frequency counter are connected to the multiplexer. (This section of course is arbitrary). The test points of the circuit under test can be connected to the multiplexer via banana plugs and jacks, aligator clips or any appropriate means of interconnection. This circuit can be very useful in analyzing prototype circuits which require various measurements at multiple test points.

The test instruments are connected to the test points of the circuit under test through the MT8804A's shown in Fig. 8. The individual instruments are selected by keys on the keypad as is the particular test point to which this equipment is connected. The system is operated as follows. First the 'TEST POINT' switch is pressed, followed by one of the numbered keys on the keypad. These correspond to the test points. Next, a sequence of keys designated the same as the test equipment is pressed. Finally the 'CONNECT' button is pressed. This completes the connection of the test equipment keyed in to the selected test point. This procedure can be repeated

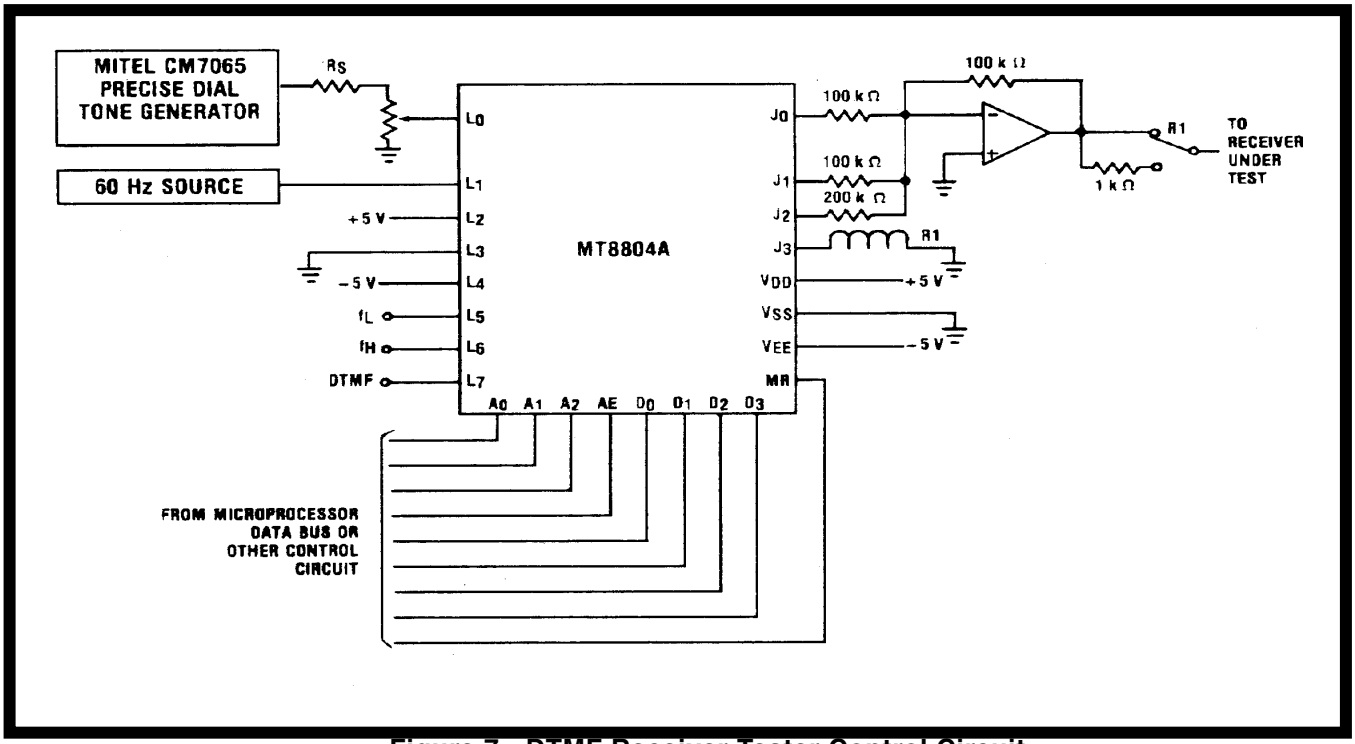

Figure 7 - DTMF Receiver Tester Control Circuit

until each test point has been connected or all of the test instruments assigned. The signal sources may be simultaneously connected to more than one test point.

It is a simple matter to disconnect all of the test instruments from a given test point. This is accomplished by again pressing the 'TEST POINT' switch, keying in the number corresponding to the appropriate test point and then pressing the

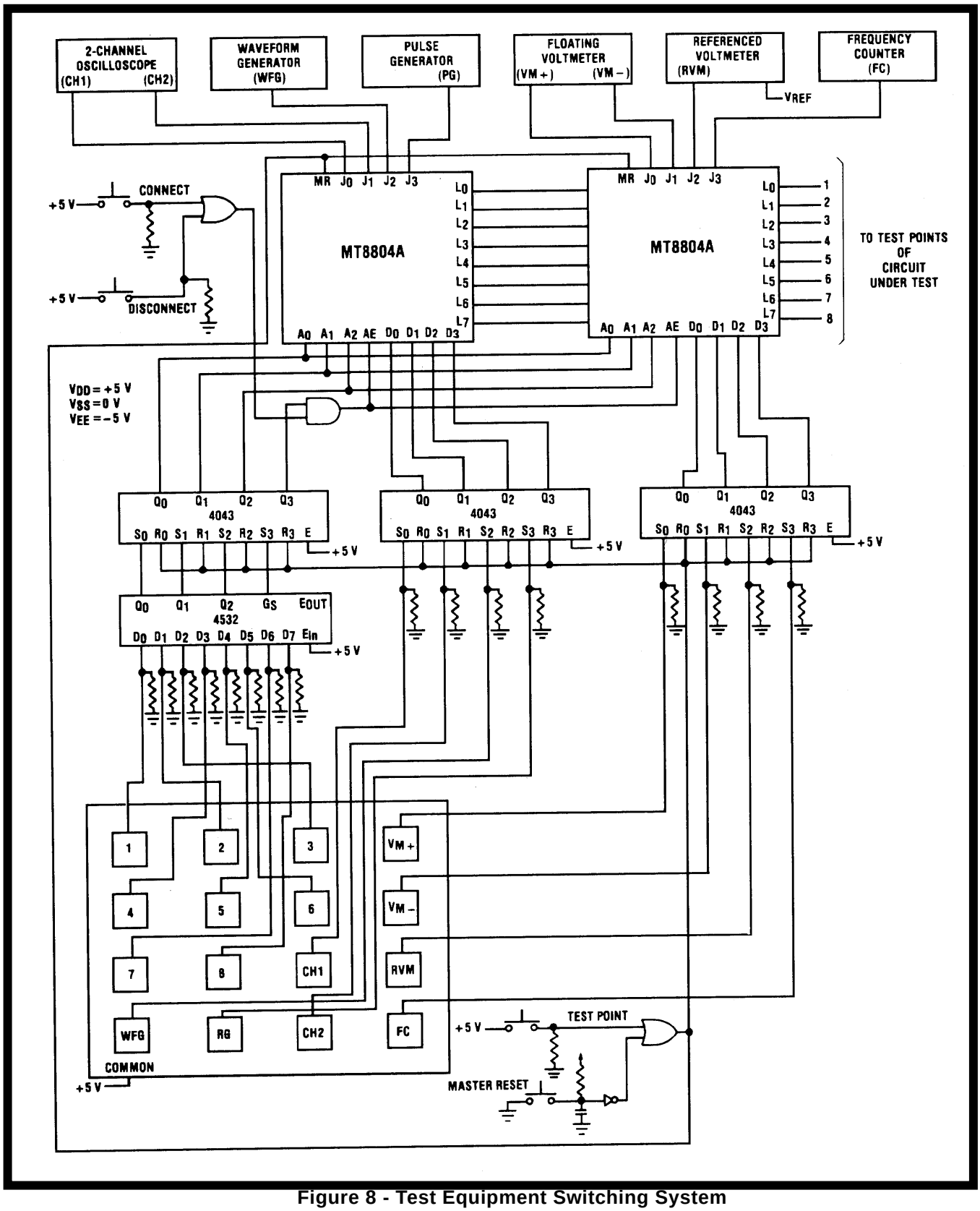

Figure 8 - Test Equipment Switching System

'DISCONNECT' button. Pressing the 'MASTER RESET' switch at any time disconnects all test instruments from all test points.

Circuit Operation

The two MT8804A's are the heart of this analog switching circuit, coupling combinations of test instruments to the eight test points of the circuit under test. Using all CMOS components and asynchronous operation results in ultra-low operating power consumption.

The allowable voltage swing from the signal sources is from +5V to -5V as determined by the MT8804A power supplies. The control inputs swing from +5V to 0V. User control of the circuit is via a standard 16 switch keypad and four additional momentary push-button switches. The keypad consists of 16 SPST switches with one common terminal which is connected to V_{DD} = +5V. The eight switches, marked '1' through '8' are connected to an 8 line to 3 bit binary encoder (4532). The remaining keys are connected to NOR R-S latches (4043) directly. All sixteen switches are pulled to ground through resistors.

Pressing the 'TEST POINT' switch clears all the latches, setting up the circuit for new data. The address (A_0, A_1, A_2) of the MT8804A from the '4532' encoder is asynchronously latched. This address is decoded by the MT8804A to select the line (L_0 - L_7) and hence the test point corresponding to the numbered key pressed. The Group Select (GS) output of the '4532' goes high whenever one of its eight data inputs goes high. This signal is also latched and used to gate the AE pulse to the MT8804A. This ensures that a test point number has been entered and hence prevents unwanted or accidental connections. A series of designated test equipment keys is pressed setting corresponding latches which are connected to the data inputs (D_0 - D_3) of the MT8804A's.

These data inputs in turn correspond to the junctors (J_0 - J_3) to which the test equipment is connected. Pushing the 'CONNECT' button pulses the AE inputs of the two MT8804A's, completing the desired connection.

During a disconnect sequence, the latches are cleared by the 'TEST POINT' switch. The numbered key pressed sets up the address of the test point to be disconnected. Pressing the 'DISCONNECT' button next pulses the AE inputs. However, this time, all data inputs are at logical 0's so that all switches to the addressed test point are opened. The 'MASTER RESET' when activated opens all switches in the MT8804A disconnecting all test equipment from all test points. A power-up reset is provided by the resistor, capacitor and inverter in the master reset line. This prevents unwanted connections on power-up. Any convenient values of resistance and capacitance are appropriate provided that the power-up time is short in comparison to the time constraint.

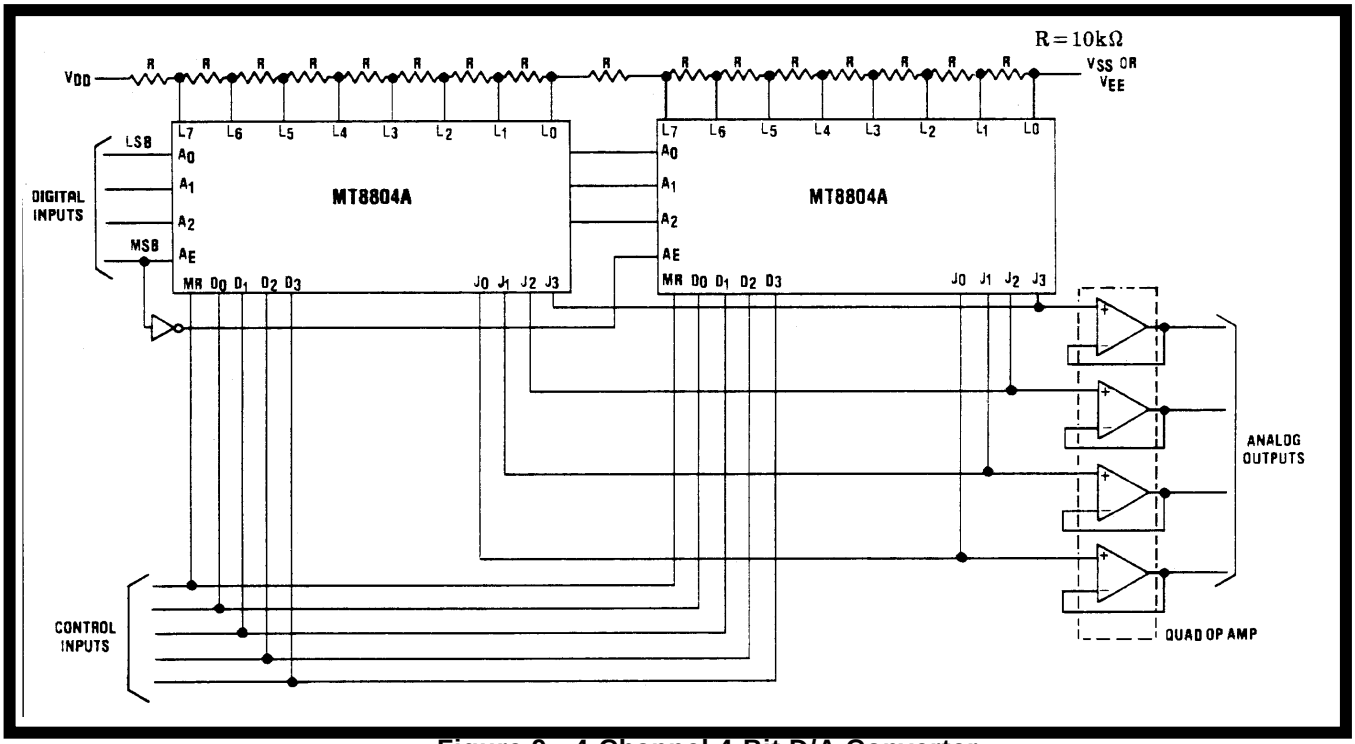

Figure 9 - 4-Channel 4-Bit D/A Converter

It is necessary, at all times, to supply power to the switching circuit prior to energizing signal sources.

4-Channel 4-Bit D/A Converter

The circuit of Figure 9 can be used to implement a low resolution (4-Bit), multichannel D/A converter. The digital signals are input on the address lines (A_0 - A1, AE) and the analog signals are switched from the resistive divider to the lines of the MT8804A (L_0 - L_7) and onto the junctors as selected by the data inputs. Any voltage profile can be programmed be it linear, logarithmic etc. by selecting the appropriate resistors for the divider network. The linearity and monotonicity of the converter are determined by the matching of resistors used. The temperature stability of the converter is dependent upon the relative tracking of the resistors in the network with temperature. The resistor network is shown with one end connected to V_{DD} and the other to V_{SS} or V_{EE}. By setting V_{EE} = -V_{DD}, the converter outputs will swing from V_{DD} to V_{SS} = 0V in one mode and symmetrically about 0V from ± V_{DD} in the other. The op amp buffers are used to reduce the effects of the ON resistance of the MT8804A.

The four analog outputs can simultaneously provide four independent voltages or any combination of outputs may be at the same voltage. The converter can be expanded to more digital inputs by extending the resistive ladder and adding MT8804's.

Programmable Attenuator

The programmable attenuator shown in Figure 10 is capable of providing up to 61dB of attenuation or 20dB of gain. Selecting the input attenuation is accomplished via the address inputs (A_0, A_1, A_2) and can be chosen in 3dB steps. The range is selected in 20dB steps by gating an attenuated input signal onto the appropriate junctor (J_0 -J_3) via the data inputs (D_0 - D_3). The attenuated input signal is buffered after passing through the MT8804A to provide constant input impedance to the attenuator circuit. The resistor multipliers shown provide a logarithmic profile of attenuation, calibrated in dB. A linear profile for use in control system applications is accomplished easily by appropriate choice of resistors. The attenuation accuracy is purely a function of resistor tolerances.

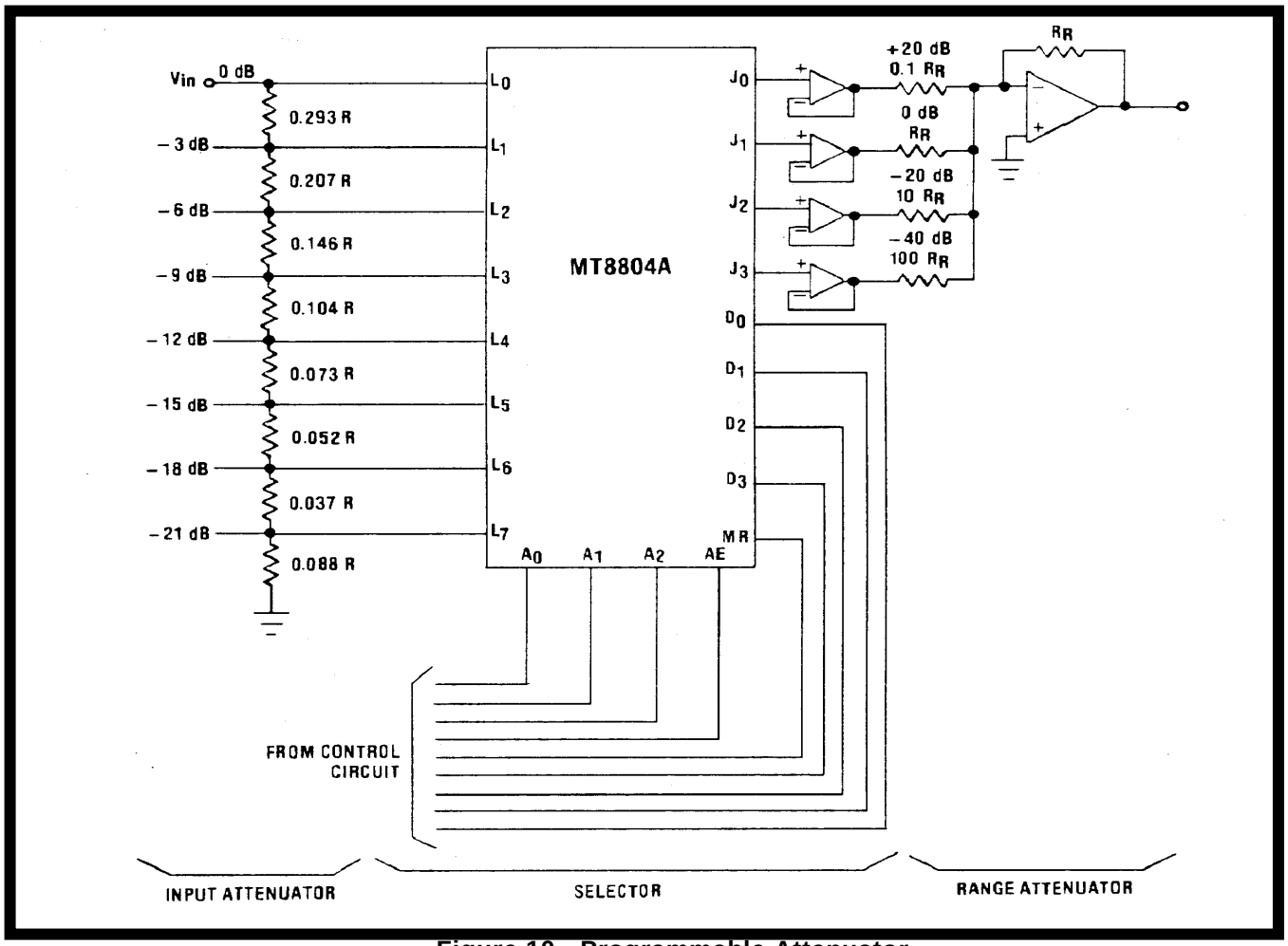

Figure 10 - Programmable Attenuator

The circuit attenuation can be expressed as follows:

FOR ADDRESS $(A_0\ A_1\ A_2)_2 = N10$

$A_{dB} = -(V_0/V_i)\ dB = (3 \times N_{10} + A_R)\ dB$

Where $(A_2\ A_1\ A_0)_2$ Address expressed as binary number

A_R Attenuation in dB of range attenuator

Multi-Output 2^n Programmable Frequency Divider

The circuit of Figure 11 provides up to 4 independent output frequencies each of which is a binary weighted multiple of a given input frequency. The frequency division factor is represented by the binary coded number of the address inputs of the MT8804A. The division range for the circuit shown is from 2^0 to 2^7. This range can be increased by adding counters for frequency division and MT8804A's to do the switching. The four data inputs (D_0 to D_3) control which output line or lines are switched to a particular frequency. The master reset (MR) when taken high turns all switches off.

MT8804A Status Indicator

In applications where the MT8804A is controlled by a hardwired control circuit as opposed to a microprocessor system, it may be necessary or desirable to have a record of line-junctor interconnections. Since outputs of the control latches are not available, a duplicate memory map is required. An 8 x 4 array of light emitting diodes is used to provide visual output of the information (See Fig. 12). Control data written into the MT8804A is copied into a Random Access Memory. The RAM shown, the Goldstar GD4710B, is a CMOS device organized as 16 four bit words. As such, 2 MT8804A's could be mapped with one device. The RAM outputs can be used for control purposes as well as visual outputs as shown in the diagram.

A scanning oscillator and counter (negative edge triggered) are used to continuously read data out of the RAM and refresh the LED matrix. The address provided by this binary counter is decoded to a one of eight active low output format by the 74HC138. Drive current is provided by two 74HC367 hex 3-state buffers. A variable duty cycle waveform may be applied to the output enables to provide intensity modulation. When data is written into the MT8804A and RAM, the address is provided by the control circuit. This address is isolated from the scanning counter by the octal three state buffer, 74HC241.

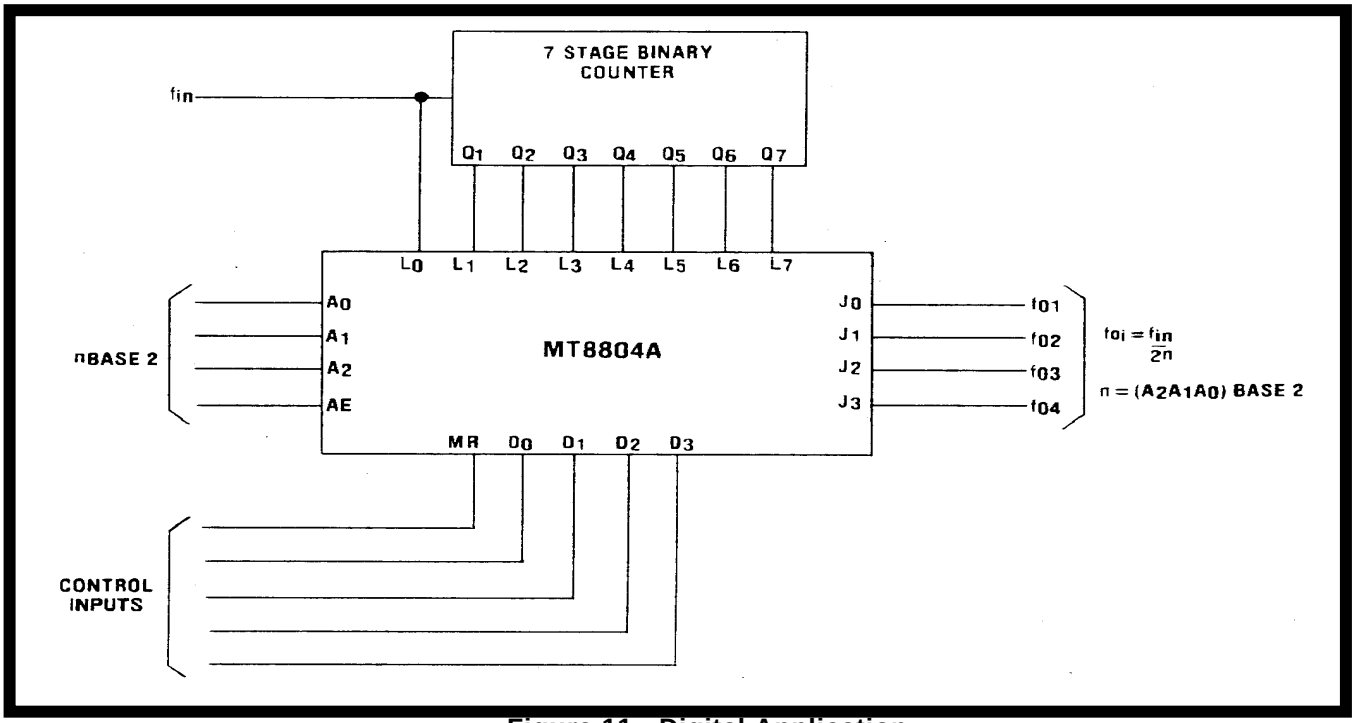

Figure 11 - Digital Application

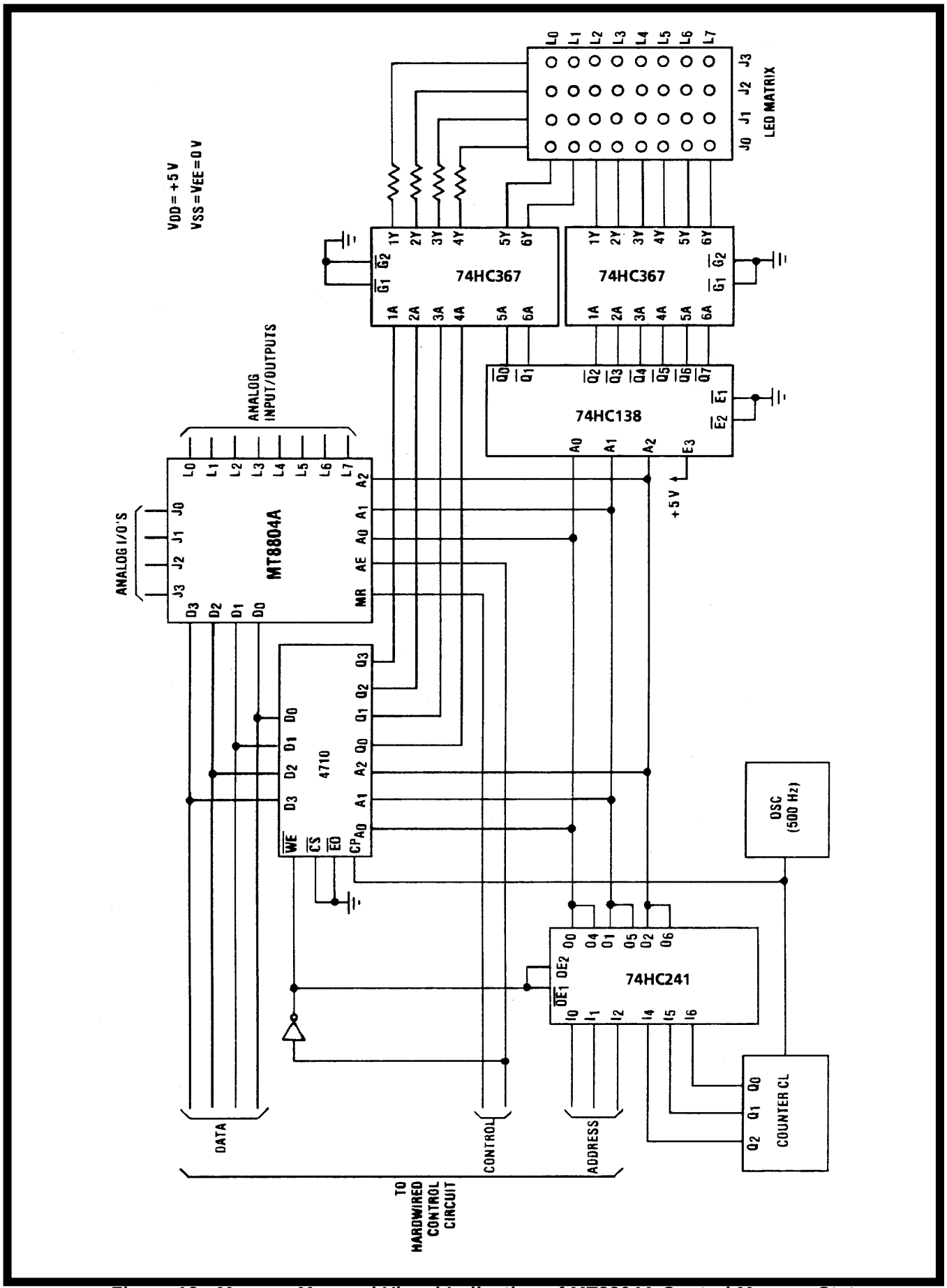

Figure 12 - Memory Map and Visual Indication of MT8804A Control Memory Status

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