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Introduction

The purpose of this Application Note is to assist both those designers who are familiar with the use of CMOS devices as well as those considering CMOS designs for the first time.

Attracted by the many advantages offered by CMOS devices, designers using them for the first time are often unaware of, or are overly sensitive to the phenomenon of latch-up. Understanding a few facts will resolve both of these situations. Basically speaking, any analog or digital device fabricated in one of the many CMOS processes available, can be made to latch-up if stressed severely enough. However, when properly applied, CMOS devices are quite insensitive to actual conditions that exist in most systems. Further, if a few simple precautions are taken at the design stage, then latch-up can be completely avoided.

Latch-up is defined as the creation of a low impedance path between the power supply rails by the triggering of parasitic, four-layer bipolar structures (SCR's) inherent in CMOS input and output circuitry. In this note, details of these SCR structures are examined in the context of Zarlink's ISO-CMOS technology. By developing an understanding of the aspects of circuit and system design related to the triggering of these SCR's, design methods and guidelines can be acquired to greatly reduce the probability of latch-up occurrence. By implementing the suggested techniques and circuitry, the designer can gain the advantages of CMOS circuitry without major concern about latch-up related problems.

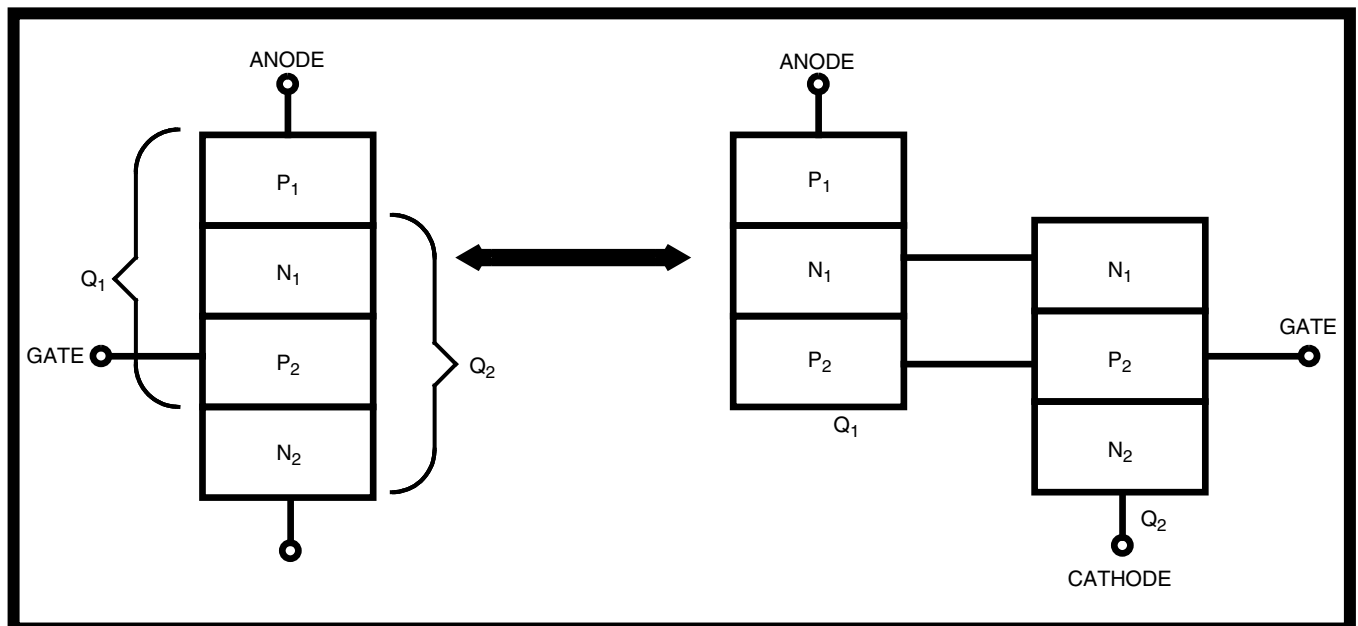


Figure 1 - Four-Layer SCR Structure

Semiconductor Device Considerations

Background on SCR's

Prior to discussing latch-up in CMOS devices, it is advantageous to briefly review the basic theory of SCR operation. This will be helpful in developing an understanding of the relationships between external circuit and system conditions and the resultant triggering of latch-up in CMOS devices. The basic SCR structure is that of a four-layer device as shown in Fig. 1. The device has three terminals: Anode, Cathode and Gate. Fig. 2 shows how the SCR can be modelled with two bipolar transistors, one NPN and one PNP. In the normal mode of operation, the SCR is turned on by injecting sufficient current into the base of Q₂ to turn this transistor on. When this is done, Q₂ begins to draw collector current via the base-emitter junction of Q₁. As a result Q₁ also turns on, injecting additional current into Q₂'s base. This in turn causes Q₂ to turn on harder, supplying more base current to Q₁. This positive feedback arrangement sustains conduction, and ensures that the SCR continues to conduct even if the gate current is interrupted.

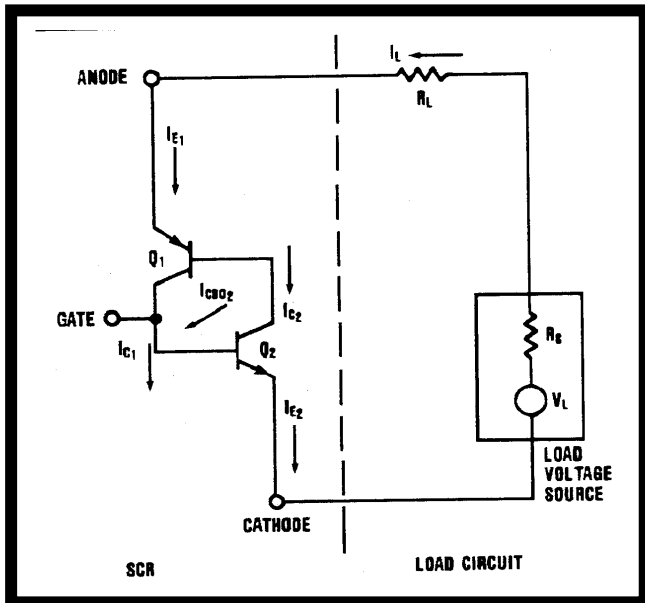


Figure 2 - Bipolar Model of an SCR

The device will remain in this latched state indefinitely. To turn the SCR off, one of two things can be done. If the voltage applied across the SCR is reduced to the point where Q₁'s base-emitter junction turns off (V_{SUS}), then Q₂ will be starved of base current and the SCR will turn off. Alternatively, if the current through the SCR is reduced below its holding current then it will also turn off. The holding current is the minimum current required to sustain conduction and is a function of the physical dimensions of the device and the transistor gains (Fig. 3). As mentioned, this is the way that the SCR

is controlled in normal applications. There are various other ways that an SCR may be triggered. These must be examined as they are directly related to latch-up problems.

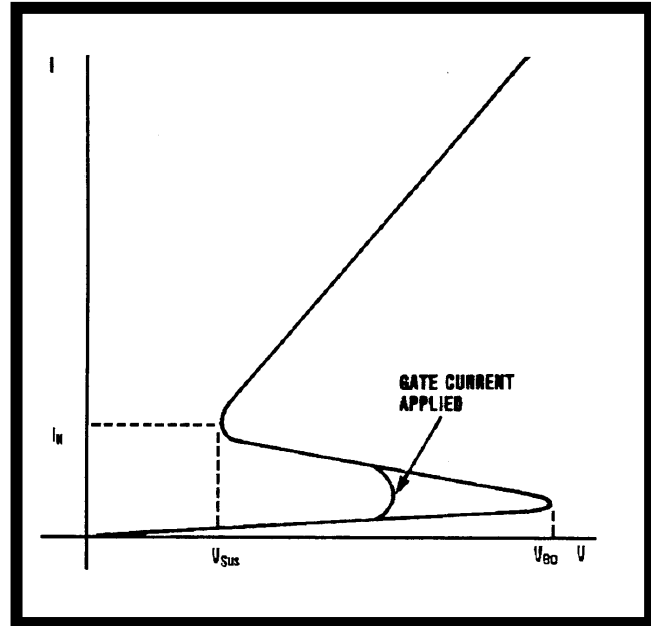


Figure 3 - SCR Current-Voltage Characteristic

Looking at Fig. 2, it can be seen that the load current and the two emitter currents of Q₁ and Q₂ are all equal. Also the load current is equal to the sums of the two collector currents and a leakage current from Q₂'s collector to its base (I_{CBO2}). It can be shown (refer to Appendix) that:

$$I_L = I_{CBO2} \left[\frac{(1 + B_1)(1 + B_2)}{(1 - B_1 B_2)} \right] \quad (1)$$

Where B₁ and B₂ are the current gains of Q₁ and Q₂ respectively.

Normally, with no base current supplied to Q₂, the load current will be small since the leakage I_{CBO2} is small, as are the current gains (B₁, B₂) at this low value of collector current. If however, the current gains increase to the point where the product, B₁ B₂, approaches unity, then the load current will become very large, limited only by the load impedance, the series impedance of the SCR, and source impedance of the power supply. There are various applied conditions that will cause this to happen. Increasing the load voltage beyond the breakover voltage, V_{BO}, will have this effect. As the anode-cathode voltage across the SCR increases, the collector-emitter voltages of Q₁ and Q₂ also increase. This corresponds to increases in the collector-base reverse biases. The collector-base junctions of the two transistors are physically the same area, the N₁-P₂ junction (Fig. 1). As the

reverse bias increases, the energy of the minority carriers increases causing more carriers to be dislodged, which in turn pick up energy. This continues until the junction undergoes an avalanche breakdown resulting in an increase in the collector currents of Q_1 and Q_2 . The resulting increase in B_1 and B_2 cause the SCR to latch on.

A very rapid change in the anode to cathode voltage of an SCR can also cause it to trigger. This is known as the “dV/dt” effect. The N_1 - P_2 junction, being reversed biased, exhibits a capacitance. This capacitance varies with the reverse bias voltage applied across the junction. Hence the current through the capacitor is described by:

$$\frac{d(C_j V_{AK})}{dt} \quad (2)$$

$$= \frac{C_j dV_{AK}}{dt} + \frac{V_{AK} dC_j}{dt} \quad (3)$$

The junction capacitance, C_j decreases with increasing reverse bias and hence the second term of equation (3) is negative. If, however, the rate of change of applied voltage is large enough, the first term of equation (3) will dominate and the current through the SCR will increase. If the current increases sufficiently to cause the $B_1 B_2$ product to approach unity, then the SCR will latch on.

The effects of temperature must also be noted at this point. Increasing temperature will cause an increase in both the leakage current through the SCR and in the current gains $B_1 B_2$ of the two bipolar transistors. As such, the magnitude of the driving force required to turn the SCR on will decrease with increasing temperature. In other words, the SCR will be more easily triggered as temperature increases for any of the triggering mechanisms described.

Corollaries exist between each of the three methods of turning an SCR on as described, and the ways in which the parasitic SCR structures of CMOS devices are triggered. The normal mode of triggering an SCR is by injecting current into its gate terminal. This corresponds to forcing current into the inputs or outputs of a CMOS device by applying voltages that go outside of the power supply rails. This is by far the most common form of latch-up triggering. The avalanche breakdown mechanism described also applies directly to CMOS devices, although its occurrence is far less prevalent. Excessive voltage on the power supply pins, whether continuous or transient, may result in latch-up occurrence. It is also theoretically possible to trigger parasitic SCR devices by the dV/dt method as a result of high speed transients on the supply rails. However, this will rarely happen in a real application. Each of

these triggering methods will be examined in the next section in the context of the ISO-CMOS topology for both the output and input structures.

Parasitic Bipolar Structures in the ISO-CMOS Topology

As with any CMOS technology, ISO-CMOS contains certain parasitic bipolar structures associated with its output devices and input protection circuitry. These parasitic transistors are interconnected in such a way as to form four-layer devices. As such, SCR devices are present at both the inputs and outputs of ISO-CMOS circuits. These devices are normally in their off state and will remain off as long as the absolute maximum ratings of the devices are not exceeded.

Output SCR Structures

A typical ISO-CMOS output driver contains one N-channel MOSFET with its source tied to V_{SS} and one P-channel MOSFET with its source tied to V_{DD} . The drains of the two transistors are connected together to form the output and the gates are commoned to form the input (Fig. 4). The fabrication of these transistors in close proximity results in the formation of a parasitic SCR connected directly across the power supply rails. When triggered, this SCR presents a low impedance to the power supply causing excessive current to flow. This situation is potentially destructive, resulting in damage to bond wires or metal supply tracks on the die due to localized overheating. The SCR is formed as follows. A vertical NPN transistor results from the fabrication of the N-channel device. The N-substrate serves as the collector and is biased at V_{DD} . The P-well acts as the base and the source and drain N-diffusions are the emitters of the transistor. One emitter is tied to V_{SS} and the other to the output. A wide base lateral PNP transistor is formed when a P-channel device is located close to a N-channel transistor. The P-channel source and

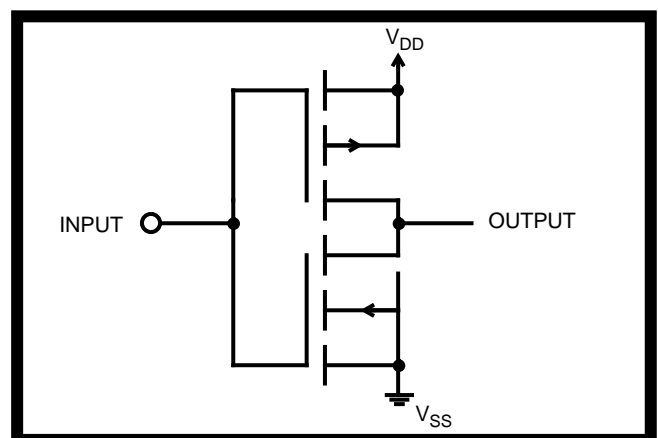


Figure 4 - Typical Output Circuit

drain diffusions are two emitters of the transistor: one tied to V_{DD} and the other to the output. The N-substrate acts as the base and hence, is in common with the collector of the vertical NPN. The P-well is the collector of the PNP which is also base of the NPN. Due to the shared diffusions, the vertical NPN and lateral PNP transistors are effectively connected as an SCR (Fig. 5). This parasitic SCR is connected directly across the supply rails. Hence, when triggered, it can cause excessive current to flow. The SCR is normally turned off for nominal operating supply voltages and with all output voltages within the power supply limits. This SCR may be externally triggered causing the output structure to latch-up. The triggering mechanism can be any one of those mentioned in the previous section.

Output voltages being forced outside of the power supply limits is the most common cause of output latch-up. Two parameters are defined at this point for use in subsequent discussions. These are I_{LU} and V_{LU} . I_{LU} is the current which must flow through the output structure to cause latch-up to occur. V_{LU} is the voltage excursion outside of the power supply rails at the output pin that results in I_{LU} flowing through the output structure. In other words I_{LU} and V_{LU} are the conditions at the output pin that will result in latch-up triggering. These same parameters also apply to input latch-up (see next section). Consider first an output voltage which goes below V_{SS} by more than V_{LU} . This causes the P-well to output base-emitter junction of the vertical NPN transistor to become forward biased. Since this acts as the SCR gate, triggering occurs. Current is pulled from V_{DD} through the lateral PNP and is injected into the P-well, causing a localized drop across this diffusion. This voltage drop will forward bias the base-emitter junction of the NPN which is referenced to V_{SS} . Once this occurs, latch-up will be sustained and a low impedance path is created from V_{DD} to V_{SS} .

A note must be taken here in regard to the amount of over-voltage required to trigger latch-up. In the above paragraph, it was mentioned that voltages exceeding the supply rails by more than V_{LU} will cause a current I_{LU} to flow and hence trigger latch-up. The guaranteed values quoted in the data sheet are 0.3V and 10mA respectively for these parameters. These limits are used in production testing and hence, appear in the Absolute Maximum Ratings for Zarlink devices. In practice, it is more likely to require from 0.6V to 2V of over-voltage and from 50 to several hundred milliamps of current to cause output latch-up to occur. For input latch-up to occur, it can take several volts of over-voltage and similar currents to induce latch-up due to the series resistance of the input protection circuitry (Fig. 6).

When the V_{DD} supply rail is exceeded by a voltage greater than V_{LU} , a similar set of events occurs. In this case, the output to substrate base-emitter junction of the lateral PNP becomes forward biased. Collector current from this transistors injected into the P-well, again causing a lateral voltage drop. This voltage drop causes the P-well to V_{SS} referenced base-emitter junction of the NPN to become forward biased. This transistor's collector current, pulled from the substrate, causes a lateral voltage drop across the substrate. This voltage drop, in turn, will forward bias the V_{DD} to substrate base-emitter junction of the PNP. Thus, latch-up will be sustained even if the output over-voltage condition is removed and a low impedance path again exists between V_{DD} and V_{SS} .

There are two other causes of output latch-up that are less likely to occur, but nonetheless must be noted. The first of these is the result of over-voltages on the power supply pins. Excessive voltage between V_{DD} and V_{SS} (i.e., greater than the absolute maximum rating) can cause an avalanche breakdown of the reverse biased substrate to P-well collector base junction of the bipolar transistors.

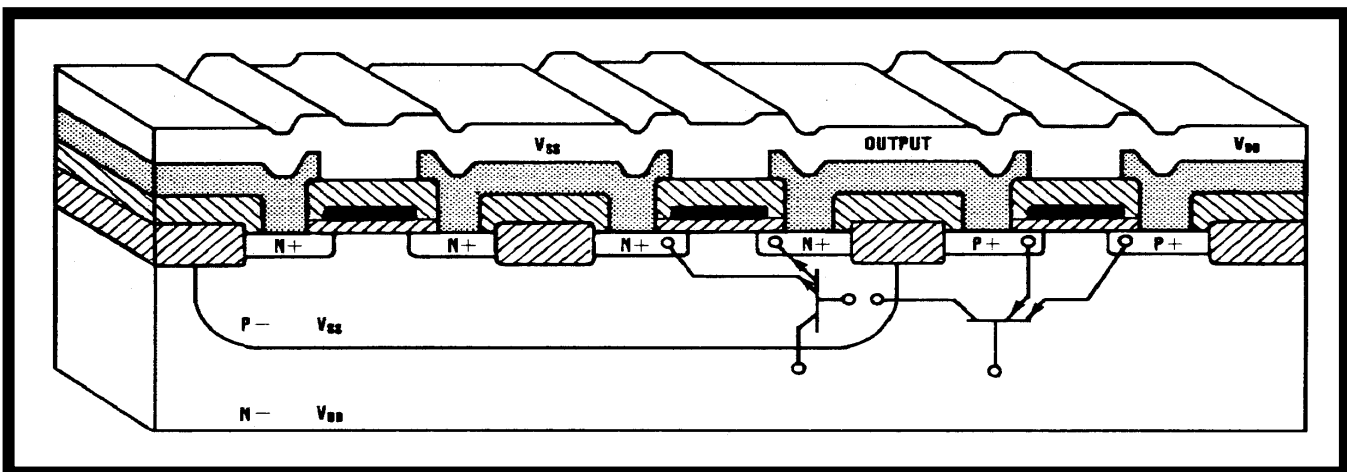


Figure 5 - Output SCR Structures

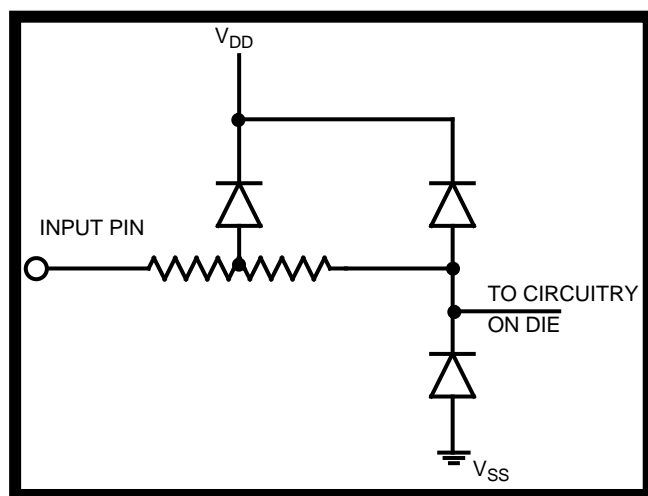


Figure 6 - Input Protection Circuit Schematic

This will cause the SCR to trigger as outlined in the previous section. The second triggering mechanism will be apparent in very few systems. Very fast voltage spikes on the power supply rails can induce a “dV/dt” triggering of the SCR, also as outlined earlier. This can potentially result in circuit damage by transients which in themselves would not have sufficient energy to cause damage due to localized power dissipation. Once triggered, the SCR may remain latched on until the supply voltage is reduced below its sustaining voltage or if the current is reduced below its holding current.

Input SCR Structures

Parasitic SCR structures can also result due to the fabrication of CMOS input protection circuitry. The ISO-CMOS input protection circuit schematic is shown in Fig. 6. As shown, there is a distributed diode connected to V_{DD} and another diode to V_{SS} . The series resistor is primarily intended for static protection, but also provides latch-up protection. The diodes are connected together at the input node. An SCR structure results when the V_{DD} referenced

diode is fabricated in close proximity to an N-channel transistor (Fig. 7) or when the V_{SS} referenced diode is located close to a P-channel device. (Fig. 8).

It is important to note here the difference between input and output SCR structures. The output SCR was connected directly between V_{DD} and V_{SS} , and hence, is more likely to be destructive once triggered. The input SCR structure is connected from the input node to one of the supply rails. Thus, for an input to remain latched, the circuitry driving the input must be capable of supplying the sustaining current of the SCR. For this latch-up to be destructive, the input driver must be capable of supplying large amounts of current. A potentially more dangerous situation occurs when a complimentary transistor, to the one forming the SCR, is located nearby. A secondary SCR structure results from this and it is connected across the supply rails (Figs. 7 and 8).

Consider the V_{SS} referenced diode situation first. The source and drain diffusions of the P-channel transistor form the emitters of a lateral PNP transistor. The substrate acts as the base and the P-diffusion of the diode is the collector. This diode, with the substrate, forms a vertical NPN transistor. The two transistors are interconnected as an SCR due to common diffusion areas. If an applied input voltage is below V_{SS} by more than V_{LU} , then the gate-cathode junction of the SCR will become forward biased and turn the SCR on. This latch-up condition will continue as long as this input condition persists or if the input circuitry can supply the minimum holding current. As mentioned, a potentially more hazardous situation can develop if an N-channel transistor is also located nearby. The P-well of this transistor serves as a second collector of the lateral PNP transistor. When the input voltage goes negative, the gate of the SCR is turned on as mentioned. However, this second collector now injects current into the P-well causing a second SCR

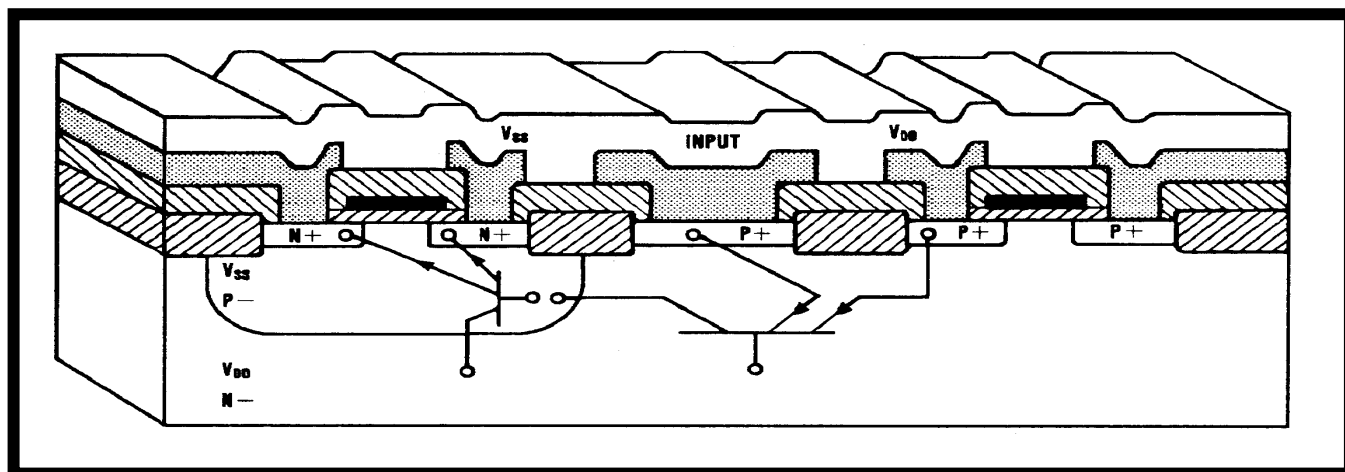
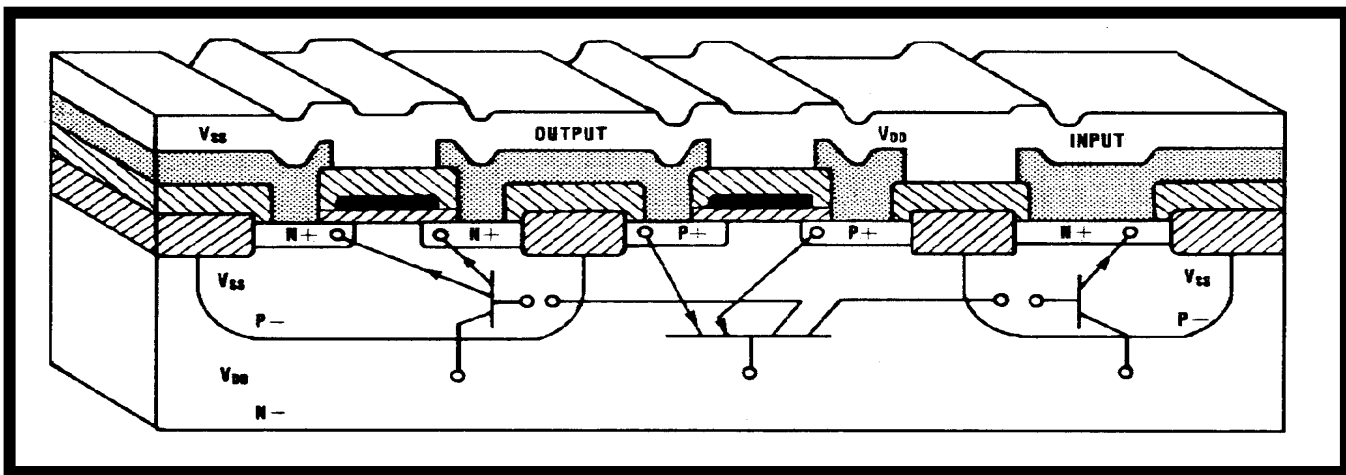


Figure 7 - Input SCR Structure with V_{DD} Diode

Figure 8 - Input SCR Structure with V_{SS} Diode

Forced I/O Condition	Latch-Up Inducing Conditions	
	V_{LU} (Volts)	I_{LU} (mA)
Outputs above V_{DD}	1.9	200
Outputs below V_{SS}	1.0	90
Inputs above V_{DD}	1.9	80
Inputs below V_{SS}	25.0	25

Table 1. MD74SC540AC Latch-up Inducing Voltages and Currents

structure to latch on. This device is connected across the power supply rails and hence, can be destructive. This same situation can result with the V_{DD} referenced protection diode. In this case, SCR structures will be triggered by voltages which exceed V_{DD} by more than V_{LU} .

As was mentioned earlier, the actual values of V_{LU} and I_{LU} are typically much greater than the 0.3V and 10mA limits on the data sheets. Table 1 shows some of the numbers pertaining to the current production version of the MD74SC540AC, one of Zarlink's Octal Interface devices. As can be seen it requires voltages from 1.0V to 1.9V and currents from 90 to 200mA to trigger output latch-up. On the input side, it requires 1.9V for V_{LU} and 80mA for I_{LU} in the V_{DD} case. For the V_{SS} case, I_{LU} is only 25mA, but V_{LU} is 25V and hence this situation would virtually never exist in a system. It has been empirically determined that if a device exhibits values of I_{LU} exceeding a few volts, then this device will be extremely insensitive to latch-up in the majority of circuits and systems. A severe system fault would be required to induce latch-up in such devices.

System and Circuit Considerations

In the majority of systems and circuits using CMOS devices, latch-up should not be a major cause for

concern. Being aware of the sources of latch-up problems will aid the designer in even further reducing the probability of latch-up damage to his circuits. Implementing some of the precautionary measures suggested in the following sections will ensure a trouble-free system.

The aspects of system and circuit design that can result in latch-up occurrence will be examined in the context of a "worst case" system example. In other words, systems containing combinations of the attributes of the example system will be more likely to experience latch-up problems. The relationships between these systems aspects and the resultant latch-up triggering mechanisms will be described. Suggestions will be made intent upon reducing the risk of triggering the parasitic SCR's through careful design techniques. The protection circuits, which will be illustrated, should help in preventing circuit damage in case latch-up occurs. It should be noted at this point, that in systems where the input and output pins of the CMOS devices never go outside of the power supply rails either during power-up or in continuous operation, latch-up is not likely to ever occur. The first step, then, is to define a system which contains various components that qualify it for a "worst case" rating in a latch-up sense.

A "Worst Case" System

A circuit or system which has all of the following attributes and/or capabilities is more likely to experience latch-up problems. This is not to say that latch-up is inevitable in systems containing many of these attributes, only that the designer must be aware of potential problems and take steps at the design stage to avoid them. The following list summarizes the system aspects most likely to be associated with latch-up problems:

- 1) System operation/maintenance procedures allow insertion or removal of printed circuit cards with system power applied.
- 2) The system is powered by multiple supply voltages (e.g. $\pm 12V$, $+ 5V$, and Gnd) or has a multi-supply at same voltage (e.g. $+5V$ regulated, $+5V$ unregulated).
- 3) Circuits utilize complex capacitive decoupling techniques particularly associated with multiple power supply voltages.
- 4) Integrated circuits on one system PCB drive other devices on different PCB's via a backplane, ribbon cable, etc.
- 5) Devices drive high capacitive loads such as long data or address busses.
- 6) System contains high speed address and/or data buses of sufficient length to cause their inductive properties to become significant at the frequencies in question (ribbon cables are a prime example).
- 7) System has electronic inputs that are directly accessible by the end user of the system.
- 8) Digital devices are driven from analog devices powered from higher supply voltages, utilizing input diodes for clamping.

Each of the above entries will now be examined in terms of its potential for triggering latch-up. The first four items are very interdependent. While each of these will be given consideration in separate sections, cross referencing will be extensive. The remaining items are relatively independent and thus, will be looked at in relative isolation.

Insertion/Removal of System PBC's "Live"

Inserting or removing printed circuit cards from a powered-up system can trigger latch-up in several different ways if certain precautions are not taken. One potential hazard that can occur is for an input or output edge terminal to make contact before the power supply pins are connected. If driven by a device on another circuit card, this input/output pin could have a voltage applied to it with no supply voltage to the device. Even if this situation exists for only a short period of time, then latch-up may be triggered when the power supply pin is connected. It is important to note that three-state outputs are also vulnerable in this situation. Such output drivers only present a high impedance to voltages within the device supply rails. Voltages on these outputs exceeding the supply can indeed trigger latch-up.

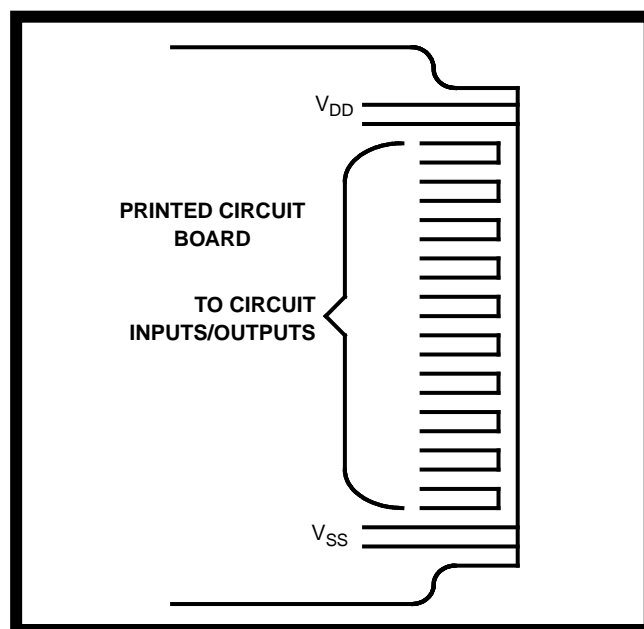


Figure 9 - PCB with Inset I/O Edge Terminals

One solution to this problem is to slightly extend the power supply terminals with respect to the remaining edge terminals on the PCB (Fig. 9). This will ensure that power supply connections are the first made and last broken on insertion and removal of the PCB respectively.

Plugging a circuit card live into a system with multi-power supply voltages can result in the application of power supply over-voltages to certain devices. Consider the local decoupling scheme shown in Fig. 10. If a PCB containing such decoupling was plugged into a system live, then the following situation could result. Assume that all capacitors are discharged and that C_1 is much greater than C_2 . It is possible that when the PCB is inserted, the $+12V$ terminal makes connection first, then the ground, and lastly the $+5V$ connection is made. In this situation, C_1 and C_2 are momentarily connected in series. The $+12V$ volts applied to C_1 causes the voltage at the ground point to increase in

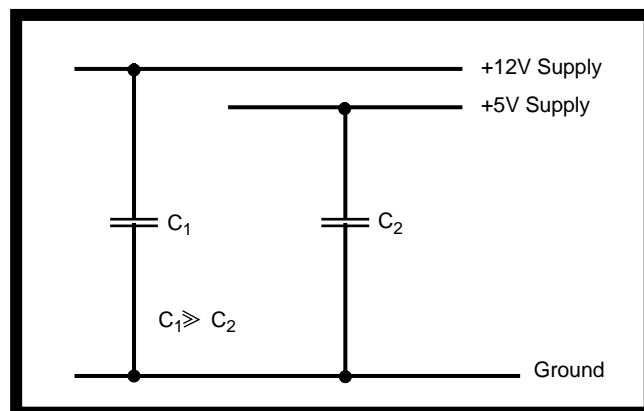


Figure 10 - Local Decoupling Scheme in Multi-Supply System

accordance with the charge sharing between C_1 and C_2 . This voltage could approach 12 volts since $C_1 \gg C_2$. When the ground terminal makes connection, the voltage at the nominal 5V rail will jump up by the amount of voltage initially present at the ground point (i.e. almost 12V). This results in an over-voltage condition being applied to the devices supplied by the 5V rail. If the applied voltage exceeds the absolute maximum rating for these devices then latch-up may be triggered by the avalanche breakdown mechanism described in an earlier section. This problem is more likely to be evident in systems with power supplies differing greatly in magnitude since potential over-voltages can become quite large. A prime example is a telephone switching system which would typically contain a -48V supply as well as +5V and other supply voltages.

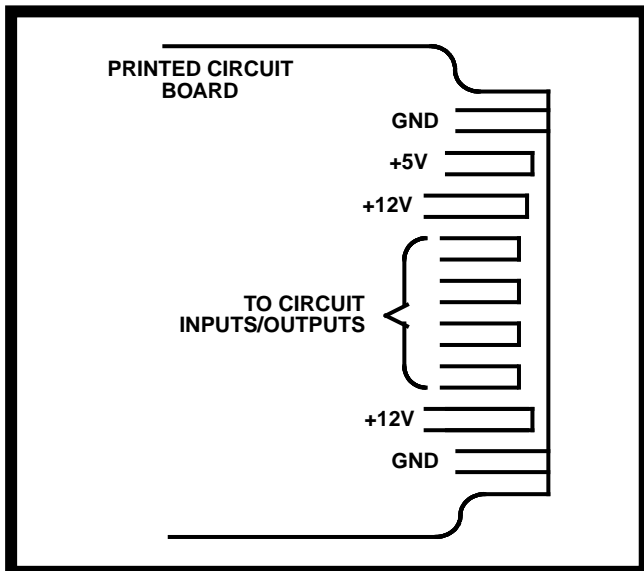


Figure 11 - Multi-Level Indentations of I/O Edge Terminals

This problem can also be overcome by indenting the edge terminals on PCB's. In this case, there must be more than one level of indentation to ensure that the power supply connections are made in a sequence that will alleviate this problem. The safest way to accomplish this is to have power supply connections made in the order of ascending voltage magnitude (Fig. 11). For example, in a system with a +5V supply and $\pm 12V$ supplies, the ground line should make connection first, the +5V supply next and finally, the +12V and -12V supplies at the same time. This ascending order of magnitudes ensures that no over-voltages occur even if one of the power supplies pulls the other through the decoupling capacitors. The ground line should always make connection first to ensure that a positive supply does not pull a negative one or vice versa. Connecting opposing power supplies (e.g. $\pm 12V$) at the same time will ensure cancellation of the effects of their connection.

In systems which have large number of power supplies to contend with, it may not be feasible to provide the required number of indentations on the PCB. In this case, a careful analysis of the decoupling used must be done to establish potential problem areas. Where possible, decoupling capacitors on different supplies should be of equal magnitude. This will tend to minimize over-voltages due to equal charge sharing between the capacitors. If after all possible precautions have been taken, there is still a possibility of power supply over-voltages occurring, then it may be necessary to provide some form of current limiting or local regulation to prevent circuit damage.

The simplest form of protection is to connect a resistor in series with the power supply (V_{DD} or V_{SS}) pin of the devices in question (Fig. 12a). The size of this resistor can be chosen to either prevent latch-up from occurring or to prevent circuit damage when latch-up does occur. If latch-up is to be prevented then the minimum resistor value is chosen as follows:

$$R = \frac{V_{\text{Supply}} - V_{DD_{\text{Max}}}}{I_{DD_{\text{Max}}}}$$

where V_{Supply} = Maximum Supply Voltage Generated
 $V_{DD_{\text{Max}}}$ = Absolute Maximum Rating for V_{DD}
 $I_{DD_{\text{Max}}}$ = Supply Current at $V_{DD_{\text{Max}}}$

This will ensure that $V_{DD_{\text{Max}}}$ is never exceeded at the device.

To simply prevent damage due to latch-up, the resistor is chosen to limit the supply current to a few hundred milliamps at the maximum applied voltage. There are a few factors which must be taken into consideration when the maximum value for this resistor is selected. The source impedance of the power supply will be increased by the amount of the added resistance. This will result in a decrease in the current sourcing or sinking capacity of the device, depending on whether the resistor is in the V_{DD} or V_{SS} line respectively. There is also a corresponding increase in the output propagation delay, proportional to product of the protection resistor and the load capacitance. Finally there is a decrease in the noise immunity of the device proportional to the product of this resistor and the total instantaneous supply current (including the output currents). For devices such as the MD74SCXXX, it is recommended that this resistor be placed in the V_{DD} line as there is more available noise immunity for high level outputs (when driving TTL or other MD74SCXXX devices).

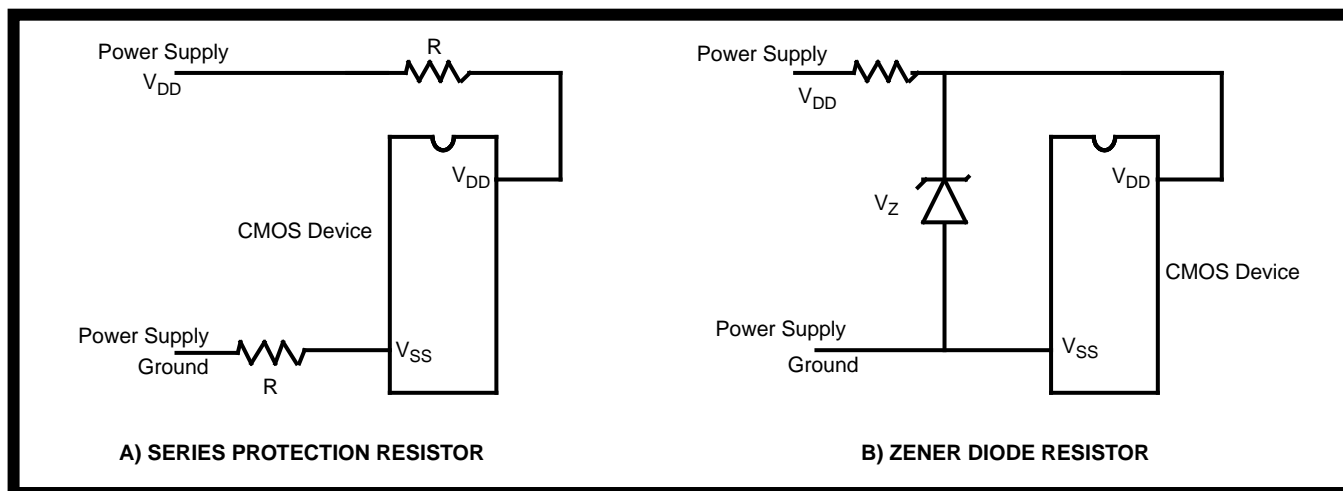


Figure 12 - Power Supply Over-Voltage Protection

If a current-limiting resistor cannot be used due to constraints on output drive, speed or noise immunity, then the alternative is to connect a zener diode between V_{DD} and V_{SS} to prevent over-voltages across the device (Fig. 12b). A current-limiting resistor may still be necessary, but its value can be very small, limited only by the power handling capacity of the zener diode.

There is one last potential hazard that can develop due to “live” insertion of PCB’s. On boards with little local decoupling, plugging the card in can result in an extremely fast transient on the power supply leads of devices on the board. These transients could theoretically result in triggering latch-up due to the dV/dt effect described earlier. This problem can be avoided by decoupling the power supply on the board with sufficiently large capacitors to slow down the power supply ramp up when the board is plugged in. These capacitors must be chosen to be compatible with the overall decoupling scheme to prevent the over-voltage problem just described.

Similar transients on the power supply can be generated due to switching of high speed, high current devices such as ECL and Schottky TTL circuits driving heavy DC current loads. Also, back EMF generated by opening of inductive loads such as relays can induce nasty voltage spikes. Adequate high frequency decoupling will usually remedy the problem. A 0.01 to 0.1 μ F ceramic capacitor connected as close to the device as possible across the power supply pins will shunt most of this high frequency energy to ground (Fig. 13). Connection of flyback diodes around inductive loads is also recommended to limit back EMF surges.

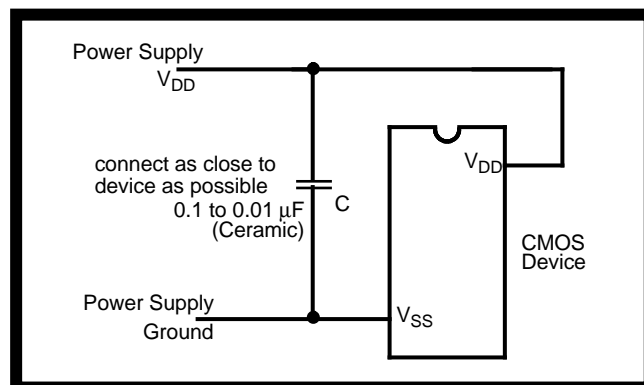


Fig. 13 - High Frequency Power Supply Decoupling

Problems Associated with Multi-Power Supply Voltages and Associated Decoupling Circuitry

In systems that have more than one independent power supply, care must be taken to ensure correct sequencing during power-up and power-down cycles. This is required to prevent input and output over-voltage conditions from developing. Consider, for example, a device powered from a +5V supply that has its outputs connected to a device powered from a +7V supply. Under steady state conditions, the output levels from the 5V devices would lie well within the supply voltage of the 7V device. However, if during power-up the 5V supply was to exceed the 7V supply, then the output voltage of the 5V device could exceed the instantaneous supply voltage of the 7V device (Fig. 14). This over-voltage could cause the 7V device to latch-up. A similar situation can occur between two devices powered by separate supplies of equal magnitude such as 5V regulated and 5V unregulated supplies. In this case there is the added concern when three-state outputs are tied together. These outputs are also subject to over-voltage triggering of latch-up. Such outputs present a high impedance only to signals lying within the power supply voltages. It must be stressed that

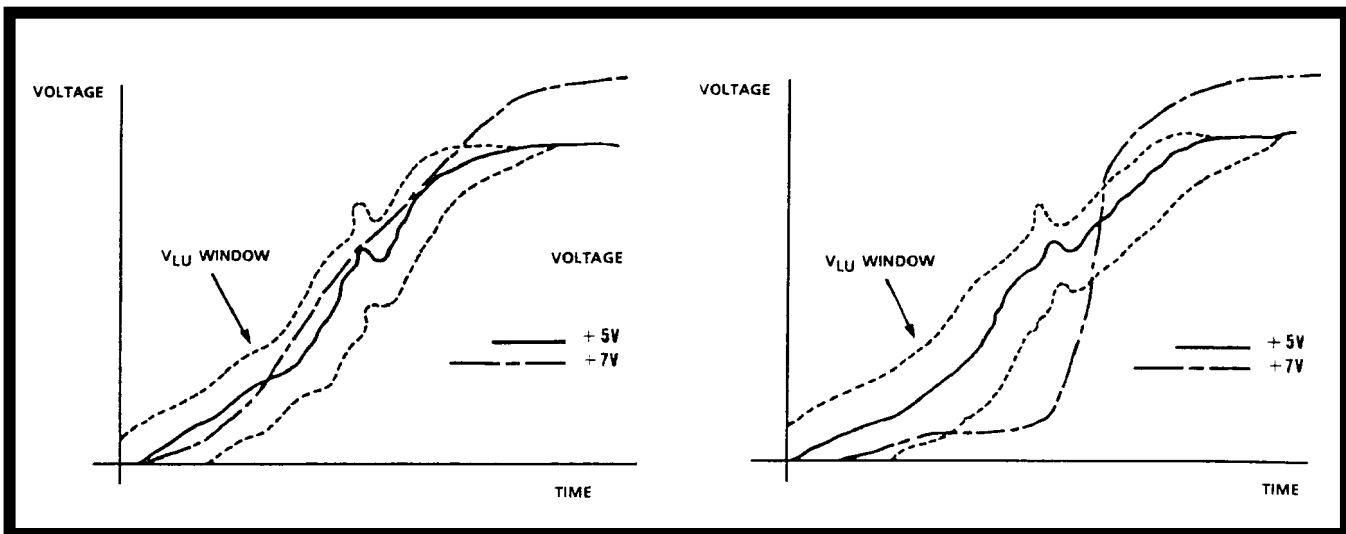


Figure 14 - Power Supply Sequencing

these over-voltage conditions need only exist for a very brief period of time to trigger latch-up. Thus, even transient over-voltages during power-up may pose a problem.

To ensure proper power supply sequencing, careful attention must be paid to the selection of decoupling components both at the initial design stage and when design revisions are done. This applies to both main power supply decoupling as well as local board decoupling. While proper sequencing may be evident at main distribution points, local sequencing can be altered by large capacitors on individual boards. Boards which have a large DC power requirement are likely to have such decoupling and hence, must be looked at carefully.

One way of ensuring that power supplies track when turning on or off is to connect a diode from the lower supply voltage to the higher one in the case of unequal supplies (Fig. 15). This will cause the supplies to track within one diode drop until they attain proper levels. In the case of two equal supplies, two diodes can be connected back to back, forcing supplies to track, independent of which supply comes up first.

Devices Driving Others on Separate PCBs

When integrated circuits in a system drive other devices on separate PCB's (via a backplane for example), then the considerations given in the previous two sections must be applied globally to the system. This was already mentioned in the section on plugging in PCB's "live". That is, when a PCB is plugged into a backplane with the system power applied, there is the danger that an input or output pin will contact an active line on the backplane

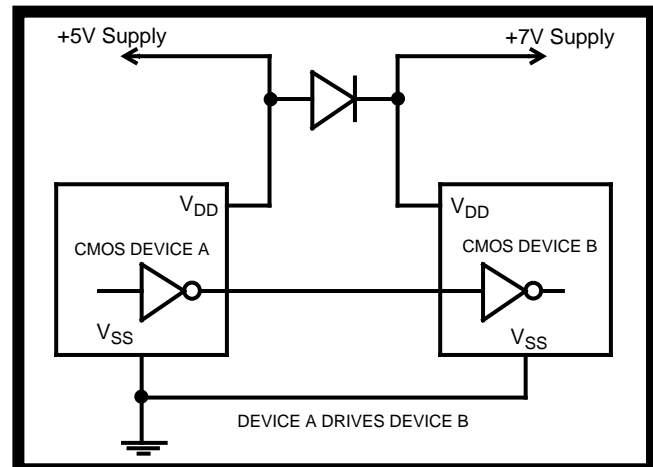


Fig. 15 - Forced Power Supply Tracking with Clamping Diode

before the power supply connection is made. The solution to this problem, as mentioned, lies in indenting the I/O edge terminations with respect to power supply terminals on the PCB.

Power supply sequencing should be given special attention in systems with devices that drive off-board. The same criteria applies here as was described for multi-supply systems. However, care must also be taken in single supply systems. In this case, large amounts of local decoupling can cause the supply voltages on some boards in the system to ramp up slower than on others. Devices on boards whose power supply ramps up quickly, can impress an over-voltage on devices on other boards. If this over-voltage is large enough, then latch-up may be triggered.

Whenever possible, local decoupling should be equalized on all boards within the system to minimize these effects. In systems where all off-board drivers are three-state devices, a simple

solution exists. All outputs should be kept in a high impedance state during power-up and power-down. Thus, no current will be available to trigger latch-up even if differential supply voltages develop from board to board. Alternatively, current limiting resistors can be connected in series with any inputs or outputs that may be subjected to over-voltages. These resistors are sized to limit current to less than 10mA:

$$R = \frac{(V_{\text{Diff}} - 0.3V)}{10\text{mA}}$$

where V_{Diff} = maximum instantaneous voltage differential between power supplies

The side effects of connecting these resistors are the same as mentioned previously for power supply over-voltage protection. There will be reductions in current drive from outputs, in speed, and in noise immunity on outputs driving DC loads through these resistors.

Devices Driving Long Address or Data Buses

Long address and data buses can exhibit quite large capacitances. Devices which drive such buses or have their inputs tied to one, can be subjected to over-voltage conditions. This is especially true if large DC current loads are switched on the same PCB (e.g. a group of LED's during a lamp test). Over-voltages can develop as follows. The change in the power supply current causes a localized voltage drop on the supply pins of the devices near to the device drawing the load current. This is a result of the finite resistance of the power supply tracks and contact resistance of any connectors. At

the same time, the bus capacitance tends to hold the voltage on the inputs and outputs connected to the bus at the full supply voltage. If a sufficient voltage differential develops between the bus and the local power supply, then the bus capacitance will discharge via the input and output structures. This current can attain a magnitude of tens of milliamps and hence trigger latch-up (Fig. 16).

Various precautions can be taken to reduce the chances of this problem occurring. Reducing the power supply resistance and bus capacitances can be done at the time of initial design. Wide power supply tracks and low contact resistance connectors should be used whenever possible. Buses should be kept as short as possible and have the largest possible spacings between the lines. If this problem still results due to system restraints on PCB layout, then the connection of a decoupling capacitor across the power supply pins of the devices latching-up should help (Fig. 17). The size of the capacitor depends upon the magnitude of the local current and the local resistance of the power supply. Normally a 10 μ F capacitor will clear up such problems and should not interfere with the local power supply sequencing on most PCB's.

There is one other way in which an input/output over-voltage can occur on long buses. There exists, on such buses, intertrack capacitance as well as capacitance to ground. When two adjacent tracks are at opposite logic levels (one at 5V, the other at ground), this capacitance charges to the full supply voltage. When the track initially at ground potential suddenly goes high, the signal is coupled through the capacitor to the other track. The voltage on this track increases from its initial value of 5V, impressing over-voltages on any devices connected to this track.

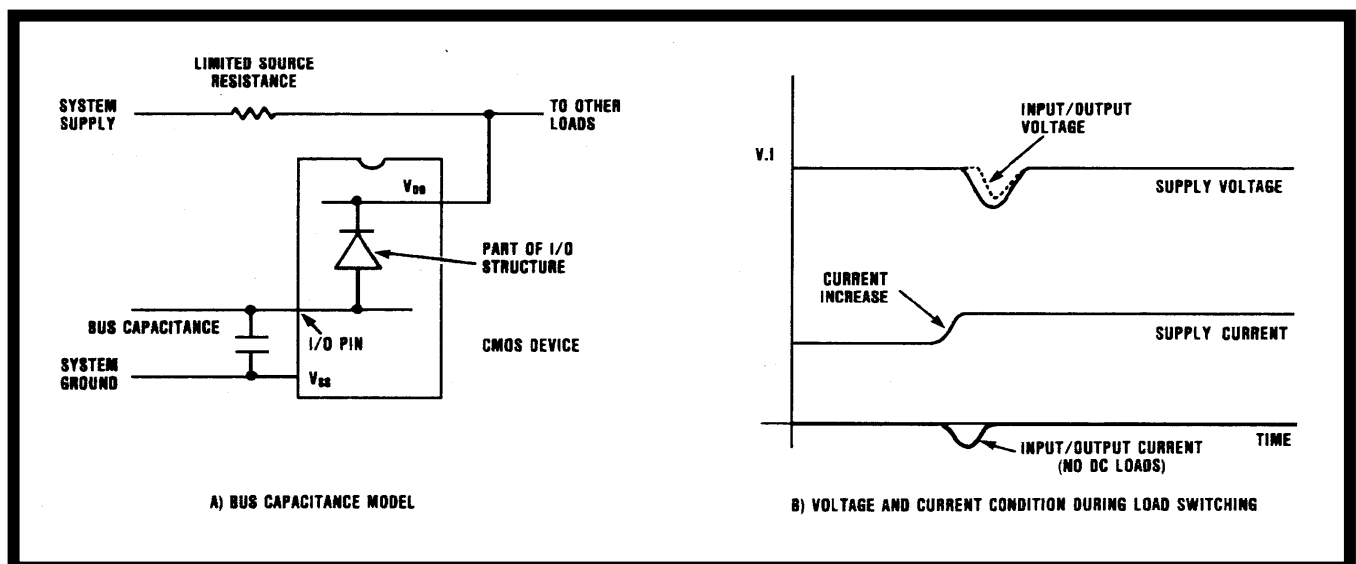


Figure 16 - Effects of Switching DC Loads Combined with Large Bus Capacitors

Minimizing intertrack capacitance by interleaving signal and ground tracks should be done wherever board space permits. Alternatively, external clamping diodes can be connected on tracks exhibiting these voltage excursions. The diodes may need be Schottky diodes if regular ones do not clamp soon enough to prevent current flow through

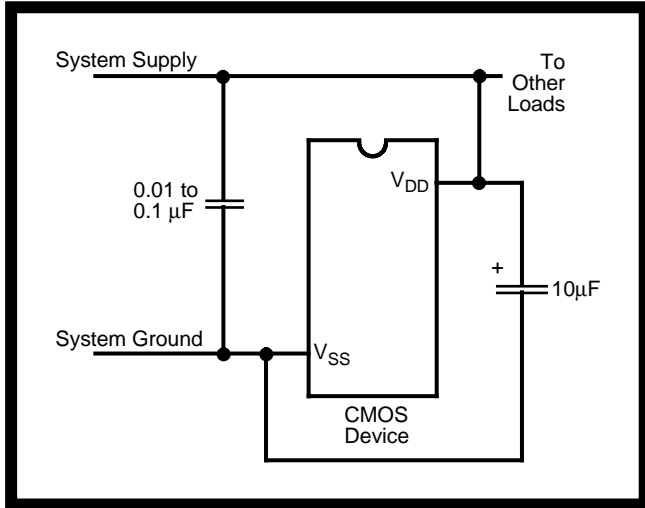


Fig. 17 - Local Decoupling to Offset Load Switching Effects

I/O structures. Regular silicon diodes may still be used if they are referenced to voltages inset by 0.7V from the supply rails. The clamping circuit shown in Fig. 18 should be quite effective, but as can be seen, this circuit will dissipate power. This may or may not be a problem depending on the overall system requirements. The decoupling capacitors help to absorb the high frequency energy. The resistor values shown are selected for a 5V supply and should be scaled for other supply voltages.

Ribbon Cables - A Special Case

A ribbon cable is a special case of long bus structure. The problems mentioned in the previous section also apply here. However, if the ribbon cable is of sufficient length, then its inductive properties become significant. The distributed inductance and capacitance form a second order circuit which can "ring" when driven by fast, digital signals. The result is the generation of damped oscillations centered about the positive and negative supply rails (Fig. 19). The positive and negative excursions outside of the supply rails impress over-voltages on inputs and outputs connected to the ribbon cable. If of sufficient amplitude, these over-voltages may trigger latch-up.

Solving the problem can be as simple as terminating each end of such cables with resistors to reduce the ringing voltages. However, these resistors will dissipate extra power. An alternative is to connect external protection diodes as shown in Fig. 20.

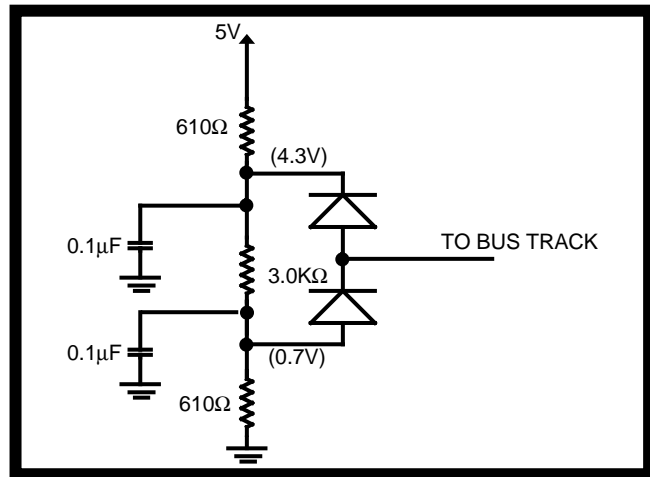


Fig. 18 - Clamping Circuit for Long Buses

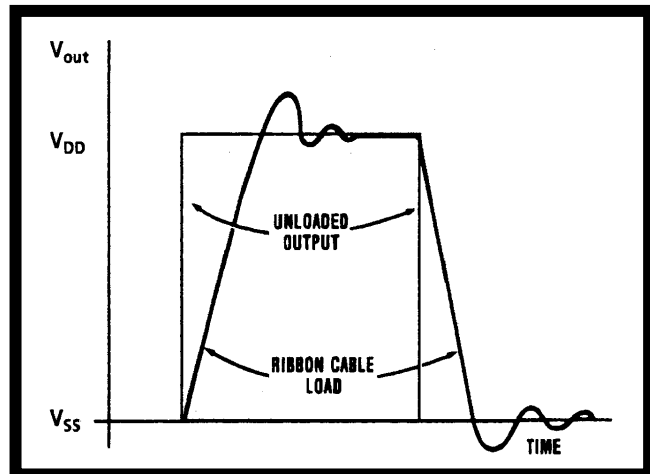


Fig. 19-Ringing Effect Due to Driving Ribbon Cable

These diodes will clamp any generated over-voltages. If the problem persists, it may be necessary to use Schottky diodes to ensure that the external diodes conduct before the input/output structures do.

Systems with End-User Accessible Inputs/Outputs

An extreme condition of input/output over-voltage can develop in systems which have end user accessible I/O ports. The user may apply signals to these ports when the system power supply is not turned on. Devices in the system connected to these ports are likely to latch-up when the power is turned on due to the current flowing through the I/O structures. Resistors can be connected in series with these I/O's to limit the current during these periods. As mentioned, these resistors will have direct effect on the speed and noise performance of these ports. Latch-up may also be triggered if the end user applies voltages to the I/O ports which exceed the system power supply voltages. The protection resistors suggested above may provide adequate protection against this hazard as well.

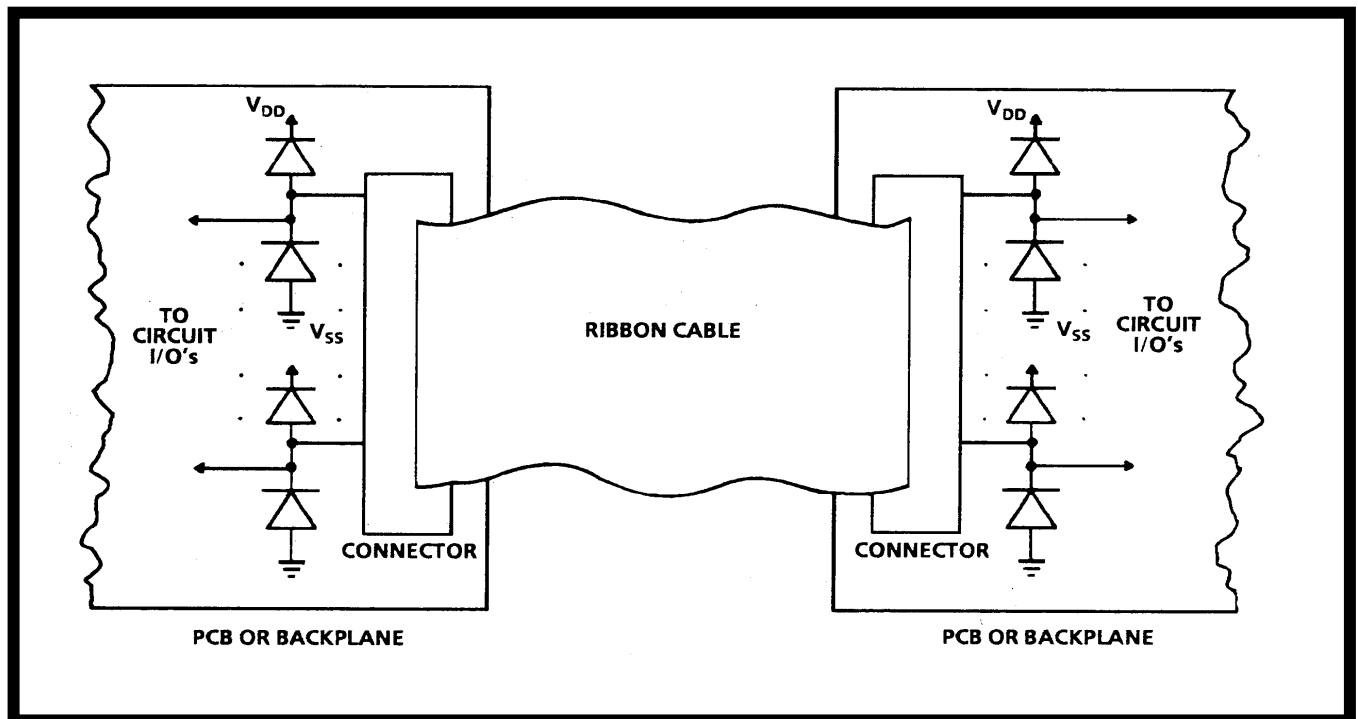


Figure 20 - External Clamping Diodes

However, performance constraints on the port may be such that the current-limiting resistors chosen are too small to protect against severe faults such as accidental connection of the AC mains supply. Protection against such faults can be provided by connection of external clamping diodes in the manner outlined for ribbon cables. Again, Schottky diodes may be required.

an over-voltage condition exists. Thus, no current will flow to trigger latch-up. The reference voltages are inset by 0.7V to allow the use of regular, low-cost diodes. Due to the potentially large currents flowing through the protection diodes, a clamping circuit similar to the one in Fig. 18 is not feasible. The output resistance in this case needs to be substantially lower.

If fault conditions are likely to be very severe, it may be necessary to reference external clamping diodes to voltages inset by 0.7V from the power supply (Fig. 21). These diodes will conduct before the input/output structures of the device on the port whenever

Digital and Analog Devices in Same System

In systems which have digital and analog devices powered by different supply voltages, there is the

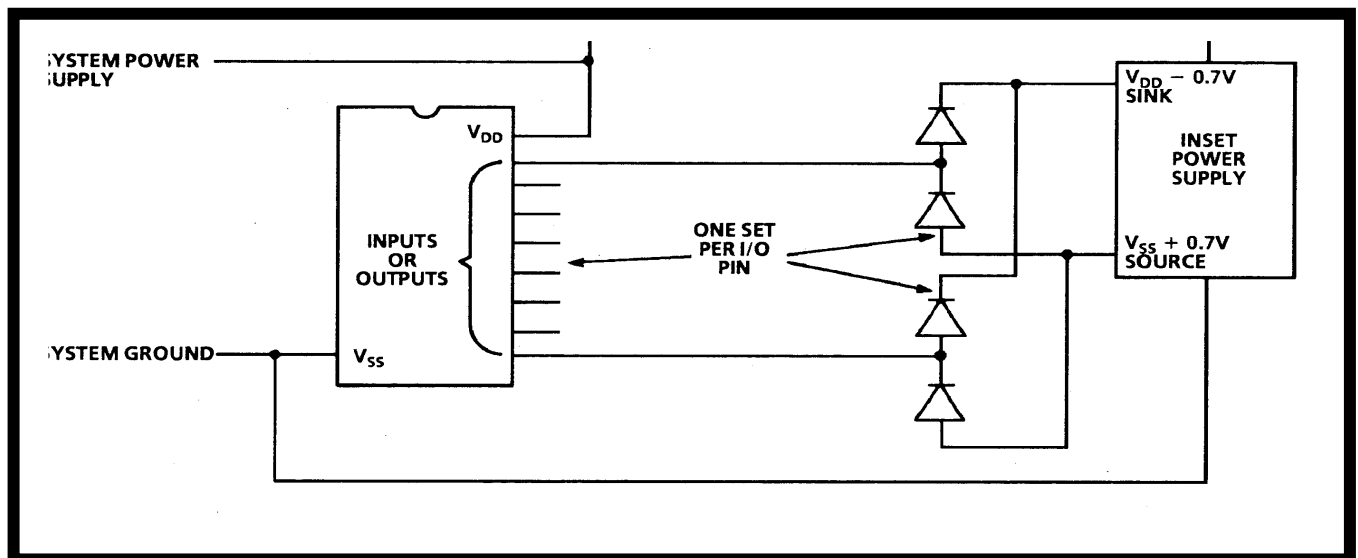


Figure 21 - Inset Supply Voltages for External Clamping

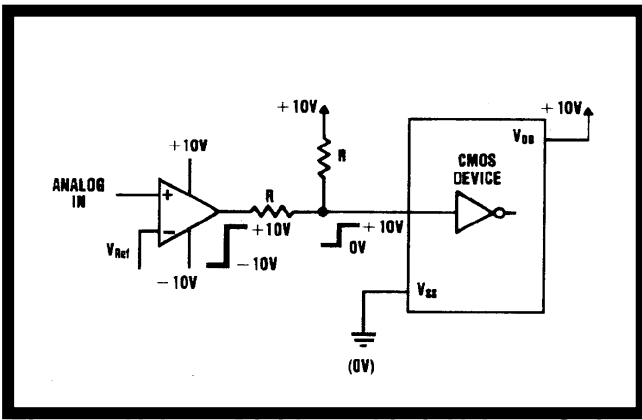


Fig. 22 - Voltage Divider to Limit Voltage Swing on CMOS Input

potential hazard of over-voltage conditions developing. Consider, for example, the case of an analog comparator powered from $\pm 10\text{V}$ driving a digital device powered from a $+10\text{V}$ supply. When the comparator output goes low, it will approach -10V and pull the digital input below V_{SS} (0V). If the comparator can pull enough current, then latch-up may be triggered. Putting a resistor in series with the input will limit the current and prevent latch-up. However, it is not a recommended procedure to use the input diodes as clamping circuits. A more advisable solution is to use a resistive divider as shown in Fig. 22. When the comparator output goes low, the divider will have 20V across it. Half of this voltage will be dropped across each resistor so that the digital input sits at 0V . When the comparator output goes high, no current flows through the divider so that the digital input sits at V_{DD} . Since the CMOS input has an extremely high input impedance, the value of these resistors can be very large ($>100\text{K}$) to minimize power consumption.

Conclusion

In the vast majority of circuits and systems employing CMOS devices, latch-up will not be a major concern. When simply applied according to manufacturers' recommendations, CMOS devices are not overly sensitive to the normal circuit conditions that exist within a system. What has been attempted in this application note is to develop an understanding of the latch-up phenomenon and its causes to assist designers in avoiding potential pitfalls caused by a simple lack of knowledge.

Having briefly reviewed the basic theory of SCR operation in general, and as it applies to CMOS input and output structures, an understanding of the mechanism of latch-up was developed. Taking a close look at various aspects of system and circuit design has revealed that various precautionary measures taken at the design stage can greatly

reduce the risk of latch-up occurrences. In cases where system performance or features create potentially hazardous situations beyond the designer's control, the implementation of simple protection circuitry will again minimize problems.

Through the use of careful design practices, augmented by protection circuitry when needed, the designer can use CMOS analog and digital integrated circuits extensively. System and circuit reliability will no longer be a function of latch-up related problems.

Reference

1. S.B. Dewan and A. Straughen, "Power Semiconductor Circuits", pp. 77-84, John Wiley and Sons, 1975.

Appendix

The following is a derivation of equation (1) of the main text. Fig. 2 is referenced for this purpose.

The collector and emitter currents of Q_1 and Q_2 are related by:

$$i_{C1} = \alpha_1 i_{E1} \quad i_{C2} = \alpha_2 i_{E2}$$

Looking at Fig. 2, it can be seen that the load current and the emitter currents of Q_1 and Q_2 are all equal. Also the load current is equal to the sums of the two collector currents and a leakage current from Q_2 's collector to its base (I_{CBO2}). Therefore:

$$\begin{aligned} I_L &= i_{C1} + i_{C2} + I_{CBO2} \\ &= \alpha_1 i_{E1} + \alpha_2 i_{E2} + I_{CBO2} \\ &= (\alpha_1 + \alpha_2) I_L + I_{CBO2} \\ &= \frac{I_{CBO2}}{1 - (\alpha_1 + \alpha_2)} \end{aligned}$$

The collector-emitter current gains (α_1, α_2) can be expressed in terms of the collector-base current gains (B_1, B_2) as:

$$\alpha_1 = \frac{B_1}{1 + B_1} \quad \alpha_2 = \frac{B_2}{1 + B_2}$$

Substituting these into the equation above yields:

$$\begin{aligned} I_L &= \frac{I_{CBO2}}{1 - \left(\frac{B_1}{1 + B_1} + \frac{B_2}{1 + B_2} \right)} \\ I_L &= I_{CBO2} \left[\frac{(1 + B_1)(1 + B_2)}{1 - B_1 B_2} \right] \end{aligned}$$



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