Technical Data
Advance Information

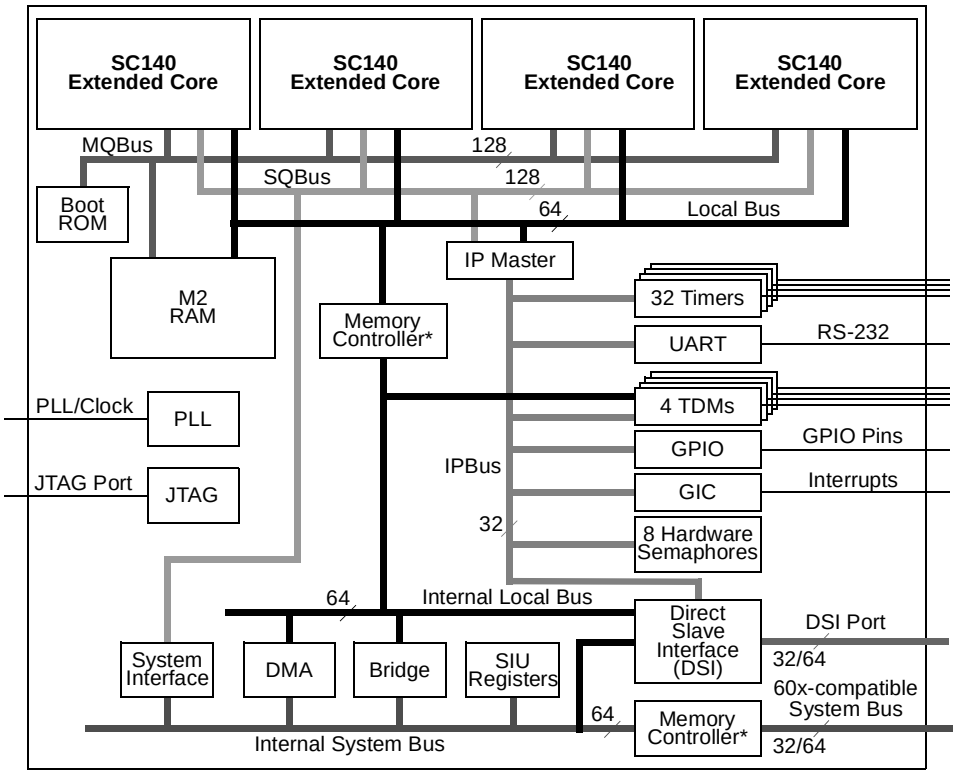
MSC8102/D
Rev. 2, 4/2003

Quad Core 16-Bit
Digital Signal Processor

MOTOROLA
intelligence everywhere™

digital dna™

The raw processing power of this highly integrated system-on-a-chip device enables developers to create next generation networking products that offer tremendous channel densities, while maintaining system flexibility, scalability, and upgradeability. The MSC8102 is offered in two core speed levels: 250 and 275 MHz.



*There is a single memory controller that controls access to both the local bus and the system bus.

Figure 1. MSC8102 Block Diagram

The MSC8102 is a highly integrated system-on-a-chip that combines four StarCore SC140 extended cores with an RS-232 serial interface, four time-division multiplexed (TDM) serial interfaces, thirty-two general-purpose timers, a flexible system interface unit (SIU), and a multi-channel DMA engine. The four extended cores can deliver a total 4400 DSP MMACS performance at 275 MHz.

Each core has four arithmetic logic units (ALUs), internal memory, a write buffer, and two interrupt controllers. The MSC8102 targets high-bandwidth highly computational DSP applications and is optimized for wireless transcoding and packet telephony as well as high-bandwidth base station applications. The MSC8102 delivers enhanced performance while maintaining low power dissipation and greatly reduces system cost.

Note: This document contains information on a new product. Specifications and information herein are subject to change without notice.

Table of Contents

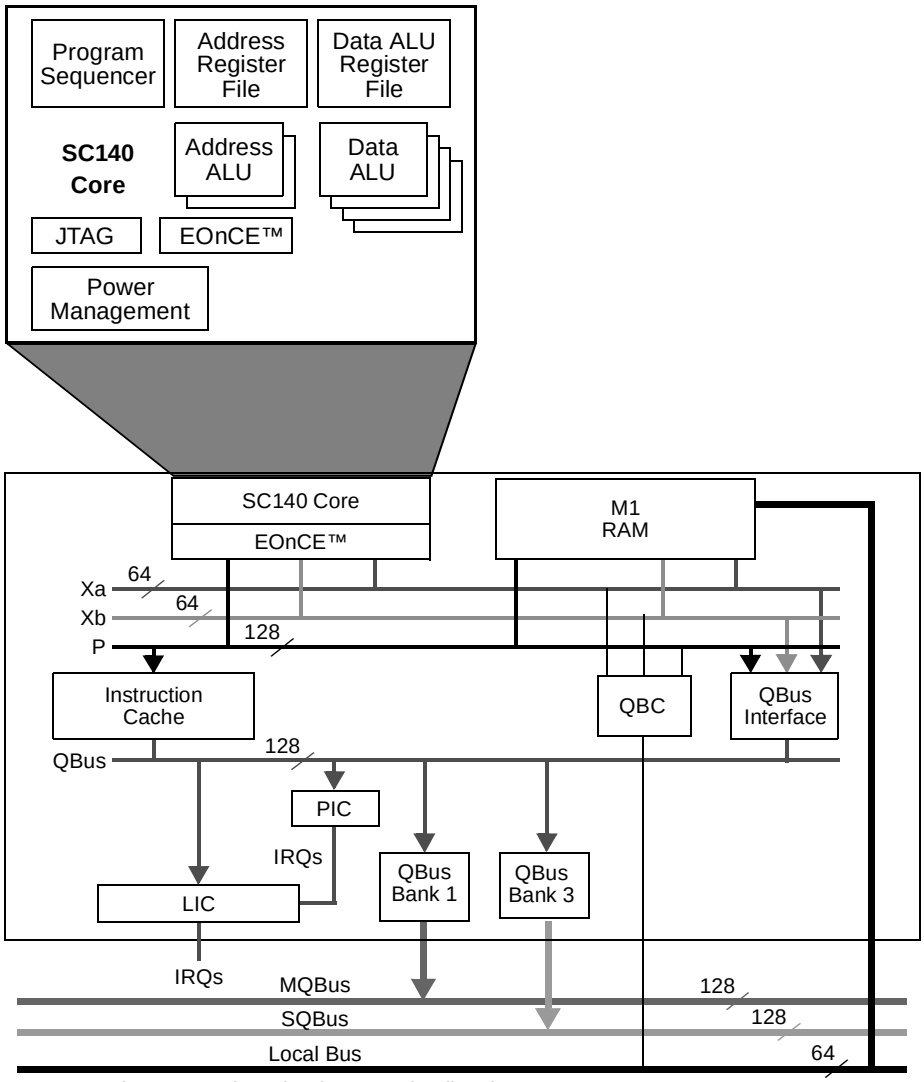
Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.



Notes: 1. The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. SC140 Extended Core Block Diagram

Features

- Four high-performance StarCore SC140 Digital Signal Processor (DSP) extended cores delivering up to 4400 MMACS using 16 ALUs running at up to 275 MHz, delivering a performance equivalent to a single SC140 core running at 1.1 GHz
- Each extended core includes:
  - SC140 core processor.
  - Local 224 KB memory space (M1) accessed by the SC140 core with no wait states and atomic access.
  - 16 KB, 16-way instruction cache (ICache).
  - Programmable interrupt controller (PIC).
  - Local interrupt controller (LIC).
- Each SC140 core provides the following:
  - Up to 1100 million multiply-accumulates per second (MMACS) using an internal 275 MHz clock at 1.6 V. A multiply-accumulate operation includes a multiply-add instruction with the associated data move and pointer update.
  - 4 ALUs per SC140 core.
  - 16 data registers, 40 bits each.
  - 27 address registers, 32 bits each.
  - Hardware support for fractional and integer data types.
  - Very rich 16-bit wide orthogonal instruction set.
  - Up to six instructions executed in a single clock cycle.
  - Variable-length execution set (VLES) that can be optimized for code density and performance.
  - IEEE 1149.1 JTAG port.
  - Enhanced on-device emulation (EOnCE) module with real-time debugging capabilities.
- Large internal memory spaces (1.440 MB total).
  - 224 KB of M1 memory per core (896 KB total).
  - 16 KB of ICache per core (64 KB total).
  - 476 KB shared memory (M2) operating at the core frequency, accessible from all four SC140 cores via the MQBus, and accessible from the local bus.
  - 4 KB boot ROM accessible from all four SC140 cores via the MQBus.
- Internal PLL for generating up to 275 MHz clock for the SC140 cores and up to 91.67 MHz for the 60x-compatible system bus, the local bus and other modules. PLL values are determined at reset based on configuration signal values.
- Very flexible System Interface Unit (SIU) with a memory controller to support a 32/64-bit wide 60x-compatible system bus to access memory and memory-mapped devices:
  - Reset controller.
  - Real-time clock register.
  - Periodic interrupt timer (PIT).
  - Hardware bus monitors for the 60x-compatible system bus and local bus.
  - Software watchdog timer function.
- Flexible eight-bank memory controller:
  - Three user-programmable machines (UPMs), general-purpose chip-select machine (GPCM), and a page-mode SDRAM machine.
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, FLASH and other user-definable peripherals.
  - Byte enables for either 64-bit or 32-bit bus width mode.
  - Eight external memory banks (banks 0–7). Two additional memory banks control IPBus peripherals and internal memories (banks 9, 11). Each bank has the following features:

    - 32-bit address decoding with programmable mask.
    - Variable block sizes (32 KB to 4 GB).
    - Selectable memory controller machine.
    - Two types of data errors check/correction (on 60x-compatible system bus only): Normal odd/even parity and Read-modify-write (RMW) odd/even parity for single accesses.
    - Write-protection capability.
    - Control signal generation machine selection on a per-bank basis.
    - Flexible chip-select assignment between the 60x-compatible system bus and local bus.
    - Support for internal or external masters on the 60x-compatible system bus.
    - Data buffer controls activated on a per-bank basis.
    - Atomic operation.
    - RMW data parity check (on 60x-compatible system bus only).
    - Extensive external memory-controller/bus-slave support.
    - Parity byte select signal, which enables a fast, glueless connection to RMW-parity devices (on 60x-compatible system bus only).
    - Data pipeline to reduce data set-up time for synchronous devices.
- Direct Slave Interface (DSI) that provides a 32/64-bit wide slave host interface. It is part of a dual-system bus architecture shared with the external system bus. The dual architecture allows the DSI data bus to be 32 or 64 bits wide and the system data bus to be 64 or 32 bits wide, respectively. It operates only as a slave device under the control of an external host processor.
- Multi-channel DMA controller:
  - 16 time-multiplexed unidirectional channels with infrastructure of 32 channels.
  - Services up to four external peripherals.
  - Supports $\overline{\text{DONE}}$ or $\overline{\text{DRACK}}$ protocol on two external peripherals.
  - Each channel group services 16 internal requests generated by eight internal FIFOs. Each FIFO generates:
    - a watermark request to indicate that the FIFO contains data for the DMA to empty and write to the destination
    - a hungry request to indicate that the FIFO can accept more data.
  - Priority-based time-multiplexing between channels using 16 internal priority levels
  - A flexible channel configuration:
    - All channels support all features.
    - All channels connect to the 60x-compatible system bus or local bus.
  - Flyby transfers in which a single data access is transferred directly from the source to the destination without using a DMA FIFO.
- External interfaces and control modules managed on the internal peripheral bus (IPBus) by an IP master device, including:
  - Four time-division multiplexing (TDM) modules, each supporting up to 64 channels (256 channels total)
  - RS-232 interface/universal asynchronous receiver/transmitter (UART)
  - Two 16-timer modules (32 timers total)
  - Eight hardware semaphore registers used by external hosts to control shared resources and ensure data coherency
  - Thirty-two general-purpose input/output (GPIO) signals
  - Global interrupt controller (GIC) to handle external interrupt functions (input and output)
- Up to four independent TDM modules, each with the following features:
  - Either totally independent receive and transmit, each having one data line, one clock line, and one frame sync line or four data lines, one clock and one frame sync that are shared between the transmit and receive.
  - Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses.

- Hardware A-law/μ-law conversion
- Up to 50 Mbps per TDM (50 MHz bit clock if one data line is used, 25 MHz if two data lines are used, 12.5 MHz if four data lines are used).
- Up to 256 channels.
- Up to 16 MB per channel buffer (granularity 8 bytes), where A/μ law buffer size is double (granularity 16 byte)
- Receive buffers share one global write offset pointer that is written to the same offset relative to their start address.
- Transmit buffers share one global read offset pointer that is read from the same offset relative to their start address.
- All channels share the same word size.
- Two programmable receive and two programmable transmit threshold levels with interrupt generation that can be used, for example, to implement double buffering.
- Each channel can be programmed to be active or inactive.
- 2-, 4-, 8-, or 16-bit channels are stored in the internal memory as 2-, 4-, 8-, or 16-bit channels, respectively.
- The TDM Transmitter Sync Signal (TxTSYN) can be configured as either input or output.
- Frame Sync and Data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock.
- Frame sync can be programmed as active low or active high.
- Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame.
- MSB or LSB first support.

• UART
- Two signals for transmit data and receive data.
- No clock, asynchronous mode.
- Can be serviced either by the SC140 DSP cores or an external host on the 60x-compatible system bus or on the DSI.
- Full-duplex operation.
- Standard mark/space non-return-to-zero (NRZ) format.
- 13-bit baud rate selection.
- Programmable 8-bit or 9-bit data format.
- Separately enabled transmitter and receiver.
- Programmable transmitter output polarity.
- Two receiver wakeup methods:
  - Idle line wakeup.
  - Address mark wakeup.
- Separate receiver and transmitter interrupt requests.
- Eight flags, the first five can generate interrupt request:
  - Transmitter empty.
  - Transmission complete.
  - Receiver full.
  - Idle receiver input.
  - Receiver overrun.
  - Noise error.
  - Framing error.
  - Parity error.
- Receiver framing error detection.
- Hardware parity checking.
- 1/16 bit-time noise detection.
- Maximum bit rate 6.25 Mbps.

  - Single-wire and loop operations.
- Timers
  - Two modules of 16 timers each.
  - Each timer has the following features:
    - Cyclic or one-shot.
    - Input clock polarity control.
    - Interrupt request when counting reaches a programmed threshold.
    - Pulse or level interrupts.
    - Dynamically updated programmed threshold.
    - Read counter any time.
  - Watchdog mode for the timers that connect to the device.
- Hardware semaphores. Eight coded hardware semaphores, locked by simple write access without need for read-modify-write mechanism.
- General-Purpose I/O (GPIO) port:
  - 32 bidirectional signal lines that either serve the peripherals or act as programmable I/O ports.
  - Each port can be programmed separately to serve up to two dedicated peripherals, and each port supports open-drain output mode.
- Global Interrupt Controller (GIC):
  - Consolidation of chip maskable interrupt and non-maskable interrupt sources and routing to $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and to the cores.
  - Generation of 32 virtual interrupts (eight to each SC140 core) by a simple write access.
  - Generation of virtual $\overline{\text{NMI}}$ (one to each SC140 core) by a simple write access.
- Software support, with support from industry-leading third parties:
  - Real-Time Operating Systems (RTOS):
    - Fully supports MSC8102 device architecture (multi-core, memory hierarchy, ICache, timers, DMA, interrupts, peripherals).
      - High-performance and deterministic, delivering predictive response time.
      - Optimized to provide low interrupt latency with high data throughput.
      - Preemptive and priority-based multitasking.
      - Fully interrupt/event driven.
      - Small memory footprint.
      - Comprehensive set of APIs.
      - Fully supports MSC8102 DMA, interrupts, and timer schemes.
    - Multi-core support:
      - Enables use of one instance of kernel code all four SC140 cores.
      - Dynamic and static memory allocation from local memory (M1) and shared memory (M2).
    - Distributed system support, enables transparent inter-task communications between tasks running inside the SC140 cores and the other tasks running on devices on the board or remote devices in the network
      - Messaging mechanism between tasks using mailboxes and semaphores.
      - Networking support; data transfer between tasks running inside and outside the device using networking protocols.
      - Includes integrated device drivers for such peripherals as TDM, UART, and external buses.
    - Additional features:
      - Incorporates task debugging utilities integrated with compilers and vendors.
      - Board support package (BSP) for MSC8102ADS.
  - Integrated Development Environment (IDE):

- C/C++ compiler with in-line assembly. Enables the developer to generate highly optimized DSP code. It translates code written in C/C++ into parallel fetch sets and maintains high code density.
- Librarian. Enables the user to create libraries for modularity.
- C libraries. A collection of C/C++ functions for the developer's use.
- Linker. Highly efficient linker to produce executables from object code.
- Debugger. Seamlessly integrated real-time, non-intrusive multi-mode debugger that enables debugging of highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode.
- Simulator. Device simulation models, enables design and simulation before the hardware arrival.
- Profiler. An analysis tool using a patented Binary Code Instrumentation (BCI) technique that enables the developer to identify program design inefficiencies.
- Version control. CodeWarrior® includes plug-ins for ClearCase, Visual SourceSafe, and CVS.

— Boot options:
- External memory.
- External host.
- UART.
- TDM.

• Power:
— Requires separate power supplies for on-chip logic (1.6 V) and I/O (3.3 V)
— Provides low-power standby modes
— Includes optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent).

• Packaging:
— 0.8 mm pitch High Temperature Coefficient for Expansion Flip Chip Ceramic Ball-Grid Array (FC-CBGA (HCTE)) or Flip Chip Plastic Ball-Grid Array (FC-PBGA) (pre-production only)
— 431-pin
— 20 mm × 20 mm

Product Documentation

The documents listed in **Table 1** are required for a complete description of the MSC8102 and are necessary to design properly with the part. Obtain documentation from a local Motorola distributor, semiconductor sales office, or a Motorola Literature Distribution Center. For documentation updates, visit the Motorola DSP website shown on the last page of this document.

Table 1. MSC8102 Documentation

Name	Description	Order Number
MSC8102 Technical Data	MSC8102 features list and physical, electrical, timing, and package specifications	MSC8102/D
MSC8102 User's Guide	User information include system functionality, getting started tutorial, and programming topics	MSC8102UG/D
MSC8102 Reference Manual	Detailed functional description of the MSC8102 memory and peripheral configuration, operation, and register programming	MSC8102RM/D
SC140 DSP Core Reference Manual	Detailed description of the SC140 family processor core and instruction set	MNSC140CORE/D
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the MSC8102 product website

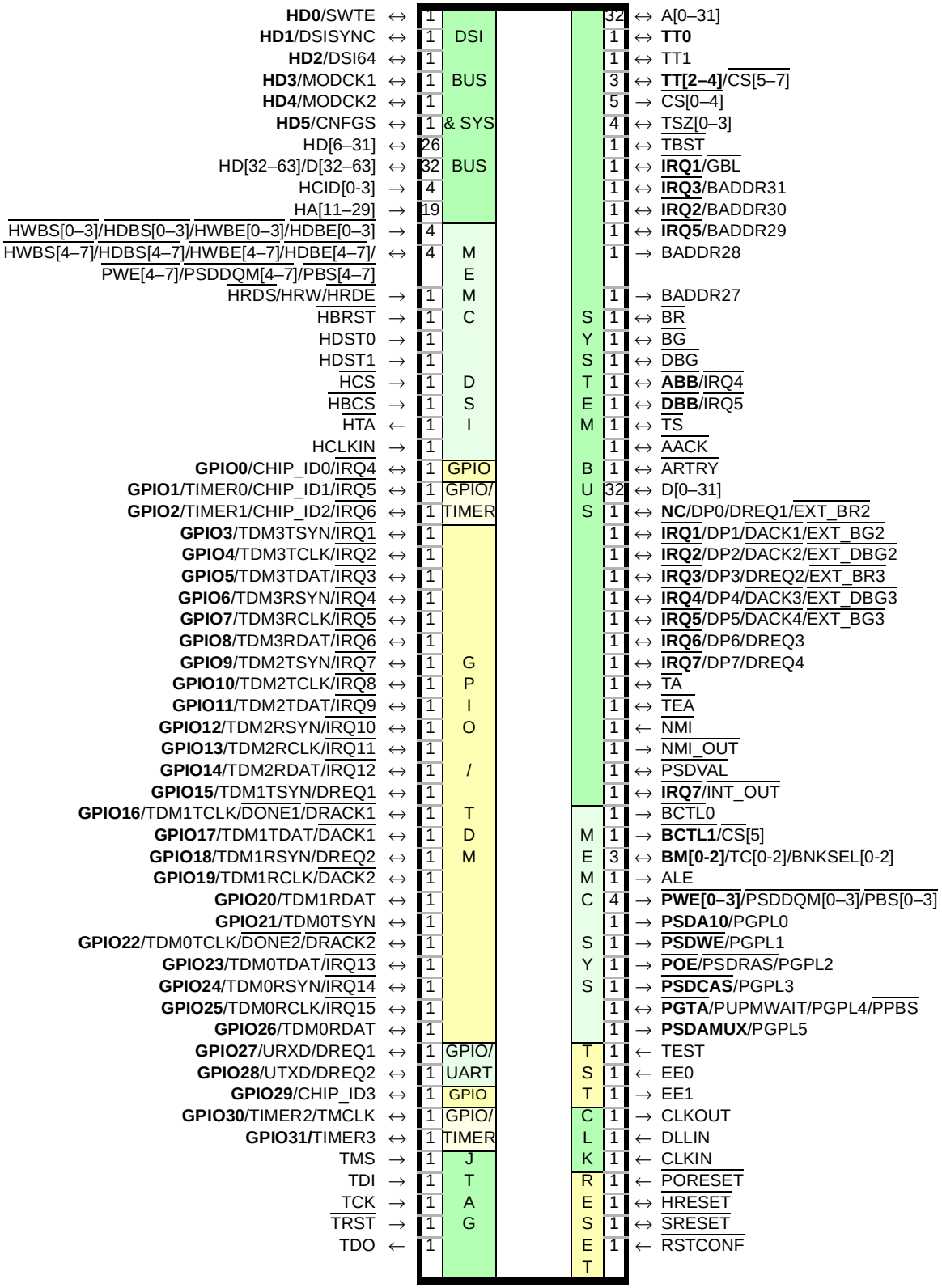
Chapter 1

Signal/ Connection Description

The MSC8102 external signals are organized into functional groups, as shown in **Table 1-1** and **Figure 1-1.**. **Table 1-1** lists the functional groups, the number of signal connections in each group, and references the table that gives a detailed listing of multiplexed signals within each group. **Figure 1-1.** shows MSC8102 external signals organized by function.

Table 1-1. MSC8102 Functional Signal Groupings

Functional Group	Number of Signal Connections	Detailed Description
Power (V_{DD}, V_{CC}, and GND)	158	**Table 1-2** on page 1-3
Clock	3	**Table 1-3** on page 1-3
Reset and Configuration	4	**Table 1-4** on page 1-4
DSI, System Bus, and Interrupts	210	**Table 1-5** on page 1-4
Memory Controller	16	**Table 1-6** on page 1-12
General-Purpose Input/Output (GPIO), Time-Division Multiplexed (TDM) Interface, Universal Asynchronous Receiver/ Transmitter (UART), and Timers	32	**Table 1-7** on page 1-14
EOnce and JTAG Test Access Port	7	**Table 1-8** on page 1-22
Reserved (denotes connections that are always reserved)	1	**Table 1-9** on page 1-22



Power signals include: V_{DD}, V_{DDH}, V_{CCSYN}, GND, and GND_{SYN}.

Figure 1-1. MSC8102 External Signals

1.1 Power Signals

Table 1-2. Power and Ground Signal Inputs

Signal Name	Description
V_{DD}	**Internal Logic Power** V_{DD} dedicated for use with the device core. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{DD} power rail.
V_{DDH}	**Input/Output Power** This source supplies power for the I/O buffers. The user must provide adequate external decoupling capacitors.
V_{CCSYN}	**System PLL Power** V_{CC} dedicated for use with the system Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
GND	**System Ground** An isolated ground for the internal processing logic and I/O buffers. This connection must be tied externally to all chip ground connections, except GND_{SYN}. The user must provide adequate external decoupling capacitors.
GND_{SYN}	**System PLL Ground** Ground dedicated for system PLL use. The connection should be provided with an extremely low-impedance path to ground.

1.2 Clock Signals

Table 1-3. Clock Signals

Signal Name	Type	Signal Description
CLKIN	Input	**Clock In** Primary clock input to the MSC8102 PLL.
CLKOUT	Output	**Clock Out** The bus clock.
DLLIN	Input	**DLLIN** Synchronizes with an external device.

1.3 Reset and Configuration Signals

Table 1-4. Reset and Configuration Signals

Signal Name	Type	Signal Description
$\overline{\text{PORESET}}$	Input	**Power-On Reset** When asserted, this line causes the MSC8102 to enter power-on reset state.
$\overline{\text{RSTCONF}}$	Input	**Reset Configuration**[1] Used during reset configuration sequence of the chip. A detailed explanation of its function is provided in the *MSC8102 Reference Manual*. This signal is sampled upon deassertion of $\overline{\text{PORESET}}$.
$\overline{\text{HRESET}}$	Input	**Hard Reset** When asserted, this open-drain line causes the MSC8102 to enter hard reset state.
$\overline{\text{SRESET}}$	Input	**Soft Reset** When asserted, this open-drain line causes the MSC8102 to enter soft reset state.

Note: When $\overline{\text{PORESET}}$ is deasserted, the MSC8102 also samples the following signals:
- BM[0–2]—Selects the boot mode.
- MODCK[1–2]—Selects the clock configuration.
- SWTE—Enables the software watchdog timer.
- DSISYNC, DSI64, CNFGS, and CHIP_ID[0–3]—Configures the DSI.

Refer to **Table 1-5** for details on these signals.

1.4 Direct Slave Interface, System Bus, and Interrupt Signals

The direct slave interface (DSI) is combined with the system bus because they share some common signal lines. Individual assignment of a signal to a specific signal line is configured through internal registers. **Table 1-5** describes the signals in this group.

Note: Although there are fifteen interrupt request (IRQ) connections to the core processors, there are multiple external lines that can connect to these internal signal lines. After reset, the default configuration enables only $\overline{\text{IRQ}}$[1–7], but includes two input lines each for $\overline{\text{IRQ}}$[1–3] and $\overline{\text{IRQ7}}$. The designer must select one line for each required interrupt and reconfigure the other external signal line or lines for alternate functions. Additional alternate IRQ lines and $\overline{\text{IRQ}}$[8–15] are enabled through the GPIO signal lines.

Table 1-5. DSI, System Bus, and Interrupt Signals

Signal Name	Type	Description
HD0	Input/ Output	**Host Data Bus 0** Bit 0 of the DSI data bus.
SWTE	Input	**Software Watchdog Timer Disable**. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD1	Input/ Output	**Host Data Bus 1** Bit 1 of the DSI data bus.
DSISYNC	Input	**DSI Synchronous** Distinguishes between synchronous and asynchronous operation of the DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
HD2	Input/ Output	**Host Data Bus 2** Bit 2 of the DSI data bus.
DSI64	Input	**DSI 64** Defines the width of the DSI and SYSTEM Data buses. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD3	Input/ Output	**Host Data Bus 3** Bit 3 of the DSI data bus.
MODCK1	Input	**Clock Mode 1** Defines the clock frequencies. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD4	Input/ Output	**Host Data Bus 4** Bit 4 of the DSI data bus.
MODCK2	Input	**Clock Mode 2** Defines the clock frequencies. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD5	Input/ Output	**Host Data Bus 5** Bit 5 of the DSI data bus.
CNFGS	Input	**Configuration Source** One signal out of two that indicates reset configuration mode. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD[6–31]	Input/O utput	**Host Data Bus 6–31** Bits 6–31 of the DSI data bus.
HD[32–63]	Input/O utput	**Host Data Bus 32–63** Bits 32–63 of the DSI data bus.
D[32–63]	Input/O utput	**System Bus Data 32–63** In write transactions, the bus master drives the valid data on this bus. In read transactions, the slave drives the valid data on this bus.
HCID[0–3]	Input	**Host Chip ID 0–3** Carries the chip ID of the DSI. The DSI is accessed only if $\overline{\text{HCS}}$ is asserted and HCID[0–3] matches the Chip_ID, or if $\overline{\text{HBCS}}$ is asserted.
HA[11–29]	Input	**Host Bus Address 11–29** Used by external host to access the internal address space.
$\overline{\text{HWBS[0–3]}}$	Input	**Host Write Byte Strobes** (In Asynchronous dual mode) One bit per byte is used as a strobe for host write accesses.
$\overline{\text{HDBS[0–3]}}$	Input	**Host Data Byte Strobe** (in Asynchronous single mode) One bit per byte is used as a strobe for host read or write accesses
$\overline{\text{HWBE[0–3]}}$	Input	**Host Write Byte Enable** (In Synchronous dual mode) One bit per byte is used to indicate a valid data byte for host read or write accesses.
$\overline{\text{HDBE[0–3]}}$	Input	**Host Data Byte Enable** (in Synchronous single mode) One bit per byte is used as a strobe enable for host write accesses

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{HWBS}}$[4–7]	Input	**Host Write Byte Strobes** (In Asynchronous dual mode) One bit per byte is used as a strobe for host write accesses.
$\overline{\text{HDBS}}$[4–7]	Input	**Host Data Byte Strobe** (in Asynchronous single mode) One bit per byte is used as a strobe for host read or write accesses
$\overline{\text{HWBE}}$[4–7]	Input	**Host Write Byte Enable** (In Synchronous dual mode) One bit per byte is used to indicate a valid data byte for host write accesses.
$\overline{\text{HDBE}}$[4–7]	Input	**Host Data Byte Enable** (in Synchronous single mode) One bit per byte is used as a strobe enable for host read or write accesses
$\overline{\text{PWE}}$[4–7]	Output	**System Bus Write Enable** Outputs of the bus general-purpose chip-select machine (GPCM). These pins select byte lanes for write operations.
$\overline{\text{PSDDQM}}$[4–7]	Output	**System Bus SDRAM DQM** From the SDRAM control machine. These pins select specific byte lanes of SDRAM devices.
$\overline{\text{PBS}}$[4–7]	Output	**System Bus UPM Byte Select** From the UPM in the memory controller, these signals select specific byte lanes during memory operations. The timing of these pins is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.
$\overline{\text{HRDS}}$	Input	**Host Read Data Strobe** (In Asynchronous dual mode) Used as a strobe for host read accesses.
HRW	Input	**Host Read/Write Select** (in Asynchronous/Synchronous single mode) Host read/write select.
$\overline{\text{HRDE}}$	Input	**Host Read Data Enable** (In Synchronous dual mode) Indicates valid data for host read accesses.
$\overline{\text{HBRST}}$	Input	**Host Burst** The host asserts this pin to indicate that the current transaction is a burst transaction in synchronous mode only.
HDST0	Input	**Host Data structure 0** Defines the data structure of the host access in DSI little-endian mode.
HDST1	Input	**Host Data structure 1** Defines the data structure of the host access in DSI little-endian mode.
$\overline{\text{HCS}}$	Input	**Host Chip Select** DSI chip select. The DSI is accessed only if $\overline{\text{HCS}}$ is asserted and HCID[0–3] matches the Chip_ID.
$\overline{\text{HBCS}}$	Input	**Host Broadcast Chip Select** DSI chip select for broadcast mode. Enables more than one DSI to share the same host chip-select pin for broadcast write accesses.
$\overline{\text{HTA}}$	Output	**Host Transfer Acknowledge** Upon a read access, indicates to the host when the data on the data bus is valid. Upon a write access, indicates to the host that the data on the data bus was written to the DSI write buffer.
HCLKIN	Input	**Host Clock Input** Host clock signal for DSI synchronous mode.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
A[0–31]	Input/ Output	**Address Bus** When the MSC8102 is in external master bus mode, these pins function as the system address bus. The MSC8102 drives the address of its internal bus masters and responds to addresses generated by external bus masters. When the MSC8102 is in internal master bus mode, these pins are used as address lines connected to memory devices and are controlled by the MSC8102 memory controller.
TT0	Input/ Output	**Bus Transfer Type 0** The bus master drives this pins during the address tenure to specify the type of the transaction.
TT1	Input/ Output	**Bus Transfer Type 1** The bus master drives this pins during the address tenure to specify the type of the transaction. Some applications use only the TT1 signal, for example, from MSC8102 to MSC8102 or MSC8102 to MSC8101 and *vice versa*. In these applications, TT1 functions as read/write signal.
TT[2–4]	Input/ Output	**Bus Transfer Type 2–4** The bus master drives these pins during the address tenure to specify the type of the transaction.
$\overline{\text{CS}}$[5–7]	Output	**Chip Select 5–7** Enables specific memory devices or peripherals connected to the system bus.
$\overline{\text{CS}}$[0–4]	Output	**Chip Select 0–4** Enables specific memory devices or peripherals connected to the system bus.
TSZ[0–3]	Input/ Output	**Transfer Size 0–3** The bus master drives these pins with a value indicating the number of bytes transferred in the current transaction.
$\overline{\text{TBST}}$	Input/ Output	**Bus Transfer Burst** The bus master asserts this pin to indicate that the current transaction is a burst transaction (transfers eight words).
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{GBL}}$	Output	**Global**[1] When a master within the MSC8102 initiates a bus transaction, it drives this pin. Assertion of this pin indicates that the transfer is global and should be snooped by caches in the system.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
BADDR31	Output	**Burst Address 31**[1] There are five burst address output pins, which are outputs of the memory controller. These pins connect directly to burstable memory devices without internal address incrementors controlled by the MSC8102 memory controller.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
BADDR30	Output	**Burst Address 30**[1] There are five burst address output pins, which are outputs of the memory controller. These pins connect directly to burstable memory devices without internal address incrementors controlled by the MSC8102 memory controller.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
BADDR29	Output	**Bus Burst Address 29**[1] There are five burst address output pins, which are outputs of the memory controller. These pins connect directly to burstable memory devices without internal address incrementors controlled by the MSC8102 memory controller.
BADDR28	Output	**Burst Address 28** There are five burst address output pins, which are outputs of the memory controller. These pins connect directly to burstable memory devices without internal address incrementors controlled by the MSC8102 memory controller.
BADDR27	Output	**Burst Address 27** There are five burst address output pins, which are outputs of the memory controller. These pins connect directly to burstable memory devices without internal address incrementors controlled by the MSC8102 memory controller.
$\overline{\text{BR}}$	Input/ Output	**Bus Request**[2] When an external arbiter is used, the MSC8102 asserts this pin as an output to request ownership of the bus. When the MSC8102 controller is used as an internal arbiter, an external master asserts this pin as an input to request bus ownership.
$\overline{\text{BG}}$	Input/ Output	**Bus Grant**[2] When the MSC8102 acts as an internal arbiter, it asserts this pin as an output to grant bus ownership to an external bus master. When an external arbiter is used, it asserts this pin as an input to grant bus ownership to the MSC8102.
$\overline{\text{DBG}}$	Input/ Output	**Data Bus Grant**[2] When the MSC8102 acts as an internal arbiter, it asserts this pin as an output to grant data bus ownership to an external bus master. When an external arbiter is used, it asserts this pin as an input to grant data bus ownership to the MSC8102.
$\overline{\text{ABB}}$	Input/ Output	**Address Bus Busy**[1] The MSC8102 asserts this pin as an output for the duration of the address bus tenure. Following an $\overline{\text{AACK}}$, which terminates the address bus tenure, the MSC8102 deasserts $\overline{\text{ABB}}$ for a fraction of a bus cycle and then stops driving this pin. The MSC8102 does not assume bus ownership as long as it senses this pin is asserted as an input by an external bus master.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{DBB}}$	Input/ Output	**Data Bus Busy**[1] The MSC8102 asserts this pin as an output for the duration of the data bus tenure. Following a $\overline{\text{TA}}$, which terminates the data bus tenure, the MSC8102 deasserts $\overline{\text{DBB}}$ for a fraction of a bus cycle and then stops driving this pin. The MSC8102 does not assume data bus ownership as long as it senses that this pin is asserted as an input by an external bus master.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{TS}}$	Input/ Output	**Bus Transfer Start** Assertion of this pin signals the beginning of a new address bus tenure. The MSC8102 asserts this signal when one of its internal bus masters begins an address tenure. When the MSC8102 senses that this pin is asserted by an external bus master, it responds to the address bus tenure as required (snoop if enabled, access internal MSC8102 resources, memory controller support).
$\overline{\text{AACK}}$	Input/ Output	**Address Acknowledge** A bus slave asserts this signal to indicate that it has identified the address tenure. Assertion of this signal terminates the address tenure.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{ARTRY}}$	Input/ Output	**Address Retry** Assertion of this signal indicates that the bus master should retry the bus transaction. An external master asserts this signal to enforce data coherency with its caches and to prevent deadlock situations.
D[0–31]	Input/ Output	**Data Bus Bits 0–31** In write transactions, the bus master drives the valid data on this bus. In read transactions, the slave drives the valid data on this bus.
Reserved	Input	The primary configuration selection (default after reset) is reserved.
DP0	Input/ Output	**System Bus Data Parity 0** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 0 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 0 and D[0–7].
DREQ1	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
$\overline{\text{EXT\_BR2}}$	Input	**External Bus Request 2** An external master asserts this pin to request bus ownership from the internal arbiter.
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP1	Input/ Output	**System Bus Data Parity** 1 The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 1 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 1 and D[8–15].
$\overline{\text{DACK1}}$	Output	**DMA Acknowledge 1** The DMA drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{EXT\_BG2}}$	Output	**External Bus Grant 2**[2] The MSC8102 asserts this pin to grant bus ownership to an external bus master.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP2	Input/ Output	**System Bus Data Parity 2** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 2 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 2 and D[16–23].
$\overline{\text{DACK2}}$	Output	**DMA Acknowledge 2** The DMA drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{EXT\_DBG2}}$	Output	**External Data Bus Grant 2**[2] The MSC8102 asserts this pin to grant data bus ownership to an external bus master.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP3	Input/ Output	**System Bus Data Parity 3** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 3 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 3 and D[24–31].
DREQ2	Input	**DMA Request 2** Used by an external peripheral to request DMA service.
$\overline{\text{EXT\_BR3}}$	Input	**External Bus Request 3**[2] An external master should assert this pin to request bus ownership from the internal arbiter.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP4	Input/ Output	**System Bus Data Parity 4** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 4 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 4 and D[32–39].
$\overline{\text{DACK3}}$	Output	**DMA Acknowledge 3** The DMA drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{EXT\_DBG3}}$	Output	**External Data Bus Grant 3**[2] The MSC8102 asserts this pin to grant data bus ownership to an external bus master.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP5	Input/ Output	**System Bus Data Parity 5** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 5 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 5 and D[40–47].
$\overline{\text{DACK4}}$	Output	**DMA Acknowledge 4** The DMA drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{EXT\_BG3}}$	Output	**External Bus Grant 3**[2] The MSC8102 asserts this pin to grant bus ownership to an external bus.
$\overline{\text{IRQ6}}$	Input	**Interrupt Request 6** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP6	Input/ Output	**System Bus Data Parity 6** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 6 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 6 and D[48–55].
DREQ3	Input	**DMA Request 3** Used by an external peripheral to request DMA service.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP7	Input/ Output	**System Bus Data Parity 7** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 7 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 7 and D[56–63].
DREQ4	Input	**DMA Request 4** Used by an external peripheral to request DMA service.
$\overline{\text{TA}}$	Input/ Output	**Transfer Acknowledge** Indicates that a data beat is valid on the data bus. For single-beat transfers, $\overline{\text{TA}}$ assertion indicates the termination of the transfer. For burst transfers, $\overline{\text{TA}}$ is asserted eight times to indicate the transfer of eight data beats, with the last assertion indicating the termination of the burst transfer.
$\overline{\text{TEA}}$	Input/ Output	**Transfer Error Acknowledge** Assertion indicates a failure of the data tenure transaction.The masters within the MSC8102 monitor the state of this pin. The MSC8102 internal bus monitor can assert this pin if it identifies a bus transfer that does not complete.
$\overline{\text{NMI}}$	Input	**Non-Maskable Interrupt** When an external device asserts this line, it generates an non-maskable interrupt in the MSC8102, which is processed internally (default) or is directed to an external host for processing (see $\overline{\text{NMI\_OUT}}$).
$\overline{\text{NMI\_OUT}}$	Output	**Non-Maskable Interrupt Output** An open-drain pin driven from the MSC8102 internal interrupt controller. Assertion of this output indicates that a non-maskable interrupt is pending in the MSC8102 internal interrupt controller, waiting to be handled by an external host.
$\overline{\text{PSDVAL}}$	Input/ Output	**Port Size Data Valid** Indicates that a data beat is valid on the data bus. The difference between the $\overline{\text{TA}}$ pin and the $\overline{\text{PSDVAL}}$ pin is that the $\overline{\text{TA}}$ pin is asserted to indicate data transfer terminations, while the $\overline{\text{PSDVAL}}$ signal is asserted with each data beat movement. When $\overline{\text{TA}}$ is asserted, $\overline{\text{PSDVAL}}$ is always asserted. However, when $\overline{\text{PSDVAL}}$ is asserted, $\overline{\text{TA}}$ is not necessarily asserted. For example, if the DMA initiates a double word (2×64 bits) transaction to a memory device with a 32-bit port size, $\overline{\text{PSDVAL}}$ is asserted three times without $\overline{\text{TA}}$ and, finally, both pins are asserted to terminate the transfer.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{INT\_OUT}}$	Output	**Interrupt Output** Assertion of this output indicates that an unmasked interrupt is pending in the MSC8102 internal interrupt controller.

Notes:
1. See the *System Interface Unit (SIU)* chapter in the *MSC8102 Reference Manual* for details on how to configure these pins.
2. When used as the bus control arbiter, the MSC8102 can support up to three external bus masters. Each master uses its own set of Bus Request, Bus Grant, and Data Bus Grant signals ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$, $\overline{\text{EXT\_BR2}}$/$\overline{\text{EXT\_BG2}}$/$\overline{\text{EXT\_DBG2}}$, and $\overline{\text{EXT\_BR3}}$/$\overline{\text{EXT\_BG3}}$/$\overline{\text{EXT\_DBG3}}$). Each of these signal sets must be configured to indicate whether the external master is or is not a MSC8102 master device. See the Bus Configuration Register (BCR) description in the *System Interface Unit (SIU)* chapter in the *MSC8102 Reference Manual* for details on how to configure these pins. The second and third set of pins is defined by EXT_xxx to indicate that they can only be used with external master devices. The first set of pins ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$) have a dual function. When the MSC8102 is not the bus arbiter, these signals ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$) are used by the MSC8102 to obtain master control of the bus.

1.5 Memory Controller Signals

Refer to the *Memory Controller* chapter in the *MSC8102 Reference Manual* for detailed information about configuring these signals.

Table 1-6. Memory Controller Signals

Signal Name	Type	Description
$\overline{\text{BCTL0}}$	Output	**System Bus Buffer Control 0** Controls buffers on the data bus. Usually used with $\overline{\text{BCTL1}}$. The exact function of this pin is defined by the value of SIUMCR[BCTLC].
$\overline{\text{BCTL1}}$	Output	**System Bus Buffer Control 1** Controls buffers on the data bus. Usually used with $\overline{\text{BCTL0}}$. The exact function of this pin is defined by the value of SIUMCR[BCTLC].
$\overline{\text{CS5}}$	Output	**System and Local Bus Chip Select 5** Enables specific memory devices or peripherals connected to MSC8102 buses.
BM[0–2]	Input	**Boot Mode 0–2** Defines the boot mode of the MSC8102. This signal is sampled on $\overline{\text{PORESET}}$ deassertion.
TC[0–2]	Input/ Output	**Transfer Code 0–2** The bus master drives these pins during the address tenure to specify the type of the code.
BNKSEL[0–2]	Output	**Bank Select 0–2** Selects the SDRAM bank when the MSC8102 is in 60x-compatible bus mode.
ALE	Output	**Address Latch Enable** Controls the external address latch used in an external master bus.
$\overline{\text{PWE[0–3]}}$	Output	**System Bus Write Enable** Outputs of the bus general-purpose chip-select machine (GPCM). These pins select byte lanes for write operations.
$\overline{\text{PSDDQM[0–3]}}$	Output	**System Bus SDRAM DQM** From the SDRAM control machine. These pins select specific byte lanes of SDRAM devices.
$\overline{\text{PBS[0–3]}}$	Output	**System Bus UPM Byte Select** From the UPM in the memory controller, these signals select specific byte lanes during memory operations. The timing of these pins is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.
PSDA10	Output	**System Bus SDRAM A10** From the bus SDRAM controller. The precharge command defines which bank is precharged. When the row address is driven, it is a part of the row address. When column address is driven, it is a part of column address.
PGPL0	Output	**System Bus UPM General-Purpose Line 0** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PSDWE}}$	Output	**System Bus SDRAM Write Enable** From the bus SDRAM controller. Should connect to SDRAM WE input.
PGPL1	Output	**System Bus UPM General-Purpose Line 1** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.

Table 1-6. Memory Controller Signals (Continued)

Signal Name	Type	Description
$\overline{\text{POE}}$	Output	**System Bus Output Enable** From the bus GPCM. Controls the output buffer of memory devices during read operations.
$\overline{\text{PSDRAS}}$	Output	**System Bus SDRAM $\overline{\text{RAS}}$** From the bus SDRAM controller. Should connect to SDRAM $\overline{\text{RAS}}$ input.
PGPL2	Output	**System Bus UPM General-Purpose Line 2** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PSDCAS}}$	Output	**System Bus SDRAM $\overline{\text{CAS}}$** From the bus SDRAM controller. Should connect to SDRAM $\overline{\text{CAS}}$ input.
PGPL3	Output	**System Bus UPM General-Purpose Line 3** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PGTA}}$	Input	**System GPCM TA** Terminates external transactions during GPCM operation. Requires an external pull-up resistor for proper operation.
PUPMWAIT	Input	**System Bus UPM Wait** An external device holds this pin low to force the UPM to wait until the device is ready to continue the operation.
PGPL4	Output	**System Bus UPM General-Purpose Line 4** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PPBS}}$	Output	**System Bus Parity Byte Select** In systems that store data parity in a separate chip, this output is used as the byte-select for that chip.
PSDAMUX	Output	**System Bus SDRAM Address Multiplexer** Controls the system bus SDRAM address multiplexer when the MSC8102 is in external master mode.
PGPL5	Output	**System Bus UPM General-Purpose Line 5** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.

1.6 GPIO, TDM, UART, and Timer Signals

The general-purpose input/output (GPIO), time-division multiplexed (TDM), universal asynchronous receiver/transmitter (UART), and timer signals are grouped together because they use a common set of signal lines. Individual assignment of a signal to a specific signal line is configured through internal registers. Table 1-7 describes the signals in this group.

Table 1-7. GPIO, TDM, UART, and Timer Signals

Signal Name	Type	Description
GPIO0	Input/ Output	**General-Purpose Input Output 0** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.
CHIP_ID0	Input	**Chip ID 0** Determines the chip ID of the MSC8102 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
GPIO1	Input/ Output	**General-Purpose Input Output 1** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.
TIMER0	Input/ Output	**Timer 0** Each signal is configured as either input to or output from the counter. See the *MSC8102 Reference* for configuration details.
CHIP_ID1	Input	**Chip ID 1** Determines the chip ID of the MSC8102 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
GPIO2	Input/ Output	**General-Purpose Input Output 2** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual*.
TIMER1	Input/ Output	**Timer 1** Each signal is configured as either input to or output from the counter. For the configuration of the pin direction, refer to the *MSC8102 Reference Manual*.
CHIP_ID2	Input	**Chip ID 2** Determines the chip ID of the MSC8102 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
GPIO3	Input/ Output	**General-Purpose Input Output 3** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM3TSYN	Input/ Output	**TDM3 Transmit Frame Sync** Transmit frame sync for TDM 3.
IRQ1	Input	**Interrupt Request 1** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO4	Input/ Output	**General-Purpose Input Output 4** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102* Reference Manual GPIO programing model.
TDM3TCLK	Input	**TDM3 Transmit Clock** Transmit Clock for TDM 3
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO5	Input/ Output	**General-Purpose Input/Output 5** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM3TDAT	Input/ Output	**TDM3 Serial Transmitter Data** The serial transmit data signal for TDM 3. As an output, it provides the DATA_D signal for TDM 3. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO6	Input/ Output	**General-Purpose Input Output 6** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM3RSYN	Input/ Output	**TDM3 Receive Frame Sync** The receive sync signal for TDM 3. As an input, this can be the DATA_B data signal for TDM 3.For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO7	Input/ Output	**General-Purpose Input Output 7** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM3RCLK	Input/ Output	**TDM3 Receive Clock** The receive clock signal for TDM 3. As an output, this can be the DATA_C data signal for TDM 3. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO8	Input/ Output	**General-Purpose Input Output 8** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM3RDAT	Input/ Output	**TDM3 Serial Receiver Data** The receive data signal for TDM 3. As an input, this can be the DATA_A data signal for TDM 3. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ6}}$	Input	**Interrupt Request 6** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO9	Input/ Output	**General-Purpose Input Output 9** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM2TSYN	Input/ Output	**TDM2 Transmit frame Sync** Transmit Frame Sync for TDM 2.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO10	Input/ Output	**General-Purpose Input Output 10** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM2TCLK	Input	**TDM 2 Transmit Clock** Transmit Clock for TDM 2.
$\overline{\text{IRQ8}}$	Input	**Interrupt Request 8** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO11	Input/ Output	**General-Purpose Input Output 11** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM2TDAT	Input/ Output	**TDM2 Serial Transmitter Data** The transmit data signal for TDM 2. As an output, this can be the DATA_D data signal for TDM 2. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ9}}$	Input	**Interrupt Request 9** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO12	Input/ Output	General-Purpose Input Output 12 One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM2RSYN	Input/ Output	**TDM2 Receive Frame Sync** The receive sync signal for TDM 2. As an input, this can be the DATA_B data signal for TDM 2. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ10}}$	Input	**Interrupt Request 10** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO13	Input/ Output	**General-Purpose Input Output 13** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM2RCLK	Input/ Output	**TDM2 Receive Clock** The receive clock signal for TDM 2. As an input, this can be the DATA_C data signal for TDM 2. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ11}}$	Input	**Interrupt Request 11** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO14	Input/ Output	**General-Purpose Input Output 14** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM2RDAT	Input/ Output Input	**TDM2 Serial Receiver Data** The receive data signal for TDM 2. As an input, this can be the DATA_A data signal for TDM 2. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ12}}$	Input	**Interrupt Request 12** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO15	Input/ Output	**General-Purpose Input Output 15** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM1TSYN	Input/ Output	**TDM1 Transmit frame Sync** Transmit Frame Sync for TDM 1.
DREQ1	Input	**DMA Request 1** Used by an external peripheral to request DMA service.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO16	Input/ Output	**General-Purpose Input Output 16** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM1TCLK	Input	**TDM1 Transmit Clock** Transmit Clock for TDM 1.
$\overline{\text{DONE1}}$	Input/ Output	**DMA Done 1** Signifies that the channel must be terminated. If the DMA generates $\overline{\text{DONE}}$, the channel handling this peripheral is inactive. As an input to the DMA, $\overline{\text{DONE}}$ closes the channel much like a normal channel closing. See the *MSC8102 Reference Manual* chapters on DMA and GPIO for information on configuring the $\overline{\text{DRACK}}$ or $\overline{\text{DONE}}$ mode and pin direction.
$\overline{\text{DRACK1}}$	Output	**DMA Data Request Acknowledge 1** Asserted by the DMA controller to indicate that the DMA controller has sampled the peripheral request.
GPIO17	Input/ Output	**General-Purpose Input Output 17** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM1TDAT	Input/ Output	**TDM1 Serial Transmitter Data** The transmit data signal for TDM 1. As an output, this can be the DATA_D data signal for TDM 1.For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
DACK1	Output	**DMA Acknowledge 1** The DMA controller drives this output to acknowledge the DMA transaction on the bus.
GPIO18	Input/ Output	**General-Purpose Input Output 18** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM1RSYN	Input/ Output	**TDM1 Receive Frame Sync** The receive sync signal for TDM 1. As an input, this can be the DATA_B data signal for TDM 1. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
DREQ2	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
GPIO19	Input/ Output	**General-Purpose Input Output 19** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM1RCLK	Input/ Output	**TDM1 Receive Clock** The receive clock signal for TDM 1. As an input, this can be the DATA_C data signal for TDM 1. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
DACK2	Output	**DMA Acknowledge 2** The DMA controller drives this output to acknowledge the DMA transaction on the bus.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO20	Input/ Output	**General-Purpose Input Output 20** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM1RDAT	Input/ Output	**TDM1 Serial Receiver Data** The receive data signal for TDM 1. As an input, this can be the DATA_A data signal for TDM 1. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
GPIO21	Input/ Output	**General-Purpose Input Output 21** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM0TSYN	Input/ Output	**TDM0 Transmit frame Sync** Transmit Frame Sync for TDM 0.
GPIO22	Input/ Output	**General-Purpose Input Output 22** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM0TCLK	Input	**TDM 0 Transmit Clock** Transmit Clock for TDM 0.
$\overline{\text{DONE2}}$	Input/ Output	**DMA Done 2** Signifies that the channel must be terminated. If the DMA generates DONE, the channel handling this peripheral is inactive. As an input to the DMA, DONE closes the channel much like a normal channel closing. **Note:** See the *MSC8102 Reference Manual* chapters on DMA and GPIO for information on configuring the $\overline{\text{DRACK}}$ or $\overline{\text{DONE}}$ mode and pin direction.
$\overline{\text{DRACK2}}$	Output	**DMA Data Request Acknowledge 2** Asserted by the DMA controller to indicate that the DMA controller has sampled the peripheral request.
GPIO23	Input/ Output	**General-Purpose Input Output 23** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM0TDAT	Input/ Output	**TDM0 Serial Transmitter Data** The transmit data signal for TDM 0. As an output, this can be the DATA_D data signal for TDM 0. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ13}}$	Input	**Interrupt Request 13** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO24	Input/ Output	**General-Purpose Input Output 24** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM0RSYN	Input/ Output	**TDM0 Receive Frame Sync** The receive sync signal for TDM 0. As an input, this can be the DATA_B data signal for TDM 0. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ14}}$	Input	**Interrupt Request 14** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO25	Input/ Output	**General-Purpose Input Output 25** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM0RCLK	Input/ Output	**TDM0 Receive Clock** The receive clock signal for TDM 0. As an input, this can be the DATA_C data signal for TDM 0. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ15}}$	Input	**Interrupt Request 15** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO26	Input/ Output	**General-Purpose Input Output 26** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TDM0RDAT	Input/ Output	**TDM0 Serial Receiver Data** The receive data signal for TDM 0. As an input, this can be the DATA_A data signal for TDM 0. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
GPIO27	Input/ Output	**General-Purpose Input Output 27** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
URXD	Input	**UART Receive Data**
GPIO28	Input/ Output	**General-Purpose Input Output 28** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
UTXD	Output	**UART Transmit Data**
GPIO29	Input/ Output	**General-Purpose Input Output 29** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
CHIP_ID3	Input	**Chip ID 3** Determines the chip ID of the MSC8102 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO30	Input/ Output	**General-Purpose Input Output 30** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TIMER2	Input/ Output	**Timer 2** Each signal is configured as either input to the counter or output from the counter. For the configuration of the pin direction, refer to the *MSC8102 Reference Manual*.
TMCLK	Input	**External TIMER Clock** An external timer can connect directly to the SIU as the SIU Clock.
GPIO31	Input/ Output	**General-Purpose Input Output 31** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programing model.
TIMER3	Input/ Output	**Timer 3** Each signal is configured as either input to or output from the counter. For the configuration of the pin direction, refer to the *MSC8102 Reference Manual*.

1.7 EOnCE Event and JTAG Test Access Port Signals

The MSC8102 uses two sets of debugging signals for the two types of internal debugging modules: EOnCE and the JTAG TAP controller. Each internal SC140 core has an EOnce module, but they are all accessed externally by the same two signals EE0 and EE1. The MSC8102 supports the standard set of Test Access Port (TAP) signals defined by IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture specification and described in **Table 1-8**.

Table 1-8. JTAG Test Access Port Signals

Signal Name	Type	Signal Description
EE0	Input	**EOnCE Event Bit 0** Used for putting the internal SC140 cores into Debug mode.
EE1	Output	**EOnCE Event Bit 1** Indicates that at least one on-chip SC140 core is in Debug mode.
TCK	Input	**Test Clock—**A test clock signal for synchronizing JTAG test logic.
TDI	Input	**Test Data Input—**A test data serial signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	**Test Data Output—**A test data serial signal for test instructions and data. TDO can be tri-stated. The signal is actively driven in the shift-IR and shift-DR controller states and changes on the falling edge of TCK.
TMS	Input	**Test Mode Select—**Sequences the test controller's state machine, is sampled on the rising edge of TCK, and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	**Test Reset—**Asynchronously initializes the test controller, has an internal pull-up resistor, and must be asserted after power up.

1.8 Reserved Signals

Table 1-9. Reserved Signals

Signal Name	Type	Signal Description
TEST	Input	**Test** Used for manufacturing testing. You ***must*** connect this pin to GND.

Chapter 2

Specifications

2.1 Introduction

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8102 User's Manual* and *MSC8102 Reference Manual*.

Note: The MSC8102 electrical specifications are preliminary and many are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after thorough characterization and device qualifications have been completed.

2.2 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 describes the maximum electrical ratings for the MSC8102.

Table 2-1. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{DD}	–0.2 to 2.1	V
PLL supply voltage	V_{CCSYN}	–0.2 to 2.1	V
I/O supply voltage	V_{DDH}	–0.2 to 4.0	V
Input voltage	V_{IN}	(GND – 0.2) to 4.0	V
Maximum operating temperature range	T_J	TBD	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 2-2.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 4.1**, *Thermal Design Considerations*, on page **1** includes a formula for computing the chip junction temperature (T_J).

2.3 Recommended Operating Conditions

Table 2-2 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2-2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	V_{DD}	1.55 to 1.7	V
PLL supply voltage	V_{CCSYN}	1.55 to 1.7	V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	–0.2 to V_{DDH}+0.2	V
Operating temperature range	T_J	250 MHz: –40 to 105 275 MHz: TBD	°C

2.4 Thermal Characteristics

Table 2-3 describes thermal characteristics of the MSC8102 for the FC-CBGA (HCTE) package.

Table 2-3. Thermal Characteristics for FC-CBGA (HCTE) Package

Characteristic	Symbol	FC-CBGA (HCTE) 20 × 20 mm[5]			Unit
		Natural Convection	100 ft/min (.5 m/s) airflow	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$ or θ_{JA}	28.5	23.7	20.7	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$ or θ_{JA}	16.6	14.3	13.1	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$ or θ_{JB}	7.5			°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the single layer (1s) board horizontal.
3. Per JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Values listed are based on simulations. Final values will be released when testing is complete.

Note: Pre-production MSC8102 devices use an FC-PBGA package. The thermal characteristics for this package have not yet been determined.

Section 4.1, *Thermal Design Considerations* provides a more detailed explanation of these characteristics.

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8102. The measurements in **Table 2-4** assume the following system conditions:

- T_A = 0–70 °C
- V_{DD} = 1.55–1.7 V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD} or both V_{DDH} and V_{DD} must vary in the same direction (for example, both V_{DDH} and V_{DD} vary by +2 percent or both vary by –2 percent).

Table 2-4. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.0	3.465	V
Input low voltage	V_{IL}	GND	0	0.4	V
CLKIN input high voltage	V_{IHC}	2.4	3.0	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0	0.4	V
Input leakage current, V_{IN} = V_{DDH}	I_{IN}	—	TBD	TBD	µA
Tri-state (high impedance off state) leakage current, V_{IN} = V_{DDH}	I_{OZ}	—	TBD	TBD	µA
Signal low input current, V_{IL} = 0.4 V	I_L	TBD	TBD	TBD	µA
Signal high input current, V_{IH} = 2.0 V	I_H	TBD	TBD	TBD	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0	0.4	V
Core power at • 250 MHz • 275 MHz	P_{CORE}	 — —	 1.84 TBD	 — —	 W W
Peripherals power at • 250 MHz • 275 MHz	P_{PERIPH}	 — —	 TBD TBD	 — —	 W W
I/O power at • 83 MHz • 92 MHz	$P_{I/O}$	 — —	 TBD TBD	 — —	 W W
Note: Power consumption was determined from the average current draw at 1.6 V core voltage when running a 4-core EFR pattern.					

2.6 AC Timings

2.6.1 Load Assumptions

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. AC timings are based on a 50 pF load, except where noted otherwise, and a 50 Ω transmission line. For any additional pF, add 0.07 ns for the delay and take the RC delay into consideration.

2.6.2 Clock and Timing Signals

The following sections include a description of clock signal characteristics.

Table 2-5. System Clock Parameters

Characteristic	Minimum	Maximum	Unit
Phase jitter between CLKOUT and DLLIN	—	0.5	ns
CLKIN frequency	36	75	MHz
CLKIN slope	—	5	ns
DLLIN slope	—	2	ns
CLKOUT frequency jitter	—	(0.01 × CLKOUT) + CLKIN jitter	ns
Delay between CLKOUT and DLLIN	—	5	ns
Note: Low CLKIN frequency causes poor PLL performance. Choose a CLKIN frequency high enough to keep the frequency after predivider (SPLLMFCLK) higher than 18 MHz			

Table 2-6 shows the maximum frequency values for internal (Core, Reference, and DSI) and external (CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

Table 2-6. Maximum Frequencies

Characteristic	Maximum in MHz
Core Frequency	250/275
Reference Frequency (REFCLK)	83.3/91.7
DSI Clock Frequency (HCLKIN)	if REFCLK ≤ 70 MHz, HCLKIN = CLKOUT if REFCLK > 70 MHz, HCLKIN = 70 MHz
External Clock Output Frequency (CLKOUT)	83.3/91.7
Note: The REFCLK is CLKOUT.	

Table 2-7. Clock Operation

Characteristics	Symbol	250 MHz Device		275 MHz Device	
		Min	Max	Min	Max
CLKIN[1] • Frequency • Cycle time	 F_{CLKIN} T_{CLKIN}	 36 MHz 13.3 ns	 75 MHz 28 ns	 36 MHz 13.3 ns	 75 MHz 28 ns
DLLIN[1] • Frequency • Cycle time	 F_{DLLIN} T_{DLLIN}	 33.3 MHz 13.3 ns	 75 MHz 30 ns	 33.3 MHz 13.3 ns	 75 MHz 30 ns
Reference Clock (REFCLK) • Frequency • Cycle time	 F_{REFCLK} T_{REFCLK}	 33.3 MHz 12 ns	 83.3 MHz 30 ns	 33.3 MHz 10.9 ns	 91.7 MHz 30 ns
Output Clock (CLKOUT) • Frequency • Cycle time	 F_{CLKOUT} T_{CLKOUT}	 33.3 MHz 12 ns	 83.3 MHz 30 ns	 33.3 MHz 10.9 ns	 91.7 MHz 30 ns
SC140 core clock • Frequency • Cycle time	 F_{CORE} T_{CORE}	 166.7 MHz 4 ns	 250 MHz 6 ns	 166.7 MHz 3.6 ns	 275 MHz 6 ns

Notes: **1.** The rise and fall time of external clocks should be 5 ns maximum
2. Measured at 50 percent of the input transition.

2.6.3 Reset Timing

The MSC8102 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8102 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 2-8** describes the reset sources.

Table 2-8. Reset Sources

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	Initiates the power-on reset flow that resets the MSC8102 and configures various attributes of the MSC8102. On $\overline{\text{PORESET}}$, the entire MSC8102 device is reset. SPLL and DLL states are reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The clock mode (MODCK bits), reset configuration mode, boot mode, Chip ID, and use of either a DSI 64 bits port or a System Bus 64 bits port are configured only when $\overline{\text{PORESET}}$ is asserted.
External Hard reset ($\overline{\text{HRESET}}$)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8102. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The most configurable features are reconfigure. These features are defined in the 32-bit hard reset configuration word described in *Hard Reset Configuration Word* section of the *Reset* chapter in the *MSC8102 Reference Manual*.

Table 2-8. Reset Sources

Name	Direction	Description
External Soft reset ($\overline{\text{SRESET}}$)	Input/ Output	Initiates the soft reset flow. The MSC8102 detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8102 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the SC140 extended cores are reset, and system configuration is maintained.
Software watchdog reset	Internal	When the MSC8102 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC8102 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.

Table 2-9 summarizes the reset actions that occur as a result of the different reset sources.

Table 2-9. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset ($\overline{\text{PORESET}}$)	Hard Reset ($\overline{\text{HRESET}}$)	Soft Reset ($\overline{\text{SRESET}}$)	
	External only	External or Internal (Software Watchdog or Bus Monitor)	External	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration Pins Sampled (Refer to **Section 2.6.3.1** for details).	Yes	No	No	No
SPLL and DLL States Reset	Yes	No	No	No
System Reset Configuration write through the DSI	Yes	No	No	No
System Reset Configuration write though the System Bus	Yes	Yes	No	No
$\overline{\text{HRESET}}$ Driven	Yes	Yes	No	No
SIU Registers reset	Yes	Yes	No	No
IPBus Modules Reset (TDM, UART, Timers, DSI, IPBus Master, GIC, HS, and GPIO)	Yes	Yes	Yes	Yes
$\overline{\text{SRESET}}$ Driven	Yes	Yes	Yes	Depends on command
SC140 Extended Cores Reset	Yes	Yes	Yes	Yes
MQBS Reset	Yes	Yes	Yes	Yes

2.6.3.1 Power-On Reset ($\overline{\text{PORESET}}$) Pin

Asserting $\overline{\text{PORESET}}$ initiates the power-on reset flow. $\overline{\text{PORESET}}$ must be asserted externally for at least 16 CLKIN cycles after external power to the MSC8102 reaches at least 2/3 V_{DD}.

2.6.3.2 Reset Configuration

The MSC8102 has two mechanisms for writing the reset configuration:

- Through the direct slave interface (DSI), or
- Through the system bus

When reset configuration written through the system bus, the MSC8102 uses as a configuration master or as a configuration slave. If a configuration slave is selected, but no special configuration word is written, a default configuration word is applied.

Fourteen signal levels (see **Chapter 1** for signal description details) are sampled on $\overline{\text{PORESET}}$ deassertion to define the Reset Configuration Mode and boot and operating conditions:

- $\overline{\text{RSTCONF}}$
- CNFGS
- DSISYNC
- DSI64
- CHIP_ID[0–3]
- BM[0–2]
- SWTE
- MODCK[1–2]

2.6.3.3 Reset Timing Tables

Table 2-10 and **Figure 2-1** describe the reset timing for a reset configuration write through the direct slave interface (DSI) or through the system bus.

Table 2-10. Timing for a Reset Configuration Write through the DSI or System Bus

No.	Characteristics	Expression	Min	Max	Unit
1	Required external $\overline{\text{PORESET}}$ duration minimum • CLKIN = 18 MHz • CLKIN = 75 MHz	16 / CLKIN	 888.8 213.3	—	ns
2	Delay from deassertion of external $\overline{\text{PORESET}}$ to deassertion of internal $\overline{\text{PORESET}}$ • CLKIN = 18 MHz • CLKIN = 75 MHz	1024 / CLKIN	 58.89 13.65		 µs µs
3	Delay from de-assertion of internal $\overline{\text{PORESET}}$ to SPLL lock • CLKIN = 18 MHz • CLKIN = 75 MHz	800 / (CLKIN/PDF) (pre-division factor)	 44.4 32.0		 µs µs
4	Delay from SPLL lock to DLL lock. • DLL enabled REFCLK = 18 Mhz REFCLK = 75 Mhz • DLL disabled	 3073 / REFCLK —	 170.72 40.97 0.0		 µs µs µs

Table 2-10. Timing for a Reset Configuration Write through the DSI or System Bus

No.	Characteristics	Expression	Min	Max	Unit
5	• Delay from SPLL and DLL lock to $\overline{\text{HRESET}}$ de-assertion				
	• DLL enabled	3585 / REFCLK			
	REFCLK = 18 Mhz		199.17		µs
	REFCLK = 75 Mhz		47.5		µs
	• DLL disabled	512 / REFCLK			
	REFCLK = 18 Mhz		28.4		µs
	REFCLK = 75 Mhz		6.83		µs
6	Delay from SPLL and DLL lock to $\overline{\text{SRESET}}$ de-assertion				
	• DLL enabled	3588 / REFCLK			
	REFCLK = 18 Mhz		199.33		µs
	REFCLK = 75 Mhz		47.84		µs
	• DLL disabled	515 / REFCLK			
	REFCLK = 18 Mhz		28.61		µs
	REFCLK = 75 Mhz		6.87		µs

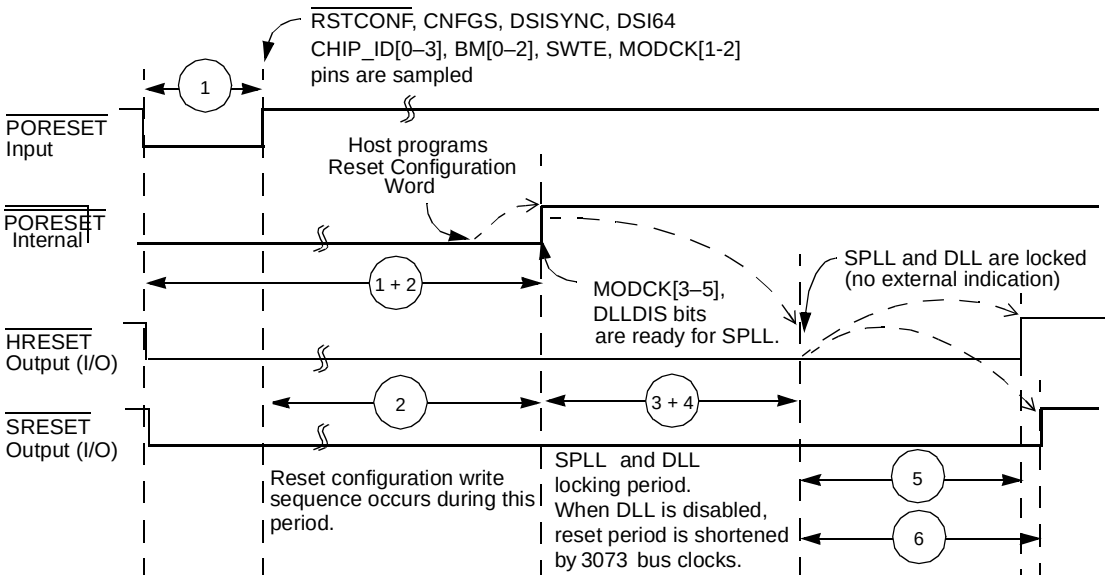


Figure 2-1. Timing Diagram for a Reset Configuration Write

2.6.4 System Bus Access Timing

2.6.4.1 Core Data Transfers

Generally, all MSC8102 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is either the DLLIN signal or, if DLL is disabled, the CLKOUT signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), as **Figure 2-2** shows.

Figure 2-2 is a graphical representation of the internal ticks.

Figure 2-2. Internal Tick Spacing for Memory Controller Signals

The UPM machine and GPCM machine outputs change on the internal tick determined by the memory controller programming, the AC specifications are relative to the internal tick. SDRAM machine outputs change only on the REFCLK rising edge.

Table 2-11. AC Timing for SIU Inputs in Non-Pipelined Mode

No.	Characteristic	Value	Units
10	Hold time for all signals after REFCLK rising edge	0.5	ns
11	$\overline{\text{AACK}}/\overline{\text{ARTRY}}/\overline{\text{TA}}/\overline{\text{TEA}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}/\overline{\text{PSDVAL}}$ setup time before REFCLK rising edge	5	ns
12	Data bus setup time before REFCLK rising edge in Normal mode	4.5	ns
13	Data bus setup time before REFCLK rising edge in ECC and PARITY modes	6	ns
14	DP setup time before REFCLK rising edge	6	ns
15	Address bus/TT[0–4]/TC[0–2]/$\overline{\text{TBST}}$/TSIZ[0–3]/$\overline{\text{GBL}}$ setup time before REFCLK rising edge	4	ns
16	Setup time before REFCLK rising edge for all other pins	4	ns

Notes: **1.** Values are measured from the TTL signal level (0.8 or 2.0 V) relative to the REFCLK rising edge.
2. SIU inputs are for the normal configuration (SIUBCR[EXDD] = 0—which gives an extra cycle for address inputs. When SIUBCR[EXDD] = 1, address setup time is 10 ns, requiring a maximum bus frequency of 50 MHz.

Table 2-12. AC Timing for SIU Inputs in Pipelined Mode

No.	Characteristic	Value	Units
10	Hold time for all signals after REFCLK rising edge	0.5	ns
11	$\overline{\text{AACK}}/\overline{\text{ARTRY}}/\overline{\text{TA}}/\overline{\text{TEA}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}$ setup time before REFCLK rising edge	4.5	ns
12	Data bus setup time before REFCLK rising edge in Normal mode	3	ns
13	Data bus setup time before REFCLK rising edge in ECC and Parity modes	5.5	ns
14	DP setup time before REFCLK rising edge	5	ns
15	Address bus/TT[0–4]/TC[0–2]/$\overline{\text{TBST}}$/TSIZ[0–3]/$\overline{\text{GBL}}$ setup time before REFCLK rising edge	3.5	ns
16	Setup time before REFCLK rising edge for all other pins	3	ns

Notes: **1.** Values are measured from the TTL signal level (0.8 or 2.0 V) relative to the REFCLK rising edge.
2. SIU inputs are for the normal configuration (SIUBCR[EXDD] = 0—which gives an extra cycle for address inputs. When SIUBCR[EXDD] = 1, address setup time is 10 ns, requiring a maximum bus frequency of 50 MHz.

Table 2-13. AC Timing for SIU Outputs for 30 pF in Non-Pipelined Mode

No.	Characteristic	Minimum	Maximum	Units
31	PSDVAL/TEA/TA delay from REFCLK rising edge	0.5	7.5	ns
32a	Address bus/TT[0–4]/TC[0–2]/TBST/TSIZ[0–3]/GBL delay from REFCLK rising edge	0.5	8[1]	ns
32b	BADDR delay from REFCLK rising edge	0.5	8	ns
33a	Data bus delay from REFCLK rising edge	0.5	7.5	ns
33b	DP delay from REFCLK rising edge	0.5	7.5	ns
34	Memory controller signals/ALE delay from REFCLK rising edge	0.5	6.5	ns
35	DBG/BR/ABB/CS delay from REFCLK rising edge	0.5	6.5	ns
36	Delay from REFCLK rising edge for all other signals	0.5	6.5	ns

Notes: **1.** In 60x-compatible mode with SIUBCR[EBM] = 1.
2. Values are measured from the 1.4 V level of the REFCLK rising edge to the TTL signal level (0.8 or 2 V)

Table 2-14. AC Timing for SIU Outputs for 30pF in Pipelined Mode

No.	Characteristic	Minimum	Maximum	Units
31	PSDVAL/TEA/TA delay from REFCLK rising edge	0.5	7	ns
32a	Address bus/TT[0–4]/TC[0–2]/TBST/TSIZ[0–3]/GBL delay from REFCLK rising edge	0.5	6[2]	ns
32b	BADDR delay from REFCLK rising edge	0.5	6	ns
33a	Data bus delay from REFCLK rising edge	0.5	6	ns
33b	DP delay from REFCLK rising edge	0.5	7	ns
34	Memory controller signals/ALE delay from REFCLK rising edge	0.5	6	ns
35	DBG/BR/ABB/CS delay from REFCLK rising edge	0.5	6.5	ns
36	Delay from REFCLK rising edge for all other signals	0.5	6.5	ns

Notes: **1.** The maximum bus frequency depends on the mode:
• In 60x-compatible mode connected to another MSC8102 device, the frequency is determined by adding the input and output longest timing values, which results in a frequency of 80 MHz.
• In single-master mode, the frequency depends on the timing of the devices connected to the MSC8102.
2. In single master mode with SIUBCR[EBM] = 0.
3. Values are measured from the 1.4 V level of the REFCLK rising edge to the TTL signal level (0.8 or 2 V)

Table 2-15. AC Timing for SIU Outputs for 50 pF in Non-Pipelined Mode

No.	Characteristic	Minimum	Maximum	Units
31	PSDVAL/TEA/TA delay from REFCLK rising edge	0.5	9.5	ns
32a	Address bus/TT[0–4]/TC[0–2]/TBST/TSIZ[0–3]/GBL delay from REFCLK rising edge	0.5	10	ns
32b	BADDR delay from REFCLK rising edge	0.5	8.5	ns
33a	Data bus delay from REFCLK rising edge	0.5	9.5	ns
33b	DP delay from REFCLK rising edge	0.5	9.5	ns
34	Memory controller signals/ALE delay from REFCLK rising edge	0.5	8	ns
35	DBG/BR/ABB/CS delay from REFCLK rising edge	0.5	8.5	ns
36	Delay from REFCLK rising edge for all other signals	0.5	8	ns

Note: Values are measured from the 1.4 V level of the REFCLK rising edge to the TTL signal level (0.8 or 2 V)

Table 2-16. AC Timing for SIU Outputs for 50 pF in Pipelined Mode

No.	Characteristic	Minimum	Maximum	Units
31	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$ delay from REFCLK rising edge	0.5	9	ns
32a	Address bus/TT[0–4]/TC[0–2]/$\overline{\text{TBST}}$/TSIZ[0–3]/$\overline{\text{GBL}}$ delay from REFCLK rising edge	0.5	8	ns
32b	BADDR delay from REFCLK rising edge	0.5	8	ns
33a	Data bus delay from REFCLK rising edge	0.5	8	ns
33b	DP delay from REFCLK rising edge	0.5	9.5	ns
34	Memory controller signals/ALE delay from REFCLK rising edge	0.5	8	ns
35	$\overline{\text{DBG}}/\overline{\text{BR}}/\overline{\text{ABB}}/\overline{\text{CS}}$ delay from REFCLK rising edge	0.5	8.5	ns
36	Delay from REFCLK rising edge for all other signals	0.5	8	ns
Note:	Values are measured from the 1.4 V level of the REFCLK rising edge to the TTL signal level (0.8 or 2 V)			

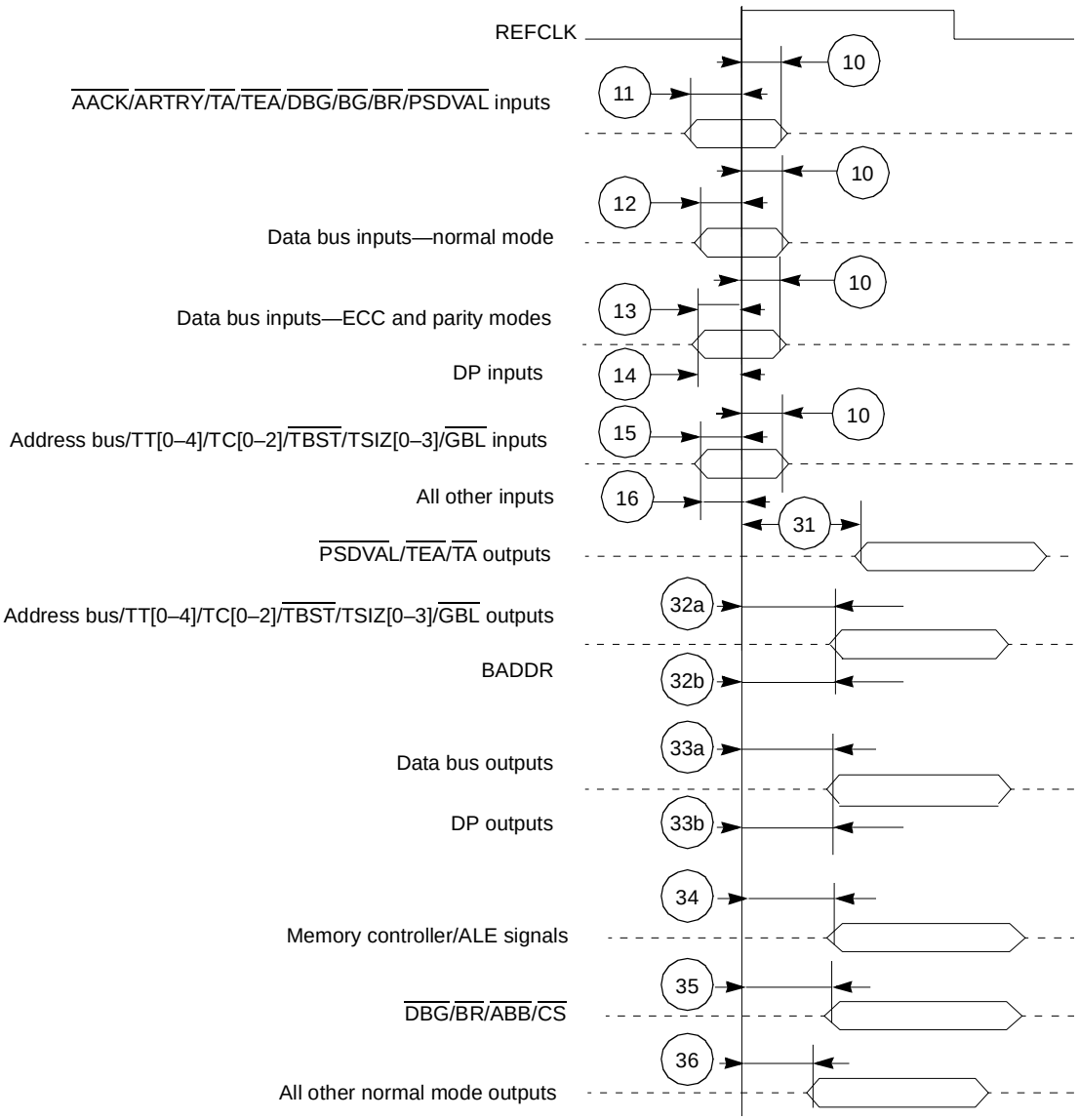


Figure 2-3. Bus Signal Timing

2.6.4.2 DMA Data Transfers

Table 2-17 describes the DMA signal timing.

Table 2-17. DMA Signals

No.	Characteristic	Minimum	Maximum	Units
37	DREQ setup time before falling edge of REFCLK	6	—	ns
38	DREQ hold time after falling edge of REFCLK	0.5	—	ns
39	$\overline{\text{DONE}}$ setup time before falling edge of REFCLK	9	—	ns
40	$\overline{\text{DONE}}$ hold time after falling edge of REFCLK	0.5	—	ns
41	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after REFCLK rising edge	0.5	9	ns

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 2-17**. **Figure 2-4** shows synchronous peripheral interaction.

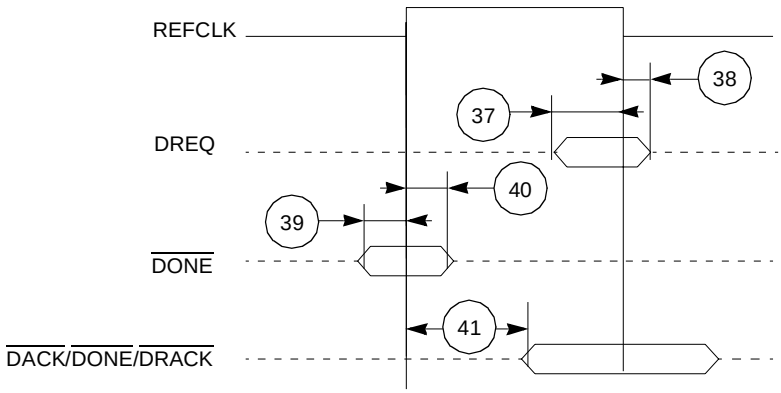


Figure 2-4. DMA Signals

2.6.5 DSI Timing

The timings in the following sections are based on a 30 pF capacitive load. See **Section 2.6.1**, *Load Assumptions*, on page **5** for more details.

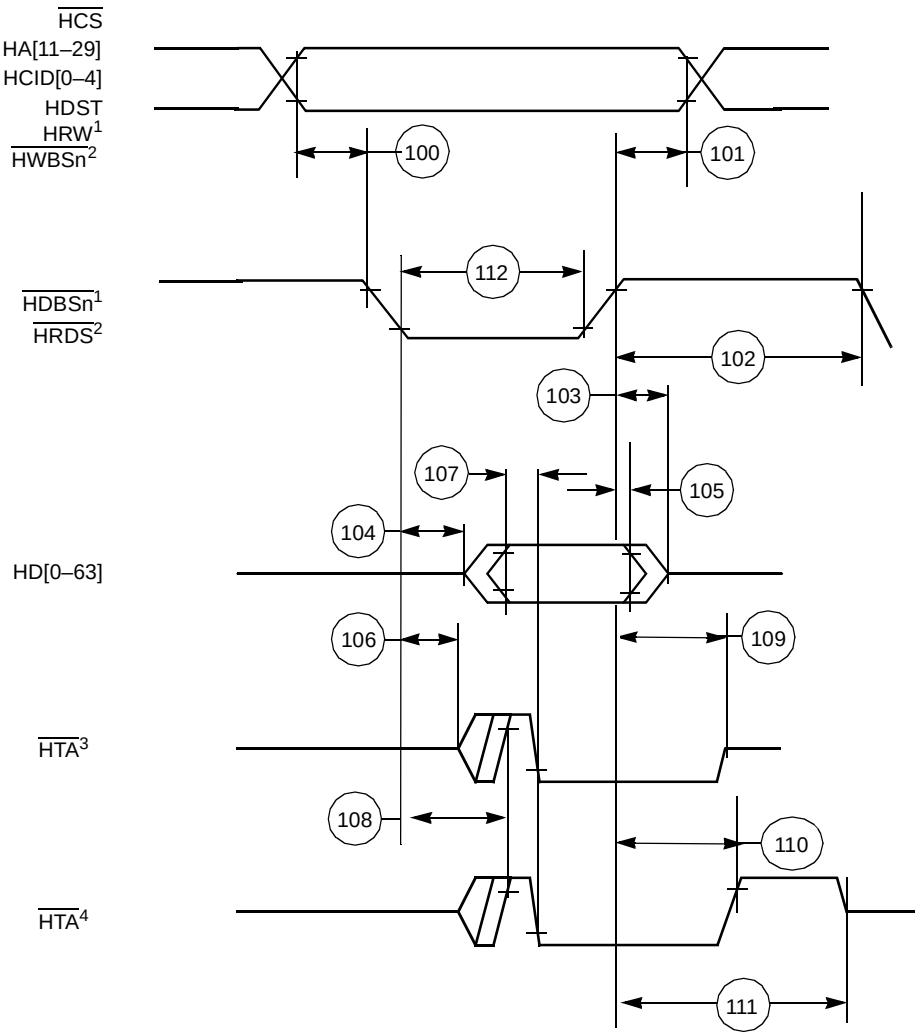
2.6.5.1 DSI Asynchronous Mode

Table 2-18. DSI Asynchronous Mode Timing

No.	Characteristics	Min	Max	Unit
100	Attributes[1] setup time before strobe ($\overline{\text{HWBS[n]}}$) assertion	3.6	—	ns
101	Attributes[1] hold time after data strobe deassertion	2.4	—	ns
102	Read/Write data strobe deassertion width[2] • DCR[HTAAD] = 1 — Consecutive access to the same DSI — Different device with DCR[HTADT] = 01 — Different device with DCR[HTADT] = 10 — Different device with DCR[HTADT] = 11 • DCR[HTAAD] = 0	 $1.8 + T_{REFCLK}$ $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$ $1.8 + T_{REFCLK}$	—	 ns ns ns ns ns
103	Read data strobe deassertion to output data high impedance	—	7.8	ns
104	Read data strobe assertion to output data active from high impedance	3.8	—	ns
105	Output data hold time after read data strobe deassertion	2.2	—	ns
106	Read/Write data strobe assertion to $\overline{\text{HTA}}$ active from high impedance	3.9	—	ns
107	Output data valid to $\overline{\text{HTA}}$ assertion	1	—	ns
108	Read/Write data strobe assertion to $\overline{\text{HTA}}$ valid	—	9.8	ns
109	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 0, $\overline{\text{HTA}}$ at end of access released at logic 0)	—	6.5	ns
110	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ deassertion. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1)	—	9.2	ns
111	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1 • DCR[HTADT] = 01 • DCR[HTADT] = 10 • DCR[HTADT] = 11	—	 $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$	 ns ns ns
112	Read/Write data strobe assertion width	$1.8 + T_{REFCLK}$	—	ns
201	Host data input setup time before write data strobe deassertion	2	—	ns
202	Host data input hold time after write data strobe deassertion	1.3	—	ns

Notes: **1.** "Attributes" refers to the following signals: $\overline{\text{HCS}}$, HA[11–29], HCID[0–4], HDST, HRW, $\overline{\text{HRDS}}$, and $\overline{\text{HWBSn}}$.

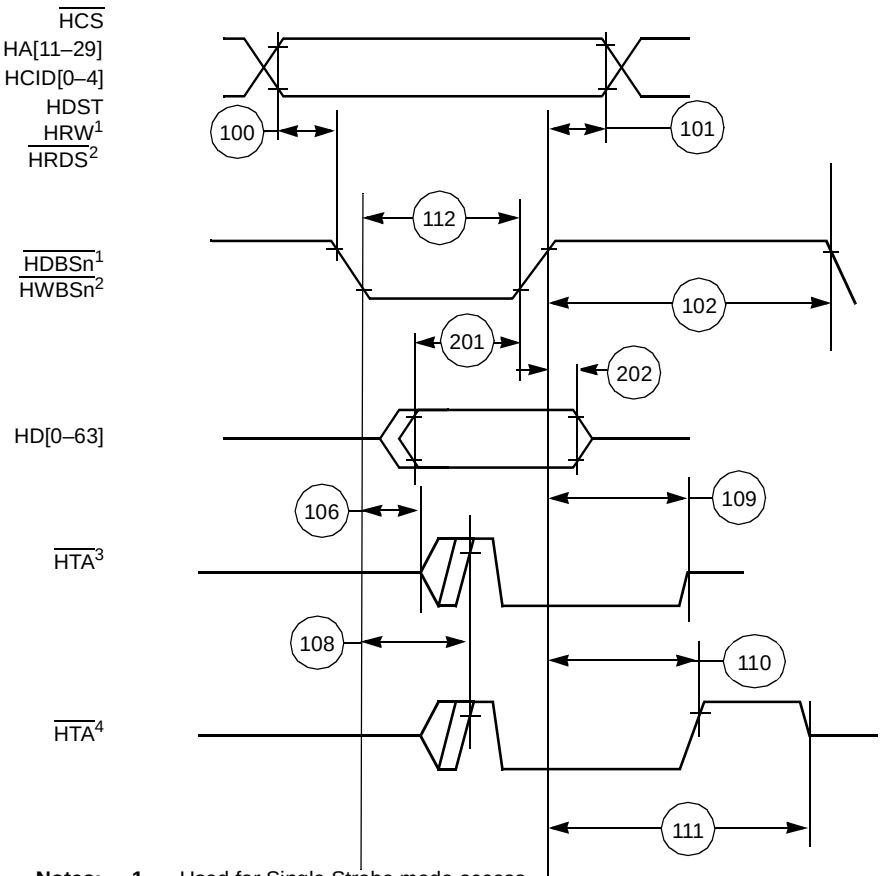
Figure 2-5 shows DSI Asynchronous Read signals timing.



Notes:
1. Used for Single Strobe mode access.
2. Used for Dual Strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 2-5. Asynchronous Single and Dual Modes Read Timing Diagram

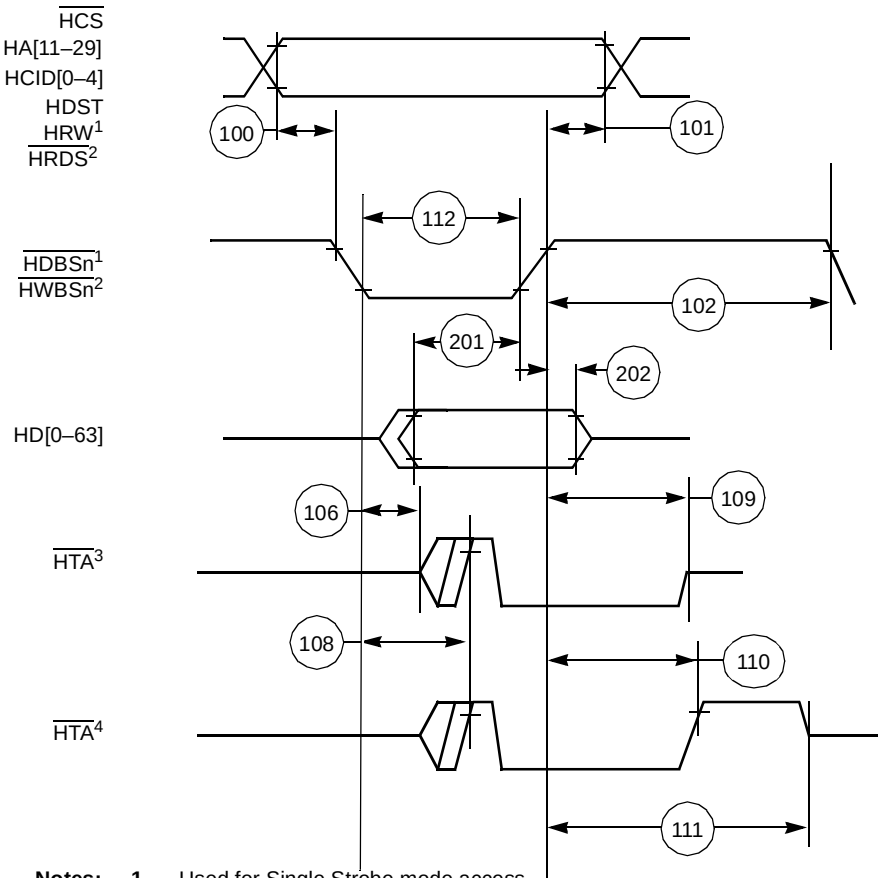
Figure 2-6 shows DSI Asynchronous Write signals timing.



Notes:
1. Used for Single Strobe mode access.
2. Used for Dual Strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 2-6. Asynchronous Single and Dual Modes Write Timing Diagram

Figure 2-7 shows DSI Asynchronous Broadcast Write signals timing.



Notes:
1. Used for Single Strobe mode access.
2. Used for Dual Strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 2-7. Asynchronous Broadcast Write Timing Diagram

2.6.5.2 DSI Synchronous Mode

Table 2-19. DSI Inputs—Synchronous Mode

Number	Characteristic	Expression	Minimum	Maximum	Units
120	HCLKIN Cycle Time[1]	HTC	14.3	55.6	ns
121	HCLKIN High Pulse Width	$(0.5 \pm 0.1) \times$ HTC	5.7	33.3	ns
122	HCLKIN Low Pulse Width	$(0.5 \pm 0.1) \times$ HTC	5.7	33.3	ns
123	HD[0–63], HA[11–29] inputs Setup time	—	2.7	—	ns
124	HCID[0–4] inputs Setup time	—	4.2	—	ns
125	All other inputs Setup time	—	1.5	—	ns
126	All inputs Hold time	—	2.2	—	ns
Notes: **1.** Values are based on a frequency range of 18–70 MHz.					

Table 2-20. DSI Outputs—Synchronous Mode

Number	Characteristic	Minimum	Maximum	Units
127	HCLKIN High to HD[0–63] output active	0	—	
128	HCLKIN High to HD[0–63] output valid	—	8.6	
129	HD[0–63] output Hold time	1.6	—	
130	HCLKIN High to HD[0–63] output high impedance	—	6.2	
131	HCLKIN High to $\overline{\text{HTA}}$ output active	0	—	
132	HCLKIN High to $\overline{\text{HTA}}$ output valid	—	7.4	
133	$\overline{\text{HTA}}$ output Hold time	1.7	—	
134	HCLKIN High to $\overline{\text{HTA}}$ high impedance	—	4.4	

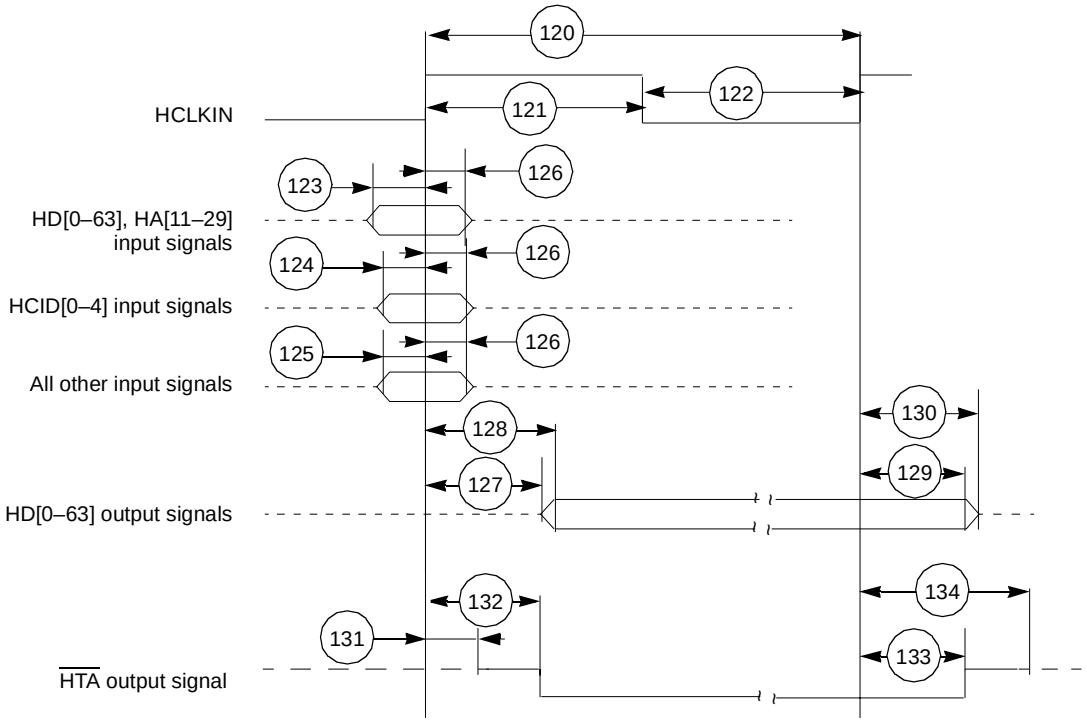


Figure 2-8. DSI Synchronous Mode Signals Timing Diagram

2.6.6 TDM Timing

Table 2-21. TDM Timing

Number	Characteristic	Expression	Minimum	Maximum	Units
300	TDMxRCLK/TDMxTCLK	TC[1]	20	111	ns
301	TDMxRCLK/TDMxTCLK High Pulse Width	$(0.5 \pm 0.1) \times TC$	8	66.7	ns
302	TDMxRCLK/TDMxTCLK Low Pulse Width	$(0.5 \pm 0.1) \times TC$	8	66.7	ns
303	TDM receive all input Setup time		2.5	—	ns
304	TDM receive all input Hold time		1	—	ns
305	TDMxTCLK High to TDmXTDAT output active[2]		4	—	ns
306	TDMxTCLK High to TDMXTDAT output valid[2]		—	14	ns
307	All output hold time[2]		5.2	—	ns
308	TDMxTCLK High to TDmXTDAT output high impedance[2]		—	10	ns
309	TDMxTCLK High to TDMXTSYN output valid[2]		—	13.5	ns
310	TDMxTSYN output hold time[2]		5.2	—	ns

Notes: **1.** Values are based on a frequency range of 9–50 MHz.
2. Values are based on 30 pF capacitive load.

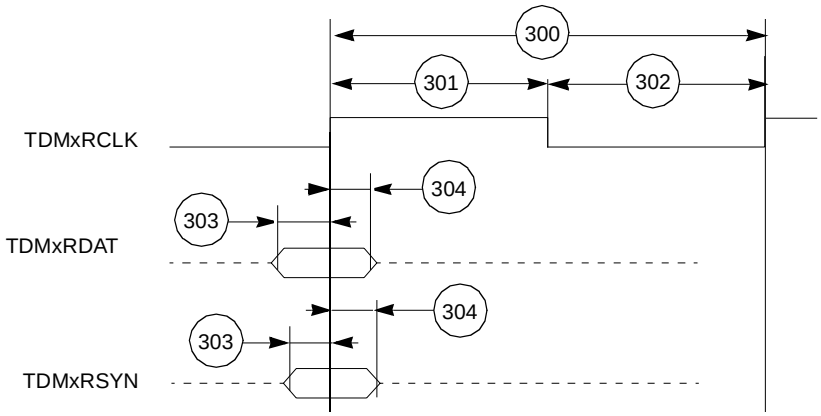


Figure 2-9. TDM Inputs Signals

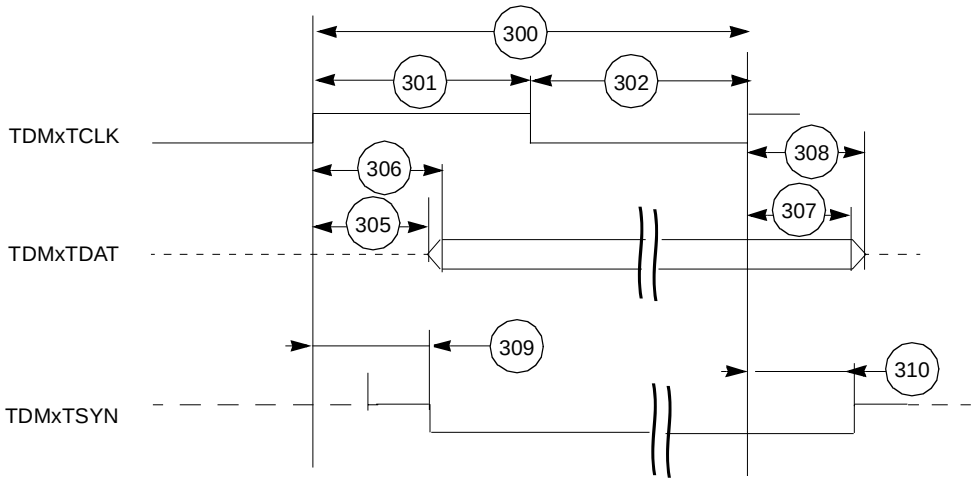


Figure 2-10. TDM Output Signals

2.6.7 UART Timing

Table 2-22. UART Timing

No.	Characteristics	Expression	Min	Max	Unit
400	URXD and UTXD inputs high/low duration	$16 \times T_{REFCLK}$	160.0	—	ns
401	URXD and UTXD inputs rise/fall time			5	ns
402	UTXD output rise/fall time			5	ns

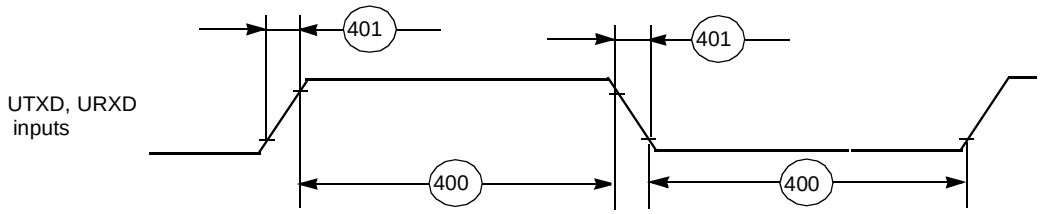


Figure 2-11. UART Input Timing

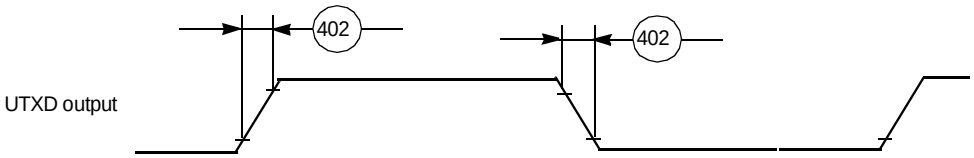


Figure 2-12. UART Output Timing

2.6.8 Timer Timing

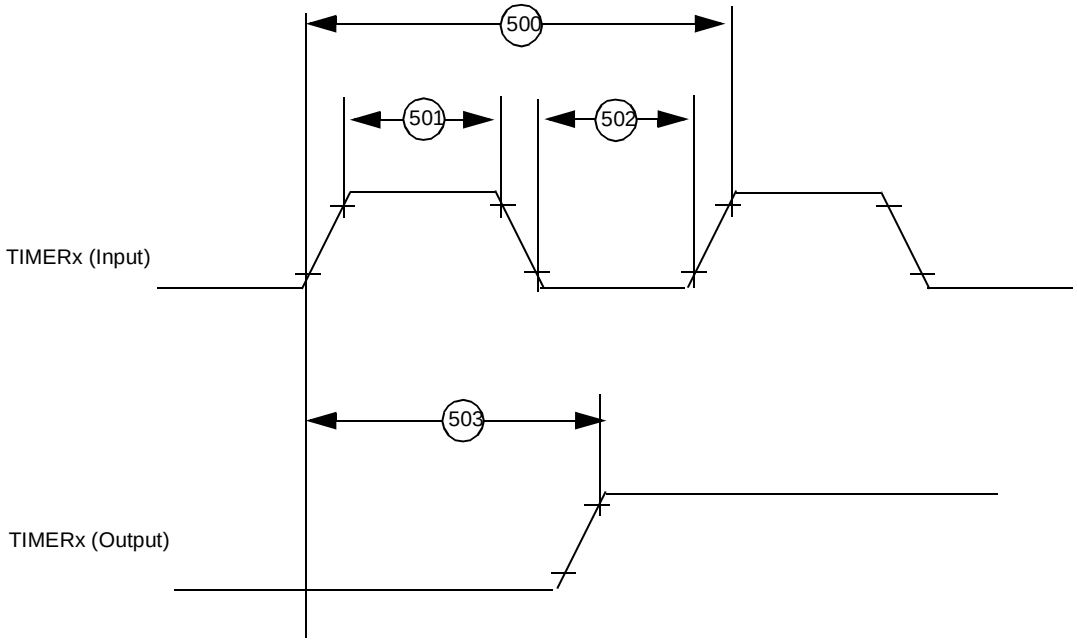


Figure 2-13. Timer Timing

Table 2-23. Timer Timing

No.	Characteristics	92 MHz		Unit
		Min.	Max	
500	TIMERx frequency	10.9	—	ns
501	TIMERx Input high period	4	—	ns
502	TIMERx Output low period	4	—	ns
503	TIMERx Propagations delay from its clock input	5.8	12.3	ns

2.6.9 GPIO Timing

Table 2-24. GPIO Timing

No.	Characteristics	92 MHz		Unit
		Min	Max	
601	REFCLK edge to GPIO out valid (GPIO out delay time)	—	8.5	ns
602	REFCLK edge to GPIO out not valid (GPIO out hold time)	2.5	—	ns
603	REFCLK edge to high impedance on GPIO out	—	3	ns
604	GPIO in valid to REFCLK edge (GPIO in setup time)	4.5	—	ns
605	REFCLK edge to GPIO in not valid (GPIO in hold time)	0.5	—	ns

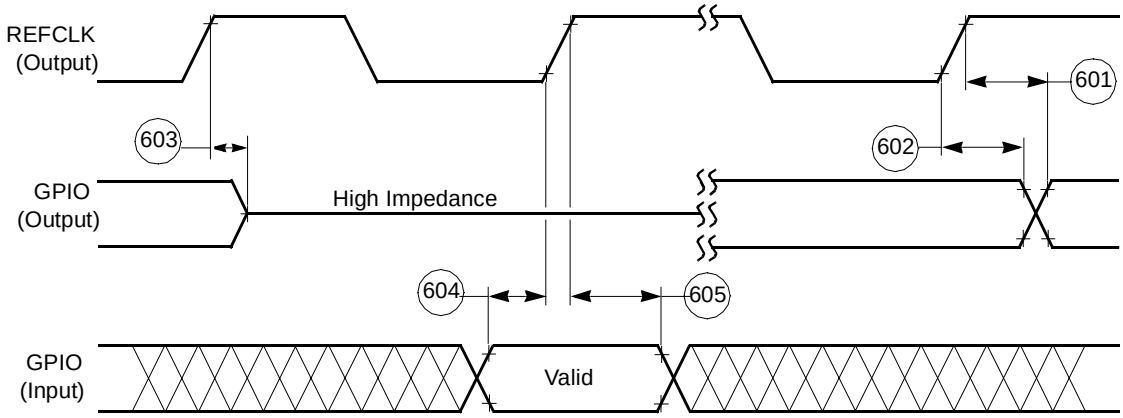


Figure 2-14. GPIO Timing

2.6.10 EE Signals

Table 2-25. EE Pin Timing

Number	Characteristics	Type	Minimum
65	EE pins as inputs	Asynchronous	4 core clock periods
66	EE pins as outputs	Synchronous to Core clock	1 core clock period

Notes:
1. The core clock is the SC140 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Direction of the EE pins is configured in the EE_CTRL register of the EOnCE (See the *SC140 Core Reference Manual* and the *MSC8102 Reference Manual* for details).
3. Refer to **Table 1-4** on page 1-6 for detailed information about EE pin functionality.

Figure 2-15 shows the signal behavior of the EE pins.

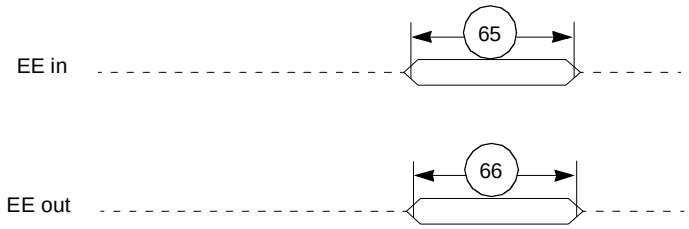


Figure 2-15. EE Pins Timing

2.6.11 JTAG Signals

Table 2-26. JTAG Timing

No.	Characteristics[1,2]	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/($T_C \times 3$); maximum 22 MHz)	0.0	22.0	MHz
701	TCK cycle time in Crystal mode	45.0	—	ns
702	TCK clock pulse width measured at V_M = 1.6 V	20.0	—	ns
703	TCK rise and fall times	0.0	3.0	ns
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	24.0	—	ns
706	TCK low to output data valid	0.0	40.0	ns
707	TCK low to output high impedance	0.0	40.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	25.0	—	ns
710	TCK low to TDO data valid	0.0	44.0	ns
711	TCK low to TDO high impedance	0.0	44.0	ns
712	$\overline{\text{TRST}}$ assert time	100.0	—	ns
713	$\overline{\text{TRST}}$ set-up time to TCK low	40.0	—	ns

Notes: **1.** V_{DDH} = 3.3 V ± 0.3 V; T_J = TBD, C_L = 50 pF
2. All timings apply to OnCE module data transfers as the OnCE module uses the JTAG port as an interface.

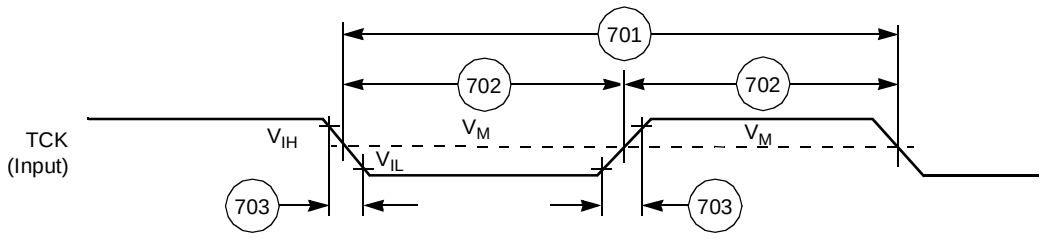


Figure 2-16. Test Clock Input Timing Diagram

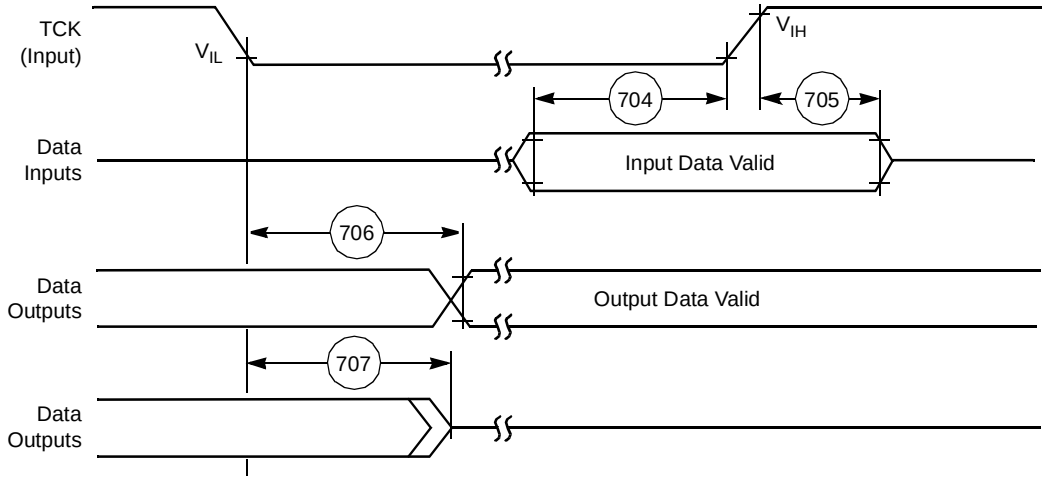


Figure 2-17. Boundary Scan (JTAG) Timing Diagram

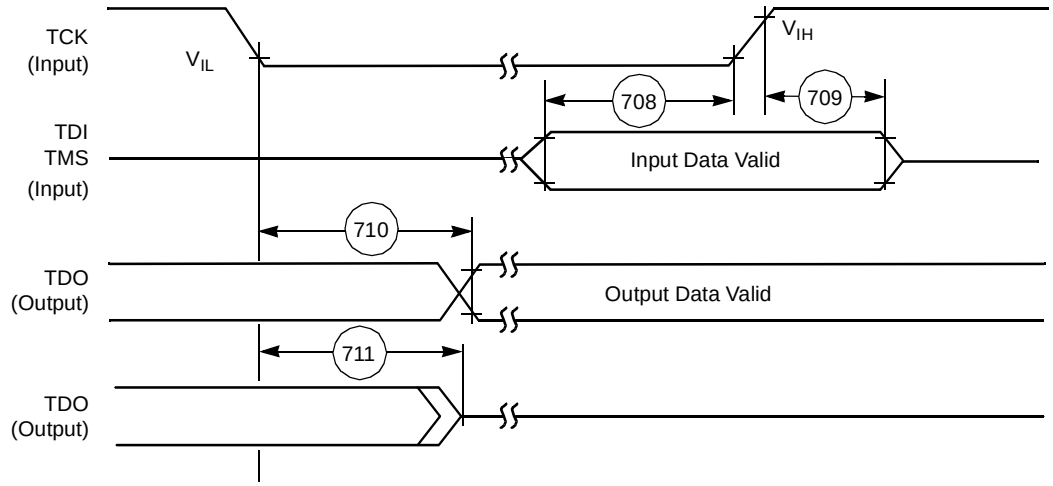


Figure 2-18. Test Access Port Timing Diagram

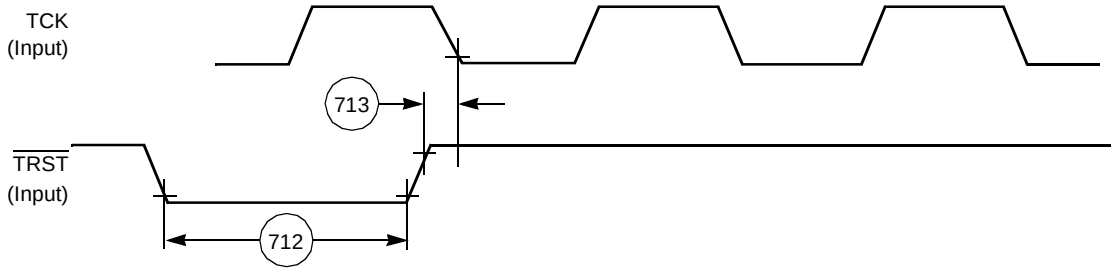


Figure 2-19. $\overline{TRST}$ Timing Diagram

Chapter 3

Packaging

3.1 Pinout and Package Information

This sections provides information about the MSC8102 package, including diagrams of the package pinouts and tables showing how the signals discussed in **Chapter 1**, *Signal/Connection Descriptions* are allocated. The MSC8102 is available in a 431-pin High Temperature Coefficient for Expansion Flip Chip-Ceramic Ball Grid Array (FC-CBGA (HCTE)) and will be used for qualified production parts. Some pre-production MSC8102 devices are provided in a 431-pin Flip Chip-Plastic Ball Grid Array (FC-PBGA) package that may include a copper lid.

3.2 FC-CBGA (HCTE) Package Description

Figure 3-1 and **Figure 3-2** show top and bottom views of the FC-CBGA (HCTE) package, including pinouts. To conform to JDEC requirements, the package is based on a 23 × 23 position (20 × 20 mm) layout with the outside perimeter depopulated. Therefore, ball position numbering starts with B2. Signal names shown in the figures are typically the signal assigned after reset. Signals that are only used during power-on reset (SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, and CHIP_ID[0–3]) are not shown in these figures if there is another signal assigned to the pin after reset. Also, there are several signals that are designated as IRQ lines immediately after reset, but represent duplicate IRQ lines that should be reconfigured by the user. To represent these signals uniquely in the figures, the second functions (BADDR[29–31], DP[1–7], and $\overline{\text{INT\_OUT}}$) are used.

Table 3-1 lists the MSC8102 signals alphabetically by signal name. Connections with multiple names are listed individually by each name. Signals with programmable polarity are shown both as signals which are asserted low (default) and high (that is, $\overline{\text{NAME}}$/NAME). **Table 3-2** lists the signals numerically by pin number. Each pin number is listed once with the various signals that are multiplexed to it. For simplicity, signals with programmable polarity are shown in this table only with their default name (asserted low).

Note: Pre-production MSC8102 devices are shipped with the FC-PBGA package. It has the same pinout as the FC-CBGA package.

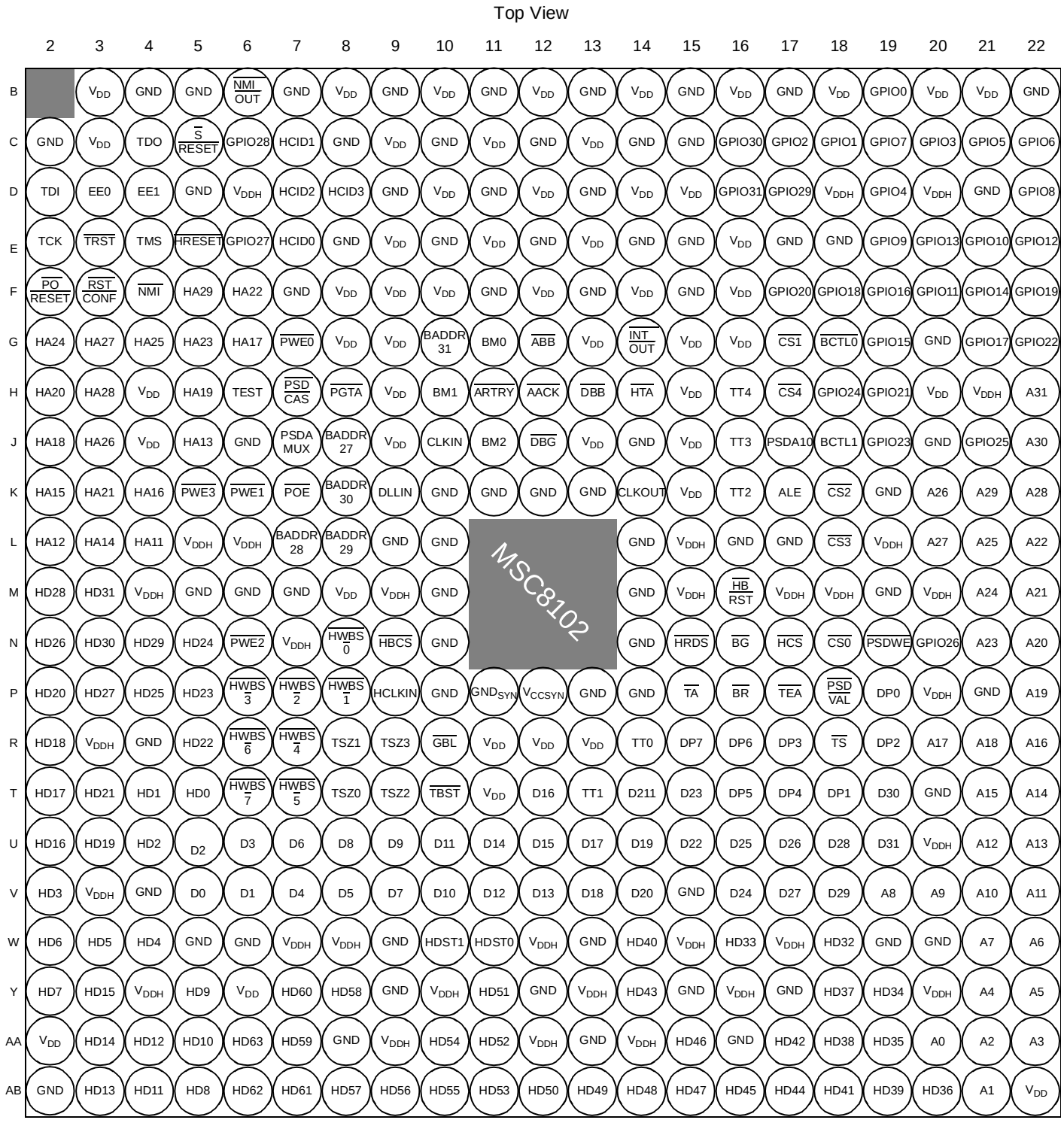


Figure 3-1. MSC8102 High Temperature Coefficient for Expansion Flip Chip Ceramic Ball Grid Array (High CTE FC-CBGA), Top View

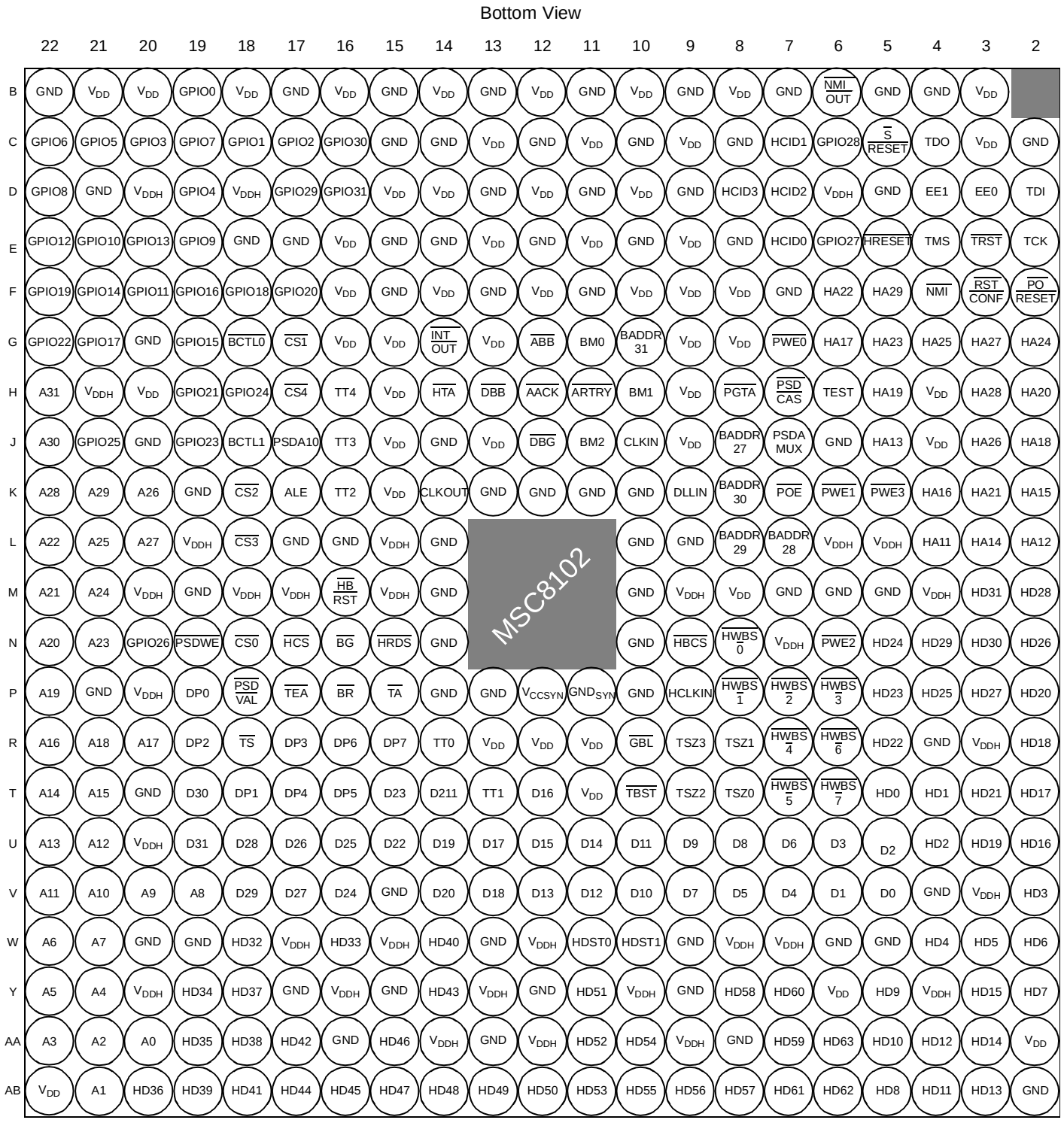


Figure 3-2. MSC8102 High Temperature Coefficient for Expansion Flip Chip Ceramic Ball Grid Array (High CTE FC-CBGA), Bottom View

Table 3-1. MSC8102 Signal Listing By Name

Signal Name	Location Designator
A0	AA20
A1	AB21
A2	AA21
A3	AA22
A4	Y21
A5	Y22
A6	W22
A7	W21
A8	V19
A9	V20
A10	V21
A11	V22
A12	U21
A13	U22
A14	T22
A15	T21
A16	R22
A17	R20
A18	R21
A19	P22
A20	N22
A21	M22
A22	L22
A23	N21
A24	M21
A25	L21
A26	K20
A27	L20
A28	K22
A29	K21
A30	J22
A31	H22
$\overline{\text{AACK}}$	H12
$\overline{\text{ABB}}$	G12
ALE	K17

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
$\overline{\text{ARTRY}}$	H11
BADDR27	J8
BADDR28	L7
BADDR29	L8
BADDR30	K8
BADDR31	G10
$\overline{\text{BCTL0}}$	G18
$\overline{\text{BCTL1}}$	J18
$\overline{\text{BG}}$	N16
BNKSEL0	G11
BNKSEL1	H10
BNKSEL2	J11
BM0	G11
BM1	H10
BM2	J11
$\overline{\text{BR}}$	P16
CHIP_ID0	B19
CHIP_ID1	C18
CHIP_ID2	C17
CHIP_ID3	D17
CLKIN	J10
CLKOUT	K14
CNFGS	W3
$\overline{\text{CS0}}$	N18
$\overline{\text{CS1}}$	G17
$\overline{\text{CS2}}$	K18
$\overline{\text{CS3}}$	L18
$\overline{\text{CS4}}$	H17
$\overline{\text{CS5}}$	K16
$\overline{\text{CS5}}$	J18
$\overline{\text{CS6}}$	J16
$\overline{\text{CS7}}$	H16
D0	V5
D1	V6
D2	U5

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
D3	U6
D4	V7
D5	V8
D6	U7
D7	V9
D8	U8
D9	U9
D10	V10
D11	U10
D12	V11
D13	V12
D14	U11
D15	U12
D16	T12
D17	U13
D18	V13
D19	U14
D20	V14
D21	T14
D22	U15
D23	T15
D24	V16
D25	U16
D26	U17
D27	V17
D28	U18
D29	V18
D30	T19
D31	U19
D32	W18
D33	W16
D34	Y19
D35	AA19
D36	AB20
D37	Y18

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
D38	AA18
D39	AB19
D40	W14
D41	AB18
D42	AA17
D43	Y14
D44	AB17
D45	AB16
D46	AA15
D47	AB15
D48	AB14
D49	AB13
D50	AB12
D51	Y11
D52	AA11
D53	AB11
D54	AA10
D55	AB10
D56	AB9
D57	AB8
D58	Y8
D59	AA7
D60	Y7
D61	AB7
D62	AB6
D63	AA6
$\overline{\text{DACK1}}$	G21
$\overline{\text{DACK1}}$	T18
$\overline{\text{DACK2}}$	F22
$\overline{\text{DACK2}}$	R19
$\overline{\text{DACK3}}$	T17
$\overline{\text{DACK4}}$	T16
$\overline{\text{DBB}}$	H13
$\overline{\text{DBG}}$	J12
DLLIN	K9

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
$\overline{\text{DONE1}}$	F19
$\overline{\text{DONE2}}$	G22
DP0	P19
DP1	T18
DP2	R19
DP3	R17
DP4	T17
DP5	T16
DP6	R16
DP7	R15
$\overline{\text{DRACK1}}$	F19
$\overline{\text{DRACK2}}$	G22
DREQ1	G19
DREQ1	P19
DREQ2	F18
DREQ2	R17
DREQ3	R16
DREQ4	R15
DSI64	U4
DSISYNC	T4
EE0	D3
EE1	D4
$\overline{\text{EXT\_BG2}}$	T18
$\overline{\text{EXT\_BG3}}$	T16
$\overline{\text{EXT\_BR2}}$	P19
$\overline{\text{EXT\_BR3}}$	R17
$\overline{\text{EXT\_DBG2}}$	R19
$\overline{\text{EXT\_DBG3}}$	T17
$\overline{\text{GBL}}$	R10
GND	B4
GND	B5
GND	B7
GND	B9
GND	B11
GND	B13

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
GND	B15
GND	B17
GND	B22
GND	C2
GND	C8
GND	C10
GND	C12
GND	C14
GND	C15
GND	D5
GND	D9
GND	D11
GND	D13
GND	D21
GND	E8
GND	E10
GND	E12
GND	E14
GND	E15
GND	E17
GND	E18
GND	F7
GND	F11
GND	F13
GND	F15
GND	G20
GND	J6
GND	J14
GND	J20
GND	K10
GND	K11
GND	K12
GND	K13
GND	K19
GND	L9

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
GND	L10
GND	L14
GND	L16
GND	L17
GND	M5
GND	M6
GND	M7
GND	M10
GND	M14
GND	M19
GND	N10
GND	N14
GND	P10
GND	P13
GND	P14
GND	P21
GND	R4
GND	T20
GND	V4
GND	V15
GND	W5
GND	W6
GND	W9
GND	W13
GND	W19
GND	W20
GND	Y9
GND	Y12
GND	Y15
GND	Y17
GND	AA8
GND	AA13
GND	AA16
GND	AB2
GND_{SYN}	P11

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
GPIO0	B19
GPIO1	C18
GPIO2	C17
GPIO3	C20
GPIO4	D19
GPIO5	C21
GPIO6	C22
GPIO7	C19
GPIO8	D22
GPIO9	E19
GPIO10	E21
GPIO11	F20
GPIO12	E22
GPIO13	E20
GPIO14	F21
GPIO15	G19
GPIO16	F19
GPIO17	G21
GPIO18	F18
GPIO19	F22
GPIO20	F17
GPIO21	H19
GPIO22	G22
GPIO23	J19
GPIO24	H18
GPIO25	J21
GPIO26	N20
GPIO27	E6
GPIO28	C6
GPIO29	D17
GPIO30	C16
GPIO31	D16
HA11	L4
HA12	L2
HA13	J5

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
HA14	L3
HA15	K2
HA16	K4
HA17	G6
HA18	J2
HA19	H5
HA20	H2
HA21	K3
HA22	F6
HA23	G5
HA24	G2
HA25	G4
HA26	J3
HA27	G3
HA28	H3
HA29	F5
$\overline{\text{HBCS}}$	N9
$\overline{\text{HBRST}}$	M16
HCID0	E7
HCID1	C7
HCID2	D7
HCID3	D8
HCLKIN	P9
$\overline{\text{HCS}}$	N17
HD0	T5
HD1	T4
HD2	U4
HD3	V2
HD4	W4
HD5	W3
HD6	W2
HD7	Y2
HD8	AB5
HD9	Y5
HD10	AA5

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
HD11	AB4
HD12	AA4
HD13	AB3
HD14	AA3
HD15	Y3
HD16	U2
HD17	T2
HD18	R2
HD19	U3
HD20	P2
HD21	T3
HD22	R5
HD23	P5
HD24	N5
HD25	P4
HD26	N2
HD27	P3
HD28	M2
HD29	N4
HD30	N3
HD31	M3
HD32	W18
HD33	W16
HD34	Y19
HD35	AA19
HD36	AB20
HD37	Y18
HD38	AA18
HD39	AB19
HD40	W14
HD41	AB18
HD42	AA17
HD43	Y14
HD44	AB17
HD45	AB16

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
HD46	AA15
HD47	AB15
HD48	AB14
HD49	AB13
HD50	AB12
HD51	Y11
HD52	AA11
HD53	AB11
HD54	AA10
HD55	AB10
HD56	AB9
HD57	AB8
HD58	Y8
HD59	AA7
HD60	Y7
HD61	AB7
HD62	AB6
HD63	AA6
$\overline{\text{HDBE4}}$	R7
$\overline{\text{HDBE5}}$	T7
$\overline{\text{HDBE6}}$	R6
$\overline{\text{HDBE7}}$	T6
$\overline{\text{HDBS4}}$	R7
$\overline{\text{HDBS5}}$	T7
$\overline{\text{HDBS6}}$	R6
$\overline{\text{HDBS7}}$	T6
HDST0	W11
HDST1	W10
$\overline{\text{HRDE}}$	N15
$\overline{\text{HRDS}}$	N15
$\overline{\text{HRESET}}$	E5
HRW	N15
$\overline{\text{HTA}}$	H14
$\overline{\text{HWBS0}}$	N8
$\overline{\text{HWBS1}}$	P8

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
$\overline{\text{HWBS2}}$	P7
$\overline{\text{HWBS3}}$	P6
$\overline{\text{HWBS4}}$	R7
$\overline{\text{HWBS5}}$	T7
$\overline{\text{HWBS6}}$	R6
$\overline{\text{HWBS7}}$	T6
$\overline{\text{INT\_OUT}}$	G14
$\overline{\text{IRQ1}}$	C20
$\overline{\text{IRQ1}}$	R10
$\overline{\text{IRQ1}}$	T18
$\overline{\text{IRQ2}}$	D19
$\overline{\text{IRQ2}}$	K8
$\overline{\text{IRQ2}}$	R19
$\overline{\text{IRQ3}}$	C21
$\overline{\text{IRQ3}}$	G10
$\overline{\text{IRQ3}}$	R17
$\overline{\text{IRQ4}}$	C22
$\overline{\text{IRQ4}}$	G12
$\overline{\text{IRQ4}}$	T17
$\overline{\text{IRQ5}}$	C19
$\overline{\text{IRQ5}}$	H13
$\overline{\text{IRQ5}}$	L8
$\overline{\text{IRQ5}}$	T16
$\overline{\text{IRQ6}}$	D22
$\overline{\text{IRQ6}}$	R16
$\overline{\text{IRQ7}}$	E19
$\overline{\text{IRQ7}}$	G14
$\overline{\text{IRQ7}}$	R15
$\overline{\text{IRQ8}}$	E21
$\overline{\text{IRQ9}}$	F20
$\overline{\text{IRQ10}}$	E22
$\overline{\text{IRQ11}}$	E20
$\overline{\text{IRQ12}}$	F21
$\overline{\text{IRQ13}}$	J19
$\overline{\text{IRQ14}}$	H18

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
$\overline{\text{IRQ15}}$	J21
MODCK1	V2
MODCK2	W4
$\overline{\text{MWBE4}}$	R7
$\overline{\text{MWBE5}}$	T7
$\overline{\text{MWBE6}}$	R6
$\overline{\text{MWBE7}}$	T6
$\overline{\text{NMI}}$	F4
$\overline{\text{NMI\_OUT}}$	B6
PBPL3	H7
$\overline{\text{PBS0}}$	G7
$\overline{\text{PBS1}}$	K6
$\overline{\text{PBS2}}$	N6
$\overline{\text{PBS3}}$	K5
$\overline{\text{PBS4}}$	R7
$\overline{\text{PBS5}}$	T7
$\overline{\text{PBS6}}$	R6
$\overline{\text{PBS7}}$	T6
PGPL0	J17
PGPL1	N19
PGPL2	K7
PGPL4	H8
PGPL5	J7
$\overline{\text{PGTA}}$	H8
$\overline{\text{POE}}$	K7
$\overline{\text{PORESET}}$	F2
$\overline{\text{PPBS}}$	H8
PSDA10	J17
PSDAMUX	J7
$\overline{\text{PSDCAS}}$	H7
$\overline{\text{PSDDQM0}}$	G7
$\overline{\text{PSDDQM1}}$	K6
$\overline{\text{PSDDQM2}}$	N6
$\overline{\text{PSDDQM3}}$	K5
$\overline{\text{PSDDQM4}}$	R7

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
$\overline{\text{PSDDQM5}}$	T7
$\overline{\text{PSDDQM6}}$	R6
$\overline{\text{PSDDQM7}}$	T6
$\overline{\text{PSDRAS}}$	K7
$\overline{\text{PSDVAL}}$	P18
$\overline{\text{PSDWE}}$	N19
$\overline{\text{PWE0}}$	G7
$\overline{\text{PWE1}}$	K6
$\overline{\text{PWE2}}$	N6
$\overline{\text{PWE3}}$	K5
$\overline{\text{PWE4}}$	R7
$\overline{\text{PWE5}}$	T7
$\overline{\text{PWE6}}$	R6
$\overline{\text{PWE7}}$	T6
PUPMWAIT	H8
$\overline{\text{RSTCONF}}$	F3
$\overline{\text{SRESET}}$	C5
SWTE	T5
$\overline{\text{TA}}$	P15
$\overline{\text{TBST}}$	T10
TC0	G11
TC1	H10
TC2	J11
TCK	E2
TDI	D2
TDM0RCLK	J21
TDM0RDAT	N20
TDM0RSYN	H18
TDM0TCLK	G22
TDM0TDAT	J19
TDM0TSYN	H19
TDM1RCLK	F22
TDM1RDAT	F17
TDM1RSYN	F18
TDM1TCLK	F19

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
TDM1TDAT	G21
TDM1TSYN	G19
TDM2RCLK	E20
TDM2RDAT	F21
TDM2RSYN	E22
TDM2TCLK	E21
TDM2TDAT	F20
TDM2TSYN	E19
TDM3RCLK	C19
TDM3RDAT	D22
TDM3RSYN	C22
TDM3TCLK	D19
TDM3TDAT	C21
TDM3TSYN	C20
TDO	C4
$\overline{\text{TEA}}$	P17
TEST	H6
TIMER0	C18
TIMER1	C17
TIMER2	C16
TIMER3	D16
TMCLK	C16
TMS	E4
$\overline{\text{TRST}}$	E3
$\overline{\text{TS}}$	R18
TSZ0	T8
TSZ1	R8
TSZ2	T9
TSZ3	R9
TT0	R14
TT1	T13
TT2	K16
TT3	J16
TT4	H16
URXD	E6

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
UTXD	C6
V_{CCSYN}	P12
V_{DD}	B8
V_{DD}	B10
V_{DD}	B12
V_{DD}	B14
V_{DD}	B16
V_{DD}	B18
V_{DD}	B20
V_{DD}	B21
V_{DD}	C3
V_{DD}	C9
V_{DD}	C11
V_{DD}	C13
V_{DD}	D10
V_{DD}	D12
V_{DD}	D14
V_{DD}	D15
V_{DD}	E9
V_{DD}	E11
V_{DD}	E13
V_{DD}	E16
V_{DD}	F8
V_{DD}	F9
V_{DD}	F10
V_{DD}	F12
V_{DD}	F14
V_{DD}	F16
V_{DD}	G8
V_{DD}	G9
V_{DD}	G13
V_{DD}	G15
V_{DD}	G16
V_{DD}	H4
V_{DD}	H9

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
V_{DD}	H15
V_{DD}	H20
V_{DD}	J4
V_{DD}	J9
V_{DD}	J13
V_{DD}	J15
V_{DD}	K15
V_{DD}	M8
V_{DD}	R11
V_{DD}	R12
V_{DD}	R13
V_{DD}	T11
V_{DD}	Y6
V_{DD}	AA2
V_{DD}	B3
V_{DD}	AB22
V_{DDH}	D6
V_{DDH}	D18
V_{DDH}	D20
V_{DDH}	H21
V_{DDH}	L5
V_{DDH}	L6
V_{DDH}	L15
V_{DDH}	L19
V_{DDH}	M4
V_{DDH}	M9
V_{DDH}	M15
V_{DDH}	M17
V_{DDH}	M18
V_{DDH}	M20
V_{DDH}	N7
V_{DDH}	P20
V_{DDH}	R3
V_{DDH}	U20
V_{DDH}	V3

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator
V_{DDH}	W7
V_{DDH}	W8
V_{DDH}	W12
V_{DDH}	W15
V_{DDH}	W17
V_{DDH}	Y4
V_{DDH}	Y10
V_{DDH}	Y13
V_{DDH}	Y16
V_{DDH}	Y20
V_{DDH}	AA9
V_{DDH}	AA12
V_{DDH}	AA14
Note: This table lists every signal name. Because many signals are multiplexed, an individual ball designator number may be listed several times.	

Table 3-2. MSC8102 Signal Listing by Ball Designator

Number	Signal Name
B3	V_{DD}
B4	GND
B5	GND
B6	$\overline{\text{NMI\_OUT}}$
B7	GND
B8	V_{DD}
B9	GND
B10	V_{DD}
B11	GND
B12	V_{DD}
B13	GND
B14	V_{DD}
B15	GND
B16	V_{DD}
B17	GND

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
B18	V_{DD}
B19	GPIO0/CHIP_ID0
B20	V_{DD}
B21	V_{DD}
B22	GND
C2	GND
C3	V_{DD}
C4	TDO
C5	$\overline{\text{SRESET}}$
C6	GPIO28/UTXD
C7	HCID1
C8	GND
C9	V_{DD}
C10	GND
C11	V_{DD}
C12	GND
C13	V_{DD}
C14	GND
C15	GND
C16	GPIO30/TIMER2/TMCLK
C17	GPIO2/TIMER1/CHIP_ID2
C18	GPIO1/TIMER0/CHIP_ID1
C19	GPIO7/TDM3RCLK/$\overline{\text{IRQ5}}$
C20	GPIO3/TDM3TSYN/$\overline{\text{IRQ1}}$
C21	GPIO5/TDM3TDAT/$\overline{\text{IRQ3}}$
C22	GPIO6/TDM3RSYN/$\overline{\text{IRQ4}}$
D2	TDI
D3	EE0
D4	EE1
D5	GND
D6	V_{DDH}
D7	HCID2
D8	HCID3
D9	GND
D10	V_{DD}

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
D11	GND
D12	V_{DD}
D13	GND
D14	V_{DD}
D15	V_{DD}
D16	GPIO31/TIMER3
D17	GPIO29/CHIP_ID3
D18	V_{DDH}
D19	GPIO4/TDM3TCLK/$\overline{\text{IRQ2}}$
D20	V_{DDH}
D21	GND
D22	GPIO8/TDM3RDAT/$\overline{\text{IRQ6}}$
E2	TCK
E3	$\overline{\text{TRST}}$
E4	TMS
E5	$\overline{\text{HRESET}}$
E6	GPIO27/URXD
E7	HCID0
E8	GND
E9	V_{DD}
E10	GND
E11	V_{DD}
E12	GND
E13	V_{DD}
E14	GND
E15	GND
E16	V_{DD}
E17	GND
E18	GND
E19	GPIO9/TDM2TSYN/$\overline{\text{IRQ7}}$
E20	GPIO13/TDM2RCLK/$\overline{\text{IRQ11}}$
E21	GPIO10/TDM2TCLK/$\overline{\text{IRQ8}}$
E22	GPIO12/TDM2RSYN/$\overline{\text{IRQ10}}$
F2	$\overline{\text{PORESET}}$
F3	$\overline{\text{RSTCONF}}$

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
F4	$\overline{\text{NMI}}$
F5	HA29
F6	HA22
F7	GND
F8	V_{DD}
F9	V_{DD}
F10	V_{DD}
F11	GND
F12	V_{DD}
F13	GND
F14	V_{DD}
F15	GND
F16	V_{DD}
F17	GPIO20/TDM1RDAT
F18	GPIO18/TDM1RSYN/DREQ2
F19	GPIO16/TDM1TCLK/$\overline{\text{DONE1}}$/$\overline{\text{DRACK1}}$
F20	GPIO11/TDM2TDAT/$\overline{\text{IRQ9}}$
F21	GPIO14/TDM2RDAT/$\overline{\text{IRQ12}}$
F22	GPIO19/TDM1RCLK/$\overline{\text{DACK2}}$
G2	HA24
G3	HA27
G4	HA25
G5	HA23
G6	HA17
G7	$\overline{\text{PWE0}}$/$\overline{\text{PSDDQM0}}$/$\overline{\text{PBS0}}$
G8	V_{DD}
G9	V_{DD}
G10	$\overline{\text{IRQ3}}$/BADDR31
G11	BM0/TC0/BNKSEL0
G12	$\overline{\text{ABB}}$/$\overline{\text{IRQ4}}$
G13	V_{DD}
G14	$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$
G15	V_{DD}
G16	V_{DD}
G17	$\overline{\text{CS1}}$

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
G18	$\overline{\text{BCTL0}}$
G19	GPIO15/TDM1TSYN/DREQ1
G20	GND
G21	GPIO17/TDM1TDAT/$\overline{\text{DACK1}}$
G22	GPIO22/TDM0TCLK/$\overline{\text{DONE2}}$/$\overline{\text{DRACK2}}$
H2	HA20
H3	HA28
H4	V_{DD}
H5	HA19
H6	TEST
H7	$\overline{\text{PSDCAS}}$/PBPL3
H8	$\overline{\text{PGTA}}$/PUPMWAIT/PGPL4/$\overline{\text{PPBS}}$
H9	V_{DD}
H10	BM1/TC1/BNKSEL1
H11	$\overline{\text{ARTRY}}$
H12	$\overline{\text{AACK}}$
H13	$\overline{\text{DBB}}$/$\overline{\text{IRQ5}}$
H14	$\overline{\text{HTA}}$
H15	V_{DD}
H16	TT4/$\overline{\text{CS7}}$
H17	$\overline{\text{CS4}}$
H18	GPIO24/TDM0RSYN/$\overline{\text{IRQ14}}$
H19	GPIO21/TDM0TSYN
H20	V_{DD}
H21	V_{DDH}
H22	A31
J2	HA18
J3	HA26
J4	V_{DD}
J5	HA13
J6	GND
J7	PSDAMUX/PGPL5
J8	BADDR27
J9	V_{DD}
J10	CLKIN

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
J11	BM2/TC2/BNKSEL2
J12	$\overline{\text{DBG}}$
J13	V_{DD}
J14	GND
J15	V_{DD}
J16	TT3/$\overline{\text{CS6}}$
J17	PSDA10/PGPL0
J18	$\overline{\text{BCTL1}}$/$\overline{\text{CS5}}$
J19	GPIO23/TDM0TDAT/$\overline{\text{IRQ13}}$
J20	GND
J21	GPIO25/TDM0RCLK/$\overline{\text{IRQ15}}$
J22	A30
K2	HA15
K3	HA21
K4	HA16
K5	$\overline{\text{PWE3}}$/$\overline{\text{PSDDQM3}}$/$\overline{\text{PBS3}}$
K6	$\overline{\text{PWE1}}$/$\overline{\text{PSDDQM1}}$/$\overline{\text{PBS1}}$
K7	$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2
K8	$\overline{\text{IRQ2}}$/BADDR30
K9	DLLIN
K10	GND
K11	GND
K12	GND
K13	GND
K14	CLKOUT
K15	V_{DD}
K16	TT2/$\overline{\text{CS5}}$
K17	ALE
K18	$\overline{\text{CS2}}$
K19	GND
K20	A26
K21	A29
K22	A28
L2	HA12
L3	HA14

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
L4	HA11
L5	V_{DDH}
L6	V_{DDH}
L7	BADDR28
L8	$\overline{\text{IRQ5}}$/BADDR29
L9	GND
L10	GND
L14	GND
L15	V_{DDH}
L16	GND
L17	GND
L18	$\overline{\text{CS3}}$
L19	V_{DDH}
L20	A27
L21	A25
L22	A22
M2	HD28
M3	HD31
M4	V_{DDH}
M5	GND
M6	GND
M7	GND
M8	V_{DD}
M9	V_{DDH}
M10	GND
M14	GND
M15	V_{DDH}
M16	$\overline{\text{HBRST}}$
M17	V_{DDH}
M18	V_{DDH}
M19	GND
M20	V_{DDH}
M21	A24
M22	A21
N2	HD26

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
N3	HD30
N4	HD29
N5	HD24
N6	$\overline{\text{PWE2}}/\overline{\text{PSDDQM2}}/\overline{\text{PBS2}}$
N7	V_{DDH}
N8	$\overline{\text{HWBS0}}$
N9	$\overline{\text{HBCS}}$
N10	GND
N14	GND
N15	$\overline{\text{HRDS}}$/HRW/$\overline{\text{HRDE}}$
N16	$\overline{\text{BG}}$
N17	$\overline{\text{HCS}}$
N18	$\overline{\text{CS0}}$
N19	$\overline{\text{PSDWE}}$/PGPL1
N20	GPIO26/TDM0RDAT
N21	A23
N22	A20
P2	HD20
P3	HD27
P4	HD25
P5	HD23
P6	$\overline{\text{HWBS3}}$
P7	$\overline{\text{HWBS2}}$
P8	$\overline{\text{HWBS1}}$
P9	HCLKIN
P10	GND
P11	GND_{SYN}
P12	V_{CCSYN}
P13	GND
P14	GND
P15	$\overline{\text{TA}}$
P16	$\overline{\text{BR}}$
P17	$\overline{\text{TEA}}$
P18	$\overline{\text{PSDVAL}}$
P19	DP0/DREQ1/$\overline{\text{EXT\_BR2}}$

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
P20	V_{DDH}
P21	GND
P22	A19
R2	HD18
R3	V_{DDH}
R4	GND
R5	HD22
R6	$\overline{\text{HWBS6}}$/$\overline{\text{HDBS6}}$/$\overline{\text{MWBE6}}$/$\overline{\text{HDBE6}}$/$\overline{\text{PWE6}}$/ $\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
R7	$\overline{\text{HWBS4}}$/$\overline{\text{HDBS4}}$/$\overline{\text{MWBE4}}$/$\overline{\text{HDBE4}}$/$\overline{\text{PWE4}}$/ $\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
R8	TSZ1
R9	TSZ3
R10	$\overline{\text{IRQ1}}$/$\overline{\text{GBL}}$
R11	V_{DD}
R12	V_{DD}
R13	V_{DD}
R14	TT0
R15	$\overline{\text{IRQ7}}$/DP7/DREQ4
R16	$\overline{\text{IRQ6}}$/DP6/DREQ3
R17	$\overline{\text{IRQ3}}$/DP3/DREQ2/$\overline{\text{EXT\_BR3}}$
R18	$\overline{\text{TS}}$
R19	$\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_DBG2}}$
R20	A17
R21	A18
R22	A16
T2	HD17
T3	HD21
T4	HD1/DSISYNC
T5	HD0/SWTE
T6	$\overline{\text{HWBS7}}$/$\overline{\text{HDBS7}}$/$\overline{\text{MWBE7}}$/$\overline{\text{HDBE7}}$/$\overline{\text{PWE7}}$/ $\overline{\text{PSDDQM7}}$/$\overline{\text{PBS7}}$
T7	$\overline{\text{HWBS5}}$/$\overline{\text{HDBS5}}$/$\overline{\text{MWBE5}}$/$\overline{\text{HDBE5}}$/$\overline{\text{PWE5}}$/ $\overline{\text{PSDDQM5}}$/$\overline{\text{PBS5}}$
T8	TSZ0
T9	TSZ2
T10	$\overline{\text{TBST}}$

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
T11	V_{DD}
T12	D16
T13	TT1
T14	D21
T15	D23
T16	$\overline{\text{IRQ5}}$/DP5/$\overline{\text{DACK4}}$/$\overline{\text{EXT\_BG3}}$
T17	$\overline{\text{IRQ4}}$/DP4/$\overline{\text{DACK3}}$/$\overline{\text{EXT\_DBG3}}$
T18	$\overline{\text{IRQ1}}$/DP1/$\overline{\text{DACK1}}$/$\overline{\text{EXT\_BG2}}$
T19	D30
T20	GND
T21	A15
T22	A14
U2	HD16
U3	HD19
U4	HD2/DSI64
U5	D2
U6	D3
U7	D6
U8	D8
U9	D9
U10	D11
U11	D14
U12	D15
U13	D17
U14	D19
U15	D22
U16	D25
U17	D26
U18	D28
U19	D31
U20	V_{DDH}
U21	A12
U22	A13
V2	HD3/MODCK1
V3	V_{DDH}

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
V4	GND
V5	D0
V6	D1
V7	D4
V8	D5
V9	D7
V10	D10
V11	D12
V12	D13
V13	D18
V14	D20
V15	GND
V16	D24
V17	D27
V18	D29
V19	A8
V20	A9
V21	A10
V22	A11
W2	HD6
W3	HD5/CNFGS
W4	HD4/MODCK2
W5	GND
W6	GND
W7	V_{DDH}
W8	V_{DDH}
W9	GND
W10	HDST1
W11	HDST0
W12	V_{DDH}
W13	GND
W14	HD40/D40
W15	V_{DDH}
W16	HD33/D33
W17	V_{DDH}

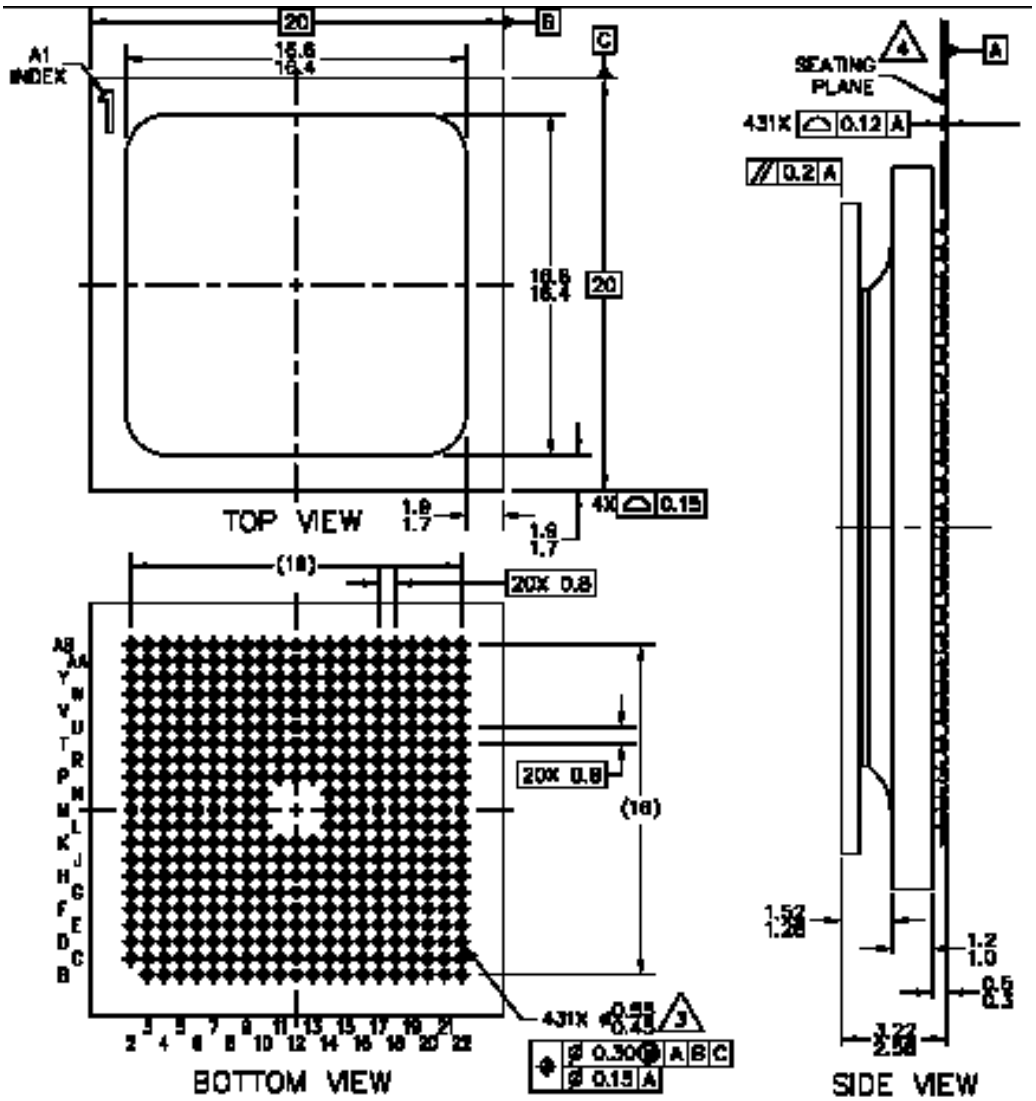
Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
W18	HD32/D32
W19	GND
W20	GND
W21	A7
W22	A6
Y2	HD7
Y3	HD15
Y4	V_{DDH}
Y5	HD9
Y6	V_{DD}
Y7	HD60/D60
Y8	HD58/D58
Y9	GND
Y10	V_{DDH}
Y11	HD51/D51
Y12	GND
Y13	V_{DDH}
Y14	HD43/D43
Y15	GND
Y16	V_{DDH}
Y17	GND
Y18	HD37/D37
Y19	HD34/D34
Y20	V_{DDH}
Y21	A4
Y22	A5
AA2	V_{DD}
AA3	HD14
AA4	HD12
AA5	HD10
AA6	HD63/D63
AA7	HD59/D59
AA8	GND
AA9	V_{DDH}
AA10	HD54/D54

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Number	Signal Name
AA11	HD52/D52
AA12	V_{DDH}
AA13	GND
AA14	V_{DDH}
AA15	HD46/D46
AA16	GND
AA17	HD42/D42
AA18	HD38/D38
AA19	HD35/D35
AA20	A0
AA21	A2
AA22	A3
AB2	GND
AB3	HD13
AB4	HD11
AB5	HD8
AB6	HD62/D62
AB7	HD61/D61
AB8	HD57/D57
AB9	HD56/D56
AB10	HD55/D55
AB11	HD53/D53
AB12	HD50/D50
AB13	HD49/D49
AB14	HD48/D48
AB15	HD47/D47
AB16	HD45/D45
AB17	HD44/D44
AB18	HD41/D41
AB19	HD39/D39
AB20	HD36/D36
AB21	A1
AB22	V_{DD}

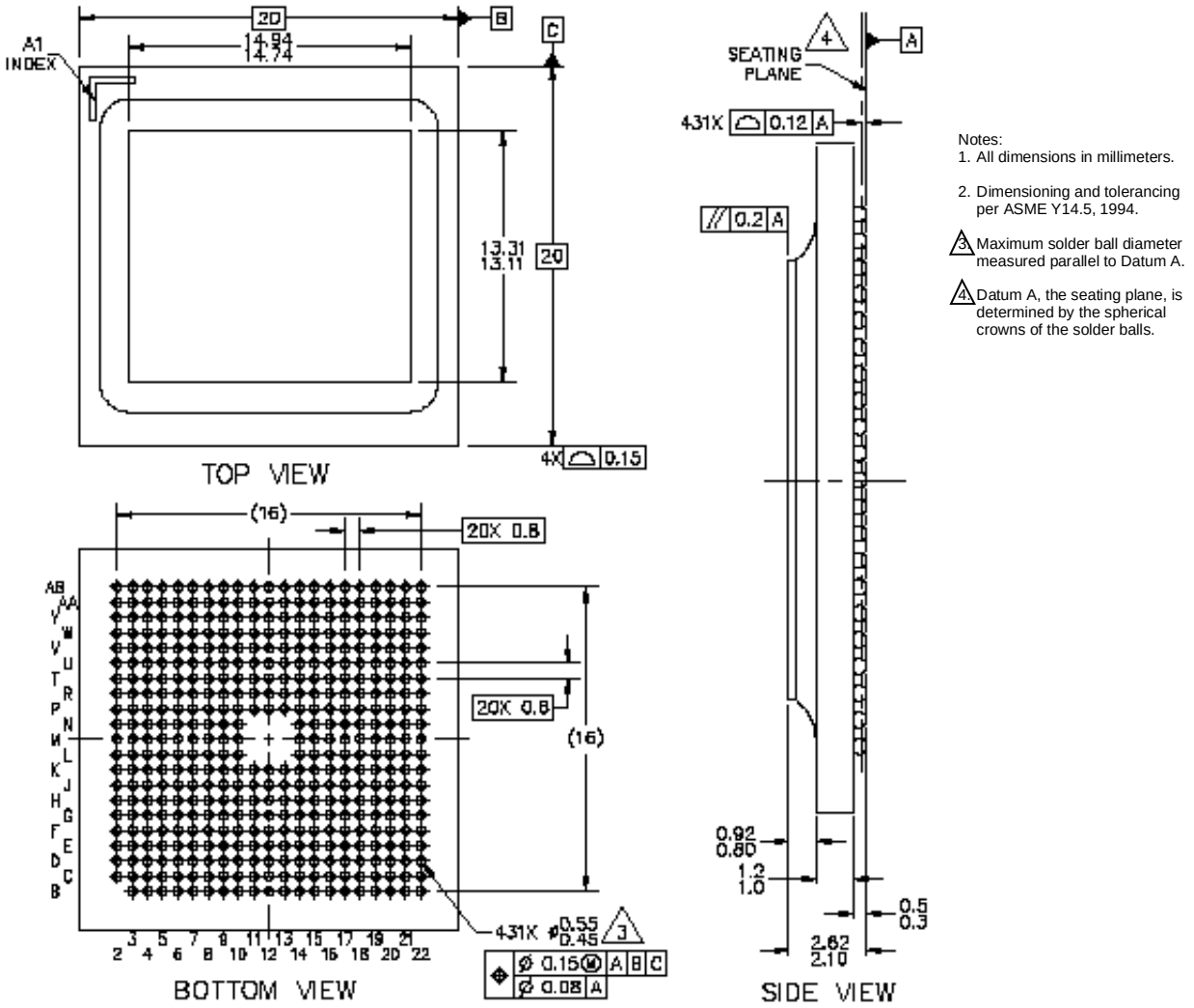
3.3 FC-CBGA (HCTE) Package Mechanical Drawing



CASE 1453-02

Figure 3-3. MSC8102 Mechanical Information, 431-pin FC-CBGA (HCTE) Package

3.4 FC-PBGA Package Mechanical Drawing



CASE 1385-01

Figure 3-4. MSC8102 Mechanical Information, 431-pin FC-PBGA Package

Note: This package is used for pre-production MSC8102 devices only. The package may include a copper lid. Addition of the copper lid increases the overall package height to 2.58–3.22 mm, the same as the FC-CGBA (HCTE) package shown in **Figure 3-3**.

Chapter 4

Design Considerations

4.1 Thermal Design Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

Equation 1: $\mathbf{T_J = T_A + (P_D \bullet \theta_{JA})}$

where

- T_A = ambient temperature °C
- θ_{JA} = package thermal resistance, junction to ambient, °C/W
- $P_D = P_{INT} + P_{I/O}$ in W
- $P_{INT} = I_{DD} \times V_{DD}$ in W—chip internal power
- $P_{I/O}$ = power dissipation on output pins in W—user determined

The user should set T_A and P_D such that T_J does not exceed the maximum operating conditions. In case T_J is too high, the user should either lower the ambient temperature or the power dissipation of the chip.

4.2 Power Supply Design Considerations

The input voltage must not exceed the I/O supply V_{DDH} by more than 2.5 V at any time, including during power-on reset. In turn V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 2.6 V at any time, including during power-on reset. V_{DD}/V_{CCSYN} must not exceed V_{DDH} by more than 0.4 V at any time, including during power-on reset. Therefore the recommendation is to use “bootstrap” diodes between the power rails, as shown in **Figure 4-1**.

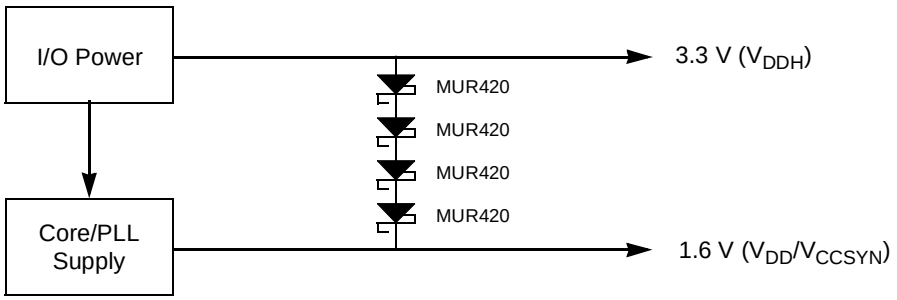


Figure 4-1. Bootstrap Diodes for Power-Up Sequencing

Select the bootstrap diodes such that a nominal V_{DD}/V_{CCSYN} is sourced from the V_{DDH} power supply until the V_{DD}/V_{CCSYN} power supply becomes active. In **Figure 4-1**, four MUR420 Schottky barrier diodes are connected in series; each has a forward voltage (V_F) of 0.6 V at high currents, so these diodes provide a 2.4 V drop, maintaining 0.9 V on the 1.6 V power line. Once the core/PLL power supply stabilizes at 1.6 V, the bootstrap diodes will be reverse biased with negligible leakage current. The V_F should be effective at the current levels required by the processor. Do not use diodes with a nominal V_F that drops too low at high current.

Figure 4-2 shows the recommended power decoupling circuit for the core power supply. The voltage regulator and the decoupling capacitors should supply the required device current without any drop in voltage on the device pins. The voltage on the package pins should not drop below 1.5 V even for a very short spikes. This can be achieved by using the following guidelines:

- For the core supply, use a voltage regulator rated at 1.6 V with nominal rating of at least 3 A.
- Decouple the supply using low-ESR capacitors mounted as close as possible to the socket.

Figure 4-2 shows three capacitors in parallel to reduce the resistance. Three capacitors is a recommended minimum number.

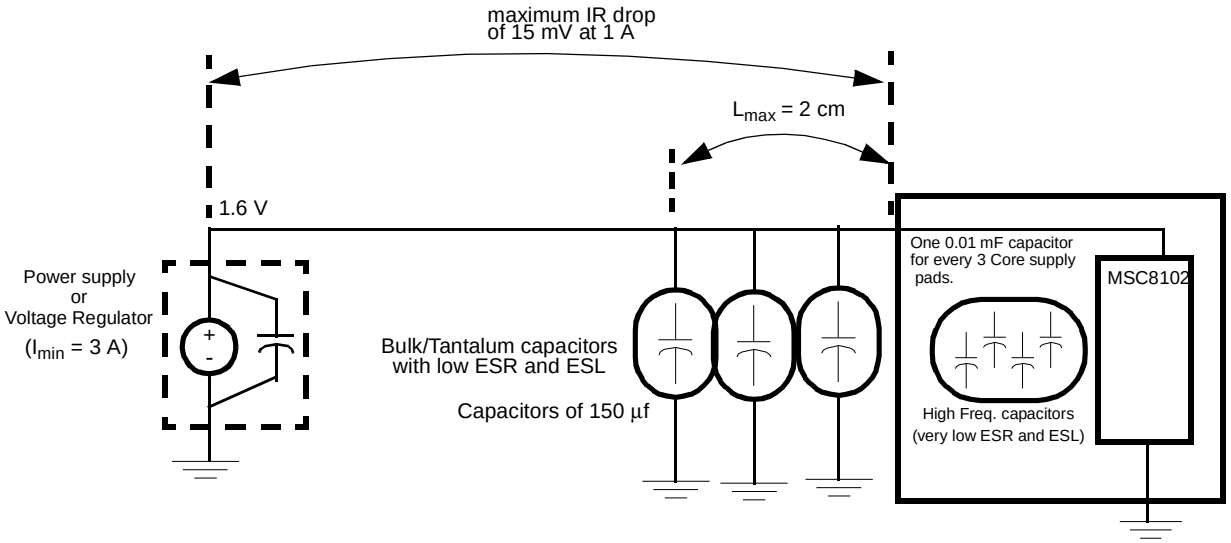


Figure 4-2. Core Power Supply Decoupling

4.3 Connectivity Guidelines

Unused output pins can be disconnected, and unused input pins should be connected to there non-active value, except for the following:

- If the DSI is unused (Bit DDR[1]:DSIDIS is set), then $\overline{\text{HCS}}$ and $\overline{\text{HBCS}}$ must be tied to V_{DD} and all the rest of the DSI signals can be disconnected.
- When the DSI uses Synchronous mode, $\overline{\text{HTA}}$ must be pulled up. In asynchronous mode, $\overline{\text{HTA}}$ should be pulled either up or down depending on design requirements.
- $\overline{\text{HDST}}$ can be disconnected if the DSI is in Big-endian mode, or if the DSI is in Little-endian mode and DCR[7]:DSRFA bit is set.
- When the DSI is in 64-bit Data bus mode and DCR[2]:BEM is cleared, the $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ and $\overline{\text{HWBS[4–7]}}$/$\overline{\text{HDBS[4–7]}}$/$\overline{\text{HWBE[4–7]}}$/$\overline{\text{HDBE[4–7]}}$/$\overline{\text{PWE[4–7]}}$/$\overline{\text{PSDDQM[4–7]}}$/$\overline{\text{PBS[4–7]}}$ must be tied to V_{DD}.
- When the DSI is in 32-bit Data bus mode and DCR[2] (BEM) is cleared, $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ must be tied to V_{DD}.
- When the DSI is in Asynchronous mode, $\overline{\text{HBRST}}$ and HCLKIN should either be disconnected or tied to V_{DD}.
- The following signals can be disconnected in single-master mode (BCR[EBM] is reset): $\overline{\text{BG}}$, $\overline{\text{DBG}}$, $\overline{\text{EXT\_BG[2–3]}}$, $\overline{\text{EXT\_DBG[2-3]}}$, $\overline{\text{GBL}}$ and $\overline{\text{TS}}$.
- The following signals must be pulled up: $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{PSDVAL}}$, and $\overline{\text{AACK}}$.

- In single master mode, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ can be selected as $\overline{\text{IRQ}}$ inputs and be connected to the non-active value. In other modes, they must be pulled up.
- If the 60x-compatible system bus is not used and SIUMCR[PBSE] is set, $\overline{\text{PPBS}}$ can be disconnected. Otherwise, it should be pulled up.
- The following signals: SWTE, DSISYNC, DSI64, MODCK[1–2], and CNFGS are used to configure the MSC8102 and are sampled on the deassertion of the $\overline{\text{PORESET}}$ signal. Therefore, they should be tied to GND or V_{DD} either directly or through a pull-down or a pull-up resistor until the deassertion of the $\overline{\text{PORESET}}$ signal.
- The following signals: CHIPID[0–3], $\overline{\text{RSTCONF}}$ and BM[0–2] are used to configure the MSC8102 and are sampled at the deassertion of the $\overline{\text{PORESET}}$ signal. Therefore, they should be tied to GND or VCC either directly or through a pull-down or a pull-up resistor.
- The $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{DBG}}$, $\overline{\text{EXT\_BR[2–3]}}$, $\overline{\text{EXT\_BG[2–3]}}$, $\overline{\text{EXT\_DBG[2–3]}}$, and $\overline{\text{TS}}$ must be pulled up if the BCR[EBM] bit is set.
- When they are used, $\overline{\text{INT\_OUT}}$ (if SIUMCR[INTODC] is cleared), $\overline{\text{NMI\_OUT}}$, and $\overline{\text{IRQxx}}$ (if not full drive) signals must be pulled up.

Note: For details on configuration, see the MSC8102 *User's Guide* and *MSC8102 Reference Manual*.

4.4 Power Considerations

The internal power dissipation consists of three components:

$$P_{INT} = P_{TCORE} + P_{SIU} + P_{BUSES} + P_{PERIPH}$$

The power dissipation depends on the operating frequency of the different portions of the chip. To determine the power dissipation at a given frequency, the following equations should be applied:

$$P_{CORE}(f_c) = ((P_{CORE} - P_{LCO})/275) \times f_c + P_{LCO}$$
$$P_{TCORE}(f_c) = (P_{CORE} \times 4)$$
$$P_{SIU}(f_c) = ((P_{SIU} - P_{LSI})/91.67) \times f_c + P_{LSI}$$
$$P_{PERIPH}(f_c) = ((P_{PERIPH} - P_{LPE})/91.67) \times f_c + P_{LPE}$$
$$P_{BUSES}(f_c) = P_{BUSES}/91.67 \times f_c$$

Where,

f_c is the operating frequency in MHz and all power numbers are in mW
P_{LCO} is the SC140 Core leakage power
P_{LSI} is the SIU leakage power
P_{LPE} is the peripheral leakage power

To determine a total power dissipation in a specific application, the following equation should be applied for each I/O output pin:

Equation 2: $$P = C \times V_{DDH}^2 \times f_s \times 10^{-3}$$

Where:

P = power in mW
C = load capacitance in pF
f_s = output switching frequency in MHz.

4.5 Layout Practices

Each V_{CC} and V_{DD} pin on the MSC8102 should be provided with a low-impedance path to the board power supply. Similarly, each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MSC8102 have fast rise and fall times. Printed circuit board (PCB) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PCB trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC}, V_{DD}, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

There is one pair of PLL supply pins: V_{CCSYN}-GND_{SYN}. To ensure internal clock stability, filter the power to the V_{CCSYN} input with a circuit similar to the one in **Figure 4-3**. To filter as much noise as possible, place the circuit as close as possible to V_{CCSYN}. The 0.01-µF capacitor should be closest to V_{CCSYN}, followed by the 10-µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to V_{DD}. These traces should be kept short and direct.

GND_{SYN} should be provided with an extremely low impedance path to ground and should be bypassed to V_{CCSYN} by a 0.01-µF capacitor located as close as possible to the chip package. The user should also bypass GND_{SYN} to V_{CCSYN} with a 0.01-µF capacitor as close as possible to the chip package

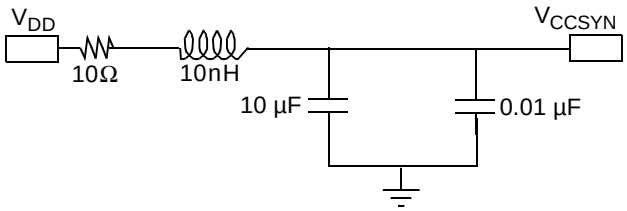


Figure 4-3. V_{CCSYN} Bypass

Ordering Information

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Order Number
MSC8102	1.6 V core 3.3 V I/O	High Temperature Coefficient for Expansion Flip Chip Ceramic Ball Grid Array (FC-CBGA (HCTE))	431	250	TBD
				275	TBD

HOW TO REACH US:

USA / EUROPE / Locations Not Listed:

Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

JAPAN:

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu Minato-ku
Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
852-26668334

HOME PAGE:
http://motorola.com/semiconductors/

MOTOROLA

MSC8102/D, REV. 2