MOTOROLA
Semiconductor Products Sector Technical Data

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MSC8101

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Advance Information

Networking Digital Signal Processor

The Motorola MSC8101 16-bit Digital Signal Processor (DSP) is the first member of the family of DSPs based on the Star*Core™ SC140 DSP core. This very versatile chip integrates the high-performance SC140 four-ALU (Arithmetic Logic Unit) DSP core along with 512 KB of on-chip memory, a Communications Processor Module (CPM), a 64-bit PowerPC™ bus, a very flexible System Integration Unit (SIU), and a 16-channel DMA engine on a single device. With its four-ALU core, the MSC8101 can execute up to four multiply-accumulate (MAC) operations in a single clock cycle. The MSC8101 CPM is a 32-bit RISC-based communications protocol engine that can network to Time-Division Multiplexed (TDM) highways, Ethernet, and Asynchronous Transfer mode (ATM) backbones. The MSC8101 60x-compatible PowerPC bus interface facilitates its connection to multi-master PowerPC-based system architectures. The very large on-chip memory, 512 KB, reduces the need for off-chip program and data memories. The MSC8101 offers 1200 DSP MIPS or 3000 RISC MIPS performance using an internal 300 MHz clock with a 1.5 V core and independent 3.3 V input/output (I/O). MSC8101 power dissipation is estimated at 0.5 W. **Figure 1** shows a block diagram of the MSC8101 processor.

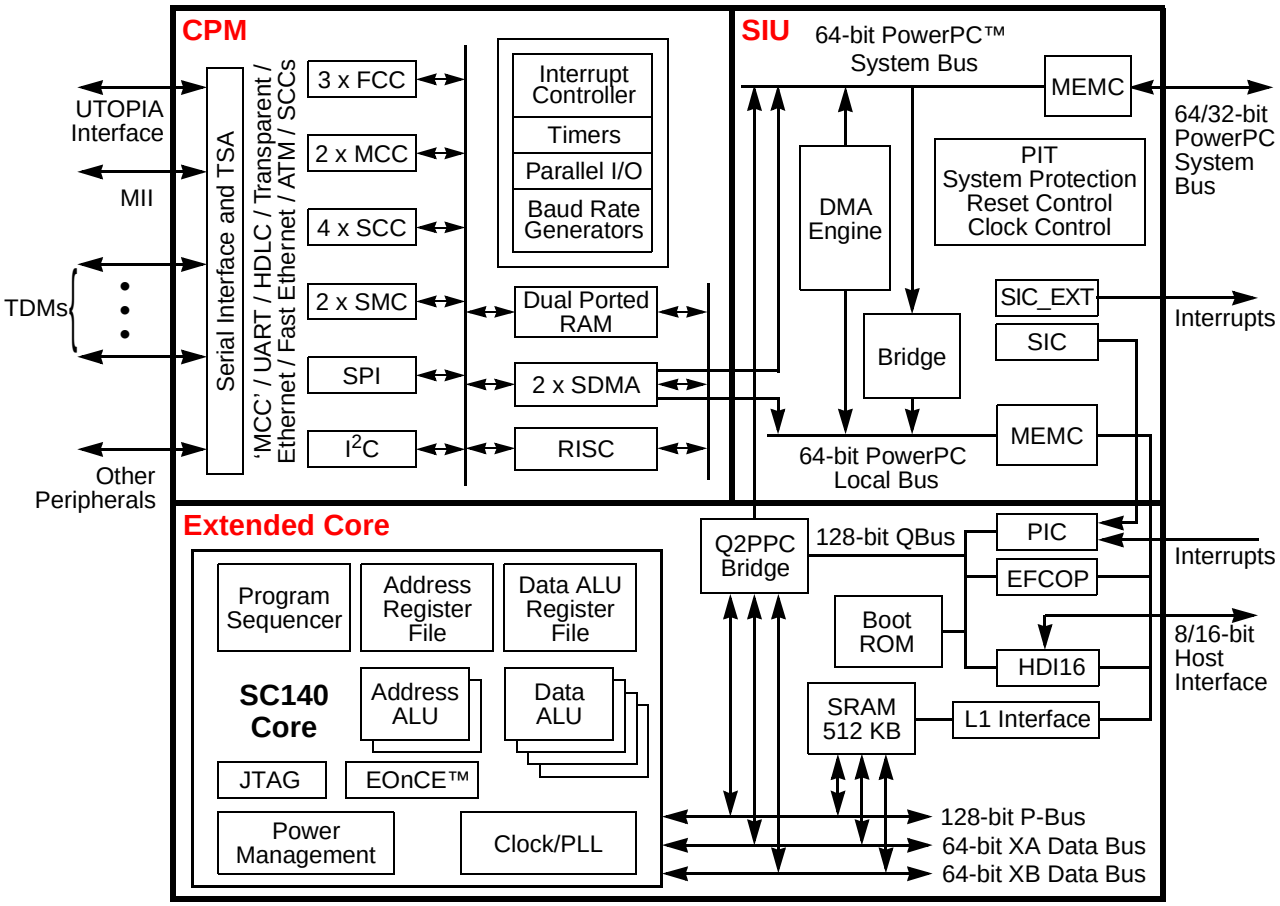


Figure 1. MSC8101 Block Diagram

Contents

Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Indicates a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)			
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low			
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high			
Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

[1]Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

FEATURES

SC140 Core

- Architecture optimized for efficient C/C++ code compilation
- Four 16-bit ALUs and two 32-bit AGUs
- 1200 DSP MIPS, 3000 RISC MIPS, running at 300 MHz
- Very low power dissipation—less than 0.25W for the core running full speed at 1.5 V
- Variable-Length Execution Set (VLES) execution model
- JTAG/Enhanced OnCE debug port

150 MHz Communications Processor Module (CPM)

- Programmable protocol machine using a 32-bit RISC engine
- 155 Mbps ATM interface (including AAL 0/1/2/5)
- 10/100 Mbit Ethernet interface
- Up to four E1/T1 interfaces or one E3/T3 interface and one E1/T1 interface
- HDLC support up to T3 rates, or 256 channels

100 MHz 64- or 32-bit wide PowerPC Bus interface

- Support for bursts for high efficiency
- Glueless interface to PowerPC bus systems
- Multi-master support

Programmable Memory Controller

- Control for up to eight banks of external memory
- User-programmable machines (UPM) allowing glueless interface to various memory types (SRAM, DRAM, EPROM, and Flash memory) and other user-definable peripherals
- Dedicated pipelined SDRAM memory interface

Large On-chip SRAM

- 256K 16-bit words (512 KB)
- Unified program and data space configurable by the application
- Word and byte addressable

DMA controller

- 16 DMA channels, FIFO based, with burst capabilities
- Sophisticated addressing capabilities

Small foot print package

- 17 mm × 17 mm plastic package

Very low power consumption

- Estimated power consumption of 500 mW for the entire device
- Separate power supply for internal logic (1.5 V) and for I/O (3.3 V)

Enhanced Filter Coprocessor (EFCOP)

- Independently and concurrently executes long filters (such as echo cancellation)
- Runs at 300 MHz

Enhanced 16-bit parallel Host Interface (HID16)

- Supports a variety of microcontroller, microprocessor, and DSP bus interfaces

Phase-Lock Loops (PLLs)

- Separate PLLs for SC140 Core, PowerPC bus, and CPM

Process Technology

- First DSP manufactured using Motorola's new copper interconnect process technology 0.13 micron

TARGET APPLICATIONS

The MSC8101 targets applications requiring very high performance, very large amounts of on-chip memory, and such networking capabilities as:

- Third-generation wideband wireless infrastructure systems
- IP Telephony systems
- Multi-channel modem banks
- Multi-channel xDSL

PRODUCT DOCUMENTATION

The three documents listed in the following table, once they are available, will be required for a complete description of the MSC8101 and will be necessary to design properly with the part. Documentation will be available from the following sources (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

Table 1. MSC8101 Documentation

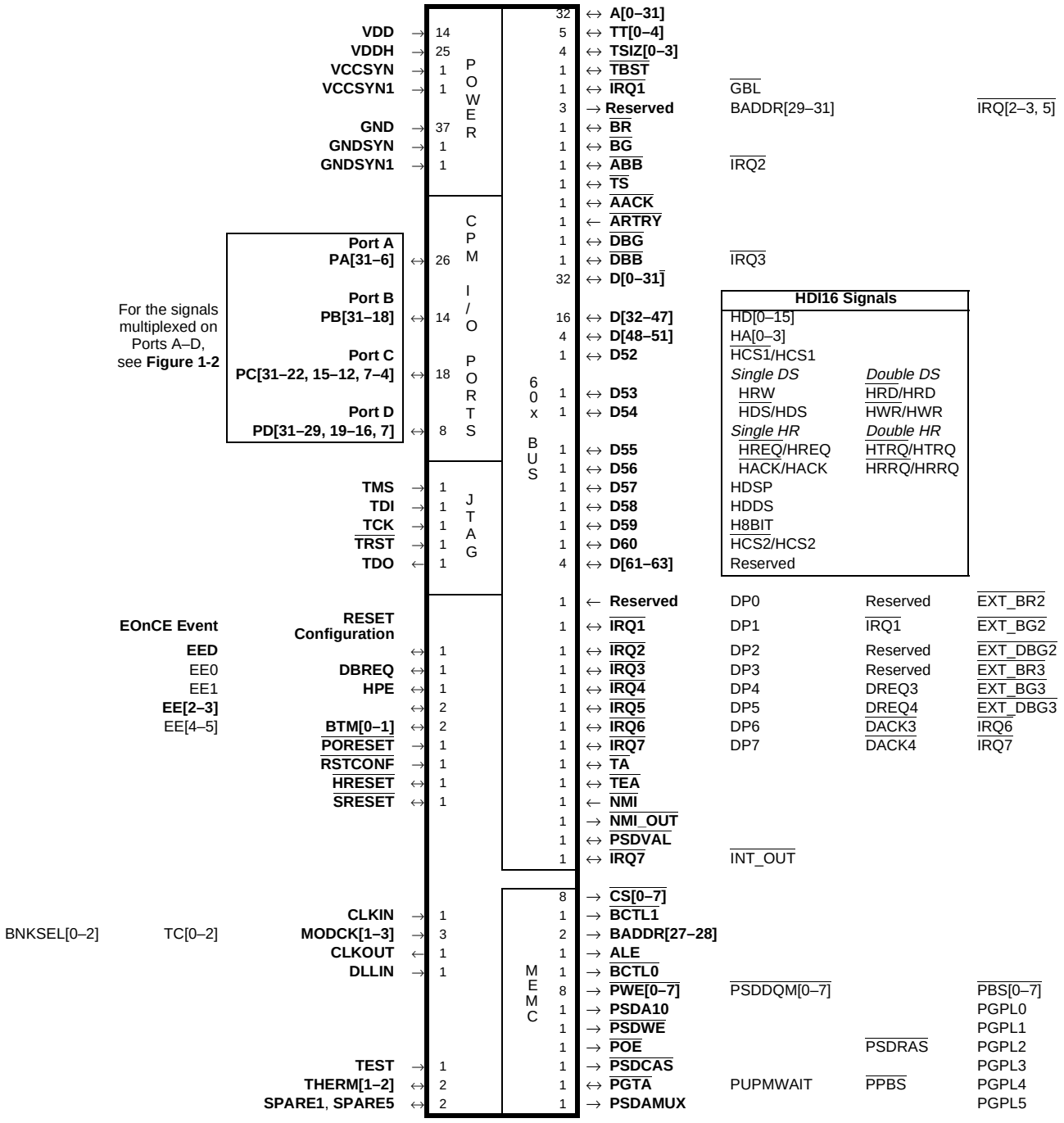
Name	Description	Order Number
SC140 DSP Core Reference Manual	Detailed description of the SC140 family processor core and instruction set	STCRCORERM/AD
MSC8101 Reference Manual	Detailed description of the MSC8101 processor core and instruction set	MSC8101RM/D
MSC8101 User's Guide	Detailed functional description of the MSC8101 memory configuration, operation, and register programming	MSC8101UG/D
MSC8101 Technical Data	MSC8101 features list and physical, electrical, timing, and package specifications	MSC8101/D
MSC8101 Pocket Guide	Quick reference information for application development.	MSC8101PG/D

Chapter 1
Signal/Connection Descriptions

The MSC8101 external signals are organized into functional groups, as shown in **Table 1-1**, **Figure 1-1**, and **Figure 1-2**. **Table 1-1** lists the functional groups, the number of signal connections in each group, and references the table that gives a detailed listing of multiplexed signals within each group. **Figure 1-1** shows MSC8101 external signals organized by function. **Figure 1-2** indicates how the parallel input/output (I/O) ports signals are multiplexed. Because the parallel I/O design supported by the MSC8101 Communications Processor Module (CPM) is a subset of the parallel I/O signals supported by the MPC8260 device, port pins are not numbered sequentially.

Table 1-1. MSC8101 Functional Signal Groupings

Functional Group		Number of Signal Connections	Detailed Description
Power (V_{CC}, V_{DD}, and GND)		80	**Table 1-2** on page 1-4
Clock		6	**Table 1-3** on page 1-5
Reset, Configuration, and EOnCE		11	**Table 1-4** on page 1-6
PowerPC System Bus, HDI16, and Interrupts		133	**Table 1-5** on page 1-8
Memory Controller		27	**Table 1-6** on page 1-16
Communications Processor Module (CPM) Input/Output Parallel Ports	Port A	26	**Table 1-7** on page 1-19
	Port B	14	**Table 1-8** on page 1-28
	Port C	18	**Table 1-9** on page 1-33
	Port D	8	**Table 1-10** on page 1-43
JTAG Test Access Port		5	**Table 1-11** on page 1-48
Reserved (denotes connections that are always reserved)		5	**Table 1-12** on page 1-48



Note: Refer to the *System Interface Unit (SIU)* chapter in the *MCS8101 Reference Manual* for details on how to configure these pins.

Figure 1-1. MSC8101 External Signals

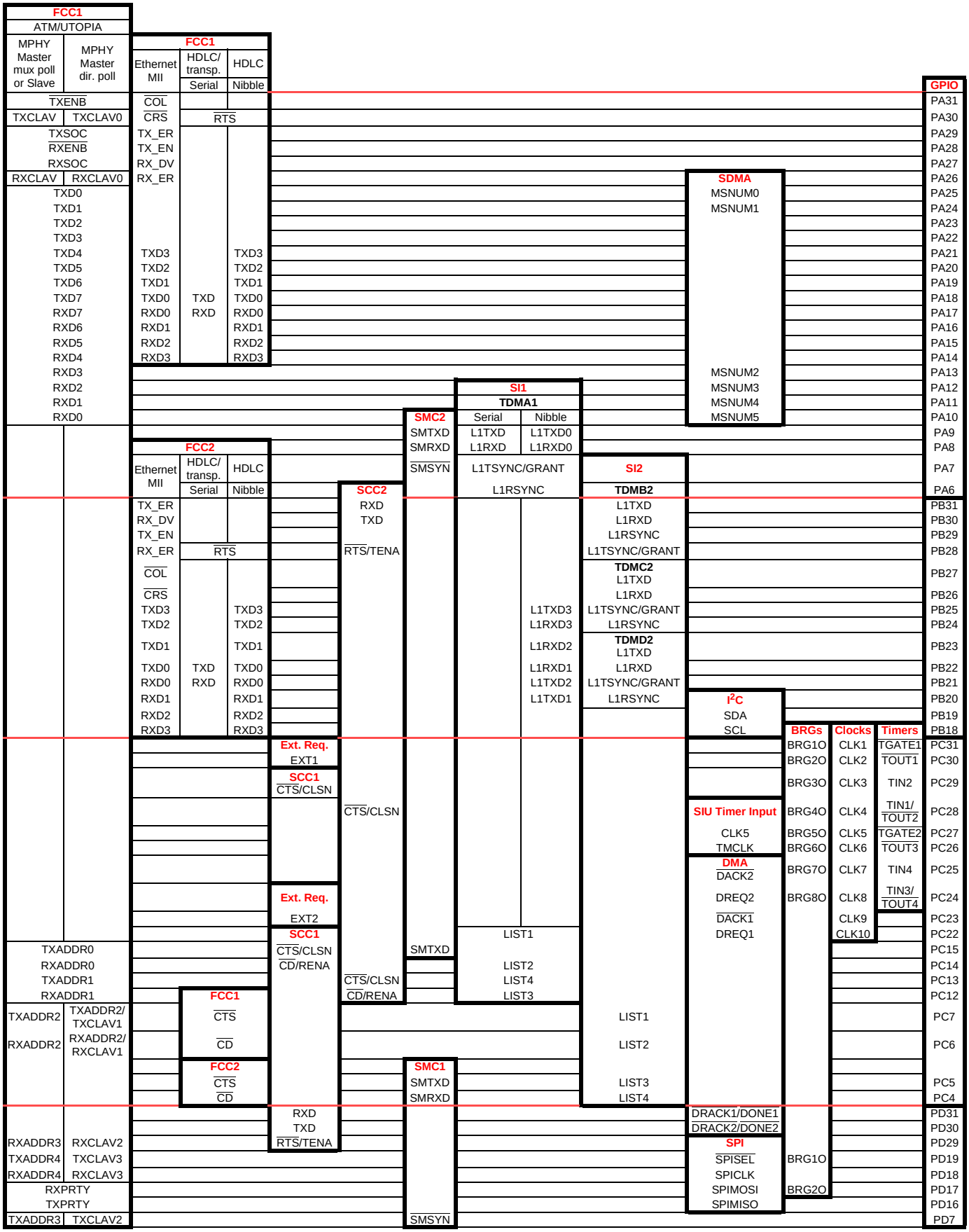


Figure 1-2. CPM Port A–D Pin Multiplexed Functionality

1.1 Power Signals

Table 1-2. Power and Ground Signal Inputs

Power Name	Description
V_{DD}	**Internal Logic Power** V_{DD} dedicated for use with the device core. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{DD} power rail.
V_{DDH}	**Input/Output Power** This source supplies power for the I/O buffers. The user must provide adequate external decoupling capacitors.
V_{CCSYN}	**System PLL Power** V_{CC} dedicated for use with the system Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
V_{CCSYN1}	**SC140 PLL Power** V_{CC} dedicated for use with the SC140 core PLL. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
GND	**System Ground** An isolated ground for the internal processing logic. This connection must be tied externally to all chip ground connections, except GND_{SYN} and GND_{SYN1}. The user must provide adequate external decoupling capacitors.
GND_{SYN}	**System PLL Ground** Ground dedicated for system PLL use. The connection should be provided with an extremely low-impedance path to ground.
GND_{SYN1}	**SC140 PLL Ground 1** Ground dedicated for SC140 core PLL use. The connection should be provided with an extremely low-impedance path to ground.

1.2 Clock Signals

Table 1-3. Clock Signals

Signal Name	Type	Signal Description
CLKIN	Input	**Clock In** Primary clock input to the MSC8101 PLL.
$\overline{\text{MODCK1}}$	Input	**Clock Mode Input 1** Defines the operating mode of internal clock circuits.
TC0	Output	**Transfer Code 0** Supplies information that can be useful for debugging bus transactions initiated by the MSC8101.
BNKSEL0	Output	**Bank Select 0** Selects the SDRAM bank when the MSC8101 is in PowerPC 60x-compatible bus mode.
$\overline{\text{MODCK2}}$	Input	**Clock Mode Input 2** Defines the operating mode of internal clock circuits.
TC1	Output	**Transfer Code 1** Supplies information that can be useful for debugging bus transactions initiated by the MSC8101.
BNKSEL1	Output	**Bank Select 1** Selects the SDRAM bank when the MSC8101 is in 60x-compatible bus mode.
$\overline{\text{MODCK3}}$	Input	**Clock Mode Input 3** Defines the operating mode of internal clock circuits.
TC2	Output	**Transfer Code 2** Supplies information that can be useful for debugging bus transactions initiated by the MSC8101.
BNKSEL2	Output	**Bank Select 2** Selects the SDRAM bank when the MSC8101 is in 60x-compatible bus mode.
CLKOUT	Output	**Clock Out** The PowerPC bus clock.
DLLIN	Input	**DLLIN** Synchronizes with an external device.

1.3 Reset, Configuration, and EOnCE Event Signals

Table 1-4. Reset, Configuration, and EOnCE Event Signals

Signal Name	Type	Signal Description
DBREQ	Input	**Debug Request** Determines whether to go into SC140 Debug mode when $\overline{\text{PORESET}}$ is deasserted.
EE0[1]		**Enhanced OnCE (EOnCE) Event 0** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE0 as an input (default) or an output.
	Input	Debug request, enable Address Event Detection Channel 0, or generate one of the EOnCE events.
	Output	Detection by Address Event Detection Channel 0. Used to trigger external debugging equipment.
HPE	Input	**Host Port Enable** When this pin is asserted during $\overline{\text{PORESET}}$, the Host port is enabled, the PowerPC data bus is 32 bits wide, and the Host *must* program the reset configuration word.
EE1[1]		**EOnCE Event 1** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE1 as an input (default) or an output.
	Input	Enable Address Event Detection Channel 1 or generate one of the EOnCE events.
	Output	Debug Acknowledge or detection by Address Event Detection Channel 1. Used to trigger external debugging equipment.
EE2[1]		**EOnCE Event 2** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE2 as an input (default) or an output.
	Input	Enable Address Event Detection Channel 2 or generate one of the EOnCE events or enable the Event Counter.
	Output	Detection by Address Event Detection Channel 2. Used to trigger external debugging equipment.
EE3[1]		**EOnCE Event 3** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE3 as an input (default) or an output. See the *Emulation and Debug* chapter in the *SC140 DSP Core Reference Manual* for details on the ERCV Register.
	Input	Enable Address Event Detection Channel 3 or generate one of the EOnCE events.
	Output	EOnCE Receive Register (ERCV) was read by the DSP. Used to trigger external debugging equipment.

Table 1-4. Reset, Configuration, and EOnCE Event Signals (Continued)

Signal Name	Type	Signal Description
BTM[0–1]	Input	**Boot Mode 0–1** Determines the MSC8101 boot mode when $\overline{\text{PORESET}}$ is deasserted. See the *Emulation and Debug* chapter in the *SC140 DSP Core Reference Manual* for details on how to set these pins.
EE4[1]		**EOnCE Event 4** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE4 as an input (default) or an output. See the *Emulation and Debug* chapter in the *SC140 DSP Core Reference Manual* for details on the ETRSMT Register.
	Input	Enable Address Event Detection Channel 4 or generate one of the EOnCE events
	Output	EOnCE Transmit Register (ETRSMT) was written by the DSP. Used to trigger external debugging equipment.
EE5[1]		**EOnCE Event 5** After $\overline{\text{PORESET}}$ is deasserted, you can configure EE5 as an input (default) or an output.
	Input	Enable Address Event Detection Channel 5.
	Output	Detection by Address Event Detection Channel 5. Used to trigger external debugging equipment.
EED[1]		**Enhanced OnCE (EOnCE) Event Detection** After $\overline{\text{PORESET}}$ is deasserted, you can configure EED as an input (default) or output:
	Input	Enable the Data Event Detection Channel.
	Output	Detection by the Data Event Detection Channel. Used to trigger external debugging equipment.
$\overline{\text{PORESET}}$	Input	**Power-On Reset** When asserted, this line causes the MSC8101 to enter power-on reset state.
$\overline{\text{RSTCONF}}$	Input	**Reset Configuration** Used during reset configuration sequence of the chip. A detailed explanation of its function is provided in the “Power-On Reset Flow” and “Hardware Reset Configuration” sections of the MSC8101 *Reference Manual*.
$\overline{\text{HRESET}}$	Input	**Hard Reset** When asserted, this open-drain line causes the MSC8101 to enter hard reset state.
$\overline{\text{SRESET}}$	Input	**Soft Reset** When asserted, this open-drain line causes the MSC8101 to enter soft reset state.

Note 1: See the *Emulation and Debug* chapter in the *SC140 DSP Core Reference Manual* for details on how to configure these pins.

1.4 PowerPC System Bus, HDI16, and Interrupt Signals

The PowerPC System Bus, HDI16, and Interrupt signals are grouped together because they use a common set of signal lines. Individual assignment of a signal to a specific signal line is configured through registers in the System Interface Unit (SIU) and the Host Interface (HDI16). Table 1-5 describes the signals in this group.

Note: To boot from the host interface, the HDI16 must be enabled by pulling up the HPE signal line during $\overline{\text{PORESET}}$. If the HPE signal is pulled up, the configuration word must then be loaded from the host. The configuration word must set the Internal Space Port Size bit in the Bus Control Register (BCR[ISPS]) to change the PowerPC system data bus width from 64 bits to 32 bits and reassign the upper 32 bits to their HDI16 functions. Never set the Host Port Enable (HEN) bit in the Host Port Control Register (HPCR) to enable the HDI16, unless the bus size is first changed from 64 bits to 32 bits by setting the BCR[ISPS] bit. Otherwise, unpredictable operation may occur.

Although there are eight interrupt request (IRQ) connections to the core processor, there are multiple external lines that can connect to these internal signal lines. After reset, the default configuration includes two $\overline{\text{IRQ1}}$ and two $\overline{\text{IRQ7}}$ input lines. The designer must select one line for each required interrupt and reconfigure the other external signal line or lines for alternate functions.

Table 1-5. PowerPC System Bus, HDI16, and Interrupt Signals

Signal	Data Flow	Description
A[0–31]	Input/Output	**Address Bus** When the MSC8101 is in external master bus mode, these pins function as the address bus. The MSC8101 drives the address of its internal bus masters and responds to addresses generated by external bus masters. When the MSC8101 is in Internal Master Bus mode, these pins are used as address lines connected to memory devices and are controlled by the MSC8101 memory controller.
TT[0–4]	Input/Output	**Bus Transfer Type** The bus master drives these pins during the address tenure to specify the type of transaction.
TSIZ[0–3]	Input/Output	**Transfer Size** The bus master drives these pins with a value indicating the number of bytes transferred in the current transaction.
$\overline{\text{TBST}}$	Input/Output	**Bus Transfer Burst** The bus master asserts this pin to indicate that the current transaction is a burst transaction (transfers four quad words).
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{GBL}}$	Input/Output	**Global**[1] When a master within the chip initiates a bus transaction, it drives this pin. When an external master initiates a bus transaction, it should drive this pin. Assertion of this pin indicates that the transfer is global and it should be snooped by caches in the system.

Table 1-5. PowerPC System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
Reserved	Output	The primary configuration is reserved.
BADDR29	Output	**Burst Address 29**[1] One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
Reserved	Output	The primary configuration is reserved.
BADDR30	Output	**Burst Address 30**[1] One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
Reserved	Output	The primary configuration is reserved.
BADDR31	Output	**Burst Address 31**[1] One of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{BR}}$	Input/Output Output	**Bus Request**[2] An output when an external arbiter is used. The MSC8101 asserts this pin to request ownership of the bus.
	Input	An input when an internal arbiter is used. An external master should assert this pin to request bus ownership from the internal arbiter.
$\overline{\text{BG}}$	Input/Output Output	**Bus Grant**[2] An output when an internal arbiter is used. The MSC8101 asserts this pin to grant bus ownership to an external PowerPC bus master.
	Input	An input when an external arbiter is used. The external arbiter should assert this pin to grant bus ownership to the MSC8101.
$\overline{\text{ABB}}$	Input/Output Output	**Address Bus Busy**[1] The MSC8101 asserts this pin for the duration of the address bus tenure. Following an address acknowledge ($\overline{\text{AACK}}$) signal, which terminates the address bus tenure, the MSC8101 negates $\overline{\text{ABB}}$ for a fraction of a bus cycle and then stops driving this pin.
	Input	The MSC8101 does not assume bus ownership as long as it senses that this pin is asserted by an external bus master.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2**[1] One of the eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-5. PowerPC System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
$\overline{TS}$	Input/Output	**Bus Transfer Start** Signals the beginning of a new address bus tenure. The MSC8101 asserts this signal when one of its internal bus masters (SC140 core or DMA) begins an address tenure. When the MSC8101 senses this pin being asserted by an external bus master, it responds to the address bus tenure as required (snoop if enabled, access internal MSC8101 resources, memory controller support).
$\overline{AACK}$	Input/Output	**Address Acknowledge** A bus slave asserts this signal to indicate that it identified the address tenure. Assertion of this signal terminates the address tenure.
$\overline{ARTRY}$	Input	**Address Retry** Assertion of this signal indicates that the bus transaction should be retried by the bus master. The MSC8101 asserts this signal to enforce data coherency with its internal cache and to prevent deadlock situations.
$\overline{DBG}$	Input/Output Output Input	**Data Bus Grant**[2] An output when an internal arbiter is used. The MSC8101 asserts this pin as an output to grant data bus ownership to an external PowerPC bus master. An input when an external arbiter is used. The external arbiter should assert this pin as an input to grant data bus ownership to the MSC8101.
$\overline{DBB}$	Input/Output Output Input	**Data Bus Busy**[1] The MSC8101 asserts this pin as an output for the duration of the data bus tenure. Following a $\overline{TA}$, which terminates the data bus tenure, the MSC8101 negates $\overline{DBB}$ for a fraction of a bus cycle and then stops driving this pin. The MSC8101 does not assume data bus ownership as long as it senses $\overline{DBB}$ is asserted by an external bus master.
$\overline{IRQ3}$	Input	**Interrupt Request 3**[1] One of the eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
D[0–31]	Input/Output	**Data Bus Most Significant Word** In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus. In Host Port Disabled mode, these 32 bits are part of the 64-bit PowerPC data bus. In Host Port Enabled mode, these bits are used as the PowerPC bus in 32-bit mode.
D[32–47]	Input/Output	**Data Bus Bits 32–47** In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus.
HD[0–15]	Input/Output	**Host Data**[2] When the HDI16 interface is enabled, these signals are lines 0-15 of the bidirectional tri-state data bus.
D[48–51]	Input/Output	**Data Bus Bits 48–51** In write transactions the bus master drives the valid data on these pins. In read transactions the slave drives the valid data on these pins.
HA[0–3]	Input	**Host Address Line 0–3**[3] When the HDI16 interface bus is enabled, these lines address internal host registers.

Table 1-5. PowerPC System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
D52	Input/Output	**Data Bus Bit 52** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
HCS1/HCS1	Input	**Host Chip Select**[3] When the HDI16 interface is enabled, this is one of the two chip-select pins. The polarity of this pin is programmable. The HDI16 chip select is a logical OR of HCS1/HCS1 and HCS2/HCS2 with appropriate polarity.
D53	Input/Output	**Data Bus Bit 53** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
HRW	Input	**Host Read Write Select**[3] When the HDI16 interface is enabled in Single Strobe mode, this is the read/write input (HRW).
HRD/HRD	Input	**Host Read Strobe**[3] When the HDI16 is programmed to interface with a double data strobe host bus, this pin is the read data strobe Schmitt trigger input (HRD/HRD). The polarity of the data strobe is programmable.
D54	Input/Output	**Data Bus Bit 54** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
HDS/HDS	Input	**Host Data Strobe**[3] When the HDI16 is programmed to interface with a single data strobe host bus, this pin is the data strobe Schmitt trigger input (HDS/HDS). The polarity of the data strobe is programmable.
HWR/HWR	Input	**Host Write Data Strobe**[3] When the HDI16 is programmed to interface with a double data strobe host bus, this pin is the write data strobe Schmitt trigger input (HWR/HWR). The polarity of the data strobe is programmable.
D55	Input/Output	**Data Bus Bit 55** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
HREQ/HREQ	Output	**Host Request**[3] When the HDI16 is programmed to interface with a single host request host bus, this pin is the host request output (HREQ/HREQ). The polarity of the host request is programmable. The host request may be programmed as a driven or open-drain output.
HTRQ/HTRQ	Output	**Transmit Host Request**[3] When the HDI16 is programmed to interface with a double host request host bus, this pin is the transmit host request output (HTRQ/HTRQ). The signal can be programmed as driven or open drain. The polarity of the host request is programmable.

Table 1-5. PowerPC System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
D56	Input/Output	**Data Bus Bit 56** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
$\overline{\text{HACK}}$/HACK	Output	**Host Acknowledge**[3] When the HDI16 is programmed to interface with a single host request host bus, this pin is the host acknowledge Schmitt trigger input (HACK). The polarity of the host acknowledge is programmable.
$\overline{\text{HRRQ}}$/HRRQ	Output	**Receive Host Request**[3] When the HDI16 is programmed to interface with a double host request host bus, this pin is the receive host request output ($\overline{\text{HRRQ}}$/HRRQ). The signal can be programmed as driven or open drain. The polarity of the host request is programmable.
D57	Input/Output	**Data Bus Bit 57** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
HDSP	Input	**Host Data Strobe Polarity**[3] When the HDI16 interface is enabled, this pin is the host data strobe polarity (HDSP).
D58	Input/Output	**Data Bus Bit 58** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
HDDS	Input	**Host Dual Data Strobe**[3] When the HDI16 interface is enabled, this pin is the host dual data strobe (HDDS).
D59	Input/Output	**Data Bus Bit 59** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
H8BIT	Input	**H8BIT**[3] When the HDI16 interface is enabled, this bit determines if the interface is in 8-bit or 16-bit mode.
D60	Input/Output	**Data Bus Bit 60** In write transactions the bus master drives the valid data on this pin. In read transactions the slave drives the valid data on this pin.
$\overline{\text{HCS2}}$/HCS2	Input	**Host Chip Select** [3] When the HDI16 interface is enabled, this is one of the two chip-select pins. The polarity of this pin is programmable. The HDI16 chip select is a logical OR of $\overline{\text{HCS1}}$/HCS1 and $\overline{\text{HCS2}}$/HCS2 with appropriate polarity.
D[61–63]	Input/Output	**Data Bus Bits 61–63** Used only in PowerPC-only mode. In write transactions the bus master drives the valid data on this bus. In read transactions the slave drives the valid data on this bus.
Reserved		These dedicated signals are reserved when the HDI16 is enabled.[3]

Table 1-5. PowerPC System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
Reserved	Input	The primary configuration is reserved.
DP0	Input/Output	**Data Parity 0**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity zero pin should give odd parity (odd number of ones) on the group of signals that includes data parity 0 and D[0–7].
$\overline{\text{EXT\_BR2}}$	Input	**External PowerPC Bus Request 2**[1,2] An external master asserts this pin to request bus ownership from the internal arbiter.
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP1	Input/Output	**Data Parity 1**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity one pin should give odd parity (odd number of ones) on the group of signals that includes data parity 1 and D[8–15].
$\overline{\text{EXT\_BG2}}$	Output	**External Bus Grant 2**[1,2] The MSC8101 asserts this pin to grant bus ownership to an external PowerPC bus master.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP2	Input/Output	**Data Parity 2**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity two pin should give odd parity (odd number of ones) on the group of signals that includes data parity 2 and D[16–23].
$\overline{\text{EXT\_DBG2}}$	Output	**External Data Bus Grant 2**[1,2] The MSC8101 asserts this pin to grant data bus ownership to an external PowerPC bus master.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP3	Input/Output	**Data Parity 3**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity three pin should give odd parity (odd number of ones) on the group of signals that includes data parity 3 and D[24–31].
$\overline{\text{EXT\_BR3}}$	Input	**External PowerPC Bus Request 3**[1,2] An external master asserts this pin to request bus ownership from the internal arbiter.

Table 1-5. PowerPC System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP4	Input/Output	**Data Parity 4**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity four pin should give odd parity (odd number of ones) on the group of signals that includes data parity 4 and D[32–39].
DREQ3	Input	**DMA Request 3**[1] An external peripheral uses this pin to request DMA service.
$\overline{\text{EXT\_BG3}}$	Output	**External PowerPC Bus Grant 3**[1,2] The MSC8101 asserts this pin to grant bus ownership to an external PowerPC bus master.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP5	Input/Output	**Data Parity 5**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity five pin should give odd parity (odd number of ones) on the group of signals that includes data parity 5 and D[40–47].
DREQ4	Input	**DMA Request 4**[1] An external peripheral uses this pin to request DMA service.
$\overline{\text{EXT\_DBG3}}$	Output	**External Data Bus Grant 3**[1,2] The MSC8101 asserts this pin to grant data bus ownership to an external PowerPC bus master.
$\overline{\text{IRQ6}}$	Input	**Interrupt Request 6**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP6	Input/Output	**Data Parity 6**[1] The agent that drives the data bus also drives the data parity signals. The value driven on the data parity six pin should give odd parity (odd number of ones) on the group of signals that includes data parity 6 and D[48–55].
$\overline{\text{DACK3}}$	Output	**DMA Acknowledge 3**[1] The DMA drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP7	Input/Output	**Data Parity 7**[1] The master or slave that drives the data bus also drives the data parity signals. The value driven on the data parity seven pin should give odd parity (odd number of ones) on the group of signals that includes data parity 7 and D[56–63].
$\overline{\text{DACK4}}$	Output	**DMA Acknowledge**[1] The DMA drives this output to acknowledge the DMA transaction on the bus.

Table 1-5. PowerPC System Bus, HDI16, and Interrupt Signals (Continued)

Signal	Data Flow	Description
$\overline{\text{TA}}$	Input/Output	**Transfer Acknowledge** Indicates that a data beat is valid on the data bus. For single beat transfers, assertion of $\overline{\text{TA}}$ indicates the termination of the transfer. For burst transfers, $\overline{\text{TA}}$ is asserted four times to indicate the transfer of four data beats with the last assertion indicating the termination of the burst transfer.
$\overline{\text{TEA}}$	Input/Output	**Transfer Error Acknowledge** Indicates a bus error. masters within the MSC8101 monitor the state of this pin. The MSC8101 internal PowerPC bus monitor can assert this pin if it identifies a bus transfer that is hung.
$\overline{\text{NMI}}$	Input	**Non-Maskable Interrupt** When an external device asserts this line, the MSC8101 NMI input is asserted.
$\overline{\text{NMI\_OUT}}$	Output	**Non-Maskable Interrupt** Driven from the MSC8101 internal interrupt controller. Assertion of this output indicates that a non-maskable interrupt, pending in the MSC8101 internal interrupt controller, is waiting to be handled by an external host.
$\overline{\text{PSDVAL}}$	Input/Output	**Data Valid** Indicates that a data beat is valid on the data bus. The difference between the $\overline{\text{TA}}$ pin and $\overline{\text{PSDVAL}}$ is that the $\overline{\text{TA}}$ pin is asserted to indicate data transfer terminations while the $\overline{\text{PSDVAL}}$ signal is asserted with each data beat movement. Thus, when $\overline{\text{TA}}$ is asserted, $\overline{\text{PSDVAL}}$ is asserted, but when $\overline{\text{PSDVAL}}$ is asserted, $\overline{\text{TA}}$ is not necessarily asserted. For example when the SDMA initiates a double word (2x64 bits) transfer to a memory device that has a 32-bit port size, $\overline{\text{PSDVAL}}$ is asserted three times without $\overline{\text{TA}}$, and finally both pins are asserted to terminate the transfer.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7**[1] One of eight external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{INT\_OUT}}$	Output	**Interrupt Output**[1] Driven from the MSC8101 internal interrupt controller. Assertion of this output indicates that an unmasked interrupt is pending in the MSC8101 internal interrupt controller.

Note: 1. See the *System Interface Unit (SIU)* chapter in the *MCS8101 Reference Manual* for details on how to configure these pins.

2. When used as the bus control arbiter for the PowerPC bus, the MSC8101 can support up to three external bus masters. Each master uses its own set of Bus Request, Bus Grant, and Data Bus Grant signals ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$, EXT_$\overline{\text{BR2}}$/EXT_$\overline{\text{BG2}}$/EXT_$\overline{\text{DBG2}}$, and EXT_$\overline{\text{BR3}}$/EXT_$\overline{\text{BG3}}$/EXT_$\overline{\text{DBG3}}$). Each of these signal sets must be configured to indicate whether the external master is or is not a MSC8101 master device. See the Bus Configuration Register (BCR) description in the *System Interface Unit (SIU)* chapter in the *MCS8101 Reference Manual* for details on how to configure these pins. The second and third set of pins is defined by EXT_xxx to indicate that they can only be used with external master devices. The first set of pins ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$) have a dual function. When the MSC8101 is not the bus arbiter, these signals ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$) are used by the MSC8101 to obtain master control of the bus.

3. See the *Host Interface (HDI16)* chapter in the *MCS8101 Reference Manual* for details on how to configure these pins.

1.5 Memory Controller Signals

Refer to the *Memory Controller* chapter in the *MSC8101 Technical Reference Manual* for detailed information about configuring these signals.

Table 1-6. Memory Controller Signals

Signal	Data Flow	Description
$\overline{\text{CS}}$[0–7]	Output	**Chip Select** Enable specific memory devices or peripherals connected to MSC8101 buses.
$\overline{\text{BCTL1}}$	Output	**Buffer Control 1** Controls buffers on the data bus. Usually used with $\overline{\text{BCTL0}}$. The exact function of this pin is defined by the value of SIUMCR[BCTLC]. See the *System Interface Unit (SIU)* chapter in the *MS8101 Technical Reference* manual for details.
BADDR[27–28]	Output	**Burst Address 27–28** Two of five outputs of the memory controller. These pins connect directly to memory devices controlled by the MSC8101 memory controller.
ALE	Output	**Address Latch Enable** Controls the external address latch used in external master bus configuration.
$\overline{\text{BCTL0}}$	Output	**Buffer Control 0** Controls buffers on the data bus. The exact function of this pin is defined by the value of SIUMCR[BCTLC]. See the *System Interface Unit (SIU)* chapter in the *MS8101 Technical Reference* manual for details.
$\overline{\text{PWE}}$[0–7]	Output	**Bus Write Enable** Outputs of the bus General-Purpose Chip-select Machine (GPCM). These pins select byte lanes for write operations.
$\overline{\text{PSDDQM}}$[0–7]	Output	**Bus SDRAM DQM** Outputs of the SDRAM control machine. These pins select specific byte lanes of SDRAM devices.
$\overline{\text{PBS}}$[0–7]	Output	**Bus UPM Byte Select** Outputs of the User-Programmable Machine (UPM) in the memory controller. These pins select specific byte lanes during memory operations. The timing of these pins is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.
PSDA10	Output	**Bus SDRAM A10** Output from the bus SDRAM controller. This pin is part of the address when a row address is driven. It is part of the command when a column address is driven.
PGPL0	Output	**Bus UPM General-Purpose Line 0** One of six general-purpose output lines of the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PSDWE}}$	Output	**Bus SDRAM Write Enable** Output from the bus SDRAM controller. This pin should connect to the SDRAM WE input signal.
PGPL1	Output	**Bus UPM General-Purpose Line 1** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.

Table 1-6. Memory Controller Signals (Continued)

Signal	Data Flow	Description
$\overline{\text{POE}}$	Output	**Bus Output Enable** Output of the bus GPCM. Controls the output buffer of memory devices during read operations.
$\overline{\text{PSDRAS}}$	Output	**Bus SDRAM RAS** Output from the bus SDRAM controller. This pin should connect to the SDRAM Row Address Strobe (RAS) input signal.
PGPL2	Output	**Bus UPM General-Purpose Line 2** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PSDCAS}}$	Output	**Bus SDRAM CAS** Output from the bus SDRAM controller. This pin should connect to the SDRAM Column Address Strobe (CAS) input signal.
PGPL3	Output	**Bus UPM General-Purpose Line 3** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
$\overline{\text{PGTA}}$	Input	**GPCM TA** Terminates transactions during GPCM operation. Requires an external pull up resistor for proper operation.
PUPMWAIT	Input	**Bus UPM Wait** Input to the UPM. An external device can hold this pin high to force the UPM to wait until the device is ready for the operation to continue.
$\overline{\text{PPBS}}$	Output	**Bus Parity Byte Select** In systems in which data parity is stored in a separate chip, this output is the byte-select for that chip.
PGPL4	Output	**Bus UPM General-Purpose Line 4** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
PSDAMUX	Output	**Bus SDRAM Address Multiplexer** Controls the SDRAM address multiplexer when the MSC8101 is in External Master mode.
PGPL5	Output	**Bus UPM General-Purpose Line 5** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.

1.6 Communications Processor Module (CPM) Ports

The MSC8101 Communications Processor Module (CPM) supports a subset of signals included in the MPC8260. The following sections describe the functionality of the signals in the MSC8101.

The MSC8101 CPM includes the following set of communication controllers:

- Two full-duplex Fast Serial Communications Controllers (FCCs) that support:
  - Asynchronous Transfer Mode (ATM) through a UTOPIA 8 interface (FCC1 only)—The MSC8101 can operate as one of the following:
    - UTOPIA slave device
    - UTOPIA multi-PHY master device using direct polling for up to 4 PHY devices
    - UTOPIA multi-PHY master device using multiplex polling that can address up to 31 PHY devices at addresses 0–30 (address 31 is reserved as a null port).
  - IEEE 802.3/Fast Ethernet through a Media-Independent Interface (MII)
  - High-Level Data Link Control (HDLC) Protocol:
    - Serial mode—Transfers data one bit at a time
    - Nibble mode—Transfers data four bits at a time
  - Transparent mode serial operation
- One FCC that operates with the TSA only
- Two Multi-Channel Controllers (MCCs) that together can handle up to 256 HDLC/transparent channels at 64 Kbps each, multiplexed on up to four TDM interfaces
- Two full-duplex serial communications controllers (SCCs) that support the following protocols:
  - IEEE 802.3/Fast Ethernet through a Media-Independent Interface (MII)
  - HDLC Protocol:
    - Serial mode—Transfers data one bit at a time
    - Nibble mode—Transfers data four bits at a time
  - Synchronous Data Link Control (SDLC)
  - LocalTalk (HDLC-based local area network protocol)
  - Universal Asynchronous Receiver/Transmitter (UART)
  - Synchronous UART (1x clock mode)
  - Binary Synchronous (BISYNC) communication
  - Transparent mode serial operation
- Two additional SCCs that operate with the TSA only
- Two full-duplex Serial Management Controllers (SMCs) that support the following protocols:
  - General Circuit Interface (GCI)/Integrated Services Digital Network (ISDN) monitor and C/I channels (TSA only)
  - UART
  - Transparent mode serial operation
- Serial Peripheral Interface (SPI) support for master or slave operation
- Inter-Integrated Circuit (I^2C) bus controller

- Time-Slot Assigner (TSA) that supports multiplexing from any of the SCCs, FCCs, SMCs, and two MCCs onto four time-division multiplexed (TDM) interfaces. The TSA uses two Serial Interfaces (SI1 and SI2). SI1 uses TDMA1 which supports both serial and nibble mode. SI2 does not support nibble mode and includes TDMB2, TDMC2, and TDMD2 which operate only in serial mode.

The individual sets of externals signals associated with a specific protocol and data transfer mode are multiplexed across any or all of the ports, as shown in **Figure 1-2**. The following sections provide detailed descriptions of the signals supported by Ports A–Port D.

1.6.1 Port A Signals

Table 1-7. Port A Signals

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated Signal *Protocol*		
PA31	FCC1: $\overline{\text{TXENB}}$ *UTOPIA master*	Output	**FCC1: UTOPIA Master Transmit Enable** In the ATM UTOPIA interface supported by FCC1, $\overline{\text{TXENB}}$ is asserted by the MSC8101 (UTOPIA master PHY) when there is valid transmit cell data (TXD[0–7]).
	FCC1: $\overline{\text{TXENB}}$ *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Transmit Enable** In the ATM UTOPIA interface supported by FCC1, $\overline{\text{TXENB}}$ is asserted by an external UTOPIA master PHY when there is valid transmit cell data (TXD[0–7]).
	FCC1: $\overline{\text{COL}}$ *MII*	Input	**FCC1: Media Independent Interface Collision Detect** In the MII interface supported by FCC1, $\overline{\text{COL}}$ is asserted by an external fast Ethernet PHY.

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA30	FCC1: TXCLAV *UTOPIA slave*	Output	**FCC1: UTOPIA Slave Transmit Cell Available** In the ATM UTOPIA interface supported by FCC1, TXCLAV is asserted by the MSC8101 (UTOPIA slave PHY) when the MSC8101 can accept one complete ATM cell.
	FCC1: TXCLAV *UTOPIA master*, or	Input	**FCC1: UTOPIA Master Transmit Cell Available** In the ATM UTOPIA interface supported by FCC1, TXCLAV is asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell.
	FCC1: TXCLAV0 *UTOPIA master, Multi-PHY, direct polling*	Input	**FCC1: UTOPIA Master Transmit Cell Available Multi-PHY Direct Polling** In the ATM UTOPIA interface supported by FCC1, TXCLAV0 is asserted by an external UTOPIA slave PHY using direct polling to indicate that it can accept one complete ATM cell.
	FCC1: $\overline{\text{RTS}}$ *HDLC, Serial and Nibble*	Output	**FCC1: Request To Send** In the standard modem interface signals supported by FCC1 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{RTS}}$ is asynchronous with the data. $\overline{\text{RTS}}$ is typically used in conjunction with $\overline{\text{CD}}$. The MSC8101 FCC1 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low.
	FCC1: $\overline{\text{CRS}}$ *MII*	Input	**FCC1: Media Independent Interface Carrier Sense** In the MII interface supported by FCC1. $\overline{\text{CRS}}$ is asserted by an external fast Ethernet PHY. It indicates activity on the cable.
PA29	FCC1: TXSOC *UTOPIA master*	Output	**FCC1: UTOPIA Transmit Start of Cell** In the ATM UTOPIA interface supported by FCC1. TXSOC is asserted by the MSC8101 (UTOPIA master PHY) when TXD[0–7] contains the first valid byte of the cell.
	FCC1: TXSOC *UTOPIA slave*	Input	**FCC1: UTOPIA Transmit Start of Cell** In the ATM UTOPIA interface supported by FCC1. TXSOC is asserted by the external UTOPIA master PHY when TXD[0–7] contains the first valid byte of the cell.
	FCC1: TX_ER *MII*	Output	**FCC1: Media Independent Interface Transmit Error** In the MII interface supported by FCC1. TX_ER is asserted by the MSC8101 to force propagation of transmit errors.

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA28	FCC1: $\overline{\text{RXENB}}$ *UTOPIA master*	Output	**FCC1: UTOPIA Master Receive Enable** In the ATM UTOPIA interface supported by FCC1. (UTOPIA master) $\overline{\text{RXENB}}$ is asserted by the MSC8101 (UTOPIA master PHY) to indicate that RXD[0–7] and RXSOC are to be sampled at the end of the next cycle. RXD[0–7] and $\overline{\text{RXSOC}}$ are enabled only in cycles following those with $\overline{\text{RXENB}}$ asserted.
	FCC1: $\overline{\text{RXENB}}$ *UTOPIA slave*	Input	**FCC1: UTOPIA Master Receive Enable** In the $\overline{\text{ATM UTOPIA}}$ interface supported by FCC1. (UTOPIA slave) $\overline{\text{RXENB}}$ is an input asserted by an external PHY to indicate that RXD[0–7] and RXSOC is to be sampled at the end of the next cycle. RXD[0–$\overline{7]\text{ and RXSOC}}$ are enabled only in cycles following those with $\overline{\text{RXENB}}$ asserted.
	FCC1: TX_EN *MII*	Output	**FCC1: Media Independent Interface Transmit Enable** In the MII interface supported by FCC1. TX_EN is asserted by the MSC8101 when transmitting data.
PA27	FCC1: RXSOC *UTOPIA master*	Input	**FCC1: UTOPIA Receive Start of Cell** Asserted by an external PHY when RXD[0–7] contains the first valid byte of the cell.
	FCC1: RXSOC *UTOPIA slave*	Output	**FCC1: UTOPIA Receive Start of Cell** Asserted by the MSC8101 (UTOPIA slave) for an external PHY when RXD[0–7] contains the first valid byte of the cell.
	FCC1: RX_DV *MII*	Input	**FCC1: Media Independent Interface Receive Data Valid** In the MII interface supported by FCC1. RX_DV is an input asserted by an external fast Ethernet PHY. RX_DV indicates that valid data is being sent. The presence of carrier sense but not RX_DV indicates reception of broken packet headers, probably due to bad wiring or a bad circuit.

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA26	FCC1: RXCLAV *UTOPIA slave*	Output	**FCC1: UTOPIA Slave Receive Cell Available** In the ATM UTOPIA interface supported by FCC1. RXCLAV is asserted by the MSC8101 (UTOPIA slave PHY) when one complete ATM cell is available for transfer.
	FCC1: RXCLAV *UTOPIA master, or*	Input	**FCC1: UTOPIA Master Receive Cell Available** In the ATM UTOPIA interface supported by FCC1. RXCLAV is asserted by an external PHY when one complete ATM cell is available for transfer.
	RXCLAV0 *UTOPIA master, Multi-PHY, direct polling*	Input	**FCC1: UTOPIA Master Receive Cell Available 0 Direct Polling** In the ATM UTOPIA interface supported by FCC1, RXCLAV0 is asserted by an external PHY when one complete ATM cell is available for transfer.
	FCC1: RX_ER *MII*	Input	**FCC1: Media Independent Interface Receive Error** In the MII interface and supported by FCC1. RX_ER is asserted by an external fast Ethernet PHY. This signal indicates a receive error, which often indicates bad wiring.
PA25	FCC1: TXD0 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 0** In the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	SDMA: MSNUM0	Output	**Module Serial Number Bit 0** MSNUM[0–4] of is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1), is active during the transfer.
PA24	FCC1: TXD1 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 1** In the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	SDMA: MSNUM1	Output	**Module Serial Number Bit 1** MSNUM[0–4] of is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1), is active during the transfer.
PA23	FCC1: TXD2 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 2** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA22	FCC1: TXD3 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 3** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
PA21	FCC1: TXD4 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 4** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	FCC1: TXD3 *MII* and *HDLC nibble*	Output	**FCC1: MII and HDLC Nibble Transmit Data Bit 3** TXD[3–0] supports MII and HDLC nibble modes in FCC1. TXD3 is the most significant bit. TXD0 is the least significant bit.
PA20	FCC1: TXD5 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 5** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	FCC1: TXD2 *MII* and *HDLC nibble*	Output	**FCC1: MII and HDLC Nibble Transmit Data Bit 2** TXD[3–0] is supported by MII and HDLC nibble modes in FCC1. TXD3 is the most significant bit. TXD0 is the least significant bit.
PA19	FCC1: TXD6 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 6** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	FCC1: TXD1 *MII* and *HDLC nibble*	Output	**FCC1: MII and HDLC Nibble Transmit Data Bit 1** TXD[3–0] is supported by MII and HDLC transparent nibble modes in FCC1. TXD3 is the most significant bit. TXD0 is the least significant bit.

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA18	FCC1: TXD7 *UTOPIA*	Output	**FCC1: UTOPIA Transmit Data Bit 7.** TXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 outputs ATM cell octets (UTOPIA interface data) on TXD[0–7]. TXD7 is the most significant bit. TXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes.
	FCC1: TXD0 *MII* and *HDLC nibble*	Output	**FCC1: MII and HDLC Nibble Transmit Data Bit 0** TXD[3–0] is supported by MII and HDLC nibble modes in FCC1. TXD3 is the most significant bit. TXD0 is the least significant bit.
	FCC1: TXD *HDLC serial* and *transparent*	Output	**FCC1: HDLC Serial and Transparent Transmit Data Bit** The TXD serial bit is supported by HDLC serial and transparent modes in FCC1.
PA17	FCC1: RXD7 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 7.** RXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when $\overline{\text{RXENB}}$ is asserted.
	FCC1: RXD0 *MII* and *HDLC nibble*	Input	**FCC1: MII and HDLC Nibble Receive Data Bit 0** RXD[3–0] is supported by MII and HDLC nibble mode in FCC1. RXD3 is the most significant bit. RXD0 is the least significant bit.
	FCC1: RXD *HDLC serial* and *transparent*	Input	**FCC1: HDLC Serial and Transparent Receive Data Bit** The RXD serial bit is supported by HDLC and transparent by FCC1.
PA16	FCC1: RXD6 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 6.** RXD[0–7] is part of the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when $\overline{\text{RXENB}}$ is asserted.
	FCC1: RXD1 *MII* and *HDLC nibble*	Input	**FCC1: MII and HDLC Nibble Receive Data Bit 1** RXD[3–0] is supported by MII and HDLC nibble mode in FCC1. RXD3 is the most significant bit. RXD0 is the least significant bit.

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA15	FCC1: RXD5 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 5** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted.
	RXD2 *MII* and *HDLC nibble*	Input	**FCC1: MII and HDLC Nibble Receive Data Bit 2** RXD[3–0] is supported by MII and HDLC nibble mode in FCC1. RXD3 is the most significant bit. RXD0 is the least significant bit.
PA14	FCC1: RXD4 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 4.** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. When no ATM data is available, idle cells are inserted. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted.
	FCC1: RXD3 *MII* and *HDLC nibble*	Input	**FCC1: MII and HDLC Nibble Receive Data Bit 3** RXD[3–0] is supported by MII and HDLC nibble mode in FCC1. RXD3 is the most significant bit. RXD0 is the least significant bit.
PA13	FCC1: RXD3 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 3** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted.
	SDMA: MSNUM2	Output	**Module Serial Number Bit 2** MSNUM[0–4] is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1), is active during the transfer.

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA12	FCC1: RXD2 *UTOPIA*	Input	**FCC1: UTOPIA Receive Data Bit 2** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted.
	SDMA: MSNUM3	Output	**Module Serial Number Bit 3** MSNUM[0-4] of is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1), is active during the transfer.
PA11	FCC1: RXD1 *UTOPIA*	Input	**FCC1: UTOPIA RX Receive Data Bit 1** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted.
	SDMA: MSNUM4	Output	**Module Serial Number Bit 4** MSNUM[0–4] of is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1) is active during the transfer.
PA10	FCC1: RXD0 *UTOPIA*	Input	**FCC1: UTOPIA RX Receive Data Bit 0** In the ATM UTOPIA interface supported by FCC1. The MSC8101 inputs ATM cell octets (UTOPIA interface data) on RXD[0–7]. RXD7 is the most significant bit. RXD0 is the least significant bit. A cell is 53 bytes. To support Multi-PHY configurations, RXD[0–7] is tri-stated, enabled only when RXENB is asserted.
	SDMA: MSNUM5	Output	**Module Serial Number Bit 5** MSNUM[0–4] of is the sub-block code of the current peripheral controller using SDMA. MSNUM5 indicates which section, transmit (0) or receive (1), is active during the transfer.
PA9	SMC2: SMTXD	Output	**SMC2: Serial Management Transmit Data** Supported by SMC2. The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI). See also PC15.
	SI1 TDMA1: L1TXD0 *TDM nibble*	Output	**Time-Division Multiplexing A1: Layer 1 Transmit Data Bit 0** In the TDMA1 interface supported by SI1. L1TXD3 is the most significant bit. L1TXD0 is the least significant bit in nibble mode. TDMA1 transmits nibble data out L1TXD[0–3].

Table 1-7. Port A Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated Signal *Protocol***		
PA8	SMC2: SMRXD	Input	**SMC2: Serial Management Receive Data** Supported by SMC2. The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI1 TDMA1: L1RXD0 *TDM nibble*	Input	**Time-Division Multiplexing A1: Layer 1 Nibble Receive Data Bit 0** In the TDMA1 interface supported by SI1. L1RXD3 is the most significant bit. L1RXD0 is the least significant bit in nibble mode. TDMA1 receives nibble data from L1RXD[0–3].
	SI1 TDMA1: L1RXD *TDM serial*	Input	**Time-Division Multiplexing A1: Layer 1 Serial Receive Data** In the TDMA1 interface supported by SI1. TDMA1 receives serial data from L1RXD**.**
PA7	SMC2: $\overline{\text{SMSYN}}$	Input	**SMC2: Serial Management Synchronization** The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI1 TDMA1: L1TSYNC/GRANT *TDM nibble* and *TDM serial*	Input	**Time-Division Multiplexing A1: Layer 1 Transmit Synchronization/Grant** In the TDMA1 interface supported by SI1, this is the synchronizing signal for the transmit channel. If Grant Mode is enabled this bit is sampled as the Grant bit for IDL mode access for the D channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Technical Reference* manual.
PA6	SI1 TDMA1: L1RSYNC *TDM nibble* and *TDM serial*	Input	**Time-Division Multiplexing A1: Layer 1 Receive Synchronization.** In the TDMA1 interface supported by SI1, this is the synchronizing signal for the receive channel.

1.6.2 Port B Signals

Table 1-8. Port B Signals

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PB31	FCC2: TX_ER *MII*	Output	**FCC2: Media Independent Interface Transmit Error** In the MII interface supported by FCC2. TX_ER is asserted by the MSC8101 to force propagation of transmit errors.
	SCC2: RXD	Input	**SCC2: Receive Data** Supported by SCC2. SCC2 receives serial data from RXD.
	SI2 TDMB2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing B2: Layer 1 Transmit Data** In the TDMB2 interface supported by SI2. L1TXD supports serial mode. TDMB2 transmits serial data out of L1TXD.
PB30	SCC2: TXD	Output	**SCC2: Transmit Data.** Supported by SCC2. SCC2 transmits serial data out of TXD.
	FCC2: RX_DV *MII*	Input	**FCC2: Media Independent Interface Receive Data Valid** In the MII interface supported by FCC2, RX_DV is asserted by an external fast Ethernet PHY. RX_DV indicates that valid data is being sent. The presence of carrier sense, but not RX_DV, indicates reception of broken packet headers, probably due to bad wiring or a bad circuit.
	SI2 TDMB2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Receive Data** In the TDMB2 interface supported by SI2. L1RXD supports serial mode. TDMB2 receives serial data from L1RXD.
PB29	FCC2: TX_EN *MII*	Output	**FCC2: Media Independent Interface Transmit Enable** In the MII interface supported by FCC2. TX_EN is asserted by the MSC8101 when transmitting data.
	SI2 TDMB2: L1RSYNC *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Receive Synchronization** In the TDMB2 interface supported by SI2, this is the synchronizing signal for the receive channel.

Table 1-8. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated I/O *Protocol*		
PB28	FCC2: $\overline{\text{RTS}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Output	**FCC2: Request to Send** One of the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{RTS}}$ is asynchronous with the data. $\overline{\text{RTS}}$ is typically used in conjunction with $\overline{\text{CD}}$. The MSC8101 FCC2 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low.
	FCC2: RX_ER *MII*	Input	**FCC2: Media Independent Interface Receive Error** In the MII interface supported by FCC2, RX_ER is asserted by an external fast Ethernet PHY. This signal indicates a receive error, which often indicates bad wiring.
	SCC2: $\overline{\text{RTS}}$, TENA	Output	**SCC2: Request to Send, Transmit Enable** Typically used in conjunction with $\overline{\text{CD}}$ supported by SCC2. The MSC8101 SCC2 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low. TENA is the signal used in Ethernet mode.
	SI2 TDMB2: L1TSYNC/GRANT *TDM serial*	Input	**Time-Division Multiplexing B2: Layer 1 Transmit Synchronization** In the TDMB2 interface supported by SI2, this is the synchronizing signal for the transmit channel. If Grant Mode is enabled this bit is sampled as the Grant bit for IDL mode access for the D channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Technical Reference* manual.
PB27	FCC2: $\overline{\text{COL}}$ *MII*	Input	**FCC2: Media Independent Interface Collision Detect** In the MII interface supported by FCC2. $\overline{\text{COL}}$ is asserted by an external fast Ethernet PHY.
	SI2 TDMC2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing C2: Layer 1 Transmit Data** In the TDMC2 interface supported by SI2. L1TXD supports serial mode. TDMC2 transmits serial data out of L1TXD.
PB26	FCC2: $\overline{\text{CRS}}$ *MII*	Input	**FCC2: Media Independent Interface Carrier Sense Input** In the MII interface, $\overline{\text{CRS}}$ is asserted by an external fast Ethernet PHY. This signal indicates activity on the cable.
	SI2 TDMC2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing C2: Layer 1 Receive Data** In the TDMC2 interface supported by SI2. L1RXD supports serial mode. TDMC2 receives serial data from L1RXD.

Table 1-8. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated I/O *Protocol*		
PB25	FCC2: TXD3 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble Transmit Data Bit 3** Supported by MII and HDLC nibble mode in FCC2. TXD3 is the most significant bit. TXD0 is the least significant bit.
	SI1 TDMA1: L1TXD3 *TDM nibble*	Output	**Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 3** TDMA1 transmits nibble data out of L1TXD[0–3]. L1TXD3 is the most significant bit and L1TXD0 is the least significant bit in nibble mode.
	SI2 TDMC2: L1TSYNC/GRANT *TDM serial*	Input	**Time-Division Multiplexing C2: Layer 1 Transmit Synchronization** In the TDMC2 interface supported by SI2, this is the synchronizing signal for the transmit channel. If Grant Mode is enabled, this bit is sampled as the Grant bit for IDL mode access for the D channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Technical Reference* manual.
PB24	FCC2: TXD2 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble: Transmit Data Bit 2** Supported by MII and HDLC nibble mode in FCC2. TXD3 is the most significant bit. TXD0 is the least significant bit.
	SI1 TDMA1: L1RXD3 *nibble*	Input	**Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 3** TDMA1 receives nibble data into L1RXD[0–3]. L1RXD3 is the most significant bit and L1RXD0 is the least significant bit in nibble mode.
	SI2 TDMC2: L1RSYNC *serial*	Input	**Time-Division Multiplexing C2: Layer 1 Receive Synchronization** In the TDMC2 interface supported by SI2, this is the synchronizing signal for the receive channel.
PB23	FCC2: TXD1 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble: Transmit Data Bit 1** Supported by MII and HDLC nibble mode in FCC2. TXD3 is the most significant bit. TXD0 is the least significant bit.
	SI1 TDMA1: L1RXD2 *TDM nibble*	Input	**Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 2** In the TDMA1 interface supported by SI1. TDMA1 supports bit and nibble modes. L1RXD3 is the most significant bit. L1RXD0 is the least significant bit in nibble mode. TDMA1 receives nibble data from L1RXD[0–3].
	SI2 TDMD2: L1TXD *TDM serial*	Output	**Time-Division Multiplexing D2: Layer 1 Transmit Data** In the TDMD2 interface supported by SI2. L1TXD supports serial mode. TDMA1 transmits serial data out of L1TXD.

Table 1-8. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated I/O *Protocol*		
PB22	FCC2: TXD0 *MII* and *HDLC nibble*	Output	**FCC2: MII and HDLC Nibble Transmit Data Bit 0** TXD[0–3] is supported by MII and HDLC nibble mode in FCC2. TXD3 is the most significant bit. TXD0 is the least significant bit.
	FCC2: TXD *HDLC serial* and *transparent*	Output	**FCC2: HDLC Serial and Transparent Transmit Data** TXD is supported by HDLC serial mode and transparent mode in FCC2.
	SI1 TDMA1: L1RXD1 *TDM nibble*	Input	**Time-Division Multiplexing A1: Nibble Layer 1 Receive Data Bit 1** In the TDMA1 interface supported by SI1. TDMA1 supports bit and nibble modes. L1RXD3 is the most significant bit. L1RXD0 is the least significant bit in nibble mode. TDMA1 receives nibble data from L1RXD[0–3].
	SI2 TDMD2: L1RXD *TDM serial*	Input	**Time-Division Multiplexing D2: Layer 1 Receive Data** In the TDMD2 interface supported by SI2. TDMD2 supports serial mode. TDMD2 receives serial data from L1RXD.
PB21	FCC2: RXD0 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble Receive Data Bit 0** RXD[0–3] is supported by MII and HDLC nibble mode in FCC2. RXD3 is the most significant bit. RXD0 is the least significant bit.
	FCC2: RXD *HDLC serial* and *transparent*	Input	**FCC2: HDLC Serial and Transparent Receive Data** Supported by HDLC serial mode and transparent mode in FCC2.
	SI1 TDMA1: L1TXD2 *TDM nibble*	Output	**Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 2** In the TDMA1 interface supported by SI1. TDMA1 supports bit and nibble modes. L1TXD3 is the most significant bit. L1TXD0 is the least significant bit in nibble mode. TDMA1 transmits nibble data out of L1TXD[0–3].
	SI2 TDMD2: L1TSYNC/GRANT *TDM serial*	Input	**Time-Division Multiplexing D2: Layer 1 Transmit Synchronize Data** In the TDMD2 interface supported by SI2, this is the synchronizing signal for the transmit channel. If Grant Mode is enabled this bit is sampled as the Grant bit for IDL mode access for the D channel. See the *Serial Interface with Time-Slot Assigner* chapter in the *MSC8101 Technical Reference* manual.

Table 1-8. Port B Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PB20	FCC2: RXD1 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble: Receive Data Bit 1** RXD[0–3] is supported by MII and HDLC nibble mode in FCC2. RXD3 is the most significant bit. RXD0 is the least significant bit.
	SI1 TDMA1: L1TXD1 *TDM nibble*	Output	**Time-Division Multiplexing A1: Nibble Layer 1 Transmit Data Bit 1** In the TDMA1 interface supported by SI1. TDMA1 supports bit and nibble modes. L1TXD3 is the most significant bit. L1TXD0 is the least significant bit in nibble mode. TDMA1 transmits nibble data out of L1TXD[0–3].
	SI2 TDMD2: L1RSYNC *TDM serial*	Input	**Time-Division Multiplexing D2: Layer 1 Receive Synchronize Data** In the TDMD2 interface supported by SI2, this is the synchronizing signal for the receive channel.
PB19	FCC2: RXD2 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble Receive Data Bit 2** RXD[0–3] is supported by MII and HDLC nibble mode in FCC2. RXD3 is the most significant bit. RXD0 is the least significant bit.
	I^2C: SDA	Input/ Output	**I^2C: Inter-Integrated Circuit Serial Data** The I^2C interface comprises two signals: serial data (SDA) and serial clock (SDA). The I^2C controller uses a synchronous, multimaster bus that can connect several integrated circuits on a board. Clock rates run up to 520 kHz@25 MHz system clock.
PB18	FCC2: RXD3 *MII* and *HDLC nibble*	Input	**FCC2: MII and HDLC Nibble Receive Data Bit 3** RXD[0–3] is supported by MII and HDLC nibble mode in FCC2. RXD3 is the most significant bit. RXD0 is the least significant bit.
	I^2C: SCL	Input/ Output	**I^2C: Inter-Integrated Circuit Serial Clock** The I^2C interface comprises two signals: serial data (SDA) and serial clock (SDA). The I^2C controller uses a synchronous, multimaster bus that can connect several integrated circuits on a board. Clock rates run up to 520 kHz@25 MHz system clock.

1.6.3 Port C Signals

Table 1-9. Port C Signals

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC31	BRG1O	Output	**Baud-Rate Generator 1 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins. BRG1O can be the internal input to the SIU timers. When CLK5 is selected (see PC27 below), it is the source for BRG1O which is the default input for the SIU timers. See the *System Interface Unit (SIU)* chapter in the *MSC8101 Technical Reference* manual for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 below), the BRG1O input to the SIU timers is disabled.
	CLK1	Input	**Clock 1** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIMER1/2: $\overline{\text{TGATE1}}$	Input	**Timer 1/2: Timer Gate 1** The timers can be gated/restarted by an external gate signal. There are two gate signals: $\overline{\text{TGATE1}}$ controls timer 1 and/or 2 and $\overline{\text{TGATE2}}$ controls timer 3 and/or 4.
PC30	BRG2O	Output	**Baud-Rate Generator 2 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK2	Input	**Clock 2** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	Timer1: $\overline{\text{TOUT1}}$	Output	**Timer 1: Timer Out 1** The timers (Timer[1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also connect internally to the input of another timer, resulting in a 32-bit timer.
	EXT1	Input	**External Request 1** External request input line 1 asserts an internal request to the CPM processor. The signal can be programmed as level- or edge-sensitive, and also has programmable priority. Refer to the RISC Controller Configuration Register (RCCR) description in the Chapter 17 of the MSC8101 Reference Manual for programming information. There are no current microcode applications for this request line. It is reserved for future development.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC29	BRG3O	Output	**Baud-Rate Generator 3 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK3	Input	**Clock 3** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIN2	Input	**Timer Input 2** A timer can have one of the following sources: another timer, system clock, system clock divided by 16 or a timer input. The CPM supports up to 4 timer inputs. The timer inputs can be captured on the rising, falling or both edges.
	SCC1: $\overline{\text{CTS}}$, CLSN	Input	**SCC1: Clear to Send, Collision** Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8101 SCC1 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC15.
PC28	BRG4O	Output	**Baud-Rate Generator 4 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK4	Input	**Clock 4** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIN1	Input	**Timer Input 1** A timer can have one of the following sources: another timer, system clock, system clock divided by 16 or a timer input. The CPM supports up to 4 timer inputs. The timer inputs can be captured on the rising, falling or both edges.
	Timer2: $\overline{\text{TOUT2}}$	Output	**Timer 2: Timer Output 2** The timers (Timer[1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also be connected internally to the input of another timer, resulting in a 32-bit timer.
	SCC2: $\overline{\text{CTS}}$, CLSN	Input	**SCC2: Clear to Send, Collision** Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8101 SCC2 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC13.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated I/O *Protocol*		
PC27	BRG5O	Output	**Baud-Rate Generator 5 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK5	Input	**Clock 5** When selected, CLK5 is a source for the SIU timers via BRG1O. See the *System Interface Unit (SIU)* chapter in the *MSC8101 Technical Reference* manual for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 below), the BRG1O input to the SIU timers is disabled.
	TIMER3/4: $\overline{\text{TGATE2}}$	Input	**Timer 3/4: Timer Gate 2** The timers can be gated/restarted by an external gate signal. There are two gate signals: $\overline{\text{TGATE1}}$ controls timer 1 and/or 2 and $\overline{\text{TGATE2}}$ controls timer 3 and/or 4.
PC26	BRG6O	Output	**Baud-Rate Generator 6 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK6	Input	**Clock 6** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	Timer3: $\overline{\text{TOUT3}}$	Output	**Timer 3: Timer Out 3** The timers (Timer[1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also connect internally to the input of another timer, resulting in a 32-bit timer.
	TMCLK	Input	**Timer Clock** When selected, TMCLK is the designated input to the SIU timers. When TMCLK is configured as the input to the SIU timers, the BRG1O input is disabled. See the *System Interface Unit (SIU)* chapter in the *MSC8101 Technical Reference* manual for additional information.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC25	BRG7O	Output	**Baud-Rate Generator 7 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK7	Input	**Clock 7** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIN4	Input	**Timer Input 4** A timer can have one of the following sources: another timer, system clock, system clock divided by 16 or a timer input. The CPM supports up to 4 timer inputs. The timer inputs can be captured on the rising, falling or both edges.
	DMA: $\overline{\text{DACK2}}$	Output	**DMA: Data Acknowledge 2** $\overline{\text{DACK2}}$, DREQ2, $\overline{\text{DRACK2}}$ and $\overline{\text{DONE2}}$ belong to the SIU DMA. $\overline{\text{DONE2}}$ and $\overline{\text{DRACK2}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
PC24	BRG8O	Output	**Baud-Rate Generator 8 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins.
	CLK8	Input	**Clock 8** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	TIN3	Input	**Timer Input 3** A timer can have one of the following sources: another timer, system clock, system clock divided by 16, or a timer input. The CPM supports up to four timer inputs. The timer inputs can be captured on the rising, falling, or both edges.
	Timer4: $\overline{\text{TOUT4}}$	Output	**Timer 4: Timer Out 4** The timers (Timer1–4]) can output a signal on a timer output ($\overline{\text{TOUT}}$[1–4]) when the reference value is reached. This signal can be an active-low pulse or a toggle of the current output. The output can also be connected internally to the input of another timer, resulting in a 32-bit timer.
	DMA: DREQ2	Input	**DMA: Data Request 2** $\overline{\text{DACK2}}$, DREQ2, $\overline{\text{DRACK2}}$, and $\overline{\text{DONE2}}$ belong to the SIU DMA. $\overline{\text{DONE2}}$ and $\overline{\text{DRACK2}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC23	CLK9	Input	**Clock 9** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	DMA: $\overline{\text{DACK1}}$	Output	**DMA: Data Acknowledge 1** $\overline{\text{DACK1}}$, DREQ1, $\overline{\text{DRACK1}}$, and $\overline{\text{DONE1}}$ belong to the SIU DMA. $\overline{\text{DONE1}}$ and $\overline{\text{DRACK1}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
	EXT2	Input	**External Request 2** External request input line 2 asserts an internal request to the CPM processor. The signal can be programmed as level- or edge-sensitive, and also has programmable priority. Refer to the RISC Controller Configuration Register (RCCR) description in the Chapter 17 of the MSC8101 Reference Manual for programming information. There are no current microcode applications for this request line. It is reserved for future development.
PC22	SI1: L1ST1	Output	**Serial Interface 1: Layer 1 Strobe 1** In the time-slot assigner supported by SI1. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	CLK10	Input	**Clock 10** The CPM supports up to 10 clock input pins. The clocks are sent to the bank-of-clocks selection logic, where they can be routed to the controllers.
	DMA: DREQ1	Input/ Output	**DMA: Request 1** $\overline{\text{DACK1}}$, DREQ1, $\overline{\text{DRACK1}}$, and $\overline{\text{DONE1}}$ belong to the SIU DMA. $\overline{\text{DONE1}}$ and $\overline{\text{DRACK1}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC15	SMC2: SMTXD	Output	**SMC2: Serial Management Transmit Data** Supported by SMC2. The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that support three protocols or modes: UART, transparent, or general-circuit interface (GCI). See also PA9.
	SCC1: $\overline{\text{CTS}}$/CLSN	Input	**SCC1: Clear To Send, Collision** Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8101 SCC1 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC29.
	FCC1: TXADDR0 *UTOPIA master*	Output	**FCC1: UTOPIA Master Transmit Address Bit 0** In the ATM UTOPIA master interface supported by FCC1, this is transmit address bit 0.
	FCC1: TXADDR0 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Transmit Address Bit 0** In the ATM UTOPIA slave interface supported by FCC1, this is transmit address bit 0.
PC14	SI1: L1ST2	Output	**Serial Interface 1: Layer 1 Strobe 2** In the time-slot assigner supported by SI1. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also be generate output wave forms for such applications as stepper-motor control.
	SCC1: $\overline{\text{CD}}$, RENA	Input	**SCC1: Carrier Detect, Receive Enable** Typically used in conjunction with $\overline{\text{RTS}}$ supported by SCC1. The MSC8101 SCC1 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low.
	FCC1: RXADDR0 *UTOPIA master*	Output	**FCC1: UTOPIA Multi-PHY Master Receive Address Bit 0** In the ATM UTOPIA master interface supported by FCC1, this is receive address bit 0.
	FCC1: RXADDR0 *UTOPIA slave*	Input	**FCC1: UTOPIA Multi-PHY Slave Receive Address Bit 0** In the ATM UTOPIA slave interface supported by FCC1, this is receive address bit 0.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC13	SI1: L1ST4	Output	**Serial Interface 1: Layer 1 Strobe 4** In the time-slot assigner supported by SI1. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	SCC2: $\overline{\text{CTS}}$,CLSN	Input	**SCC2: Clear to Send, Collision** Typically used in conjunction with $\overline{\text{RTS}}$. The MSC8101 SCC2 transmitter sends out a request to send data signal ($\overline{\text{RTS}}$). The request is accepted when $\overline{\text{CTS}}$ is returned low. CLSN is the signal used in Ethernet mode. See also PC28.
	FCC1:TXADDR1 *UTOPIA master*	Output	**FCC1: UTOPIA Multi-PHY Master Transmit Address Bit 1** In the ATM UTOPIA master interface supported by FCC1, this is transmit address bit 1.
	FCC1: TXADDR1 *UTOPIA slave*	Input	**FCC1: UTOPIA Multi-PHY Slave Transmit Address Bit 1** In the ATM UTOPIA slave interface supported by FCC1, this is transmit address bit 1.
PC12	SI1: L1ST3	Output	**Serial Interface 1: Layer 1 Strobe 3** In the time-slot assigner supported by SI1. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	SCC2: $\overline{\text{CD}}$, RENA	Input	**SCC2: Carrier Detect, Request Enable** Typically used in conjunction with $\overline{\text{RTS}}$ supported by SCC2. The MSC8101 SCC2 transmitter requests to the receiver that it sends data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low.
	FCC1: RXADDR1 *UTOPIA master*	Output	**FCC1: UTOPIA Multi-PHY Master Receive Address Bit 1** In the ATM UTOPIA master interface supported by FCC1, this is receive address bit 1.
	FCC1: RXADDR1 *UTOPIA slave*	Input	**FCC1: UTOPIA Multi-PHY Slave Receive Address Bit 1** In the ATM UTOPIA slave interface supported by FCC1, this is receive address bit 1.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC7	SI2: L1ST1	Output	**Serial Interface 2: Strobe 1** In the time-slot assigner supported by SI2. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	FCC1: $\overline{\text{CTS}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Input	**FCC1: Clear To Send** In the standard modem interface signals supported by FCC1 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{CTS}}$ is asynchronous with the data.
	FCC1: TXADDR2 *UTOPIA master*	Output	**FCC1: UTOPIA Multi-PHY Master Transmit Address Bit 2** In the ATM UTOPIA master interface supported by FCC1, this is transmit address bit 2.
	FCC1: TXADDR2 *UTOPIA slave*	Input	**FCC1: UTOPIA Multi-PHY Slave Transmit Address Bit 2** In the ATM UTOPIA slave interface supported by FCC1 using multiplexed polling, this is transmit address bit 2.
	FCC1: TXCLAV1 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Transmit Cell Available 1 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, TXCLAV1 is asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC6	SI2: L1ST2	Output	**Serial Interface 2: Layer 1 Strobe 2** In the time-slot assigner supported by SI2. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	FCC1: $\overline{\text{CD}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Input	**FCC1: Carrier Detect** In the standard modem interface signals supported by FCC1 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{CD}}$ is an input asynchronous with the data.
	FCC1: RXADDR2 *UTOPIA master*	Output	**FCC1: UTOPIA Multi-PHY Master Receive Address Bit 2** In the ATM UTOPIA master interface supported by FCC1, this is receive address bit 2.
	FCC1: RXADDR2 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Receive Address Bit 2** In the ATM UTOPIA slave interface supported by FCC1 using multiplexed polling, this is receive address bit 2.
	FCC1: RXCLAV1 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Receive Cell Available 1 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, RXCLAV1 is asserted by an external PHY when one complete ATM cell is available for transfer.
PC5	SMC1: SMTXD	Output	**SMC1: Transmit Data** Supported by SMC1. The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI2: L1ST3	Output	**Serial Interface 2: Layer 1 Strobe 3** In the time-slot assigner supported by SI2. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	FCC2: $\overline{\text{CTS}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Input	**FCC2: Clear To Send** In the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$). $\overline{\text{CTS}}$ is asynchronous with the data.

Table 1-9. Port C Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PC4	SMC1: SMRXD	Input	**SMC1: Receive Data** Supported by SMC1. The SMC interface consists of SMTXD, SMRXD, SMSYN, and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent, or general-circuit interface (GCI).
	SI2: L1ST4	Output	**Serial Interface 2: Layer 1 Strobe 4** In the time-slot assigner supported by SI2. The MSC8101 time-slot assigner supports up to four strobe outputs that can be asserted on a bit or byte basis. The strobe outputs are useful for interfacing to other devices that do not support the multiplexed interface or for enabling/disabling three-state I/O buffers in a multiple-transmitter architecture. These strobes can also generate output wave forms for such applications as stepper-motor control.
	FCC2: $\overline{\text{CD}}$ *HDLC serial*, *HDLC nibble*, and *transparent*	Input	**FCC2: Carrier Detect** In the standard modem interface signals supported by FCC2 ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$ and $\overline{\text{CD}}$). $\overline{\text{CD}}$ is asynchronous with the data.

1.6.4 Port D Signals

Table 1-10. Port D Signals

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PD31	SCC1: RXD	Input	**SCC1: Receive Data** Supported by SCC1. SCC1 receives serial data from RXD.
	DMA: $\overline{\text{DRACK1}}$	Output	**DMA: Data Request Acknowledge 1** $\overline{\text{DACK1}}$, $\overline{\text{DREQ1}}$, $\overline{\text{DRACK1}}$, and $\overline{\text{DONE1}}$ belong to the SIU DMA. $\overline{\text{DONE1}}$ and $\overline{\text{DRACK1}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
	DMA: $\overline{\text{DONE1}}$	Input/ Output	**DMA: Done 1** $\overline{\text{DACK1}}$, $\overline{\text{DREQ1}}$, $\overline{\text{DRACK1}}$, and $\overline{\text{DONE1}}$ belong to the SIU DMA. $\overline{\text{DONE1}}$ and $\overline{\text{DRACK1}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
PD30	SCC1: TXD	Output	**SCC1: Transmit Data** Supported by SCC1. SCC1 transmits serial data out of TXD.
	DMA: $\overline{\text{DRACK2}}$	Output	**DMA: Data Request Acknowledge 2** $\overline{\text{DACK2}}$, $\overline{\text{DREQ2}}$, $\overline{\text{DRACK2}}$, and $\overline{\text{DONE2}}$ belong to the SIU DMA. $\overline{\text{DONE2}}$ and $\overline{\text{DRACK2}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.
	DMA: $\overline{\text{DONE2}}$	Input/ Output	**DMA: Done 2** $\overline{\text{DACK2}}$, $\overline{\text{DREQ2}}$, $\overline{\text{DRACK2}}$, and $\overline{\text{DONE2}}$ belong to the SIU DMA. $\overline{\text{DONE2}}$ and $\overline{\text{DRACK2}}$ are signals on the same pin and therefore cannot be used simultaneously. There are two sets of DMA pins associated with the PIO ports.

Table 1-10. Port D Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PD29	SCC1: $\overline{\text{RTS}}$, TENA	Output	**SCC1: Request to Send, Transmit Enable** Typically used in conjunction with $\overline{\text{CD}}$ supported by SCC2. The MSC8101 SCC1 transmitter requests the receiver to send data by asserting $\overline{\text{RTS}}$ low. The request is accepted when $\overline{\text{CTS}}$ is returned low. TENA is the signal used in Ethernet mode.
	FCC1: RXADDR3 UTOPIA master	Output	**FCC1: UTOPIA Multi-PHY Master Receive Address Bit 3** In the ATM UTOPIA master interface supported by FCC1 using multiplexed polling, this is receive address bit 3.
	FCC1: RXADDR3 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Receive Address Bit 3** In the ATM UTOPIA slave interface supported by FCC1 using multiplexed polling, this is receive address bit 3.
	FCC1: RXCLAV2 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Receive Cell Available 2 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, RXCLAV2 is asserted by an external PHY when one complete ATM cell is available for transfer.

Table 1-10. Port D Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PD19	FCC1: TXADDR4 *UTOPIA master*	Output	**FCC1: Multi-PHY Master Transmit Address Bit 4 Multiplexed Polling** In the ATM UTOPIA master interface supported by FCC1 using multiplexed polling, this is transmit address bit 4.
	FCC1: TXADDR4 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Transmit Address Bit 4** In the ATM UTOPIA slave interface supported by FCC1 using multiplexed polling, this is transmit address bit 4.
	FCC1: TXCLAV3 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY master Transmit Cell Available 3 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, TXCLAV3 is asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell.
	BRG1O	Output	**Baud Rate Generator 1 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally by the bank-of-clocks selection logic and/or provide an output to one of the 8 BRG pins. BRG1O can be the internal input to the SIU timers. When CLK5 is selected (see PC27 above), it is the source for BRG1O which is the default input for the SIU timers. See the *System Interface Unit (SIU)* chapter in the *MSC8101 Technical Reference* manual for additional information. If CLK5 is not enabled, BRG1O uses an internal input. If TMCLK is enabled (see PC26 above), the BRG1O input to the SIU timers is disabled.
	SPI: $\overline{\text{SPISEL}}$	Input	**SPI: Select** The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select ($\overline{\text{SPISEL}}$). The SPI can be configured as a slave or master in single- or multiple-master environments. $\overline{\text{SPISEL}}$ is the enable input to the SPI slave. In a multimaster environment, $\overline{\text{SPISEL}}$ (always an input) detects an error when more than one master is operating. SPI masters must output a slave select signal to enable SPI slave devices by using a separate general-purpose I/O signal. Assertion of an SPI $\overline{\text{SPISEL}}$ while it is master causes an error.

Table 1-10. Port D Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	**Peripheral Controller: Dedicated I/O *Protocol***		
PD18	FCC1: RXADDR4 *UTOPIA master*	Output	**FCC1: UTOPIA Master Receive Address Bit 4** In the ATM UTOPIA master interface supported by FCC1 using multiplexed polling, this is receive address bit 4.
	FCC1: RXADDR4 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Receive Address Bit 4** In the ATM UTOPIA slave interface supported by FCC1, this is the receive address bit 4.
	FCC1: RXCLAV3 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Receive Cell Available 3 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, RXCLAV3 is asserted by an external PHY when one complete ATM cell is available for transfer.
	SPI: SPICLK	Input/ Output	**SPI: Clock** The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select (SPISEL). The SPI can be configured as a slave or master in single- or multiple-master environments. SPICLK is a gated clock, active only during data transfers. Four combinations of SPICLK phase and polarity can be configured. When the SPI is a master, SPICLK is the clock output signal that shifts received data in from SPIMISO and transmitted data out to SPIMOSI.
PD17	BRG2O	Output	**Baud Rate Generator 2 Output** The CPM supports up to 8 BRGs. The BRGs can be used internally to the MSC8101 and/or provide an output to one of the 8 BRG pins.
	FCC1: RXPRTY *UTOPIA*	Input	**FCC1: UTOPIA Receive Parity** In the ATM UTOPIA interface supported by FCC1, this is the odd parity bit for RXD[0–7].
	SPI: SPIMOSI	Input/ Output	**SPI: Master Output Slave Input** The SPI interface comprises our signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK) and select ($\overline{\text{SPISEL}}$)**.** The SPI can be configured as a slave or master in single- or multiple-master environments. When the SPI is a slave, SPICLK is the clock input that shifts received data in from SPIMOSI and transmitted data out through SPIMISO.

Table 1-10. Port D Signals (Continued)

Name		Dedicated I/O Data Direction	Description
General-Purpose I/O	Peripheral Controller: Dedicated I/O *Protocol*		
PD16	FCC1: TXPRTY *UTOPIA*	Output	**FCC1: UTOPIA Transmit Parity** In the ATM UTOPIA interface supported by FCC1, this is the odd parity bit for TXD[0–7].
	SPI: SPIMISO	Input/ Output	**SPI: Master Input Slave Output** The SPI interface comprises four signals: master out slave in (SPIMOSI), master in slave out (SPIMISO), clock (SPICLK), and select ($\overline{\text{SPISEL}}$). The SPI can be configured as a slave or master in single- or multiple-master environments. When the SPI is a slave, SPICLK is the clock input that shifts received data in from SPIMOSI and transmitted data out through SPIMISO.
PD7	SMC1: $\overline{\text{SMSYN}}$	Input	**SMC1: Serial Management Synchronization** Supported by SMC1. $\overline{\text{SMSYN}}$ is an input. The SMC interface consists of SMTXD, SMRXD, $\overline{\text{SMSYN}}$ and a clock. Not all signals are used for all applications. SMCs are full-duplex ports that supports three protocols or modes: UART, transparent or general-circuit interface (GCI).
	FCC1: TXADDR3 *UTOPIA master*	Output	**FCC1: UTOPIA Master Transmit Address Bit 3** In the ATM UTOPIA master interface supported by FCC1 using multiplexed polling, this is transmit address bit 3.
	FCC1: TXADDR3 *UTOPIA slave*	Input	**FCC1: UTOPIA Slave Transmit Cell Available 2** In the ATM UTOPIA slave interface supported by FCC1 using multiplexed polling, this is transmit address bit 3.
	FCC1: TXCLAV2 *UTOPIA multi-PHY master, direct polling*	Input	**FCC1: UTOPIA Multi-PHY Master Transmit Cell Available 2 Direct Polling** In the ATM UTOPIA master interface supported by FCC1 using direct polling, TXCLAV2 is asserted by an external UTOPIA slave PHY to indicate that it can accept one complete ATM cell.

1.7 JTAG Test Access Port Signals

The MSC8101 supports the standard set of Test Access Port (TAP) signals defined by IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture specification and described in **Table 1-11**.

Table 1-11. JTAG Test Access Port Signals

Signal Name	Type	Signal Description
TCK	Input	**Test Clock—**A test clock signal for synchronizing JTAG test logic.
TDI	Input	**Test Data Input—**A test data serial signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	**Test Data Output—**A test data serial signal for test instructions and data. TDO can be tri-stated. The signal is actively driven in the shift-IR and shift-DR controller states and changes on the falling edge of TCK.
TMS	Input	**Test Mode Select—**Sequences the test controller's state machine, is sampled on the rising edge of TCK, and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	**Test Reset—**Asynchronously initializes the test controller, has an internal pull-up resistor, and must be asserted after power up.

1.8 Reserved Signals

Table 1-12. Reserved Signals

Signal Name	Type	Signal Description
TEST	Input	**Test** Used for manufacturing testing. You must connect this input to GND.
THERM[1–2]	—	Leave disconnected.
SPARE1, 5	—	**Spare Pins** Leave disconnected for backward compatibility with future revisions of this device.

Chapter 2
Hardware Specifications

2.1 Introduction

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MSC8101 communications processor. For additional information, see the *MSC8101 User's Manual.*

Note: The MSC8101 electrical specifications are preliminary and many are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after thorough characterization and device qualifications have been completed.

Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 describes the maximum electrical ratings for the MSC8101.

Table 2-1. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{DD}	–0.2 to 1.6	V
PLL supply voltage	V_{CCSYN}	–0.2 to 1.6	V
I/O supply voltage	V_{DDH}	–0.2 to 3.6	V
Input voltage	V_{IN}	(GND – 0.2) to 3.6	V
Maximum operating temperature range	T_j	0 to 120	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Note: 1. Functional operating conditions are given in **Table 2-2.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 4.1**, *Thermal Design Considerations*, on page 4-1 includes a formula for computing the chip junction temperature (T_J).

2.2 Recommended Operating Conditions

Table 2-2 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2-2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	V_{DD}	1.4 to 1.6	V
PLL supply voltage	V_{CCSYN}	1.4 to 1.6	V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	-0.2 to V_{DDH}+0.2	V
Operating temperature range	T_j	0 to 105	°C

2.3 Thermal Characteristics

Table 2-3 describes thermal characteristics of the MSC8101.

Table 2-3. Thermal Characteristics

Characteristic	Symbol	FC-PBGA 17 × 17mm	Unit
Junction-to-ambient[1, 2]	$R_{\theta JA}$ or θ_{JA}	52	^{0}C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$ or θ_{JA}	25	^{0}C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$ or θ_{JB}	22	^{0}C/W
Junction-to-case (top)[5]	$R_{\theta JC}$ or θ_{JC}	0.3	^{0}C/W
Junction-to-package (top)[6]	Ψ_{JT}	0.3	^{0}C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the single layer (1s) board horizontal.
3. Per JESD51-6 with the boards horizontal.
4. Thermal resistance between the die and the printed circuit board per JESD 51-8.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature, per EIA/JESD51-2.

Section 4.1, *Thermal Design Considerations*, on page 4-1 provides a more detailed explanation of these characteristics.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8101. The measurements in **Table 2-4** assume the following system conditions:

- T_A = 0–70 °C
- V_{DD} = 1.5 V ± 5% V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD} or both V_{DDH} and V_{DD} must vary in the same direction (for example, both V_{DDH} and V_{DD} vary by ± 5 percent).

Table 2-4. DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.4	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = V_{DDH}	I_{IN}	—	TBD	µA
Tri-state (high impedance off state) leakage current, V_{IN} = V_{DDH}	I_{OZ}	—	TBD	µA
Signal low input current, V_{IL} = 0.4 V	I_L	TBD	TBD	µA
Signal high input current, V_{IH} = 2.0 V	I_H	TBD	TBD	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.0	—	V
Output low voltage, I_{OL}= 3.2 mA	V_{OH}	—	0.4	V
Core power dissipation at 300 MHz	P_{CORE}	—	250	mW
Input/Output Ports power dissipation at 150 MHz	P_{CPM}	—	210	mW
SIU power dissipation at 100 MHz	P_{SIU}	—	70	mW
Core’s leakage power	P_{LCO}	—	3	mW
Input/Output Ports leakage power	P_{LCP}	—	6	mW
SIU leakage power	P_{LSI}	—	2	mW

2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. AC timings are based on a 50 pF load, except where noted otherwise, and 50 Ω transmission line.

2.5.1 Clock and Timing Signals

The following sections include a description of clock configuration and signal characteristics.

2.5.1.1 Clock Signal Configuration

Table 2-5 shows the maximum frequency values for internal (Core, Bus, SCC, CPM, and BRG) and external (CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

Table 2-5. Maximum Frequencies

Characteristic	Maximum in MHz
Core Frequency	300
CPM Frequency (CPMCLK)	150
Bus Frequency (BCLK)	100
Serial Communication Controller Clock Frequency (SCLK)	75
Baud Rate Generator Clock Frequency (BRGCLK)	75
External Clock Output Frequency (CLKOUT)	100

Six bit values map the MSC8101 clocks to one of 64 configuration mode options. Each option determines the CLKIN, SC140 core, PowerPC bus, SCC clock, CPM, and CLKOUT frequencies. The six bit values are derived from three dedicated input pins (MODCK[1–3]) and three bits from the reset configuration word (MODCK_H). To configure the SPLL pre-division factor, SPLL multiplication factor, and the frequencies for the SC140 core, SCC clocks, CPM parallel I/O ports, and PowerPC buses, the MODCK[1–3] pins are sampled and combined with the MODCK_H values when the internal power-on Reset (internal $\overline{\text{PORESET}}$) is deasserted. Clock configuration changes only when the internal $\overline{\text{PORESET}}$ signal is deasserted.

The following factors are configured:

- SPLL pre-division factor (SPLL PDF)
- SPLL multiplication factor (SPLL MF)
- Bus post-division factor (Bus DF)
- CPLL pre-division factor (CPLL PDF)
- CPLL multiplication factor (SPLL MF)

The SCC division factor (SCC DF) is fixed at 4 and the CPM division factor (CPM DF) is fixed at 2. The BRG division factor (BRG DF) is configured through the System Clock Control Register (SCCR) and can be 4, 16 (default after reset), 64, or 256.

Table 2-6 lists the available values for each of these configurable factors, as well as the 64 possible configuration mode options.

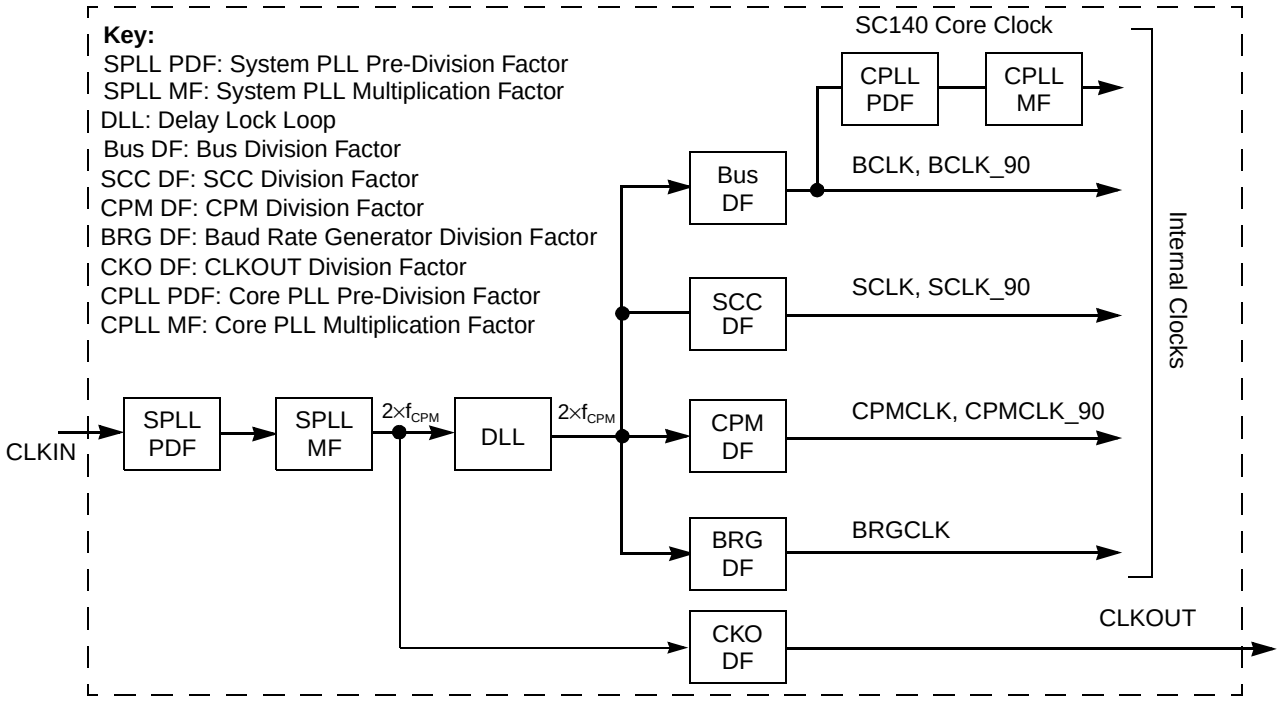
Table 2-6. Clock Configuration Modes

Mode #	MODCK_H[1]	MODCK[1–3][2]	SPLL PDF	SPLL MF	CPM:CLKIN Ratio	Bus DF	CPM:Bus Ratio	CPLL PDF	CPLL MF	Ratio Bus:CPM:Core
0	000	000	1	30	15x	3	1.5x	4	12	1, 1.5, 3
1	000	001	1	26	13x	4	2x	3	12	1, 2, 4
2	000	010	1	24	12x	3	1.5x	4	12	1, 1.5, 3
3	000	011	1	20	10x	3	1.5x	4	12	1, 1.5, 3
4	000	100	2	30	7.5x	3	1.5x	4	12	1, 1.5, 3
5	000	101	2	18	4.5x	3	1.5x	4	12	1, 1.5, 3
6	000	110	3	12	2x	4	2x	3	12	1, 2, 4
7	000	111	4	12	1.5x	3	1.5x	4	12	1, 1.5, 3
8	001	000	1	30	15x	5	2.5x	2	10	1, 2.5, 5
9	001	001	1	30	15x	4	2x	3	12	1, 2, 4
10	001	010	1	30	15x	5	2.5x	2	12	1, 2.5, 6
11	001	011	1	30	15x	5	2.5x	3	12	1, 2.5, 4
12	001	100	1	26	13x	4	2x	2	10	1, 2, 5
13	001	101	1	26	13x	3	1.5x	4	12	1, 1.5, 3
14	001	110	1	24	12x	5	2.5x	2	10	1, 2.5, 5
15	001	111	1	24	12x	4	2x	3	12	1, 2, 4
16	010	000	1	26	13x	5	2.5x	2	10	1, 2.5, 5
17	010	001	1	28	13x	4	2x	3	12	1, 2, 4
18	010	010	1	28	14x	5	2.5x	2	10	1, 2.5, 5
19	010	011	1	28	14x	5	2.5x	3	12	1, 2.5, 4
20	010	100	1	22	11x	4	2x	3	12	1, 2, 4
21	010	101	1	22	11x	4	2x	2	10	1, 2, 5
22	010	110	1	22	11x	3	1.5x	4	12	1, 1.5, 3
23	010	111	1	20	10x	5	2.5x	2	10	1, 2.5, 5
24	011	000	1	20	10x	5	2.5x	2	12	1, 2.5, 6
25	011	001	1	22	11x	5	2.5x	2	10	1, 2.5, 5
26	011	010	1	22	11x	5	2.5x	3	12	1, 2.5, 4
27	011	011	1	22	11x	4	2x	3	12	1, 2, 4
28	011	100	1	18	9x	4	2x	3	12	1, 2, 4
29	011	101	1	16	8x	4	2x	3	12	1, 2, 4
30	011	110	1	20	10x	4	2x	3	12	1, 2, 4
31	011	111	2	30	7.5x	5	2.5x	2	10	1, 2.5, 5
32	100	000	2	30	7.5x	4	2x	3	12	1, 2, 4
33	100	001	2	30	7.5x	5	2.5x	2	12	1, 2.5, 6
34	100	010	2	30	7.5x	4	2x	2	10	1, 2, 5

Table 2-6. Clock Configuration Modes (Continued)

Mode #	MODCK_H[1]	MODCK[1–3][2]	SPLL PDF	SPLL MF	CPM:CLKIN Ratio	Bus DF	CPM:Bus Ratio	CPLL PDF	CPLL MF	Ratio Bus:CPM:Core
35	100	011	2	26	6.5x	4	2x	3	12	1, 2, 4
36	100	100	2	26	6.5x	4	2x	2	10	1, 2, 5
37	100	101	2	26	6.5x	3	1.5x	4	12	1, 1.5, 3
38	100	110	1	14	7x	4	2x	3	12	1, 2, 4
39	100	111	1	16	8x	5	2.5x	2	10	1, 2.5, 5
40	101	000	1	12	6x	5	2.5x	2	10	1, 2.5, 5
41	101	001	1	12	6x	4	2x	3	12	1, 2, 4
42	101	010	1	12	6x	3	1.5x	4	12	1, 1.5, 3
43	101	011	1	10	5x	5	2.5x	2	12	1, 2.5, 6
44	101	100	2	18	4.5x	5	2.5x	2	10	1, 2.5, 5
45	101	101	2	18	4.5x	4	2x	3	12	1, 2, 4
46	101	110	2	16	4x	4	2x	3	12	1, 2, 4
47	101	111	2	16	4x	4	2x	2	10	1, 2, 5
48	110	000	1	10	5x	5	2.5x	2	10	1, 2.5, 5
49	110	001	4	30	3.75x	5	2.5x	2	10	1, 2.5, 5
50	110	010	4	30	3.75x	4	2x	3	12	1, 2, 4
51	110	011	4	30	3.75x	3	1.5x	4	12	1, 1.5, 3
52	110	100	4	26	3.25x	4	2x	3	12	1, 2, 4
53	110	101	2	12	3x	5	2.5x	2	10	1, 2.5, 5
54	110	110	2	12	3x	4	2x	3	12	1, 2, 4
55	110	111	2	12	3x	3	1.5x	4	12	1, 1.5, 3
56	111	000	2	10	2.5x	5	2.5x	2	12	1, 2.5, 6
57	111	001	2	10	2.5x	5	2.5x	2	10	1, 2.5, 5
58	111	010	3	12	2x	4	2x	2	10	1, 2, 5
59	111	011	2	10	2.5x	5	2.5x	3	12	1, 2.5, 4
60	111	100	Reserved							
61	111	101	Reserved							
62	111	110	Reserved							
63	111	111	Reserved							

Note:
1. MODCK_H is a 3-bit field that occupies bits 28–30 of the Hard Reset Configuration Word. The bits are listed in the table in the following order: bit 28, bit 29, bit 30. For example, the value 110 indicates that bit 28 = 1, bit 29 = 1, and bit 30 = 0.
2. MODCK[1–3] are external signal inputs that are either pulled up (1) or pulled down (0) to configure the system clock mode. The values are listed in the table in the following order: MODCK1, MODCK2, MODCK3. For example, the value 110 indicates that MODCK1 is pulled up, MODCK2 is pulled up, and MODCK3 is pulled down.



Notes:
1. SPLL PDF is determined by the clock configuration mode.
2. SPLL MF is determined by the clock configuration mode.
3. The Bus DF = CLKOUT DF and is 4 or 5 as determined by the clock configuration mode.
4. SCC DF is always 4.
5. CPM DF is always 2.
6. BRG DF is set by the System Clock Control Register (SCCR) and is 4, 16 (default), 64, or 256.

Figure 2-1. Clocking Scheme

2.5.1.2 Clocking and Timing Characteristics

Table 2-7. System Clock Parameters

Characteristic	Minimum	Maximum	Unit
Phase Jitter between BCLK and DLLIN	—	0.5	ns
CLKIN frequency[1]	10	100	MHz
CLKIN slope	—	5	ns
DLLIN slope	—	2	ns
CLKOUT frequency jitter	—	(0.01 × CLKOUT) + CLKIN jitter	ns
Delay between CLKOUT and DLLIN	—	5	ns

Note: 1. Low CLKIN frequency causes poor PLL performance. Choose a CLKIN frequency high enough to keep the frequency after the predivider higher than 10 MHz.

Table 2-8. Clock Operation

Characteristics	Symbol	Min	Max
CLKIN[1]			
■ Frequency	CKIf	10 MHz[2]	100.0 MHz
■ Input high[3] (50% duty cycle)	$CKIT_H$	5 ns	50 ns
■ Input low[3] (50% duty cycle)	$CKIT_L$	5 ns	50 ns
■ Cycle time	$CKIT_C$	10 ns	100 ns
Reference clock (CLKIN/PDF)			
■ Frequency	RCf	10 MHz	30 MHz
■ Cycle time	RCT_C	33.3 ns	100 ns
Bus Clock (BCLK)			
■ Frequency	BCKf	20 MHz	100 MHz
■ Cycle time	$BCKT_C$	10 ns	50 ns
Output Clock (CLKOUT)			
■ Frequency	CKOf	20 MHz	100 MHz
■ Cycle time	$CKOT_C$	10 ns	50 ns
Serial Communications Controller Clock (SCLK)			
■ Frequency	SCCf	25 MHz	75 MHz
■ Cycle time	ST_C	13.3 ns	40 ns
Communications Processor Module Clock (CPMCLK)			
■ Frequency	CPMf	50 MHz	150 MHz
■ Cycle time	$CPMT_C$	6.67 ns	20 ns
Baud Rate Generator Clock (BRGCLK)			
■ For BRG DF = 4			
— Frequency	BRGf	25 MHz	75 MHz
— Cycle time	$BRGT_C$	13.3 ns	40 ns
■ For BRG DF = 16 (default)			
— Frequency	BRGf	6.25 MHz	18.75 MHz
— Cycle time	$BRGT_C$	53.3 ns	160 ns
■ For BRG DF = 64			
— Frequency	BRGf	1.56 MHz	4.69 MHz
— Cycle time	$BRGT_C$	213.3 ns	640 ns
■ For BRG DF = 256			
— Frequency	BRGf	390 KHz	1.17 MHz
— Cycle time	$BRGT_C$	853.3 ns	2.56 µs
SC140 core clock			
■ Frequency	COREf	75 MHz	300 MHz
■ Cycle time	$CORET_C$	3.33 ns	13.33 ns

2.5.2 Reset Timing

The MSC8101 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)

Asserting an external $\overline{\text{PORESET}}$ causes concurrent assertion of an internal $\overline{\text{PORESET}}$ signal, $\overline{\text{HRESET}}$, and $\overline{\text{SRESET}}$. When the external $\overline{\text{PORESET}}$ signal is deasserted, the MSC8101 samples several configuration pins:

- $\overline{\text{RSTCONF}}$—determines whether the MSC8101 is a master (0) or slave (1) device
- DBREQ—determines whether to operate in normal mode (0) or invoke the SC140 debug mode (1)
- HPE—disable (0) or enable (1) the host port (HDI16)
- BTM[0–1]—boot from external memory (00) or the HDI16 (01)

All these reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the last sources to cause a reset. **Table 2-9** describes reset causes.

Table 2-9. Reset Causes

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	$\overline{\text{PORESET}}$ initiates the power-on reset flow that resets all the MSC8101s and configures various attributes of the MSC8101, including its clock mode.
Hard reset ($\overline{\text{HRESET}}$)	Input/Output	The MSC8101 can detect an external assertion of $\overline{\text{HRESET}}$ only if it occurs while the MSC8101 is not asserting reset. During $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ is asserted. $\overline{\text{HRESET}}$ is an open-drain pin.
Soft reset ($\overline{\text{SRESET}}$)	Input/Output	The MSC8101 can detect an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8101 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin.

2.5.2.1 Reset Operation

The reset control logic determines the cause of a reset, synchronizes it if necessary, and resets the appropriate logic modules. The memory controller, system protection logic, interrupt controller, and parallel I/O pins are initialized only on hard reset. Soft reset initializes the internal logic while maintaining the system configuration. The MSC8101 has two mechanisms for reset configuration: host reset configuration and hardware reset configuration.

2.5.2.1.1 Power-On Reset Flow

Asserting the $\overline{\text{PORESET}}$ external pin initiates the power-on reset flow. $\overline{\text{PORESET}}$ should be asserted externally for at least 16 input clock cycles after external power to the MSC8101 reaches at least 2/3 V_{CC}. As **Table 2-10** shows, the MSC8101 has five configuration pins, four of which are multiplexed with the SC140 core EONCE Event (EE[0–1], EE[4–5]) pins and the fifth of which is the $\overline{\text{RSTCONF}}$ pin. These pins are sampled at the rising edge of $\overline{\text{PORESET}}$. In addition to these configuration pins, three (MODCK[1–3]) pins are sampled by the MSC8101. The signals on these pins and the MODCK_H value in the Hard Reset Configuration Word determine the PLL locking mode, by defining the ratio between the DSP clock, the bus clocks, and the CPM clock frequencies.

Table 2-10. External Configuration Signals

Pin	Description	Settings
RSTCONF	**Reset Configuration** Input line sampled by the MSC8101 at the rising edge of PORESET.	0 Reset Configuration Master. 1 Reset Configuration Slave.
DBREQ/ EE0	**EONCE Event Bit 0** Input line sampled after SC140 core PLL locks. Holding EE0 high when PORESET is deasserted puts the SC140 core into Debug mode.	0 SC140 core starts the normal processing mode after reset. 1 SC140 core enters Debug mode immediately after reset.
HPE/EE1	**Host Port Enable** Input line sampled at the rising edge of PORESET. If asserted, the Host port is enabled, the PowerPC system data bus is 32-bit wide, and the Host *must* program the reset configuration word.	0 Host port disabled (hardware reset configuration enabled). 1 Host port enabled.
BTM[0–1]/ EE[4–5]	**Boot Mode** Input lines sampled at the rising edge of PORESET, which determine the MSC8101 Boot mode.	00 MSC8101 boots from external memory. 01 MSC8101 boots from HDI16. 10 Reserved. 11 Reserved.

Table 2-11. Reset Timing

No.	Characteristics	Expression	Min	Max	Unit
1	Required external PORESET duration minimum ■ CLKIN = 10 MHz ■ CLKIN = 100 MHz	$16 \times CKIT_C$	 1.6 160	 — —	 µs ns
2	Delay from deassertion of external PORESET to deassertion of internal PORESET ■ CLKIN = 10 MHz ■ CLKIN = 100 MHz	$1024 \times CKIT_C$	 102.4 10.24		 µs µs
3	Delay from deassertion of internal PORESET to SPLL lock ■ CLKIN/SPLL PDF = 10 MHz ■ CLKIN/SPLL PDF = 30 MHz	$800 \times RCT_C$	 80.0 26.67		 µs µs
4	Delay from SPLL lock to DLL lock ■ DLL enabled — BCLK = 20 MHz — BCLK = 100 MHz ■ DLL disabled	 $3073 \times BCKT_C$ —	 153.65 30.73 0.0		 µs µs ns
5	Delay from SPLL lock to HRESET deassertion ■ DLL enabled — BCLK = 20 MHz — BCLK = 100 MHz ■ DLL disabled — BCLK = 20 MHz — BCLK = 100 MHz	 $3585 \times BCKT_C$ $512 \times BCKT_C$	 179.25 35.86 25.6 5.12		 µs µs µs µs

Table 2-11. Reset Timing (Continued)

No.	Characteristics	Expression	Min	Max	Unit
6	Delay from SPLL lock to $\overline{\text{SRESET}}$ deassertion				
	■ DLL enabled	$3588 \times BCKT_C$			
	— BCLK = 20 MHz		179.40		µs
	— BCLK = 100 MHz		35.88		µs
	■ DLL disabled	$515 \times BCKT_C$			
	— BCLK = 20 MHz		25.75		µs
	— BCLK = 100 MHz		5.15		µs
Notes: 1. Value given for lowest possible CLKIN frequency 10 MHz to ensure proper initialization of reset sequence.					

2.5.2.1.2 Host Reset Configuration

Host reset configuration allows the host to program the reset configuration word via the Host port after $\overline{\text{PORESET}}$ is deasserted, as described in the *MSC8101 Technical Reference Manual*. The MSC8101 samples the signals described in **Table 2-10** one the rising edge of $\overline{\text{PORESET}}$ when the signal is deasserted.

If HPE is sampled high, the host port is enabled. In this mode the $\overline{\text{RSTCONF}}$ pin *must* be pulled up. The device extends the internal $\overline{\text{PORESET}}$ until the host programs the reset configuration word register. The host must write four 8-bit half-words to the Host Reset Configuration Register address to program the reset configuration word, which is 32 bits wide. For more information, see the *MSC8101 Technical Reference Manual.* The reset configuration word is programmed before the internal PLL and DLL in the MSC8101 are locked. The host must program it after the rising edge of the $\overline{\text{PORESET}}$ input. In this mode, the host must have its own clock that does not depend on the MSC8101 clock. After the PLL and DLL are locked, $\overline{\text{HRESET}}$ remains asserted for another 512 bus clocks and is then released. The $\overline{\text{SRESET}}$ is released three bus clocks later (see **Figure 2-2**).

2.5.2.1.3 Hardware Reset Configuration

Hardware reset configuration is enabled if HPE is sampled low at the rising edge of $\overline{\text{PORESET}}$. The value driven on $\overline{\text{RSTCONF}}$ while $\overline{\text{PORESET}}$ changes from assertion to deassertion determines the MSC8101 configuration. If $\overline{\text{RSTCONF}}$ is deasserted (driven high) while $\overline{\text{PORESET}}$ changes, the MSC8101 acts as a configuration slave. If $\overline{\text{RSTCONF}}$ is asserted (driven low) while $\overline{\text{PORESET}}$ changes, the MSC8101 acts as a configuration master. **Section 2.5.2.1.3**, *Hardware Reset Configuration*, explains the configuration sequence and the terms “configuration master” and “configuration slave.”

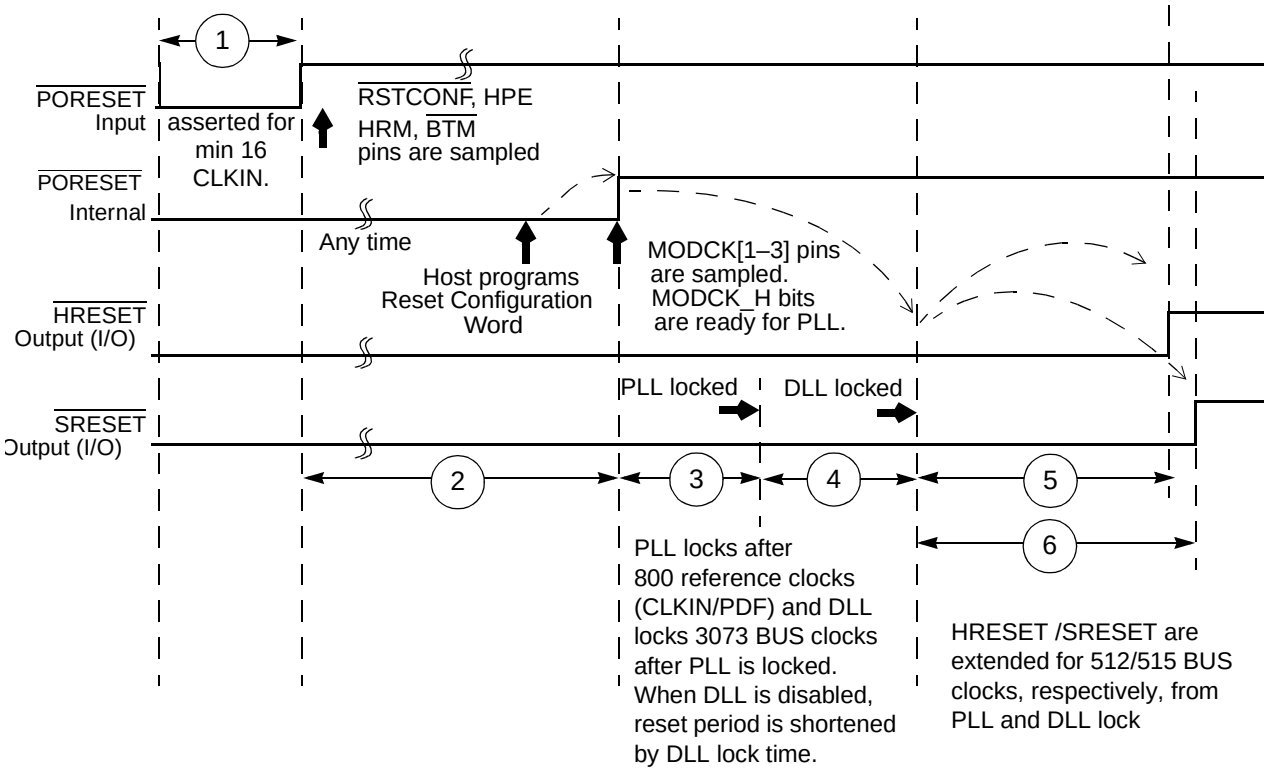


Figure 2-2. Host Reset Configuration Timing

Directly after the deassertion of PORESET and choice of the reset operation mode as configuration master or configuration slave, the MSC8101 starts the configuration process. The MSC8101 asserts HRESET and SRESET throughout the power-on reset process, including configuration. Configuration takes 1,024 CLOCKIN cycles, after which MODCK[1–3] are sampled to determine the MSC8101's working mode.

Next, the MSC8101 halts until the SPLL locks. The SPLL locks according to MODCK[1–3], which are sampled, and to MODCK_H taken from the Reset Configuration Word. SPLL locking time is 800 reference clocks, which is the clock at the output of the SPLL Pre-divider. After the SPLL is locked, all the clocks to the MSC8101 are enabled. If the DLLDIS bit in the reset configuration word is reset, the DLL starts the locking process after the SPLL is locked. During PLL and DLL locking, HRESET and SRESET are asserted. HRESET remains asserted for another 512 BUS clocks and is then released. The SRESET is released three bus clocks later. If the DLLDIS bit in the reset configuration word is set, the DLL is bypassed and there is no locking process, thus saving the DLL locking time. **Figure 2-3** shows the power-on reset flow.

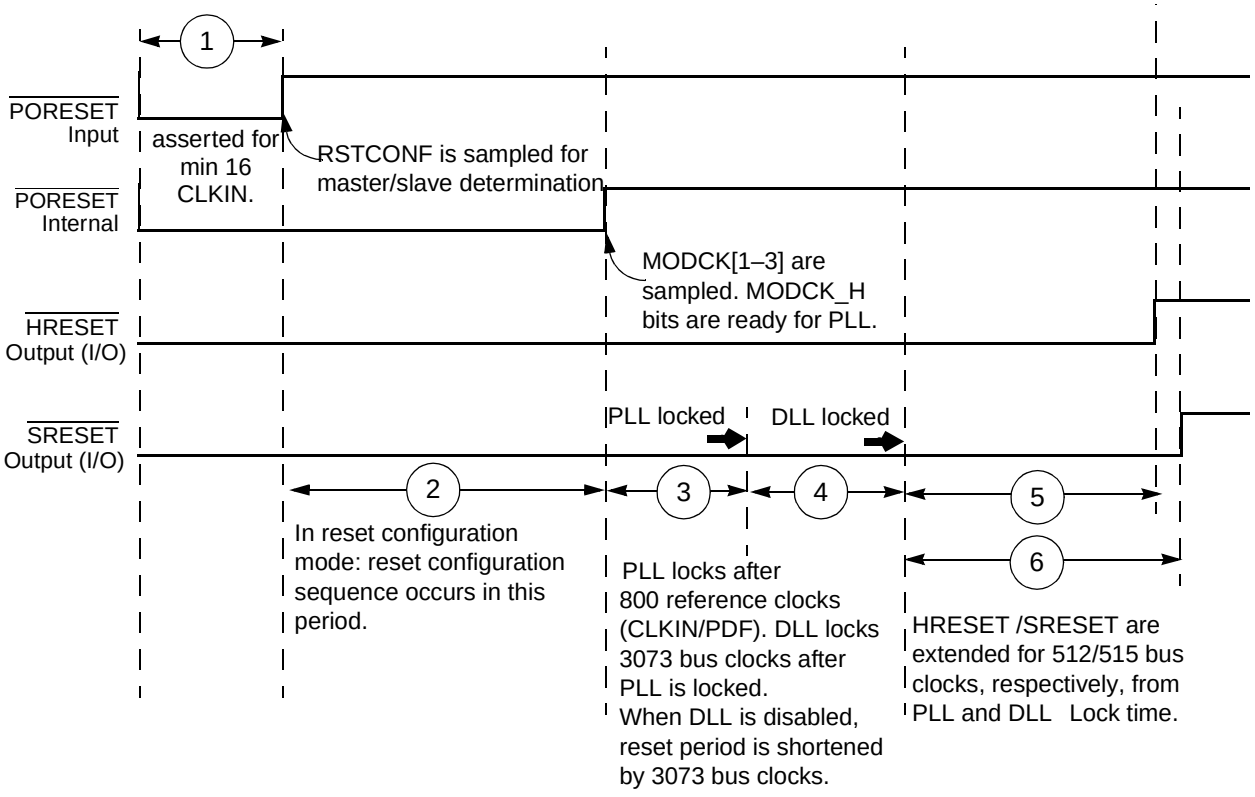


Figure 2-3. Hardware Reset Configuration Timing

2.5.3 PowerPC System Bus Access Timing

2.5.3.1 Core Data Transfers

Generally, all MSC8101 bus and system output signals are driven from the rising edge of the input clock (CLKIN). Memory controller signals, however, trigger on four points within a CLKIN cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of CLKIN (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 2-12** shows.

Table 2-12. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKIN)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKIN	1/2 CLKIN	3/4 CLKIN
1:2.5	3/10 CLKIN	1/2 CLKIN	8/10 CLKIN
1:3.5	4/14 CLKIN	1/2 CLKIN	11/14 CLKIN

Figure 2-4 is a graphical representation of **Table 2-12**.

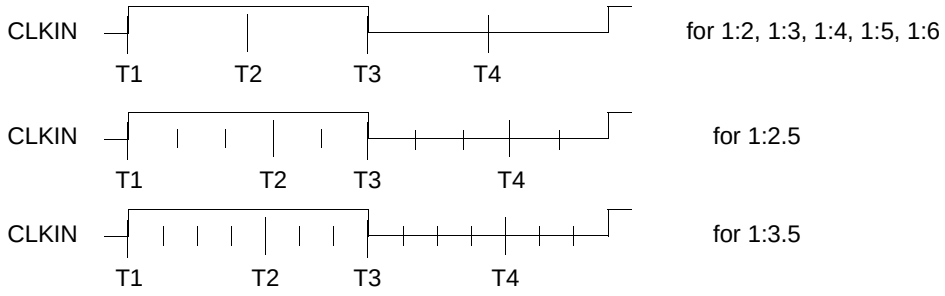


Figure 2-4. Internal Tick Spacing for Memory Controller Signals

Note: The UPM machine and GPCM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. SDRAM machine outputs change only on the CLKIN rising edge.

Table 2-13. AC Characteristics for SIU Inputs

Number	Characteristic	Value	Units
10	Hold time for all signals after CLKIN rising edge	0.5	ns
11	$\overline{\text{AACK}}$/$\overline{\text{ARTRY}}$/$\overline{\text{TA}}$/$\overline{\text{TEA}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$ setup time before CLKIN rising edge	5	ns
12	Data bus setup time before CLKIN rising edge a. Normal mode b. ECC and parity mode	 4.55 6	 ns ns
14	DP setup time before CLKIN rising edge	6	ns
15	Setup time before CLKIN rising edge for all other signals	4	ns
Note: Input specifications are measured from the TTL signal level (0.8 or 2.0 V) relative to the CLKIN rising edge.			

Table 2-14. AC Characteristics for SIU Outputs

Number	Characteristic	Maximum	Minimum	Units
31	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$ delay from CLKIN rising edge	9	0.5	ns
32a	Address bus/Address attributes/$\overline{\text{GBL}}$ delay from CLKIN rising edge	8.5	0.5	ns
32b	BADDR delay from CLKIN rising edge	10	0.5	ns
33a	Data bus delay from CLKIN rising edge	8.5	0.5	ns
33b	DP delay from CLKIN rising edge	10	0.5	ns
34	Memory controller signals/ALE delay from CLKIN rising edge	5.5	0.5	ns
35	All other signals delay from CLKIN rising edge	6	0.5	ns
Note: Output specifications are measured from the 1.4 V level of the CLKIN rising edge to the TTL signal level (0.8 or 2.0 V).				

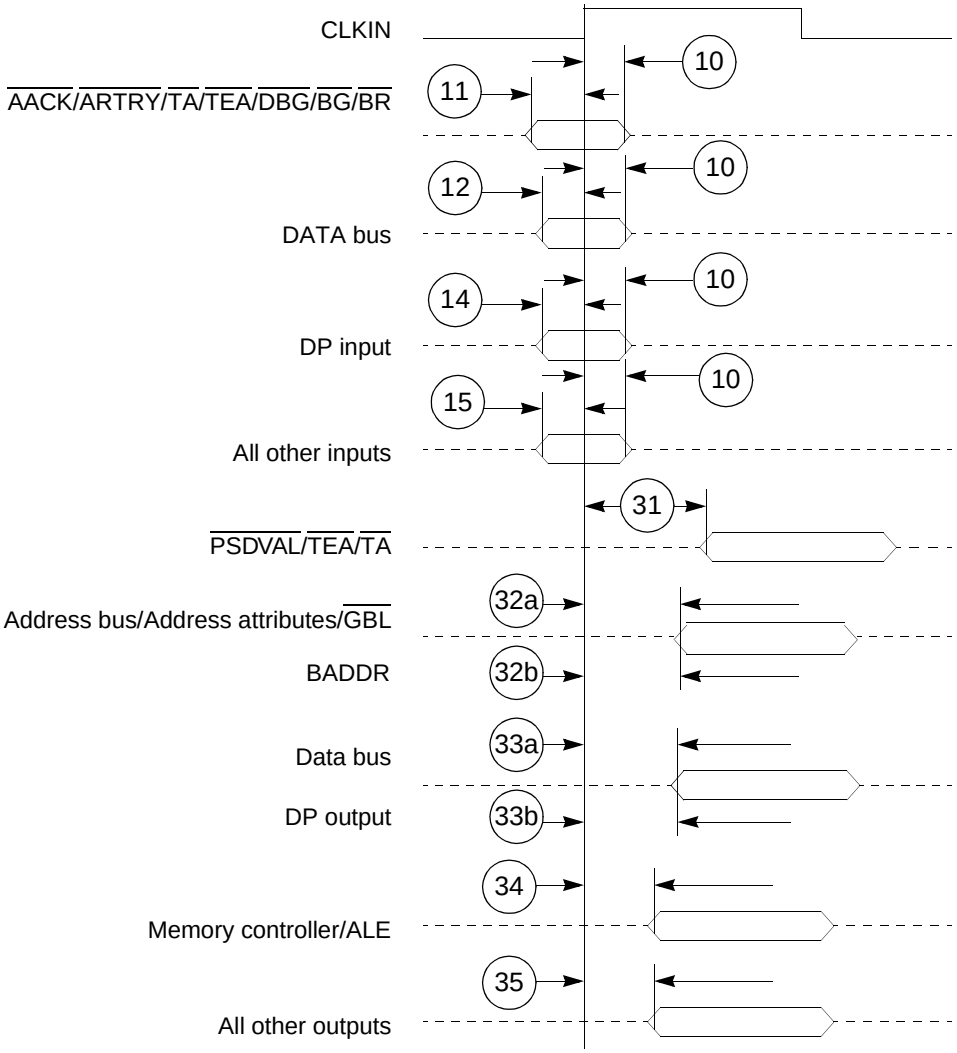


Figure 2-5. Bus Signals

2.5.3.2 DMA Data Transfers

Table 2-15 describes the DMA signals.

Table 2-15. DMA Signals

Number	Characteristic	Minimum	Maximum	Units
36	DREQ setup time before CLKIN falling edge	6	—	ns
37	DREQ hold time after CLKIN falling edge	0.5	—	ns
38	$\overline{\text{DONE}}$ setup time before CLKIN rising edge	9	—	ns
39	$\overline{\text{DONE}}$ hold time after CLKIN rising edge	0.5	—	ns
40	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after CLKIN rising edge	0.5	9	ns

The DREQ signal is synchronized with the falling edge of CLKIN. $\overline{\text{DONE}}$ timing is relative to the rising edge of CLKIN. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 2-15**. **Figure 2-6** shows synchronous peripheral interaction.

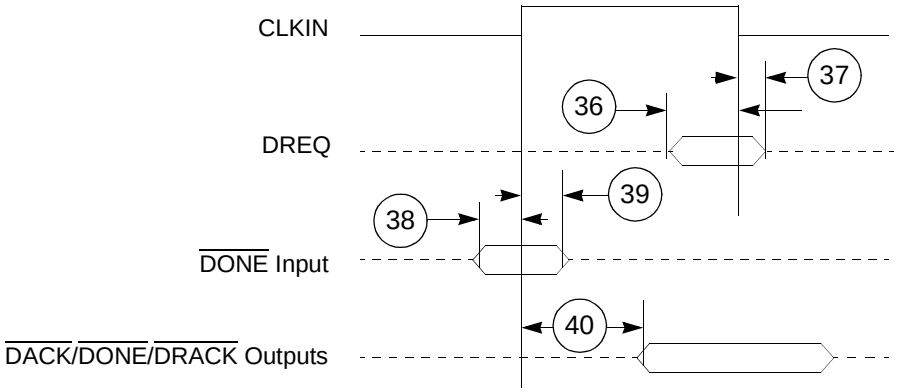


Figure 2-6. DMA Signals

2.5.4 HDI16 Signals

Table 2-16. Host Interface (HDI16) Timing[1, 2]

Number	Characteristics[3]	Expression	Min	Max	Unit
42	Read data strobe assertion width[4] HACK read assertion width	$T_C + 3.3$	6.6	—	ns
43	Read data strobe deassertion width[4] HACK read deassertion width	$T_C + 3.3$	6.6	—	ns
44	Read data strobe deassertion width[4] after "Last Data Register" reads[5,6], or between two consecutive CVR, ICR, or ISR reads[7] HACK deassertion width after "Last Data Register" reads[5,6]	$(2.5 \times T_C) + 3.3$	11.6	—	ns
45	Write data strobe assertion width[8] HACK write assertion width	$T_C + 3.3$	6.6	—	ns
46	Write data strobe deassertion width[8] HACK write deassertion width after ICR, CVR and Data Register writes[5]	$(2.5 \times T_C) + 3.3$	11.6	—	ns
47	Host data input setup time before write data strobe deassertion[8] Host data input setup time before HACK write deassertion	—	3.3	—	ns
48	Host data input hold time after write data strobe deassertion[8] Host data input hold time after HACK write deassertion	—	3.3	—	ns
49	Read data strobe assertion to output data active from high impedance[4] HACK read assertion to output data active from high impedance	—	3.3	—	ns
50	Read data strobe assertion to output data valid[4] HACK read assertion to output data valid	$(1.5 \times T_C) + 3.3$	—	8.25	ns
51	Read data strobe deassertion to output data high impedance[4] HACK read deassertion to output data high impedance	—	—	3.3	ns
52	Output data hold time after read data strobe deassertion[4] Output data hold time after HACK read deassertion	—	3.3	—	ns
53	HCS[1–2] assertion to read data strobe deassertion[4]	$T_C + 3.3$	6.6	—	ns
54	HCS[1–2] assertion to write data strobe deassertion[8]	$T_C + 3.3$	6.6	—	ns

Table 2-16. Host Interface (HDI16) Timing[1, 2] (Continued)

Number	Characteristics[3]	Expression	Min	Max	Unit
55	$\overline{\text{HCS}}$[1–2] assertion to output data valid	T_C + 3.3	—	6.6	ns
56	$\overline{\text{HCS}}$[1–2] hold time after data strobe deassertion[9]	—	0.0	—	ns
57	HA[0–3], HRW setup time before data strobe assertion[9] ■ Read ■ Write	—	 0 3.3	 — —	 ns ns
58	HA[0–3], HRW hold time after data strobe deassertion[9]	—	3.3	—	ns
59	Delay from read data strobe deassertion to host request assertion for “Last Data Register” read[4, 5, 10]	$(2.5 \times T_C) + 3.3$	11.6	—	ns
60	Delay from write data strobe deassertion to host request assertion for “Last Data Register” write[5,8,10]	$(2.5 \times T_C) + 3.3$	11.6	—	ns
61	Delay from read data strobe deassertion to host request deassertion for “Last Data Register” read[4, 5, 10]	$(2.5 \times T_C) + 3.3$	—	11.6	ns
62	Delay from write data strobe deassertion to host request deassertion for “Last Data Register” write[5,8,10]	$(2.5 \times T_C) + 3.3$	—	11.6	ns
63	Delay from DMA $\overline{\text{HACK}}$ (OAD=0) or Read/Write data strobe(OAD=1) deassertion to $\overline{\text{HREQ}}$ assertion.	$(2.5 \times T_C) + 3.3$	11.6		ns
64	Delay from DMA $\overline{\text{HACK}}$ (OAD=0) or Read/Write data strobe(OAD=1) assertion to $\overline{\text{HREQ}}$ deassertion	$(2.5 \times T_C) + 3.3$	—	11.6	ns

Note:
1. T_C = 1/ DSPCLK. At 300 MHz T_C = 3.3 ns
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. V_{CC} = 3.3 V ± 0.3 V; T_J = -40°C to +100 °C, C_L = 50 pF
4. The read data strobe is $\overline{\text{HRD}}$/HRD in the dual data strobe mode and $\overline{\text{HDS}}$/HDS in the single data strobe mode.
5. In 64-bit mode, The “last data register” is the register at address $7, which is the last location to be read or written in data transfers. This is RX0/TX0 in the little endian mode (HBE = 0), or RX3/TX3 in the big endian mode (HBE = 1).
6. This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the $\overline{\text{HREQ}}$/HREQ signal.
7. This timing is applicable only if two consecutive reads from one of these registers are executed.
8. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
9. The data strobe is host read ($\overline{\text{HRD}}$/HRD) or host write ($\overline{\text{HWR}}$/HWR) in the dual data strobe mode and host data strobe ($\overline{\text{HDS}}$/HDS) in the single data strobe mode.
10. The host request is $\overline{\text{HREQ}}$/HREQ in the single host request mode and $\overline{\text{HRRQ}}$/HRRQ and $\overline{\text{HTRQ}}$/HTRQ in the double host request mode. $\overline{\text{HRRQ}}$/HRRQ is deasserted only when HOTX fifo is empty, $\overline{\text{HTRQ}}$/HTRQ is deasserted only if HORX fifo is full (treat as level Host Request).

Figure 2-7 shows HDI16 Read signals timing.

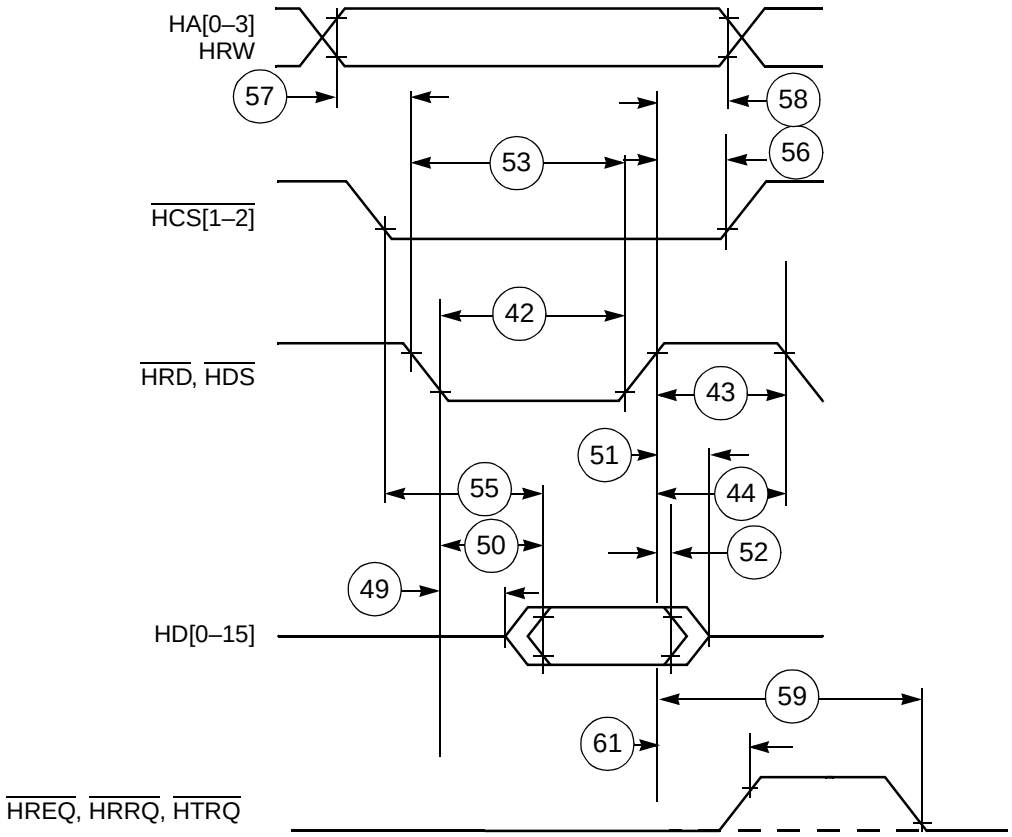


Figure 2-7. Read Timing Diagram

Figure 2-8 shows HDI16 write signals timing.

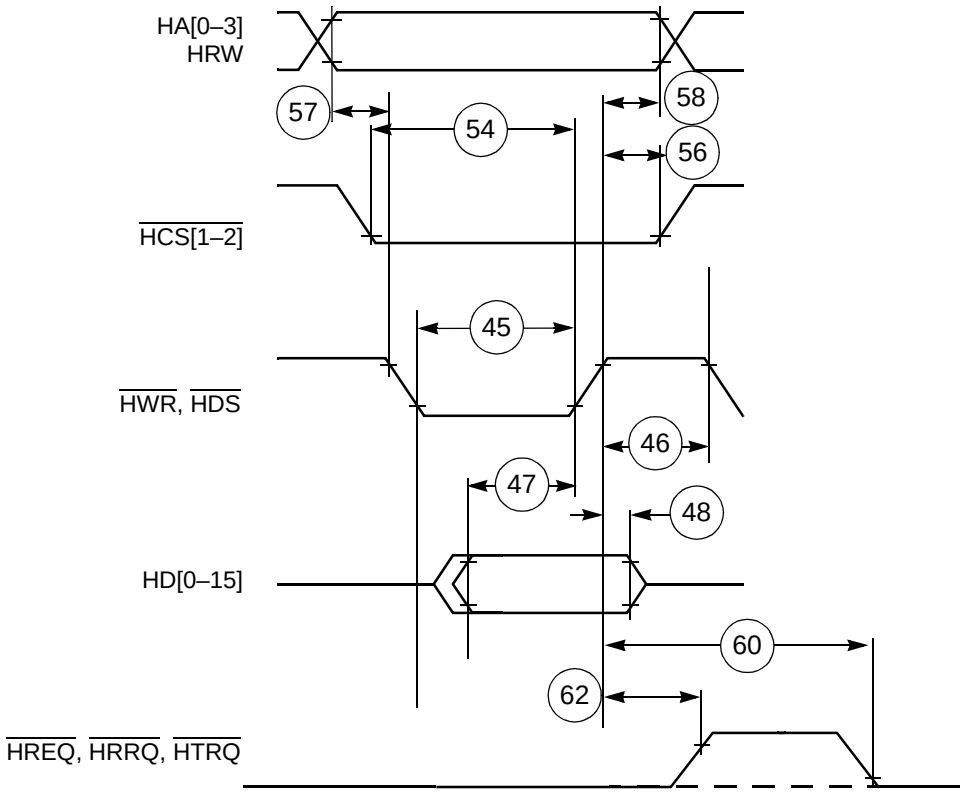


Figure 2-8. Write Timing Diagram

Figure 2-9 shows Host DMA write timing.

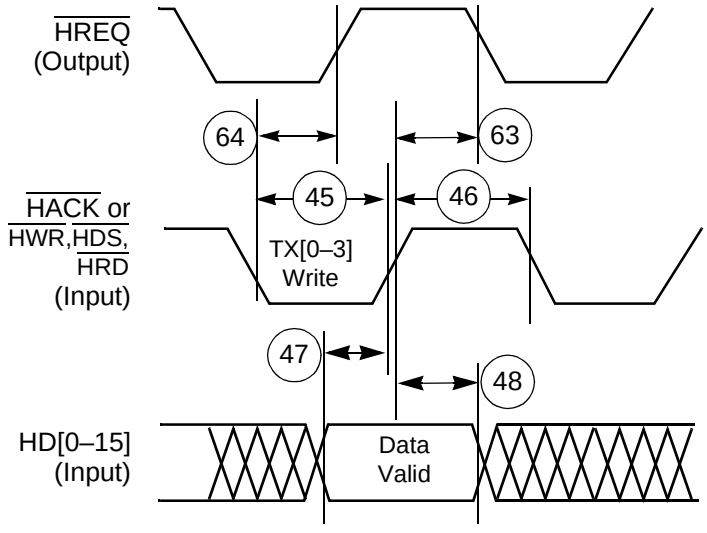


Figure 2-9. Host DMA Write Timing Diagram

Figure 2-10 shows Host DMA read timing.

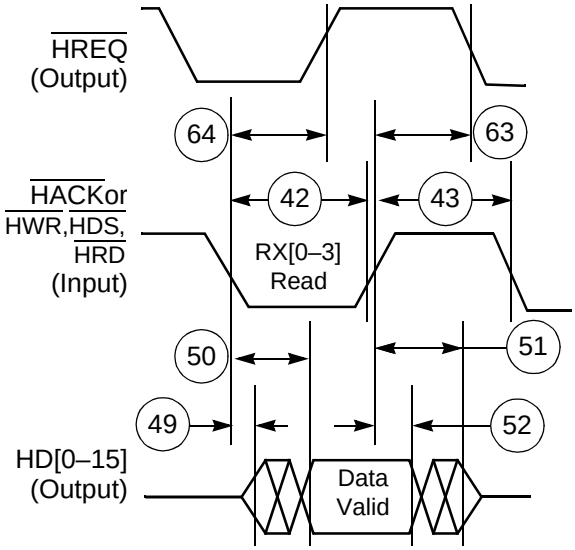


Figure 2-10. Host DMA Read Timing Diagram

2.5.5 CPM Timings

Table 2-17. CPM Input Characteristics

No.	Characteristic	Typical	Unit
16	FCC input setup time before low-to-high clock transition[1] a. internal clock (BRGxO) b. external clock (serial clock input)	 10 5	 ns ns
17	FCC input hold time after low-to-high clock transition[1] a. internal clock (BRGxO) b. external clock (serial clock input)	 0 3	 ns ns
18	SCC/SMC/SPI/I2C input setup time before low-to-high clock transition[1] a. internal clock (BRGxO) b. external clock (serial clock input)	 20 5	 ns ns
19	SCC/SMC/SPI/I^{2}C input hold time after low-to-high clock transition[1] a. internal clock (BRGxO) b. external clock (serial clock input)	 0 5	 ns ns
20	TDM input setup time before low-to-high serial clock transition	20	ns
21	TDM input hold time after low-to-high serial transition	20	ns
22	PIO/TIMER/DMA input setup time before low-to-high serial clock transition	10	ns
23	PIO/TIMER/DMA input hold time after low-to-high serial clock transition	3	ns

Note: 1. Non-Multiplexed Serial Interface signals.

Table 2-18. CPM Output Characteristics

No.	Characteristic	Min	Max	Unit
36	FCC output delay after low-to-high clock transition[1] a. internal clock (BRGxO) b. external clock (serial input clock)	 0 2	 6 18	 ns ns
38	SCC/SMC/SPI/I^{2}C output delay after low-to-high clock transition[1] a. internal clock (BRGxO) b. external clock (serial input clock)	 0 0	 20 30	 ns ns
40	TDM output delay after low-to-high serial clock transition	5	35	ns
42	PIO/TIMER/DMA output delay after low-to-high serial clock transition	1	14	ns

Note: 1. Non-Multiplexed Serial Interface signals.

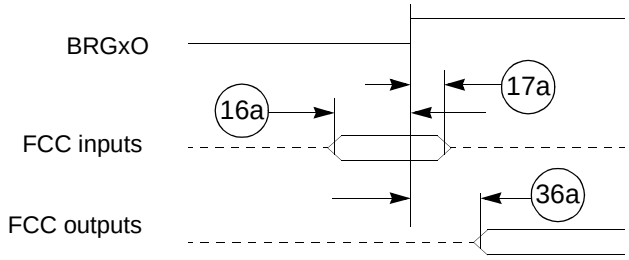


Figure 2-11. FCC Internal Clock Diagram

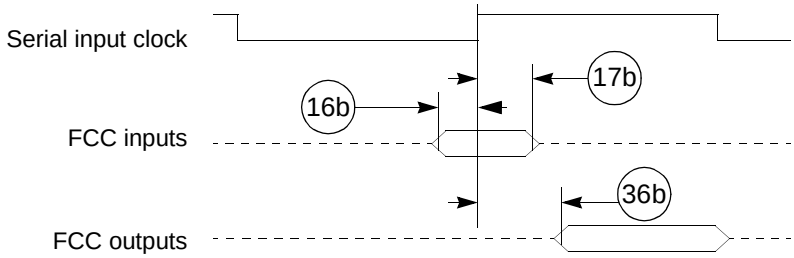


Figure 2-12. FCC External Clock Diagram

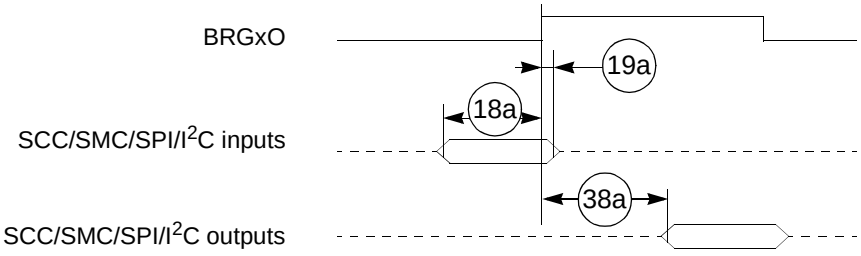


Figure 2-13. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

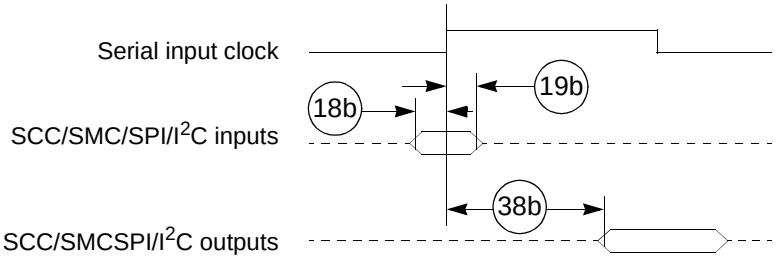


Figure 2-14. SCC/SMC/SPI/I^{2}C External Clock Diagram

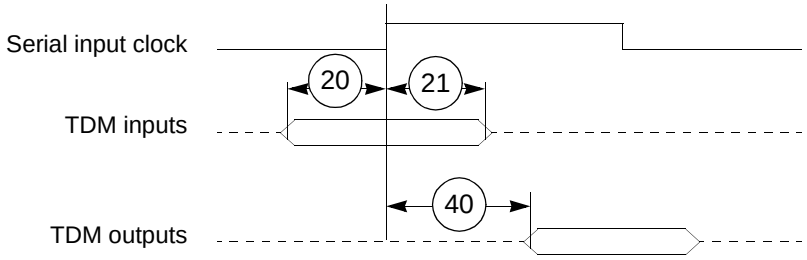


Figure 2-15. TDM Signal Diagram

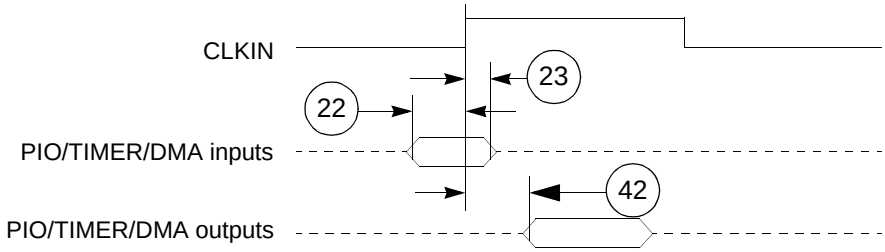


Figure 2-16. PIO, Timer, and DMA Signal Diagram

Note: The timing values listed are preliminary and refer to minimum system timing requirements. Actual implementation requires conformance to the specific protocol requirements. Refer to **Section Chapter 1**, *Signal/Connection Descriptions* to identify the specific input and output signals associated with the referenced internal controllers and supported communication protocols. For example, FCC1 supports ATM/Utopia operation in slave mode, multi-PHY master direct polling mode, and multi-PHY master multiplexed polling mode and each of these modes supports its own set of signals; the direction (input or output) of some of the shared signal names depends on the selected mode.

2.5.6 EE Signals

Table 2-19. EE Pins Timing

Number	Characteristics	Type	Minimum
65	EE pins as inputs	Asynchronous	4 GCLK periods
66	EE pins as outputs	Synchronous to GCLK	1 GCLK period

Note:
1. GCLK is the DSP core clock. The ratio between the DSP clock and CLKOUT is configured during power-on-reset. See **Table 2-6** on page 2-6.
2. Direction of the EE pins is configured in the EE_CTRL register of the EOnCE (See the *SC140 Core Reference Manual*, MNSC140CORE/D).
3. Refer to **Table 1-4** on page 1-6 for detailed information about EE pin functionality.

Figure 2-17 shows the signal behavior of the EE pins.

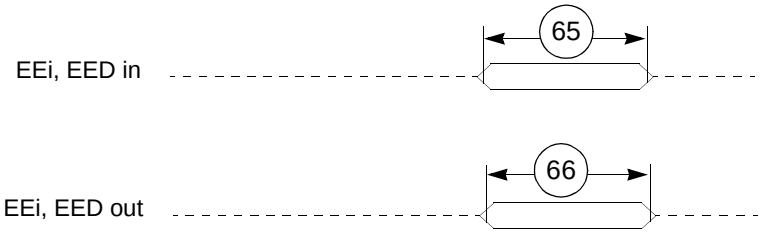


Figure 2-17. EE Pins Timing

2.5.7 JTAG Signals

Table 2-20. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
500	TCK frequency of operation	0.0	40.0	MHz
501	TCK cycle time	25.0	—	ns
502	TCK clock pulse width measured at 1.5 V	12.5	—	ns
503	TCK rise and fall times	0.0	3.0	ns
504	Boundary scan input data set-up time	5.0	—	ns
505	Boundary scan input data hold time	3.0	—	ns
506	TMS, TDI data set-up time	6.0	—	ns
507	TMS, TDI data hold time	3.0	—	ns
508	TCK low to TDO data valid	0.0	5.0	ns
509	TCK low to TDO high impedance	0.0	5.0	ns
510	$\overline{\text{TRST}}$ assert time	100.0	—	ns
511	$\overline{\text{TRST}}$ set-up time to TCK low	40.0	—	ns

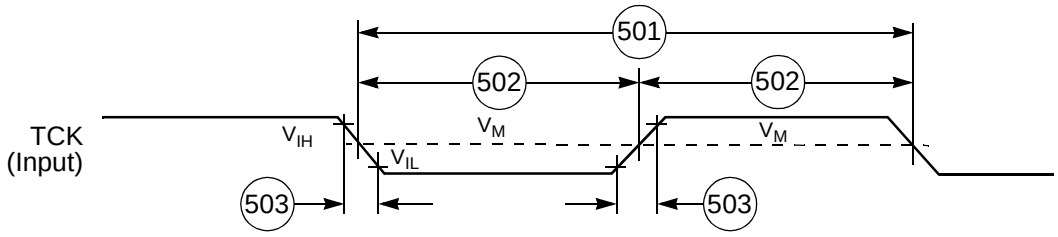


Figure 1-1. Test Clock Input Timing Diagram

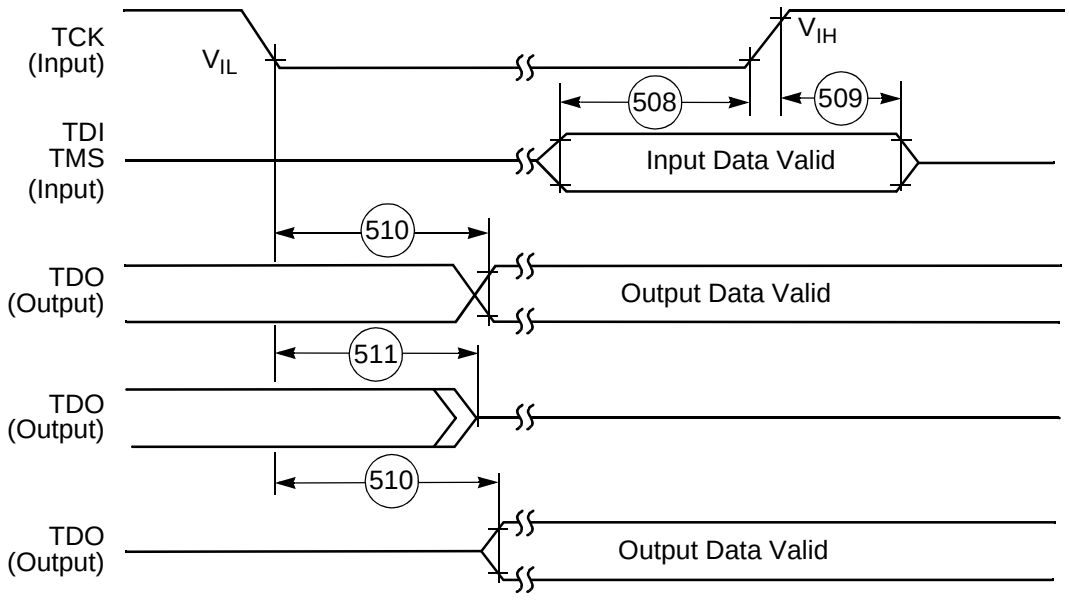


Figure 1-2. Test Access Port Timing Diagram

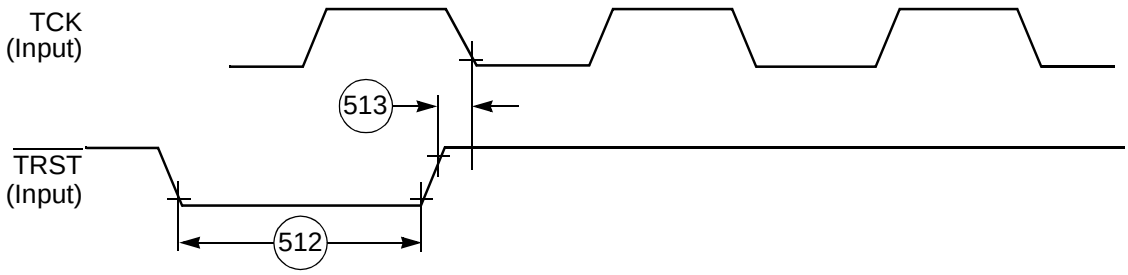


Figure 1-3. $\overline{\text{TRST}}$ Timing Diagram

Chapter 3
Packaging

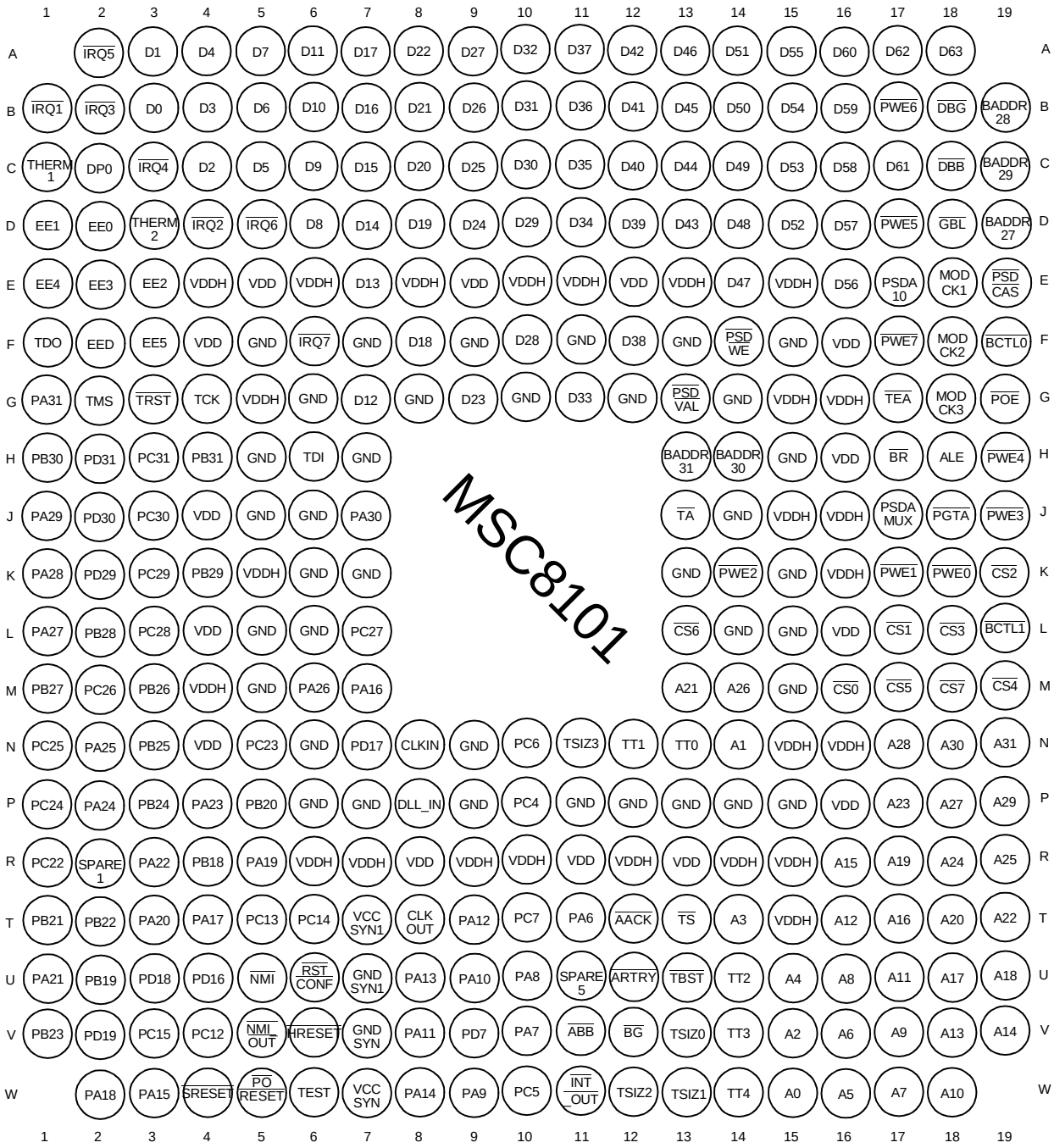
3.1 Pinout and Package Information

This sections provides information about the MSC8101 package, including diagrams of the package pinouts and tables showing how the signals discussed in **Chapter 1**, *Signal/Connection Descriptions* are allocated. The MSC8101 is available in a 332-pin Flip Chip-Plastic Ball Grid Array (FC-PBGA).

3.2 FC-PBGA Package Description

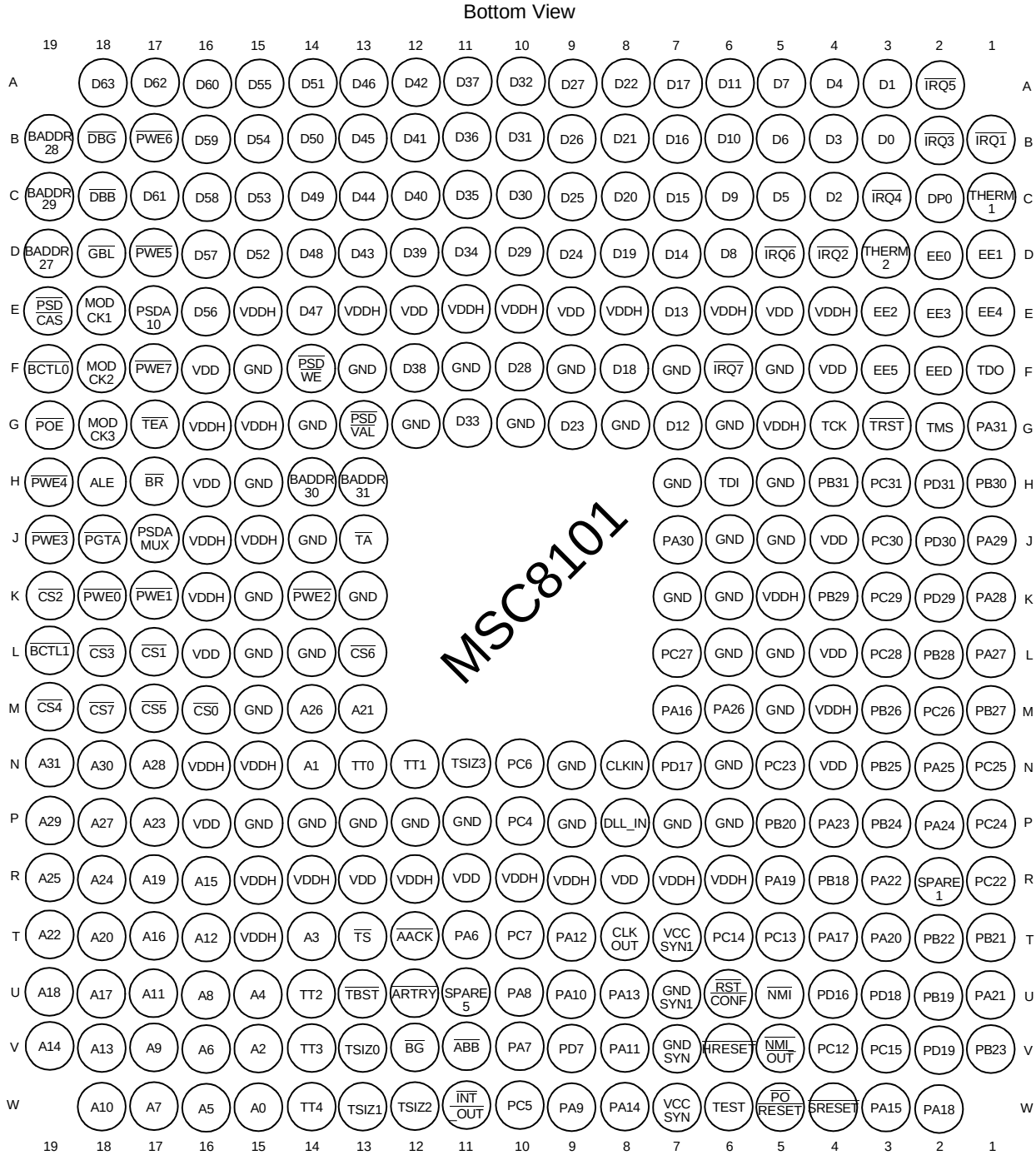
Figure 3-1 and **Figure 3-2** show top and bottom views of the FC-PBGA package, including pinouts. **Table 3-1** lists the MSC8101 signals alphabetically by signal name. Connections with multiple names are listed individually by each name. Signals with programmable polarity are shown both as signals which are asserted low (default) and high (i.e., $\overline{\text{NAME}}$/NAME). **Table 3-2** lists the signals numerically by pin number. Each pin number is listed once with the various signals that are multiplexed to it. For simplicity, signals with programmable polarity are shown in this table only with their default name (asserted low).

Top View



Note: Signal names in this figure are the default signals after reset, except for signals C2, C19, D1, D2, D18, E1, F3, H13, H14, and W11 which show the second configuration signal name.

Figure 3-1. MSC8101 Flip Chip Plastic Ball Grid Array (FC-PBGA), Top View



Note: Signal names in this figure are the default signals after reset, except for signals C2, C19, D1, D2, D18, E1, F3, H13, H14, and W11 which show the second configuration signal name.

Figure 3-2. MSC8101 Flip Chip Plastic Ball Grid Array (FC-PBGA), Bottom Vie

Table 3-1. MSC8101 Signal Listing By Name

Signal Name	Number
A0	W15
A1	N14
A2	V15
A3	T14
A4	U15
A5	W16
A6	V16
A7	W17
A8	U16
A9	V17
A10	W18
A11	U17
A12	T16
A13	V18
A14	V19
A15	R16
A16	T17
A17	U18
A18	U19
A19	R17
A20	T18
A21	M13
A22	T19
A23	P17
A24	R18
A25	R19
A26	M14
A27	P18
A28	N17
A29	P19
A30	N18

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
A31	N19
$\overline{\text{AACK}}$	T12
$\overline{\text{ABB}}$	V11
ALE	H18
$\overline{\text{ARTRY}}$	U12
BADDR27	D19
BADDR28	B19
BADDR29	C19
BADDR30	H14
BADDR31	H13
$\overline{\text{BCTL0}}$	F19
$\overline{\text{BCTL1}}$	L19
$\overline{\text{BG}}$	V12
BNKSEL0	E18
BNKSEL1	F18
BNKSEL2	G18
$\overline{\text{BR}}$	H17
BTM0	E1
BTM1	F3
CLKIN	N8
CLKOUT	T8
$\overline{\text{CS0}}$	M16
$\overline{\text{CS1}}$	L17
$\overline{\text{CS2}}$	K19
$\overline{\text{CS3}}$	L18
$\overline{\text{CS4}}$	M19
$\overline{\text{CS5}}$	M17
$\overline{\text{CS6}}$	L13
$\overline{\text{CS7}}$	M18
D0	B3
D1	A3
D2	C4

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
D3	B4
D4	A4
D5	C5
D6	B5
D7	A5
D8	D6
D9	C6
D10	B6
D11	A6
D12	G7
D13	E7
D14	D7
D15	C7
D16	B7
D17	A7
D18	F8
D19	D8
D20	C8
D21	B8
D22	A8
D23	G9
D24	D9
D25	C9
D26	B9
D27	A9
D28	F10
D29	D10
D30	C10
D31	B10
D32	A10
D33	G11
D34	D11

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
D35	C11
D36	B11
D37	A11
D38	F12
D39	D12
D40	C12
D41	B12
D42	A12
D43	D13
D44	C13
D45	B13
D46	A13
D47	E14
D48	D14
D49	C14
D50	B14
D51	A14
D52	D15
D53	C15
D54	B15
D55	A15
D56	E16
D57	D16
D58	C16
D59	B16
D60	A16
D61	C17
D62	A17
D63	A18
$\overline{\text{DBB}}$	C18
$\overline{\text{DBG}}$	B18
DBREQ	D2

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
DLLIN	P8
DP0	C2
DP1	B1
DP2	D4
DP3	B2
DP4	C3
DP5	A2
DP6	D5
DP7	F6
$\overline{\text{DACK3}}$	D5
$\overline{\text{DACK4}}$	F6
DREQ3	C3
DREQ4	A2
EE0	D2
EE1	D1
EE2	E3
EE3	E2
EE4	E1
EE5	F3
EED	F2
$\overline{\text{EXT\_BG2}}$	B1
$\overline{\text{EXT\_BG3}}$	C3
$\overline{\text{EXT\_BR2}}$	C2
$\overline{\text{EXT\_BR3}}$	B2
$\overline{\text{EXT\_DBG2}}$	D4
$\overline{\text{EXT\_DBG3}}$	A2
$\overline{\text{GBL}}$	D18
GND	F11
GND	F13
GND	F15
GND	F5
GND	F7

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
GND	F9
GND	G10
GND	G12
GND	G14
GND	G6
GND	G8
GND	H15
GND	H5
GND	H7
GND	J14
GND	J5
GND	J6
GND	K13
GND	K15
GND	K6
GND	K7
GND	L14
GND	L15
GND	L5
GND	L6
GND	M15
GND	M5
GND	N6
GND	N9
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P6
GND	P7
GND	P9

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
GNDSYN	V7
GNDSYN1	U7
H8BIT	B16
HA0	D14
HA1	C14
HA2	B14
HA3	A14
$\overline{\text{HACK}}$/HACK	E16
$\overline{\text{HCS1}}$/HCS1	D15
$\overline{\text{HCS2}}$/HCS2	A16
HD0	A10
HD1	G11
HD2	D11
HD3	C11
HD4	B11
HD5	A11
HD6	F12
HD7	D12
HD8	C12
HD9	B12
HD10	A12
HD11	D13
HD12	C13
HD13	B13
HD14	A13
HD15	E14
HDDS	C16
$\overline{\text{HDS}}$ /HDS	B15
HDSP	D16
HPE	D1
$\overline{\text{HRD}}$/HRD	C15
$\overline{\text{HREQ}}$/HREQ	A15

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
$\overline{\text{HRESET}}$	V6
$\overline{\text{HRRQ}}$/HRRQ	E16
HRW	C15
$\overline{\text{HTRQ}}$/HTRQ	A15
$\overline{\text{HWR}}$/HWR	B15
$\overline{\text{INT\_OUT}}$	W11
$\overline{\text{IRQ1}}$	B1
$\overline{\text{IRQ1}}$	D18
$\overline{\text{IRQ2}}$	C19
$\overline{\text{IRQ2}}$	D4
$\overline{\text{IRQ2}}$	V11
$\overline{\text{IRQ3}}$	B2
$\overline{\text{IRQ3}}$	C18
$\overline{\text{IRQ3}}$	H14
$\overline{\text{IRQ4}}$	C3
$\overline{\text{IRQ5}}$	A2
$\overline{\text{IRQ5}}$	H13
$\overline{\text{IRQ6}}$	D5
$\overline{\text{IRQ7}}$	F6
$\overline{\text{IRQ7}}$	W11
MODCK1	E18
MODCK2	F18
MODCK3	G18
$\overline{\text{NMI}}$	U5
$\overline{\text{NMI\_OUT}}$	V5
PA6	T11
PA7	V10
PA8	U10
PA9	W9
PA10	U9
PA11	V8
PA12	T9

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
PA13	U8
PA14	W8
PA15	W3
PA16	M7
PA17	T4
PA18	W2
PA19	R5
PA20	T3
PA21	U1
PA22	R3
PA23	P4
PA24	P2
PA25	N2
PA26	M6
PA27	L1
PA28	K1
PA29	J1
PA30	J7
PA31	G1
PB18	R4
PB19	U2
PB20	P5
PB21	T1
PB22	T2
PB23	V1
PB24	P3
PB25	N3
PB26	M3
PB27	M1
PB28	L2
PB29	K4
PB30	H1

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
PB31	H4
$\overline{\text{PBS0}}$	K18
$\overline{\text{PBS1}}$	K17
$\overline{\text{PBS2}}$	K14
$\overline{\text{PBS3}}$	J19
$\overline{\text{PBS4}}$	H19
$\overline{\text{PBS5}}$	D17
$\overline{\text{PBS6}}$	B17
$\overline{\text{PBS7}}$	F17
PC4	P10
PC5	W10
PC6	N10
PC7	T10
PC12	V4
PC13	T5
PC14	T6
PC15	V3
PC22	R1
PC23	N5
PC24	P1
PC25	N1
PC26	M2
PC27	L7
PC28	L3
PC29	K3
PC30	J3
PC31	H3
PD7	V9
PD16	U4
PD17	N7
PD18	U3
PD19	V2

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
PD29	K2
PD30	J2
PD31	H2
PGPL0	E17
PGPL1	F14
PGPL2	G19
PGPL3	E19
PGPL4	J18
PGPL5	J17
$\overline{\text{PGTA}}$	J18
$\overline{\text{POE}}$	G19
$\overline{\text{PORESET}}$	W5
$\overline{\text{PPBS}}$	J18
PSDA10	E17
PSDAMUX	J17
$\overline{\text{PSDCAS}}$	E19
$\overline{\text{PSDDQM0}}$	K18
$\overline{\text{PSDDQM1}}$	K17
$\overline{\text{PSDDQM2}}$	K14
$\overline{\text{PSDDQM3}}$	J19
$\overline{\text{PSDDQM4}}$	H19
$\overline{\text{PSDDQM5}}$	D17
$\overline{\text{PSDDQM6}}$	B17
$\overline{\text{PSDDQM7}}$	F17
$\overline{\text{PSDRAS}}$	G19
$\overline{\text{PSDVAL}}$	G13
$\overline{\text{PSDWE}}$	F14
PUPMWAIT	J18
$\overline{\text{PWE0}}$	K18
$\overline{\text{PWE1}}$	K17
$\overline{\text{PWE2}}$	K14
$\overline{\text{PWE3}}$	J19

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
$\overline{\text{PWE4}}$	H19
$\overline{\text{PWE5}}$	D17
$\overline{\text{PWE6}}$	B17
$\overline{\text{PWE7}}$	F17
Reserved	A17
Reserved	A18
Reserved	C2
Reserved	C17
Reserved	C19
Reserved	H14
Reserved	H13
$\overline{\text{RSTCONF}}$	U6
SPARE1	R2
SPARE5	U11
$\overline{\text{SRESET}}$	W4
$\overline{\text{TA}}$	J13
$\overline{\text{TBST}}$	U13
TC0	E18
TC1	F18
TC2	G18
TCK	G4
TDI	H6
TDO	F1
$\overline{\text{TEA}}$	G17
TEST	W6
THERM1	C1
THERM2	D3
TMS	G2
$\overline{\text{TRST}}$	G3
$\overline{\text{TS}}$	T13
TSZ0	V13
TSZ1	W13

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
TSZ2	W12
TSZ3	N11
TT0	N13
TT1	N12
TT2	U14
TT3	V14
TT4	W14
VCCSYN	W7
VCCSYN1	T7
VDD	E12
VDD	E5
VDD	E9
VDD	F16
VDD	F4
VDD	H16
VDD	J4
VDD	L16
VDD	L4
VDD	N4
VDD	P16
VDD	R11
VDD	R13
VDD	R8
VDDH	E10
VDDH	E11
VDDH	E13
VDDH	E15
VDDH	E4
VDDH	E6
VDDH	E8
VDDH	G15
VDDH	G16

Table 3-1. MSC8101 Signal Listing By Name (Continued)

Signal Name	Number
VDDH	G5
VDDH	J15
VDDH	J16
VDDH	K16
VDDH	K5
VDDH	M4
VDDH	N15
VDDH	N16
VDDH	R10
VDDH	R12
VDDH	R14
VDDH	R15
VDDH	R6
VDDH	R7
VDDH	R9
VDDH	T15

Table 3-2. MSC8101 Signal Listing by Pin Designator

Number	Signal Name
A2	$\overline{\text{IRQ5}}$ / DP5 / DREQ4 / $\overline{\text{EXT\_DBG3}}$
A3	D1
A4	D4
A5	D7
A6	D11
A7	D17
A8	D22
A9	D27
A10	D32 / HD0
A11	D37 / HD5
A12	D42 / HD10
A13	D46 / HD14

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
A14	D51 / HA3
A15	D55 / $\overline{\text{HREQ}}$ / $\overline{\text{HTRQ}}$
A16	D60 / $\overline{\text{HCS2}}$
A17	D62 / Reserved
A18	D63 / Reserved
B1	$\overline{\text{IRQ1}}$ / DP1 / $\overline{\text{EXT\_BG2}}$
B2	$\overline{\text{IRQ3}}$ / DP3 / $\overline{\text{EXT\_BR3}}$
B3	D0
B4	D3
B5	D6
B6	D10
B7	D16
B8	D21
B9	D26
B10	D31
B11	D36 / HD4
B12	D41 / HD9
B13	D45 / HD13
B14	D50 / HA2
B15	D54 / $\overline{\text{HDS}}$ / $\overline{\text{HWR}}$
B16	D59 / H8BIT
B17	$\overline{\text{PWE6}}$ / $\overline{\text{PSDDQM6}}$ / $\overline{\text{PBS6}}$
B18	$\overline{\text{DBG}}$
B19	BADDR28
C1	THERM1
C2	Reserved / DP0 / $\overline{\text{EXT\_BR2}}$
C3	$\overline{\text{IRQ4}}$ / DP4 / DREQ3 / $\overline{\text{EXT\_BG3}}$
C4	D2
C5	D5
C6	D9
C7	D15
C8	D20

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
C9	D25
C10	D30
C11	D35 / HD3
C12	D40 / HD8
C13	D44 / HD12
C14	D49 / HA1
C15	D53 / HRW / $\overline{\text{HRD}}$
C16	D58 / HDDS
C17	D61
C18	$\overline{\text{DBB}}$ / $\overline{\text{IRQ3}}$
C19	BADDR29 / $\overline{\text{IRQ2}}$
D1	HPE / EE1
D2	DBREQ / EE0
D3	THERM2
D4	$\overline{\text{IRQ2}}$ / DP2 / $\overline{\text{EXT\_DBG2}}$
D5	$\overline{\text{IRQ6}}$ / DP6 / $\overline{\text{DACK3}}$
D6	D8
D7	D14
D8	D19
D9	D24
D10	D29
D11	D34 / HD2
D12	D39 / HD7
D13	D43 / HD11
D14	D48 / HA0
D15	D52 / $\overline{\text{HCS1}}$
D16	D57 / HDSP
D17	$\overline{\text{PWE5}}$ / $\overline{\text{PSDDQM5}}$ / $\overline{\text{PBS5}}$
D18	$\overline{\text{IRQ1}}$ / $\overline{\text{GBL}}$
D19	BADDR27
E1	BTM0 / EE4
E2	EE3

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
E3	EE2
E4	VDDH
E5	VDD
E6	VDDH
E7	D13
E8	VDDH
E9	VDD
E10	VDDH
E11	VDDH
E12	VDD
E13	VDDH
E14	D47 / HD15
E15	VDDH
E16	D56 / $\overline{\text{HACK}}$ / $\overline{\text{HRRQ}}$
E17	PSDA10 / PGPL0
E18	MODCK1 / TC0 / BNKSEL0
E19	$\overline{\text{PSDCAS}}$ / PGPL3
F1	TDO
F2	EED
F3	BTM1 / EE5
F4	VDD
F5	GND
F6	$\overline{\text{IRQ7}}$ / DP7 / $\overline{\text{DACK4}}$
F7	GND
F8	D18
F9	GND
F10	D28
F11	GND
F12	D38 / HD6
F13	GND
F14	$\overline{\text{PSDWE}}$ / PGPL1
F15	GND

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
F16	VDD
F17	$\overline{\text{PWE7}}$ / $\overline{\text{PSDDQM7}}$ / $\overline{\text{PBS7}}$
F18	MODCK2 / TC1 / BNKSEL1
F19	$\overline{\text{BCTL0}}$
G1	PA31
G2	TMS
G3	$\overline{\text{TRST}}$
G4	TCK
G5	VDDH
G6	GND
G7	D12
G8	GND
G9	D23
G10	GND
G11	D33 / HD1
G12	GND
G13	$\overline{\text{PSDVAL}}$
G14	GND
G15	VDDH
G16	VDDH
G17	$\overline{\text{TEA}}$
G18	MODCK3 / TC2 / BNKSEL2
G19	$\overline{\text{POE}}$ / $\overline{\text{PSDRAS}}$ / PGPL2
H1	PB30
H2	PD31
H3	PC31
H4	PB31
H5	GND
H6	TDI
H7	GND
H13	Reserved / BADDR31 / $\overline{\text{IRQ5}}$
H14	Reserved / BADDR30 / $\overline{\text{IRQ3}}$

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
H15	GND
H16	VDD
H17	$\overline{\text{BR}}$
H18	ALE
H19	$\overline{\text{PWE4}}$ / $\overline{\text{PSDDQM4}}$ / $\overline{\text{PBS4}}$
J1	PA29
J2	PD30
J3	PC30
J4	VDD
J5	GND
J6	GND
J7	PA30
J13	$\overline{\text{TA}}$
J14	GND
J15	VDDH
J16	VDDH
J17	PSDAMUX / PGPL5
J18	$\overline{\text{PGTA}}$ / PUPMWAIT / $\overline{\text{PPBS}}$ / PGPL4
J19	$\overline{\text{PWE3}}$ / $\overline{\text{PSDDQM3}}$ / $\overline{\text{PBS3}}$
K1	PA28
K2	PD29
K3	PC29
K4	PB29
K5	VDDH
K6	GND
K7	GND
K13	GND
K14	$\overline{\text{PWE2}}$ / $\overline{\text{PSDDQM2}}$ / PBS2
K15	GND
K16	VDDH
K17	$\overline{\text{PWE1}}$ / $\overline{\text{PSDDQM1}}$ / $\overline{\text{PBS1}}$
K18	$\overline{\text{PWE0}}$ / $\overline{\text{PSDDQM0}}$ / $\overline{\text{PBS0}}$

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
K19	$\overline{CS2}$
L1	PA27
L2	PB28
L3	PC28
L4	VDD
L5	GND
L6	GND
L7	PC27
L13	$\overline{CS6}$
L14	GND
L15	GND
L16	VDD
L17	$\overline{CS1}$
L18	$\overline{CS3}$
L19	$\overline{BCTL1}$
M1	PB27
M2	PC26
M3	PB26
M4	VDDH
M5	GND
M6	PA26
M7	PA16
M13	A21
M14	A26
M15	GND
M16	$\overline{CS0}$
M17	$\overline{CS5}$
M18	$\overline{CS7}$
M19	$\overline{CS4}$
N1	PC25
N2	PA25
N3	PB25

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
N4	VDD
N5	PC23
N6	GND
N7	PD17
N8	CLKIN
N9	GND
N10	PC6
N11	TSZ3
N12	TT1
N13	TT0
N14	A1
N15	VDDH
N16	VDDH
N17	A28
N18	A30
N19	A31
P1	PC24
P2	PA24
P3	PB24
P4	PA23
P5	PB20
P6	GND
P7	GND
P8	DLLIN
P9	GND
P10	PC4
P11	GND
P12	GND
P13	GND
P14	GND
P15	GND
P16	VDD

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
P17	A23
P18	A27
P19	A29
R1	PC22
R2	SPARE1
R3	PA22
R4	PB18
R5	PA19
R6	VDDH
R7	VDDH
R8	VDD
R9	VDDH
R10	VDDH
R11	VDD
R12	VDDH
R13	VDD
R14	VDDH
R15	VDDH
R16	A15
R17	A19
R18	A24
R19	A25
T1	PB21
T2	PB22
T3	PA20
T4	PA17
T5	PC13
T6	PC14
T7	VCCSYN1
T8	CLKOUT
T9	PA12
T10	PC7

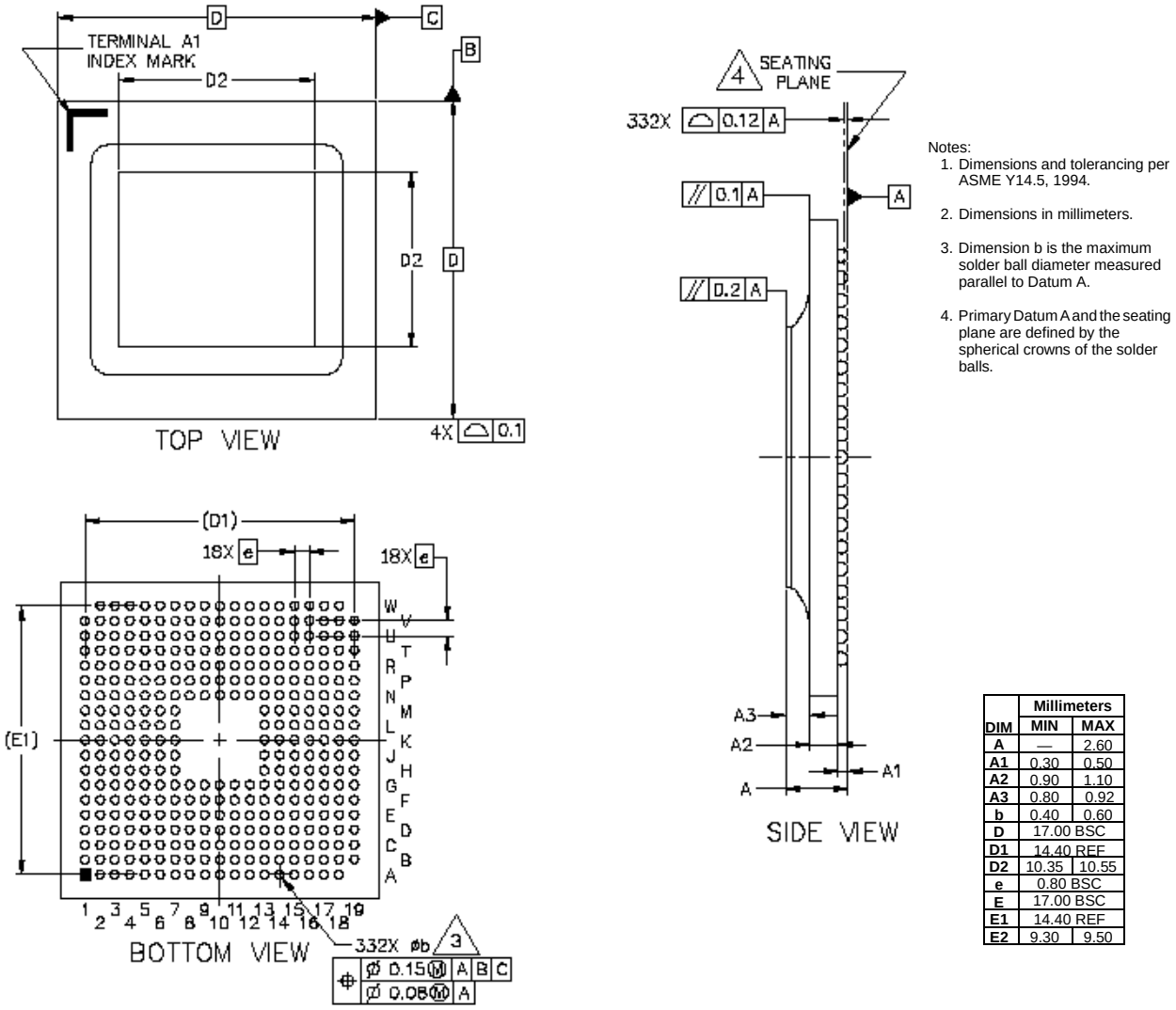
Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
T11	PA6
T12	$\overline{\text{AACK}}$
T13	$\overline{\text{TS}}$
T14	A3
T15	VDDH
T16	A12
T17	A16
T18	A20
T19	A22
U1	PA21
U2	PB19
U3	PD18
U4	PD16
U5	$\overline{\text{NMI}}$
U6	$\overline{\text{RSTCONF}}$
U7	GNDSYN1
U8	PA13
U9	PA10
U10	PA8
U11	SPARE5
U12	$\overline{\text{ARTRY}}$
U13	$\overline{\text{TBST}}$
U14	TT2
U15	A4
U16	A8
U17	A11
U18	A17
U19	A18
V1	PB23
V2	PD19
V3	PC15
V4	PC12

Table 3-2. MSC8101 Signal Listing by Pin Designator (Continued)

Number	Signal Name
V5	$\overline{\text{NMI\_OUT}}$
V6	$\overline{\text{HRESET}}$
V7	GNDSYN
V8	PA11
V9	PD7
V10	PA7
V11	$\overline{\text{ABB}}$ / $\overline{\text{IRQ2}}$
V12	$\overline{\text{BG}}$
V13	TSZ0
V14	TT3
V15	A2
V16	A6
V17	A9
V18	A13
V19	A14
W2	PA18
W3	PA15
W4	$\overline{\text{SRESET}}$
W5	$\overline{\text{PORESET}}$
W6	TEST
W7	VCCSYN
W8	PA14
W9	PA9
W10	PC5
W11	$\overline{\text{IRQ7}}$ / $\overline{\text{INT\_OUT}}$
W12	TSZ2
W13	TSZ1
W14	TT4
W15	A0
W16	A5
W17	A7
W18	A10

3.3 FC-PBGA Package Mechanical Drawing



Notes:
1. Dimensions and tolerancing per ASME Y14.5, 1994.
2. Dimensions in millimeters.
3. Dimension b is the maximum solder ball diameter measured parallel to Datum A.
4. Primary Datum A and the seating plane are defined by the spherical crowns of the solder balls.

	Millimeters	
DIM	MIN	MAX
A	—	2.60
A1	0.30	0.50
A2	0.90	1.10
A3	0.80	0.92
b	0.40	0.60
D	17.00 BSC	
D1	14.40 REF	
D2	10.35	10.55
e	0.80 BSC	
E	17.00 BSC	
E1	14.40 REF	
E2	9.30	9.50

CASE 1169-01

Figure 3-3. MSC8101 Mechanical Information, 332-pin FC-PBGA Package

Chapter 4
Design Considerations

4.1 Thermal Design Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

Equation 1: $T_J = T_A + (P_D \bullet \theta_{JA})$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$ in W

$P_{INT} = I_{DD} \times V_{DD}$ in W—chip internal power

$P_{I/O}$ = power dissipation on output pins in W—user determined

The user should set T_A and P_D such that T_J does not exceed the maximum operating conditions. In case T_J is too high, the user should either lower the ambient temperature or the power dissipation of the chip.

4.2 Electrical Design Considerations

Not yet implemented.

4.3 Power Considerations

The internal power dissipation consists of three components:

$$P_{INT} = P_{CORE} + P_{SIU} + P_{CPM}$$

The power dissipation depends on the operating frequency of the different portions of the chip. The numbers given in **Table 4-1** refer to 300 MHz core frequency, 150 MHz CPM frequency, and 100 MHz SIU frequency.

To determine the power dissipation at a given frequency, the following equations should be applied:

$$P_{CORE}\ (f) = ((P_{CORE} - P_{LCO})/300) \times f + P_{LCO}$$

$$P_{SIU}\ (f) = ((P_{SIU} - P_{LSI})/100) \times f + P_{LSI}$$

$$P_{CPM}\ (f) = ((P_{CPM} - P_{LCP})/150) \times f + P_{LCP}$$

Where f is the operating frequency in MHz and all power numbers are in mW.

To determine a total power dissipation in a specific application, the following equation should be applied for each I/O output pin:

Equation 2: $P = C \times V_{DDH}^2 \times f \times 10^{-3}$

Where: P = power in mW, C = load capacitance in pF, f = output switching frequency in MHz.

Example:

For an application in which external data memory is used in a 32-bit single bus mode and no other outputs are active, the core runs at 200 MHz, the CPM runs at 100 MHz and the SIU runs at 50 MHz, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every second cycle with 10% of address pins switching.
- External data memory writes occurs once every eight cycles with 50% of data pins switching.
- Each address and data pin has a 30 pF total load at the pin.
- The application operates at VDDH = 3.3 V.

Since the address pins switch once at every second cycle, the address pins frequency is a quarter of the bus frequency (i.e., 25 MHz).

For the same reason the data pins frequency is 3.125 MHz.

Table 4-1. Power Dissipation

Pins	# of pins switching	$\times$ C	$\times V_{DDH}^2$	$\times f \times 10^{-3}$	Power in mW
Address	4	$\times$ 30	$\times 3.3^2$	$\times 12.5 \times 10^{-3}$	16.25
Data, $\overline{HRD}$, $\overline{HRW}$	34	$\times$ 30	$\times 3.3^2$	$\times 3.125 \times 10^{-3}$	34.75
CLKOUT	1	$\times$ 30	$\times 3.3^2$	$\times 50 \times 10^{-3}$	16
Total $P_{I/O}$					67

Calculating internal power:

P_{CORE} (200) = ((P_{CORE} – P_{LCO})/300) × 200 + P_{LCO} =((250 – 3) / 300 × 200 + 3=168

P_{SIU} (50) = ((P_{SIU} – P_{LSI}) / 100) × 50 + P_{LSI} = ((70 – 2) / 100) × 50 + 2 = 36

P_{CPM} (100) = ((P_{CPM} – P_{LCP}) / 150) × 100 + P_{LCP} = ((210 – 6) / 150) × 100 + 6 = 142

P_{INT} = P_{CORE}(200) + P_{SIU}(50) + P_{CPM}(100) =168 + 36 + 142 = 346

P_D = P_{INT} + $P_{I/O}$ = 346 + 67 = 413

Maximum allowed ambient temperature is:

TA = TJ – (PD × θ_{JA})

4.4 Layout Practices

Each VCC and VDD pin on the MSC8101 should be provided with a low-impedance path to the board's power supply. Similarly, each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The VCC power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip VCC, VDD, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as VCC and GND planes.

All output pins on the MSC8101 have fast rise and fall times. Printed circuit board (PCB) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PCB trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VCC, VDD, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

There are 2 pairs of PLL supply pins: VCCSYN-GNDSYN and VCCSYN1-GNDSYN1. Each pair supplies one PLL. To ensure internal clock stability, filter the power to the VCCSYN and VCCSYN1 inputs with a circuit similar to the one in **Figure 4-1**. To filter as much noise as possible, place the circuit as close as possible to VCCSYN and VCCSYN1. The 0.1-µF capacitor should be closest to VCCSYN and VCCSYN1, followed by the 10-µF capacitor, and finally the 10-Ω resistor to VDD. These traces should be kept short and direct.

GNDSYN and GNDSYN1 should be provided with an extremely low impedance path to ground and should be bypassed to VCCSYN and VCCSYN1, respectively, by a 0.1-µF capacitor located as close as possible to the chip package. The user should also bypass GNDSYN and GNDSYN1 to VCCSYN and VCCSYN1 with a 0.01-µF capacitor as closely as possible to the chip package

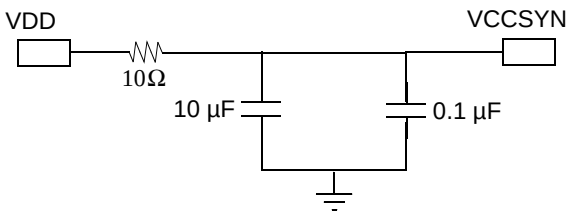


Figure 4-1. VCCSYN and VCCSYN1 Bypass

ORDERING INFORMATION

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and to place an order.

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
MSC8101	1.5 V core 3.3 V I/O	Flip Chip Plastic Ball Grid Array (FC-PBGA)	332	300	TBD

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