OKI semiconductor

T-52-13-09

MSC7110-xx / MSC7112-xx

12-SEGMENT, 16-DIGIT / 16-SEGMENT, 12-DIGIT

GENERAL DESCRIPTION

The MSC7110-xx and MSC7112-xx are general purpose display controllers for vacuum fluorescent display tube.

The MSC7110-xx drives 12-segment bargraph or 7-segment plus comma and decimal point alphanumeric displays with up to 16 display positions, and drives 5 LEDs.

The MSC7112-xx drives 16-segment bargraph, 7-segment plus comma and decimal point or 16-segment alphanumeric displays with up to 12 display positions, and drives 5LEDs.

The controller accepts command and display data input words on a clocked serial input line.

Commands control the on/off duty cycle, starting character position, number of characters to be displayed and display modes (PLA mode, PLA bypass mode and LED mode).

Encoded data words display bargraph position (single segment or increasing length), characters, decimal point, comma and LEDs.

No external drive circuit is required for displays that operate on 40mA of drive current up to 45 volts.

A 32 x 16 bit PLA (ROM) code is programmable.

FEATURES

- Logic and LED driver supply voltage (V_{DD}) : +5V
- VF driver supply voltage (V_{EE}) : −40V
- Driver output current
  - VF grid driver (source) : −40mA
  - VF segment driver (source) : −6mA
  - LED driver (source) : −10mA
- Direct drive capability for vacuum fluorescent display
- 12 segment drivers (MSC7110-xx)
  16 segment drivers (MSC7112-xx)
- 16 digit drivers (MSC7110-xx)
  12 digit drivers (MSC7112-xx)
- 5 LED drivers
- Built-in oscillator circuit
- Built-in power-on-reset circuit with external C
- Serial host interface (data in, clock, load)
- Serial data input for 18-bit control and display data words

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- Command functions
  - On/off duty cycle
  - Starting character position
    - : 1 to 16 (MSC7110-xx)
    - : 1 to 12 (MSC7112-xx)
  - Number of characters
    - : 1 to 16 (MSC7110-xx)
    - : 1 to 12 (MSC7112-xx)
  - 3-display modes
    - PLA mode, PLA bypass mode and LED mode
- 32 x 16 bit PLA provides data decoding to drive
  - 1 to 12 bargraph segments
  - Any 1 of 12 bargraph segment
  - 7-segment plus comma and decimal point alphanumeric characters (MSC7110-xx)
  - 1 to 16 bargraph segment
  - Any 1 of 16 bargraph segment
  - 7-segment plus comma and decimal point alphanumeric characters
  - 14-segment alphanumeric characters (MSC7112-xx)
- The number of character decoded by PLA is 32
- Programmable PLA code
- 42 pin shrink DIP package/44 pin flat pacage

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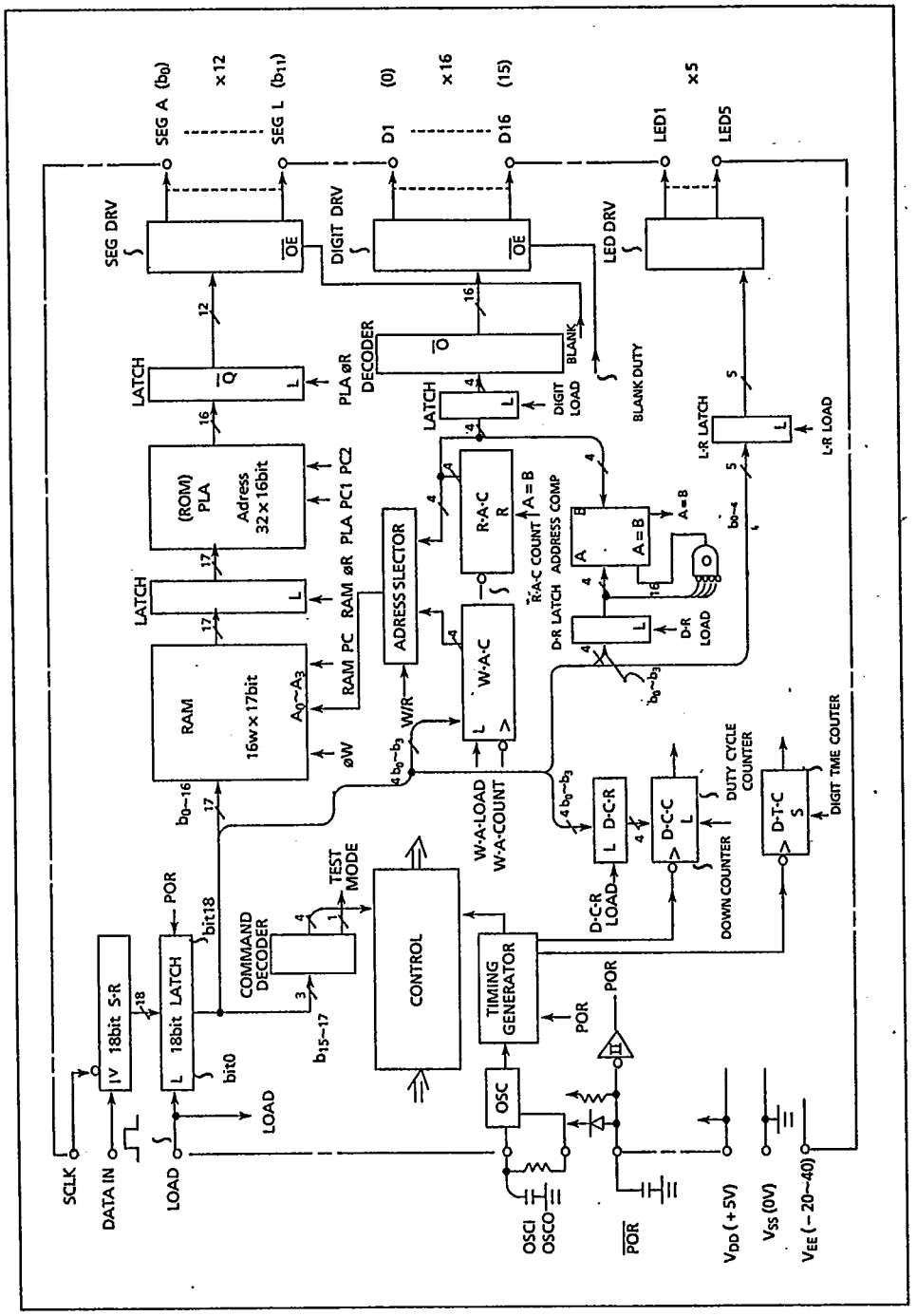
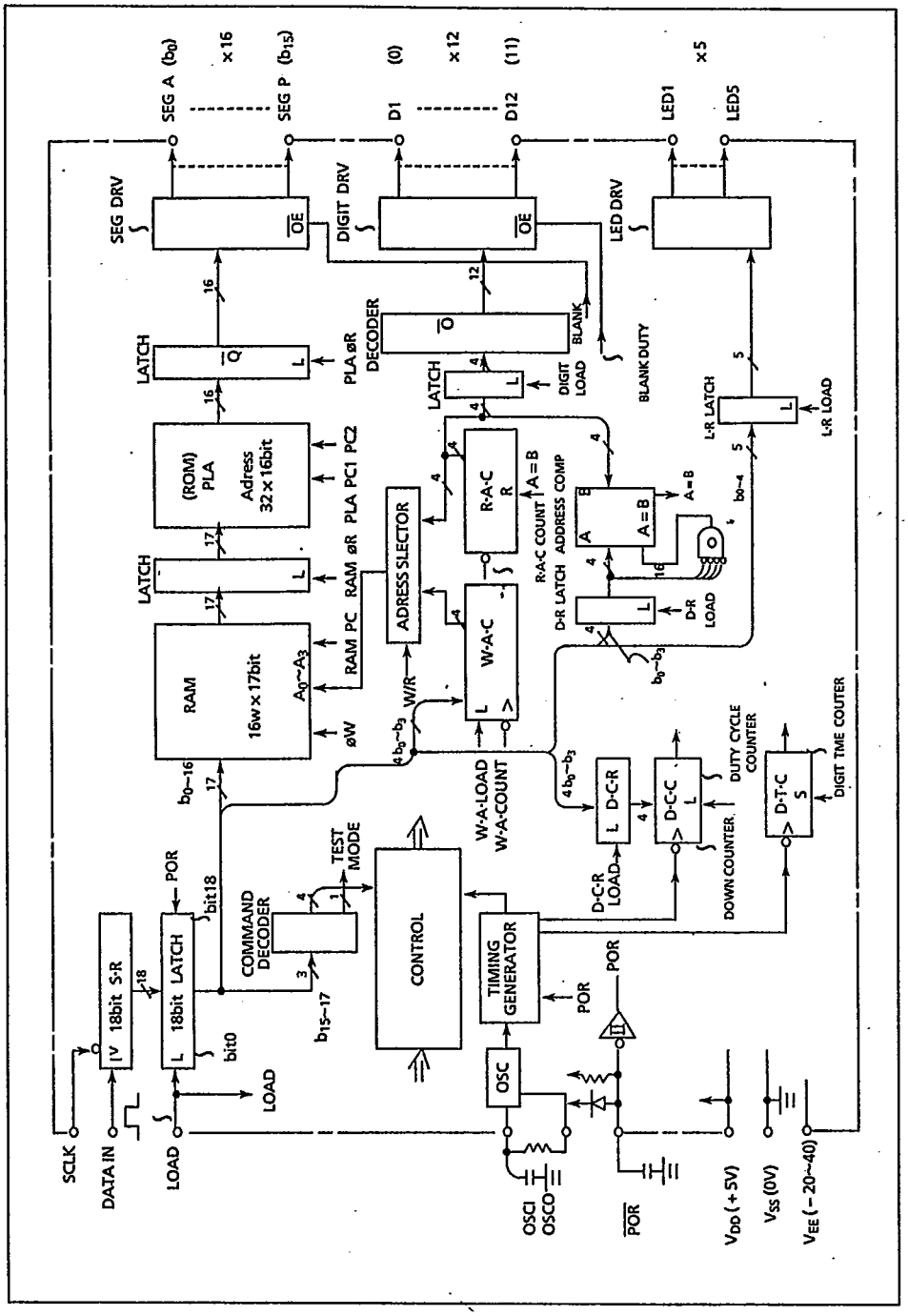
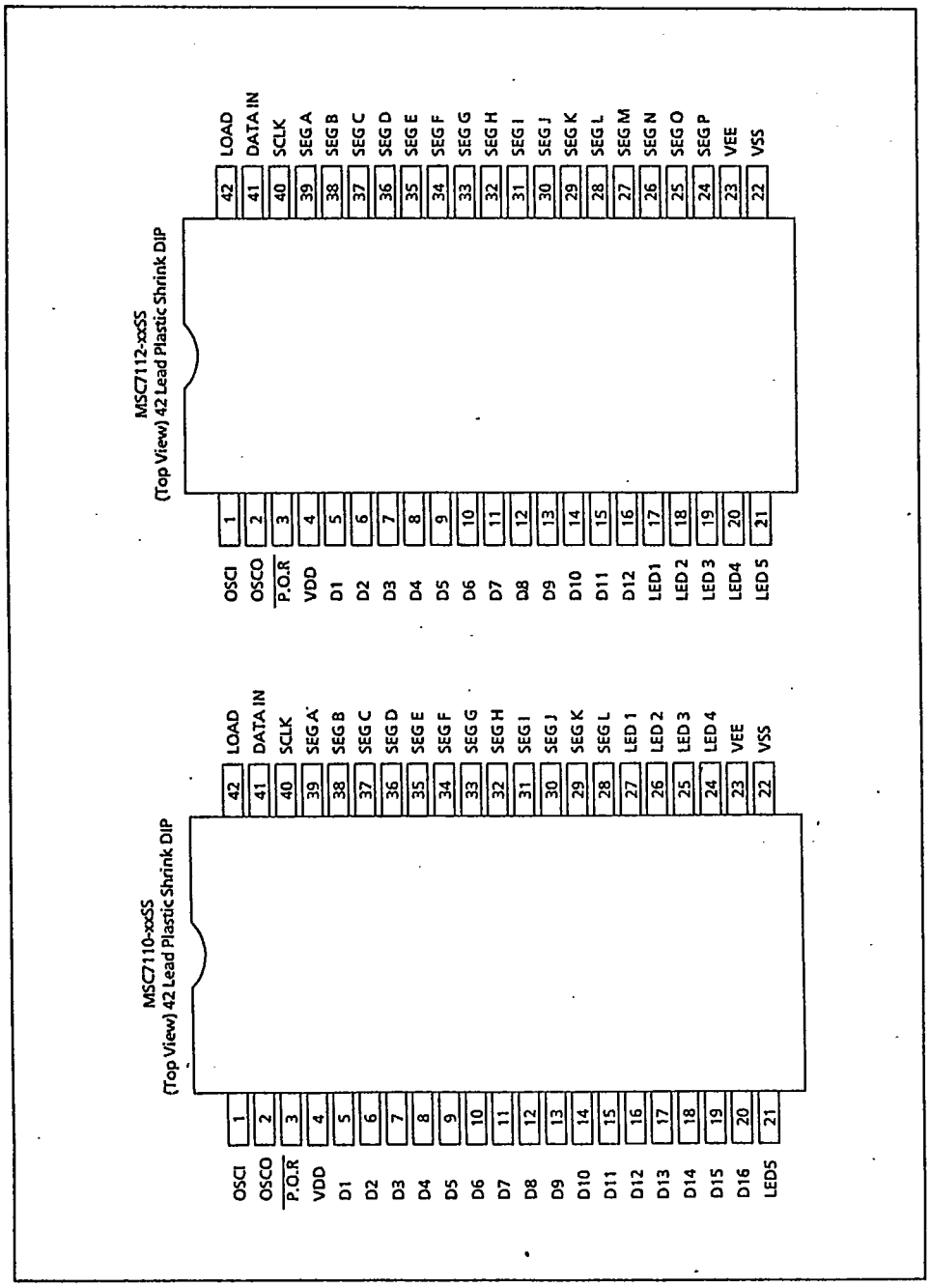
BLOCK DIAGRAM MSC7110-xx



BLOCK DIAGRAM MSC7112-xx



PIN CONFIGURATION



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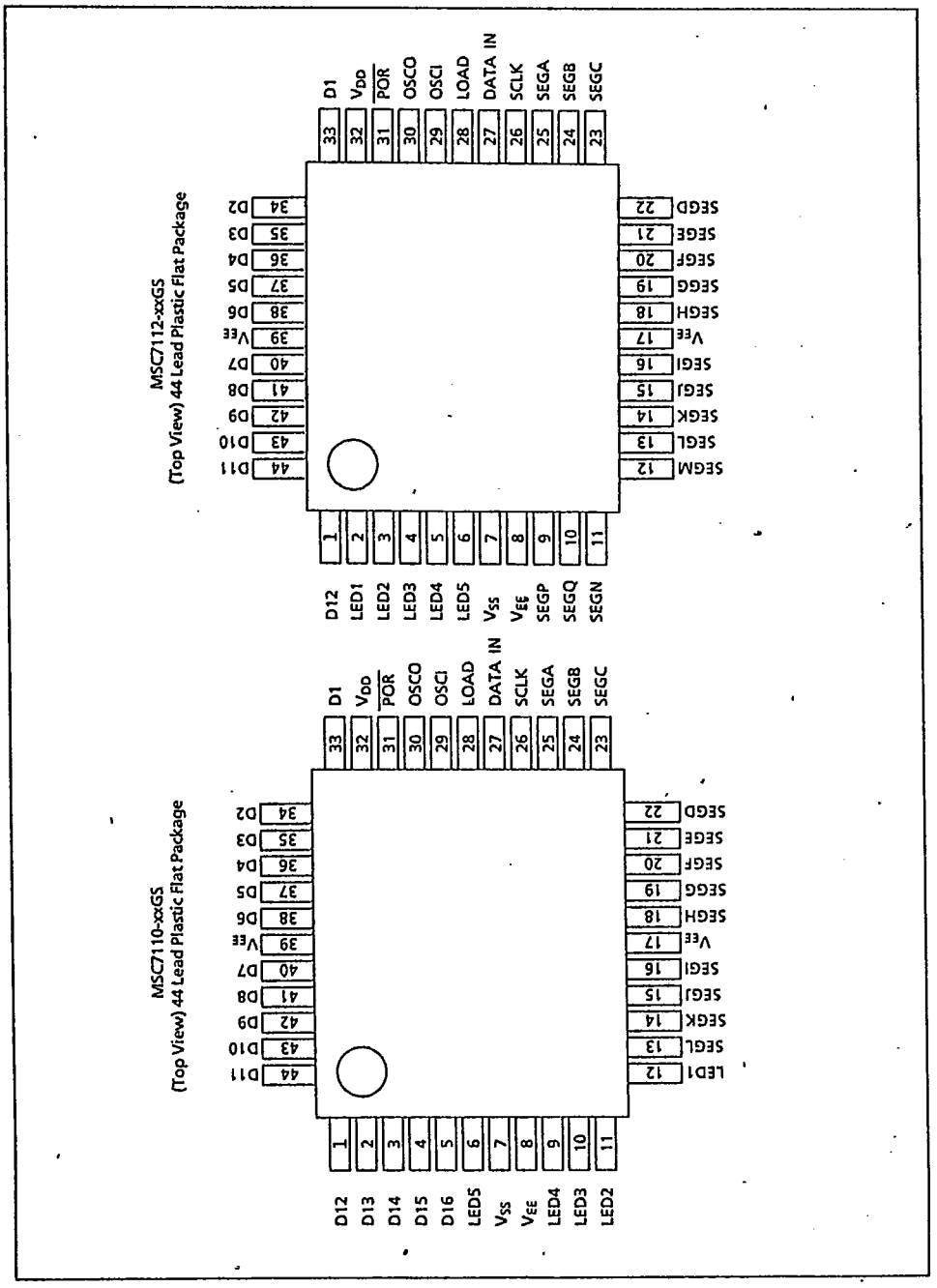
PIN CONFIGURATION



PIN DESCRIPTION

Terminal name	No. of terminals	Input, output	Connected to	Function
V_{DD} V_{SS} V_{EE}	1 1 1		Power source	V_{DD}-V_{SS} : Supply voltage for internal logic V_{DD}-V_{EE} : Supply voltage for VF driving circuit logic
DATA IN	1	Input	Microcomputer	Input shift register display data from the MSB (positive logic).
SCLK	1	Input	Microcomputer	Shift clock of the shift register. Data is shifted at the falling edge of SCLK.
LOAD	1	Input	Microcomputer	When the terminal is high, transfer of data from the shift register to the latch occurs.
$\overline{POR}$	1	Input Schmitt with pull-up register and diode		Internal logic reset input when power is turned on. When the terminal is Low, the 18-bit latch, the duty cycle register, the digit register, the LED register and the write/read address register are all reset. And the outputs of SEGA to SEGP (*a), D_1 to D_{12}(*b), and LED_1 to LED_5 are all turned off. When the terminal is connected to an external capacitor, the auto-power-on-reset function can be executed.
OSCI OSCO	1 1	Input Output		When an external resistor and a capacitor are connected, an oscillation circuit is formed. C = 100 pF, r = 47kΩ, f_{OSC} = 235 KHz ± 20%
SEGA~L SEGA~P	12*1 16*2	Output	Anode side of VF display tube	VF display tube driving output. The output is complementary.
D_1~D_{12} D_1~D_{16}	12*2 16*1	Output	Grid side of VF display tube	VF display tube driving output. The output is complementary.
LED1 ~LED5	5	Output	LED	LED driving output. The output is complementary.

*a SEGA to SEGL in case of MSC7110-xx
*b D_1 to D_{16} in case of MSC7110-xx
*1 In case of MSC7110-xx
*2 In case of MSC7112-xx

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ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Limits	Unit
Supply voltage (1)	V_{DD}	—	−0.3~+6.5	V
Supply voltage (2)	$V_{DD}-V_{EE}$	—	0~50	V
Input voltage	V_I	—	−0.3~V_{DD}+0.3	V
Allowable loss	Pd	Ta≧25°C	~500	mW
Storage temperature	t_{STg}	—	−55~+150	°C
Output current	I_{01}	All SEG output	−10	mA
	I_{02}	All digit output	−60	
	I_{03}	LED1~LED5	−20	

• Operating Range

Parameter	Symbol	Conditions	Limits	Unit
Supply voltage (1)	V_{DD}	←	4.5~5.5	V
Supply voltage (2)	$V_{DD}-V_{EE}$	—	25~45	V
Oscillation frequency	f_{OSC}	C=100pF R=47kΩ	235 ±20%	kHz
Operating temperature	T_{OP}	—	−20~+75	°C

- **DC Characteristics**

($V_{DD} - V_{EE} = 45V$, $V_{DD} = 5V \pm 10\%$, $Ta = -20 \sim +75°C$)

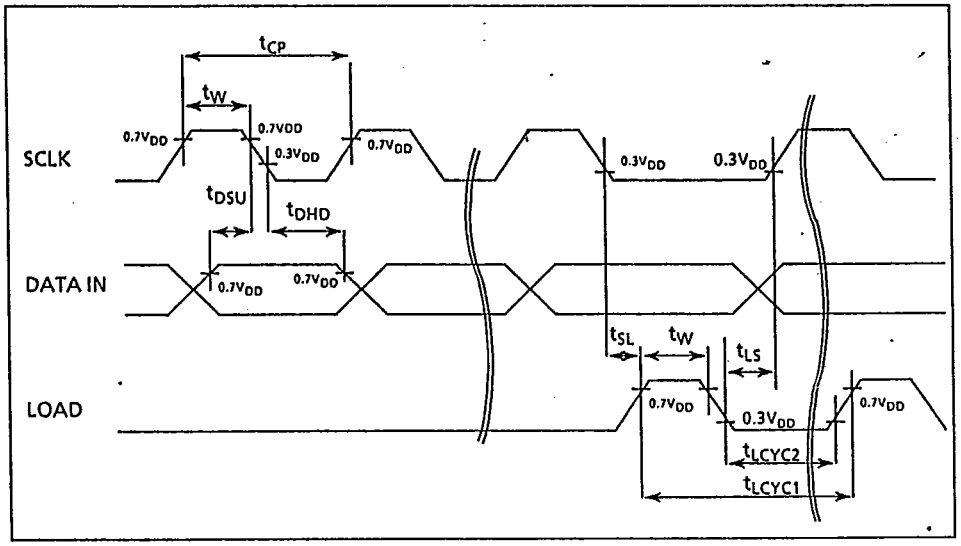
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Terminal
High level input voltage	V_{IH}	—	$0.7V_{DD}$	—	—	V	All input
Low level input voltage	V_{IL}	—	—	—	$0.3V_{DD}$	V	All input
High level input current	I_{IH}	$V_{DD} = 5.5V$ $V_I = V_{DD}$	—	—	1	μA	All input
Low level input current (1)	I_{IL1}	$V_{DD} = 5.5V$ $V_I = 0V$	—	—	−1	μA	All input except $\overline{POR}$
Low level input current (2)	I_{IL2}	$V_{DD} = 5.5V$ $V_I = 0V$	−27	−55	−110	μA	$\overline{POR}$
High level output voltage (1)	V_{OH1}	$V_{DD} = 4.5$ $I_{OH} = -6mA$	$V_{DD} - 2.2$	$V_{DD} - 1.5$	—	V	All SEG output
Low level output voltage (1)	V_{OL1}	$V_{DD} = 4.5$ $I_{OL} = 0.2mA$	—	$V_{EE} + 0.8$	$V_{EE} + 1.3$	V	All SEG output
High level output vltage (2)	V_{OH2}	$V_{DD} = 4.5$ $I_{OH} = -30mA$	$V_{DD} - 2.9$	$V_{DD} - 2.3$	—	V	All digit output
Low level output voltage (2)	V_{OL2}	$V_{DD} = 4.5$ $I_{OL} = 02.mA$	—	$V_{EE} + 0.8$	$V_{EE} + 1.3$	V	All digit output
High level input voltage (3)	V_{OH3}	$V_{DD} = 4.5$ $I_{OH} = -10mA$	$V_{DD} - 1.5$	—	—	V	LED1~ LED5
High level output voltage (3)	V_{OL3}	$V_{DD} = 4.5$ $I_{OL} = 0.1mA$	—	—	0.5	V	LED1~ LED5
Supply current	I_{DD}	$V_{DD} = 5.5V$ No load $f_{OSC} = 245kHz$	—	8.5	15	mA	

- AC Characteristics

V_{DD} = 5V ± 10% Ta = −20~ +75°C

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCLK cycle time	t_{CP}	—	2	—	—	µS
SCLK, LOAD pulse width	t_W	—	1	—	—	µS
Data setup time	t_{DSU}	—	500	—	—	nS
Data hold time	t_{DHD}	—	500	—	—	nS
SCLK-LOAD time	t_{SL}	—	2	—	—	µS
LOAD-SCLK time	t_{LS}	—	2	—	—	µS
LOAD cycle time 1	t_{LCYC1}	f_{OSC} = 245kHz	205	—	—	µS
LOAD cycle time 2	t_{LCYC2}	f_{OSC} = 245kHz	200	—	—	µS

- Timing Chart



FUNCTIONAL DESCRIPTION

- **LED display**

Display data is output to the LED1 to LED5 terminals in correspondence with each bit by executing the L. R LOAD command. Input data uses positive logic. When the data is 1, the LED lights. When the data is 0, the LED goes off.

- **VF display (PLA (ROM) used)**

Set optional data in the digit register and the duty register, and execute the W. A. C LOAD command to set the display digit position. Execute the PLA (ROM) DISPLAY command to write the display character address (PLA (ROM) address) in the RAM. The write address counter is incremented by one. The write address counter counts sequentially 0, 1, 2, -----, 14, 15, 0, 1, ----- regardless of the value of the digit register.

The segment code (ROM code) corresponding to the PLA (ROM) address is a user option.

- **VF display (RAM direct display)**

Set optional data in the digit resister and the duty register, and execute the W. A. C LOAD command to set the display digit position. Execute the DATA DISPLAY command to write the b_0 to b_{15} (*1) display data in the RAM. The write address counter is incremented by one. The write address counter counts sequentially 0, 1, 2, -----, 14, 15, 0, 1, ----- regardless of the value of the digit register.

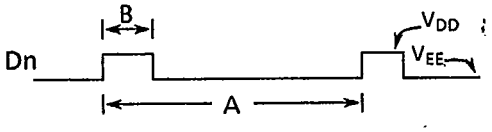
*1 : b_0 to b_{11} display data in case of MSC7110-xx.

• Brightness adjustment

The drightness can be adjusted by using the values of the duty cycle register and the digit register. The value of the duty cycle register changes the pulse width (B) at the D_1 to D_{16} output terminals, and the value of the digit register changes the cycle (A).

The table indicated below gives the relation between the value of the duty cycle register and the duty. When all the values of the duty cycle register are 0 (in the case of 16-digit display), the display is blank.

D. C. R				DUTY	D. C. R				DUTY	D. C. R				DUTY	D. C. R				DUTY
b_3	b_2	b_1	b_0	$\frac{B}{A}$	b_3	b_2	b_1	b_0	$\frac{B}{A}$	b_3	b_2	b_1	b_0	$\frac{B}{A}$	b_3	b_2	b_1	b_0	$\frac{B}{A}$
0	0	0	0	—	0	1	0	0	$\frac{16}{1024}$	1	0	0	0	$\frac{32}{1024}$	1	1	0	0	$\frac{48}{1024}$
0	0	0	1	$\frac{4}{1024}$	0	1	0	1	$\frac{20}{1024}$	1	0	0	1	$\frac{36}{1024}$	1	1	0	1	$\frac{52}{1024}$
0	0	1	0	$\frac{8}{1024}$	0	1	1	0	$\frac{24}{1024}$	1	0	1	0	$\frac{40}{1024}$	1	1	1	0	$\frac{56}{1024}$
0	0	1	1	$\frac{12}{1024}$	0	1	1	1	$\frac{28}{1024}$	1	0	1	1	$\frac{44}{1024}$	1	1	1	1	$\frac{60}{1024}$



$A = 64 \times n = 64 \times 16 = 1024$

n : Number of display digits

• Number of display digits

The number of display digits is set by the digit register. The number of display digits ranges from 1 to 16 (*1). The value of the digit register and the number of digits are as follows :

D. R				Control digit	D. R				Control digit	D. R				Control digit	D. R				Control digit
b_3	b_2	b_1	b_0		b_3	b_2	b_1	b_0		b_3	b_2	b_1	b_0		b_3	b_2	b_1	b_0	
0	0	0	0	*2 D_1~D_{16}	0	1	0	0	D_1~D_4	1	0	0	0	D_1~D_8	1	1	0	0	D_1~D_{12}
0	0	0	1	D_1~D_1	0	1	0	1	D_1~D_5	1	0	0	1	D_1~D_9	1	1	0	1	*2 D_1~D_{13}
0	0	1	0	D_1~D_2	0	1	1	0	D_1~D_6	1	0	1	0	D_1~D_{10}	1	1	1	0	*2 D_1~D_{14}
0	0	1	1	D_1~D_3	0	1	1	1	D_1~D_7	1	0	1	1	D_1~D_{11}	1	1	1	1	*2 D_1~D_{15}

*1 : 1 to 12 digita in the case of the MSC7112-xx
*2 : Ignored in the case of the MSC7112-xx

● Command

Command	Function	Input data																	
		MSB b_{17}	b_{16}	b_{15}	b_{14}	b_{13}	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	LSB b_0
DATA DISPLAY	The RAM data is output directly to the SEGA to SEGP terminals. (Positive logic)	0	0	*1 SEGP	*1 SEGO	*2 SEGN	*3 SEGM	SEGL	SEGK	SEGJ	SEGI	SEGH	SEGG	SEGF	SEGE	SEGD	SEGC	SEGB	SEGA
PLA DISPLAY	The RAM data is converted in code by the PLA and output to the SEGA to SEGP terminals. (Positive logic) *2	0	1	×	×	×	×	×	×	×	×	×	×	×	2^4	2^3	2^2	2^1	2^0
L. R LOAD	Display data is set in the LED register and output to the LED1 to LED5 terminals. (Positive logic)	1	0	0	×	×	×	×	×	×	×	×	×	×	LED5	LED4	LED3	LED2	LED1
D. R LOAD	The number of digits is set in the digit register.	1	0	1	0	×	×	×	×	×	×	×	×	×	×	2^3	2^2	2^1	2^0
W. A. C LOAD	The write address is set in the write address counter. (The write position is set.)	1	1	0	×	×	×	×	×	×	×	×	×	×	×	2^3	2^2	2^1	2^0
D. C. R LOAD	The duty value is set in the duty cycle register.	1	1	1	×	×	×	×	×	×	×	×	×	×	×	2^3	2^2	2^1	2^0
TEST MODE LOAD	The TEST mode is set.	1	0	1	1	×	×	×	×	×	×	×	×	×	×	×	×	×	×

*1 : Ignored in case of MSC7110-xx × : Don't Care
*2 : Output to the SEGA to SEGL terminals in case of MSC7110-xx

Relation between write address and digit output

Write address count	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Corresponding digit output	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	*1 D_{13}	*1 D_{14}	*1 D_{15}	*1 D_{16}

*1 : Ignored in case of MSC7112-xx

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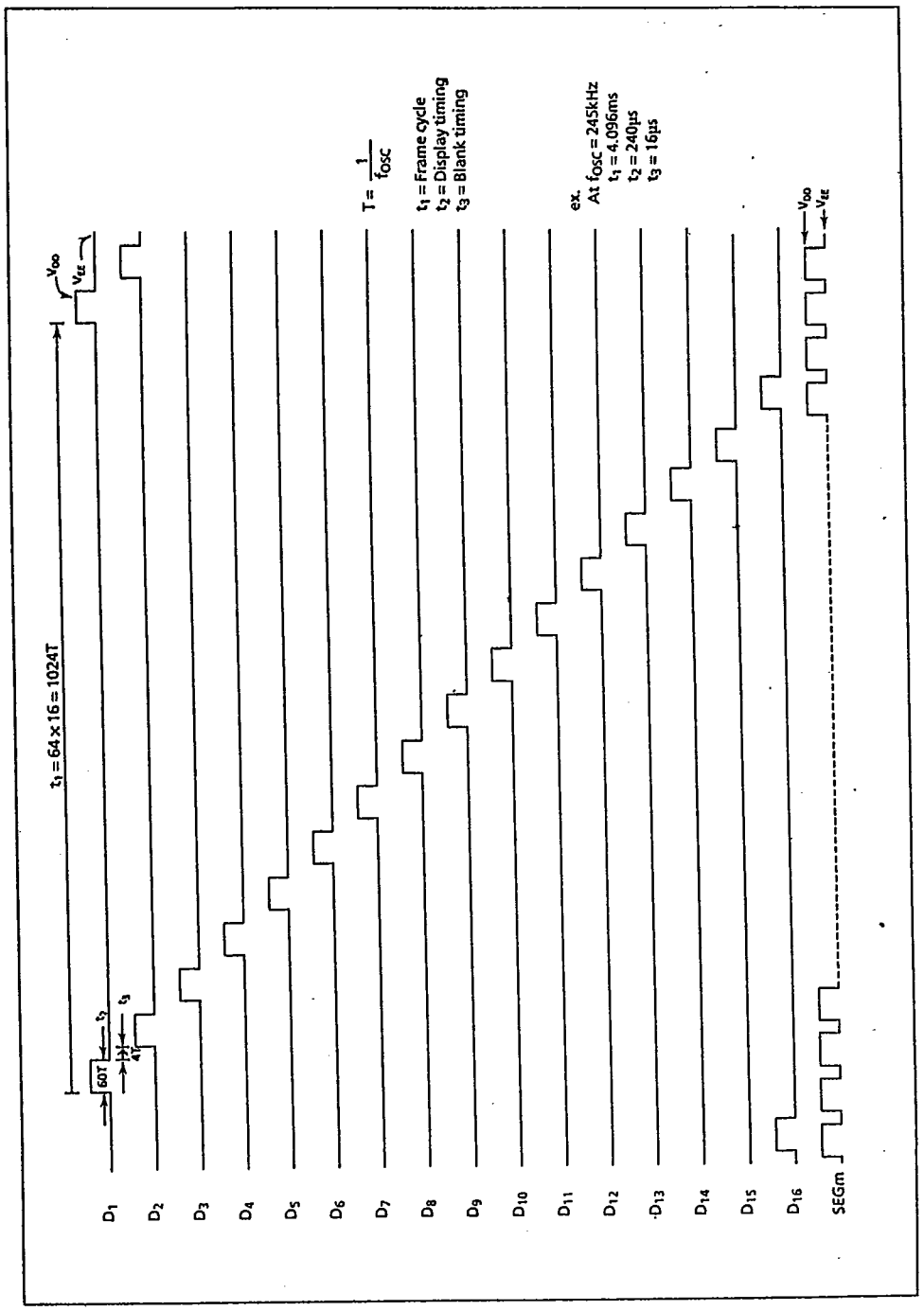
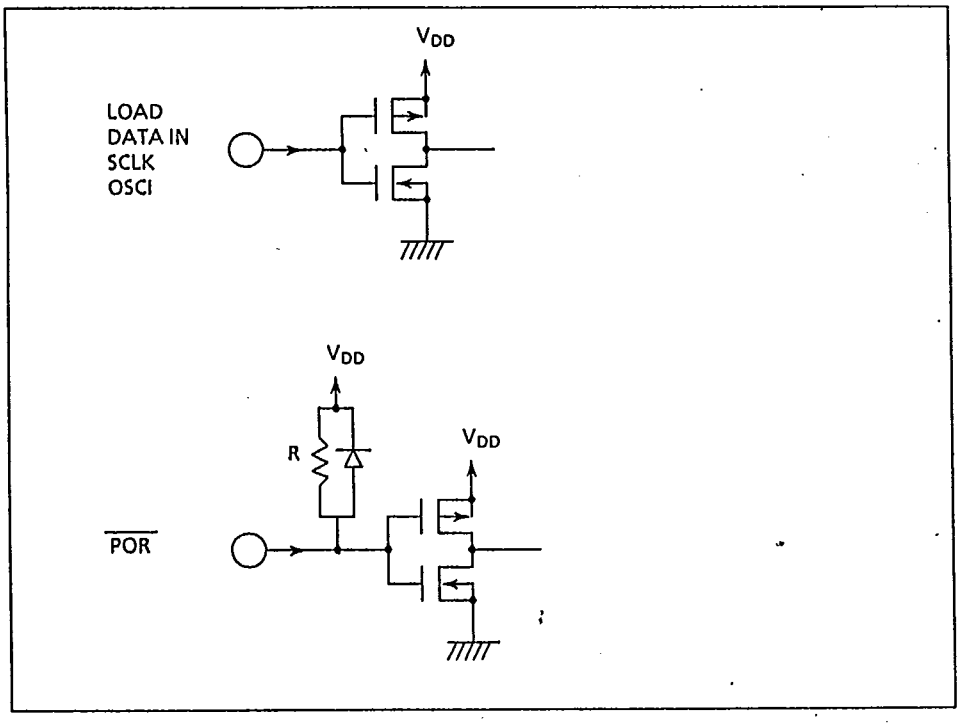
- **Digit timing chart (Display 16 digits in length)**

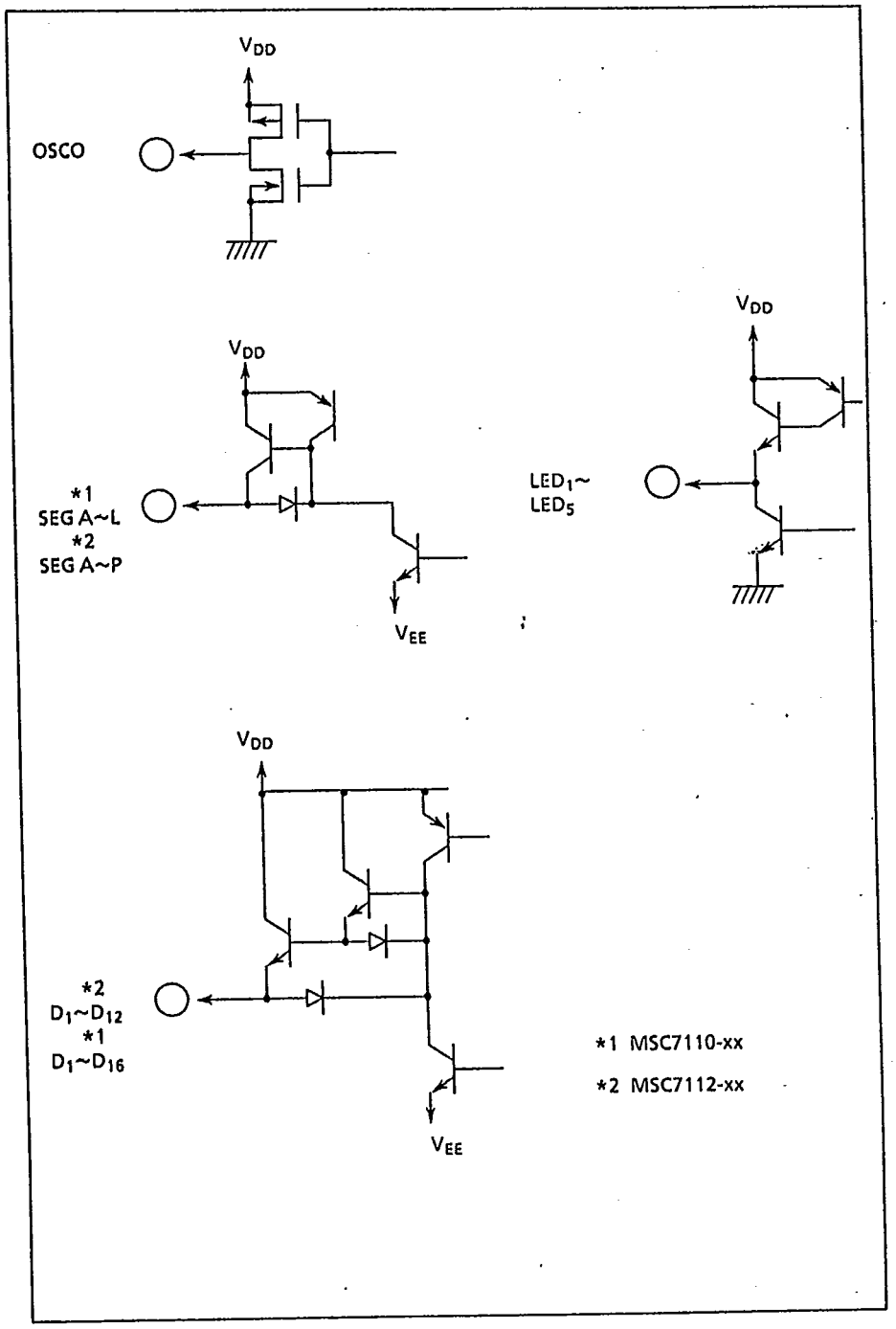


SCHEMATIC DIAGRAMS OF INPUT AND OUTPUT CIRCUIT

- **Input terminal**



- **Output terminal**



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APPLICATION NOTE (MSM7112-xx)