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CA3020, CA3020A

**8MHz Power Amps For Military,
Industrial and Commercial Equipment**

November 2000

Features

- High Power Output Class B Amplifier
 - CA3020 0.5W (Typ) at $V_{CC} = 9V$
 - CA3020A 1.0W (Typ) at $V_{CC} = 12V$
- Wide Frequency Range .. Up to 8MHz with Resistive Loads
- High Power Gain..... 75dB (Typ)
- Single Power Supply For Class B Operation With Transformer
 - CA3020 3V to 9V
 - CA3020A 3V to 12V
- Built-In Temperature-Tracking Voltage Regulator Provides Stable Operation Over -55°C to 125°C Temperature Range

Applications

- AF Power Amplifiers For Portable and Fixed Sound and Communications Systems
- Servo-Control Amplifiers
- Wide-Band Linear Mixers
- Video Power Amplifiers
- Transmission-Line Driver Amplifiers (Balanced and Unbalanced)
- Fan-In and Fan-Out Amplifiers For Computer Logic Circuits
- Lamp-Control Amplifiers
- Motor-Control Amplifiers
- Power Multivibrators
- Power Switches

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3020	-55 to 125	12 Pin Metal Can	T12.B
CA3020A	-55 to 125	12 Pin Metal Can	T12.B

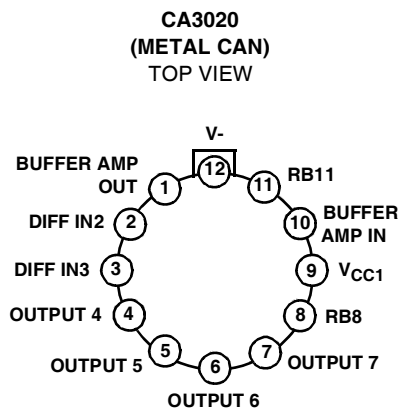
Description

The CA3020 and CA3020A are integrated-circuit, multi-stage, multipurpose, wide-band power amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

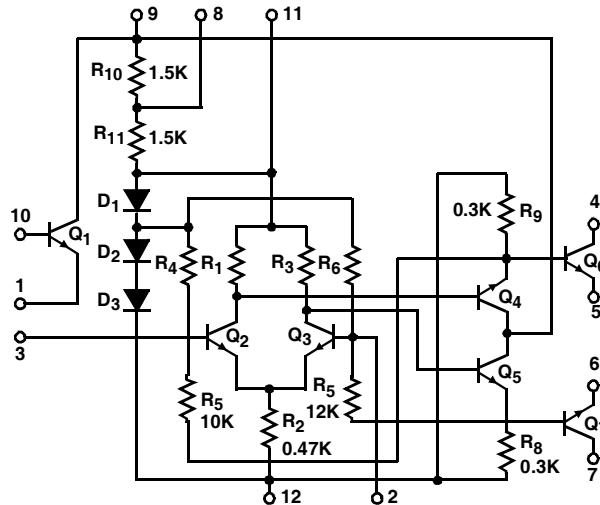
The CA3020 and CA3020A are particularly suited for service as class B power amplifiers. The CA3020A can provide a maximum power output of 1W from a 12V_{DC} supply with a typical power gain of 75dB. The CA3020 provides 0.5W power output from a 9V supply with the same power gain.

Refer to AN5766 for application information.

Pinout



Schematic Diagram



The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

Intersil reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

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Absolute Maximum Ratings

Maximum Pin 9 Supply Voltage, V_{CC1} (Note 1)	
CA3020	10V
CA3020A	12V
Maximum Pin 9 Supply Current, I_{CC1}	20mA
Maximum Pin 11 Sink Current, I_{11}	20mA
Output Voltage, V_4 and V_7 (Note 1)	
CA3020	25V
CA3020A	18V
Output Current, I_O	300mA
Input Voltage Range, V_2, V_3	-2V to 2V
Maximum Input Voltage, V_{10} (Ref to Pin 1)	-3V
Maximum Source Current, V_1	1mA

Operating Conditions

Temperature Range -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	165	80
Maximum Junction Temperature (Metal CanPackage)	175°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- The voltage ratings for Pin 9, Pin 4 and Pin 7 are referenced to the V- (Pin 12). A normal bias configuration for Pin 8 and Pin 11 is shown in Figure 1B. Refer to Application Note AN5766 for other options.
- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS			CA3020			CA3020A			UNITS	
		CIRCUIT AND PROCEDURE	DC SUPPLY VOLTAGE		MIN	TYP	MAX	MIN	TYP	MAX		
			FIGURE	V_{CC1}								V_{CC2}
Collector-to-Emitter Breakdown Voltage, Q_6 and Q_7 at 10mA	$V_{(BR)CER}$	1A	-	-	18	-	-	25	-	-	V	
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V	
Idle Currents, Q_6 and Q_7	I_4 IDLE I_7 IDLE	7	9.0	2.0	-	5.5	-	-	5.5	-	mA	
Peak Output Currents, Q_6 and Q_7	I_4 PK I_7 PK	7	9.0	2.0	140	-	-	180	-	-	mA	
Cutoff Currents, Q_6 and Q_7	I_4 CUTOFF I_7 CUTOFF	7	9.0	2.0	-	-	1.0	-	-	1.0	mA	
Differential Amplifier Current Drain	I_{CC1}	7	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA	
Total Current Drain	$I_{CC1} + I_{CC2}$	7	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA	
Differential Amplifier Input Terminal Voltages	V_2 V_3	7	9.0	2.0	-	1.11	-	-	1.11	-	V	
Regulator Terminal Voltage	V_{11}	7	9.0	2.0	-	2.35	-	-	2.35	-	V	
Q_1 Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	μA	
	Emitter-to-Base		I_{EBO}	3.0	-	-	-	0.1	-	-	0.1	μA
	Collector-to-Base		I_{CBO}	3.0	-	-	-	0.1	-	-	0.1	μA
Forward Current Transfer Ratio, Q_1 at 3mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-		
Bandwidth at -3dB Point	BW	8	6.0	6.0	-	8	-	-	8	-	MHz	
Maximum Power Output for $R_{CC} = 130\Omega$	$P_{O(MAX)}$	9	6.0	6.0	200	300	-	200	300	-	mW	
		9	9.0	9.0	400	550	-	400	550	-	mW	
		9	9.0	12.0	-	-	-	800	1000	-	mW	
Maximum Power Output for $R_{CC} = 200\Omega$		9	9.0	12.0	-	-	-	800	1000	-	mW	
Sensitivity for $P_{OUT} = 400\text{mW}$, $R_{CC} = 130\Omega$	e_{IN}	9	9.0	9.0	-	35	55	-	-	-	mV	
Sensitivity for $P_{OUT} = 800\text{mW}$, $R_{CC} = 200\Omega$	e_{IN}	9	9.0	12.0	-	-	-	-	50	100	mV	
Input Resistance - Terminal 3 to Ground	R_{IN3}	10	6.0	6.0	-	1000	-	-	1000	-	Ω	

Test Circuits and Waveforms (Continued)

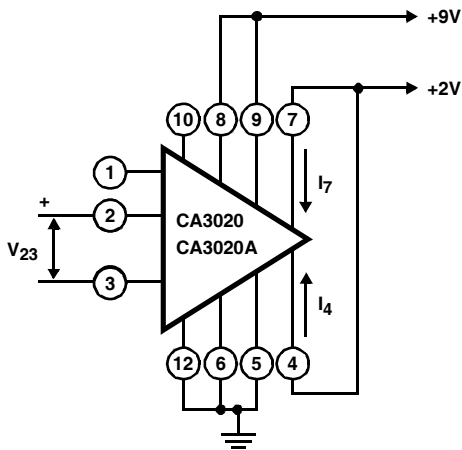


FIGURE 2A. TEST SETUP

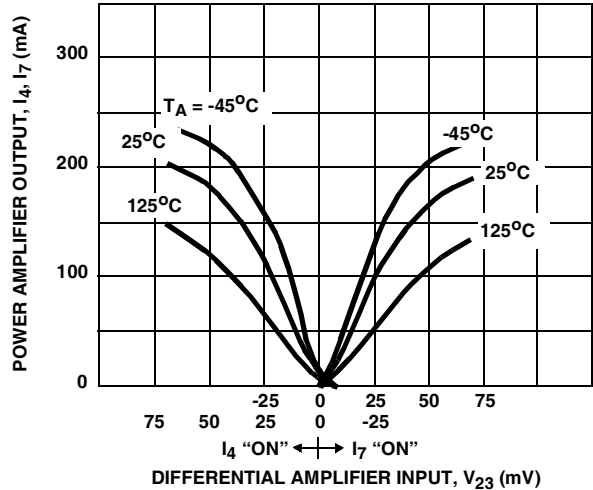


FIGURE 2B. CHARACTERISTICS WITH R₁₀ SHORTED OUT

FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

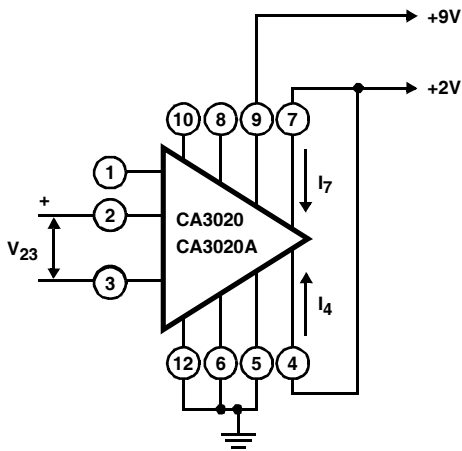


FIGURE 3A. TEST SETUP

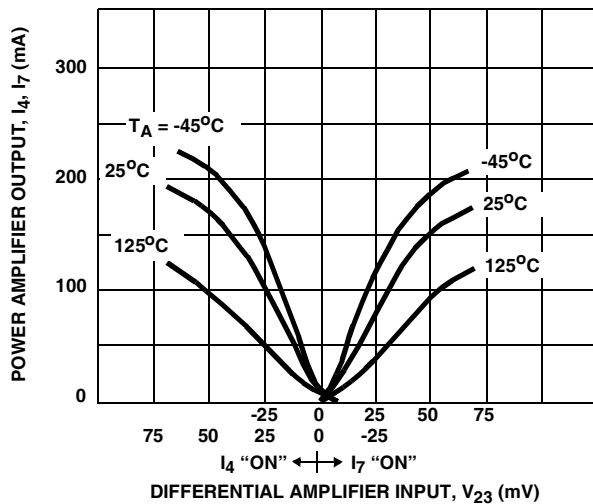


FIGURE 3B. CHARACTERISTIC WITH R₁₀ IN CIRCUIT

FIGURE 3. TYPICAL TRANSFER CHARACTERISTICS

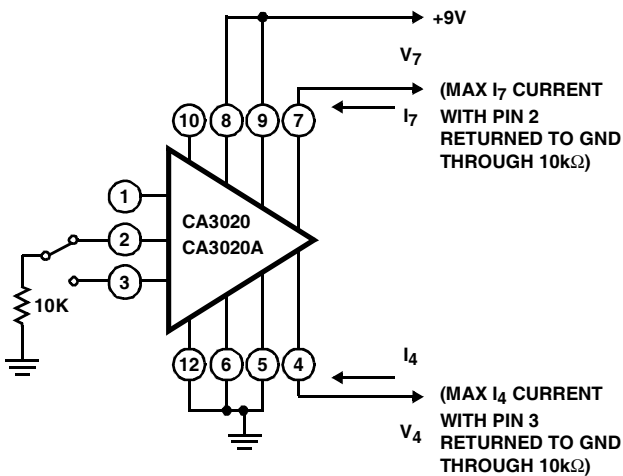


FIGURE 4A. TEST SETUP

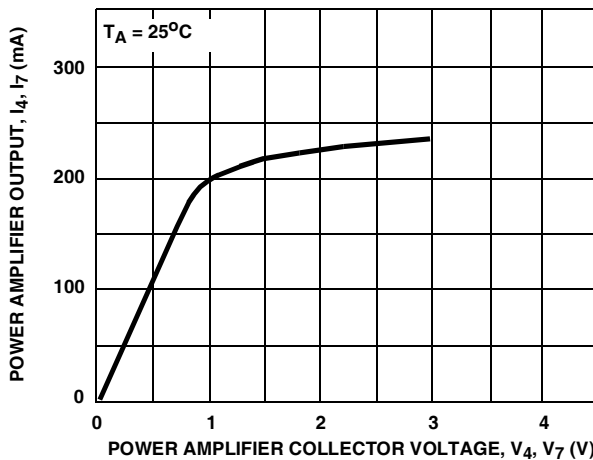


FIGURE 4B. CHARACTERISTIC

FIGURE 4. "MINIMUM DRIVE" TYPICAL CURRENT-VOLTAGE SATURATION CURVE

Test Circuits and Waveforms (Continued)

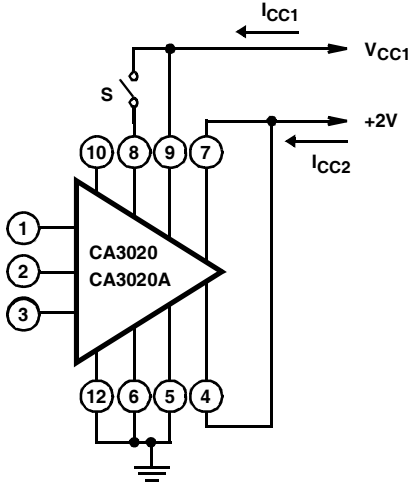


FIGURE 5A. TEST SETUP

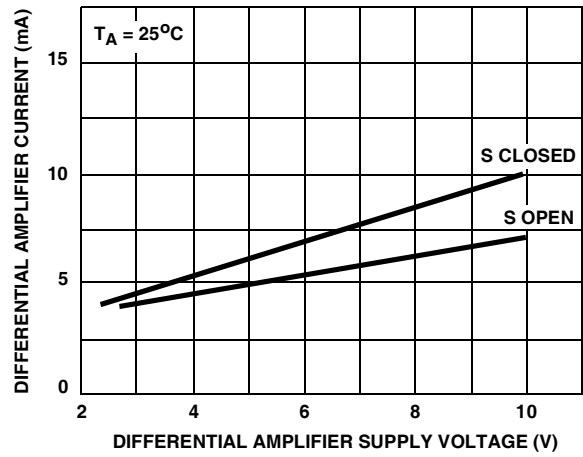


FIGURE 5B. DIFFERENTIAL AMPLIFIER CHARACTERISTICS OF I_{CC1} CURRENT vs V_{CC1} VOLTAGE

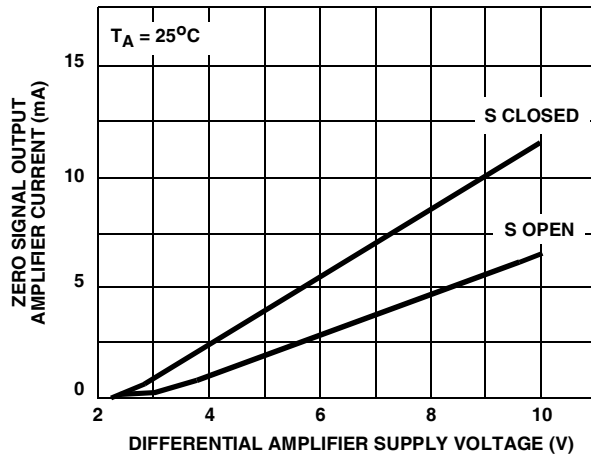


FIGURE 5C. OUTPUT AMPLIFIER CHARACTERISTICS OF I_{CC2} CURRENT vs V_{CC1} VOLTAGE

FIGURE 5. ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE

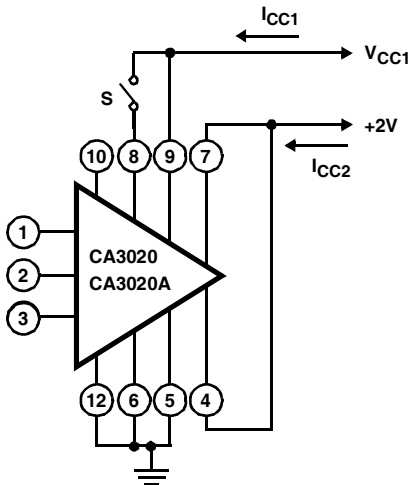


FIGURE 6A. TEST SETUP

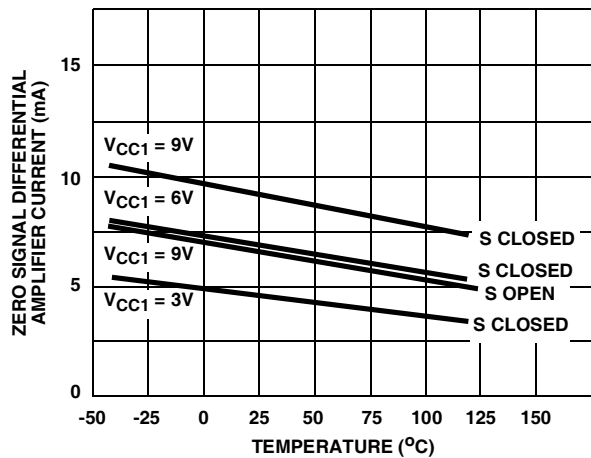


FIGURE 6B. DIFFERENTIAL AMPLIFIER CHARACTERISTICS OF I_{CC1} CURRENT vs AMBIENT TEMPERATURE

FIGURE 6. ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE

Test Circuits and Waveforms (Continued)

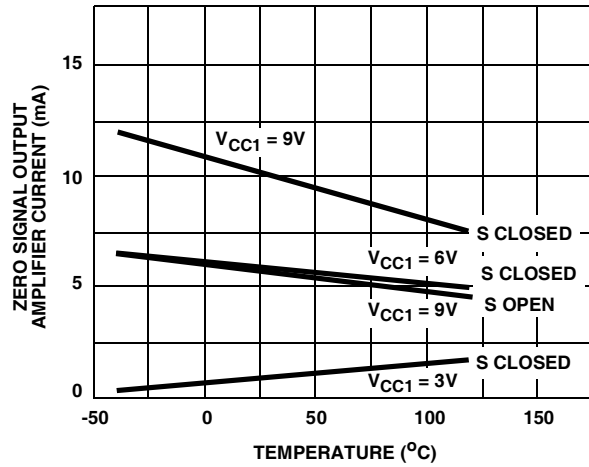
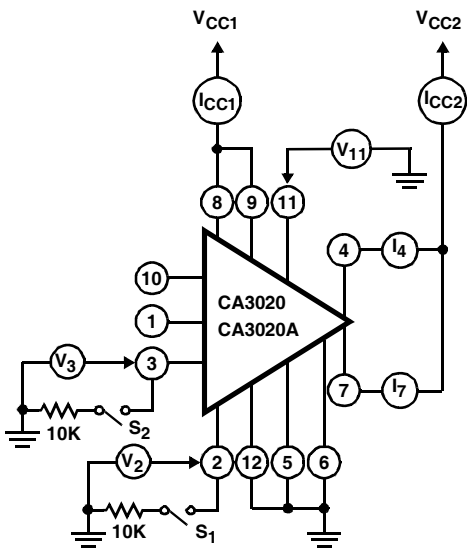


FIGURE 6C. OUTPUT AMPLIFIER CHARACTERISTICS OF I_{CC2} CURRENT vs AMBIENT TEMPERATURE
 FIGURE 6. ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE



CURRENTS OR VOLTAGES	S ₁	S ₂
I ₄ -IDLE	OPEN	OPEN
I ₇ -IDLE	OPEN	OPEN
I ₄ -PEAK	OPEN	CLOSE
I ₇ -PEAK	CLOSE	OPEN
I ₄ -CUTOFF	CLOSE	OPEN
I ₇ -CUTOFF	OPEN	CLOSE

CURRENTS OR VOLTAGES	S ₁	S ₂
I _{CC1}	OPEN	OPEN
I _{CC2}	OPEN	OPEN
V ₂	OPEN	OPEN
V ₃	OPEN	OPEN
V ₁₁	OPEN	OPEN

FIGURE 7. STATIC CURRENT AND VOLTAGE TEST CIRCUIT

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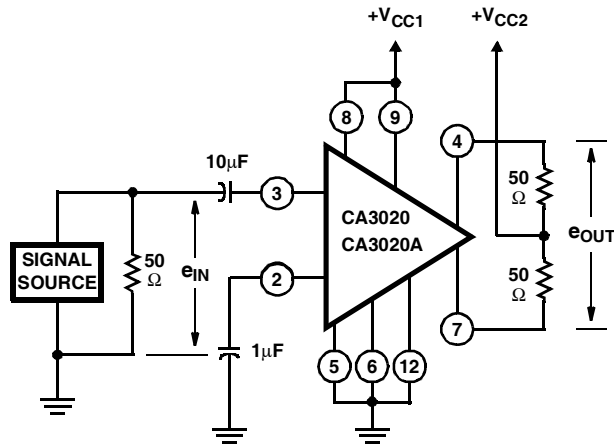
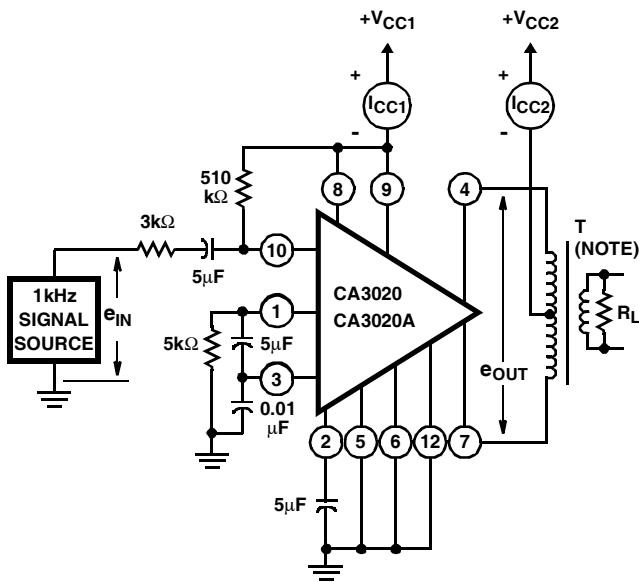


FIGURE 8. MEASUREMENT OF BANDWIDTH AT -3dB POINTS

PROCEDURES:

1. Apply desired value of V_{CC1} and V_{CC2} .
2. Apply 1kHz input signal and adjust for $e_{IN} = 5mV_{RMS}$.
3. Record the resulting value of e_{OUT} in dB (reference value).
4. Vary input-signal frequency, keeping e_{IN} constant at 5mV, and record frequencies above and below 1kHz at which e_{OUT} decreases 3dB below reference value.
5. Record bandwidth as frequency range between -3dB points.



NOTE: Push-pull output transformer; load resistance (R_L) should be selected to provide indicated collector-to-collector load impedance (R_{CC}).

PROCEDURES:

1. Apply desired value of V_{CC1} and V_{CC2} and reduce e_{IN} to 0V.
2. Record resulting values of I_{CC1} and I_{CC2} in mA as Zero-Signal DC Current Drain.
3. Apply desired value of V_{CC1} and V_{CC2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%.
4. Record resulting value of I_{CC1} and I_{CC2} in mA as Maximum Signal DC Current Drain.
5. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT}).
6. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100 \frac{P_{OUT}}{V_{CC1}I_{CC1} + V_{CC2}I_{CC2}}$$

where P_{OUT} is in watts, V_{CC1} and V_{CC2} are in volts, and I_{CC1} and I_{CC2} are in amperes.

7. Record value of e_{IN} in mV_{RMS} required in Step 3 as Sensitivity (e_{IN}).
8. Calculate Transducer Power Gain (G_p) in dB as follows:

$$G_p = 10 \log_{10} \frac{P_{OUT}}{P_{IN}}$$

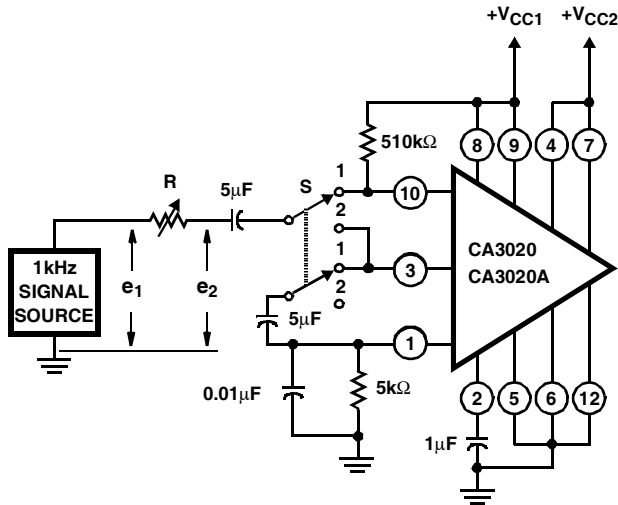
$$\text{where } P_{IN}(\text{in mW}) = \frac{e_{IN}^2}{3000 + R_{IN(10)}(\text{Note 4})}$$

NOTE:

4. See Figure 10 for definition of $R_{IN(10)}$.

FIGURE 9. MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN

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PROCEDURES:

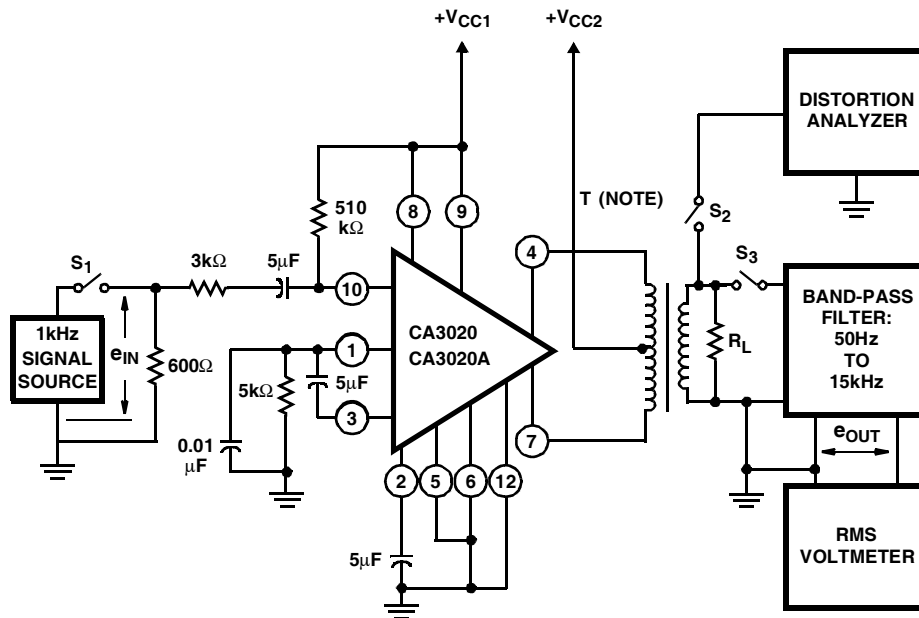
Input Resistance Terminal 10 to Ground (R_{IN10}).

1. Apply desired value of V_{CC1} and V_{CC2} and set S in Position 1.
2. Adjust 1kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$.
4. Record resulting value of R as R_{IN10} .

Input Resistance Terminal 3 to Ground (R_{IN3}).

1. Apply desired value of V_{CC1} and V_{CC2} and set S in Position 2.
2. Adjust 1kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$.
4. Record resulting value of R as R_{IN3} .

FIGURE 10. MEASUREMENT OF INPUT RESISTANCE



NOTE: Push-pull output transformer; load resistance (R_L) should be selected to provide indicated collector-to-collector load impedance (R_{CC}).

PROCEDURES:

Signal-to-Noise Ratio

1. Close S_1 and S_3 ; open S_2 .
2. Apply desired values of V_{CC1} and V_{CC2} .
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of e_{OUT} in dB as e_{OUT1} (reference value).
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT2}
5. Signal-to-Noise Ratio (S/N) = $20\log_{10} \frac{e_{OUT1}}{e_{OUT2}}$.

Total Harmonic Distortion

1. Close S_1 and S_2 ; open S_3 .
2. Apply desired values of V_{CC1} and V_{CC2} .
3. Adjust e_{IN} for desired level amplifier output power.
4. Record Total Harmonic Distortion (THD) in %.

FIGURE 11. MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION

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