



C Series Open Mode Design

Type:

C2012 [EIA CC0805] C3216 [EIA CC1206] C3225 [EIA CC1210] C4532 [EIA CC1812] C5750 [EIA CC2220]

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Version B11

MULTILAYER CERAMIC CHIP CAPACITORS

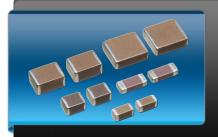
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Please read before using this product

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C Series

Open Mode Design Type: C2012, C3216, C3225, C4532, C5750

Features



temperature cycle, vibration, and electrical stresses Available in X7R and X8R dielectrics · When a chip capacitor is cracked by mechanical stress such as board bending, open mode construction helps user reduce the risk of short circuits • The Open Mode design defines that the L-Gap length

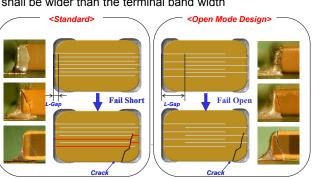
· Increase resistance to mechanical bending,

shall be wider than the terminal band width

Applications



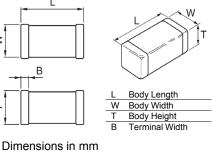
- · Automotive and other high stress applications
- · Battery line circuits with high board flex stress



· The Open Mode concept does not guaranteed MLCC will always fail open. This design is intended to reduce the risk of the MLCC failing short. All MLCC caution guidelines apply.



≥



Symbol Design 5 Open Mode

Part Number Construction

Series Name		<u>C</u>	<u>3216</u>	<u>X7R</u> 2A	ΤĪ	<u>5XXX</u>	Internal Codes	
imensions L x	W (mm)						Termination Code	Style
Case Code	Length	Width					5xxx	Open Mode Design
C2012	2.00 ± 0.20	1.25 ± 0.20	_		1 5		Packaging Style	
C3216	$\textbf{3.20} \pm \textbf{0.20}$	1.60 ± 0.20	_				Packaging Code	Style
C3225	$\textbf{3.20} \pm \textbf{0.40}$	2.50 ± 0.30	_				Т	Tape & Reel
C4532	4.50 ± 0.40	3.20 ± 0.40	-				Capacitance Toler	
C5750	5.70 ± 0.40	5.00 ± 0.40	_				-	
							Tolerance Code	Tolerance
Temperature C	naracteristic -			- 1			K	± 10%
Temperature	Capacitance	Temperature					М	$\pm 20\%$
Characteristics	Change	Range					Nominal Capacita	nce (pF)
X7R	±15%	-55 to +125°C	-				The capacitance i	s expressed in three
X8R	±15%	-55 to +150°C	-				digit codes and in	units of pico Farads
Rated Voltage	(DC)						•	d second digits identify
•	. ,						u /	nd significant figures of
Voltage Code	Voltage (DC)							The third digit identifies
1C	16V						•	•
1E	25V							lesignates a decimal
1H	50V						point.	
2A	100V						Capacitance Code	Capacitance
2E	250V						0R5	
2J	630V						010	0.5pF 1pF
							010	INL
							102	1,000pF (1nF)

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MULTILAYER CERAMIC CHIP CAPACITORS



C2012 [EIA CC0805]

Capacitance Range Chart

Temperature Characteristics: X7R, (± 15%), X8R (± 15%) Rated Voltage: 250V (2E), 100V (2A), 50V (1H)





Capacitance Range Table

C2012 [EIA CC0805]

Class 2 (Temperature Stable)

Temperature Characteristics X7R (-55 to +125°C, ±15%), X8R (-55 to +150°C, ±15%)

IDK Part Number Ordering Code)	Temperature Characteristics	Rated Voltage	Capacitance (pF)	Capacitance Tolerance	Thickness (mm)
C2012X7R1H104KT5	X7R	50V	100,000	± 10%	1.25 ± 0.20
2012X7R2A102KT5	X7R	100V	1,000	± 10%	0.85 ± 0.10
2012X7R2A152KT5	X7R	100V	1,500	± 10%	0.85 ± 0.10
2012X7R2A222KT5	X7R	100V	2,200	± 10%	0.85 ± 0.10
2012X7R2A332KT5	X7R	100V	3,300	± 10%	0.85 ± 0.10
2012X7R2A472KT5	X7R	100V	4,700	± 10%	0.85 ± 0.10
2012X7R2A682KT5	X7R	100V	6,800	± 10%	0.85 ± 0.10
2012X7R2A103KT5	X7R	100V	10,000	± 10%	0.85 ± 0.10
2012X7R2A153KT5	X7R	100V	15,000	± 10%	1.25 ± 0.20
2012X7R2A223KT5	X7R	100V	22,000	± 10%	1.25 ± 0.20
2012X7R2E102KT5	X7R	250V	1,000	± 10%	0.85 ± 0.10
2012X7R2E152KT5	X7R	250V	1,500	± 10%	0.85 ± 0.10
2012X7R2E222KT5	X7R	250V	2,200	± 10%	0.85 ± 0.10
2012X7R2E332KT5	X7R	250V	3,300	± 10%	0.85 ± 0.10
2012X7R2E472KT5	X7R	250V	4,700	± 10%	0.85 ± 0.10
2012X7R2E682KT5	X7R	250V	6,800	± 10%	1.25 ± 0.20
2012X7R2E103KT5	X7R	250V	10,000	± 10%	1.25 ± 0.20
2012X7R2E153KT5	X7R	250V	15,000	± 10%	1.25 ± 0.20
2012X8R1H223KT5	X8R	50V	22,000	± 10%	0.85 ± 0.10
2012X8R1H333KT5	X8R	50V	33,000	± 10%	0.85 ± 0.10
2012X8R1H473KT5	X8R	50V	47,000	± 10%	1.25 ± 0.20
2012X8R1H683KT5	X8R	50V	68,000	± 10%	1.25 ± 0.20

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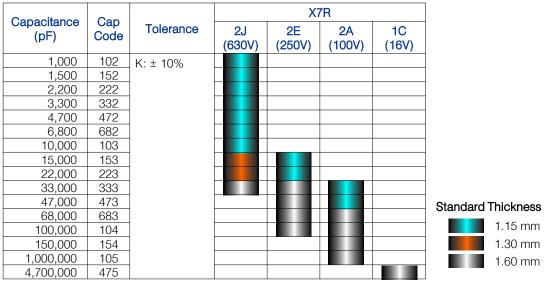
MULTILAYER CERAMIC CHIP CAPACITORS



C3216 [EIA CC1206]

Capacitance Range Chart

Temperature Characteristics: X7R, (± 15%) Rated Voltage: 630V (2J), 250V (2E), 100V (2A), 16V (1C)





Capacitance Range Table

C3216 [EIA CC1206]

Class 2 (Temperature Stable)

Temperature Characteristics X7R (-55 to +125°C, ±15%)

TDK Part Number (Ordering Code)	Temperature Characteristics	Rated Voltage	Capacitance (pF)	Capacitance Tolerance	Thickness (mm)
C3216X7R1C475MT5	X7R	16V	4,700,000	± 20%	1.60 ± 0.30
C3216X7R2A333KT5	X7R	100V	33,000	± 10%	1.15 ± 0.10
C3216X7R2A473KT5	X7R	100V	47,000	± 10%	1.15 ± 0.10
C3216X7R2A683KT5	X7R	100V	68,000	± 10%	1.60 ± 0.30
C3216X7R2A104KT5	X7R	100V	100,000	± 10%	1.60 ± 0.30
C3216X7R2A154KT5	X7R	100V	150,000	± 10%	1.60 ± 0.30
C3216X7R2A105KT5	X7R	100V	1,000,000	± 10%	1.60 ± 0.30
C3216X7R2E153KT5	X7R	250V	15,000	± 10%	1.15 ± 0.10
C3216X7R2E223KT5	X7R	250V	22,000	± 10%	1.15 ± 0.10
C3216X7R2E333KT5	X7R	250V	33,000	± 10%	1.60 ± 0.30
C3216X7R2E473KT5	X7R	250V	47,000	± 10%	1.60 ± 0.30
C3216X7R2E683KT5	X7R	250V	68,000	± 10%	1.60 ± 0.30
C3216X7R2E104KT5	X7R	250V	100,000	± 10%	1.60 ± 0.30
C3216X7R2J102KT5	X7R	630V	1,000	± 10%	1.15 ± 0.10
C3216X7R2J152KT5	X7R	630V	1,500	± 10%	1.15 ± 0.10
C3216X7R2J222KT5	X7R	630V	2,200	± 10%	1.15 ± 0.10
C3216X7R2J332KT5	X7R	630V	3,300	± 10%	1.15 ± 0.10
C3216X7R2J472KT5	X7R	630V	4,700	± 10%	1.15 ± 0.10
C3216X7R2J682KT5	X7R	630V	6,800	± 10%	1.15 ± 0.10
C3216X7R2J103KT5	X7R	630V	10,000	± 10%	1.15 ± 0.10
C3216X7R2J153KT5	X7R	630V	15,000	± 10%	1.30 ± 0.15
C3216X7R2J223KT5	X7R	630V	22,000	± 10%	1.30 ± 0.15
C3216X7R2J333KT5	X7R	630V	33,000	± 10%	1.60 ± 0.30

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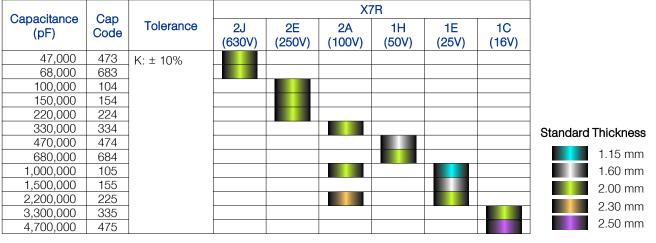
MULTILAYER CERAMIC CHIP CAPACITORS



C3225 [EIA CC1210]

Capacitance Range Chart

Temperature Characteristics: X7R, (± 15%) Rated Voltage: 630V (2J), 250V (2E), 100V (2A), 50V (1H), 25V (1E), 16V (1C)





Capacitance Range Table

C3225 [EIA CC1210]

Class 2 (Temperature Stable)

Temperature Characteristics X7R (-55 to +125°C, ±15%)

C3225X7R1C335KT5	X7R	16V			
		101	3,300,000	± 10%	2.00 ± 0.20
C3225X7R1C475KT5	X7R	16V	4,700,000	± 10%	2.50 ± 0.30
C3225X7R1E105KT5	X7R	25V	1,000,000	± 10%	1.15 ± 0.10
C3225X7R1E155KT5	X7R	25V	1,500,000	± 10%	1.60 ± 0.30
C3225X7R1E225KT5	X7R	25V	2,200,000	± 10%	2.00 ± 0.20
C3225X7R1H474KT5	X7R	50V	470,000	± 10%	1.60 ± 0.30
C3225X7R1H684KT5	X7R	50V	680,000	± 10%	2.00 ± 0.20
C3225X7R2A334KT5	X7R	100V	330,000	± 10%	2.00 ± 0.20
C3225X7R2A105KT5	X7R	100V	1,000,000	± 10%	2.00 ± 0.20
C3225X7R2A225KT5	X7R	100V	2,200,000	± 10%	2.30 ± 0.20
C3225X7R2E104KT5	X7R	250V	100,000	± 10%	2.00 ± 0.20
C3225X7R2E154KT5	X7R	250V	150,000	± 10%	2.00 ± 0.20
C3225X7R2E224KT5	X7R	250V	220,000	± 10%	2.00 ± 0.20
C3225X7R2J473KT5	X7R	630V	47,000	± 10%	2.00 ± 0.20
C3225X7R2J683KT5	X7R	630V	68,000	± 10%	2.00 ± 0.20

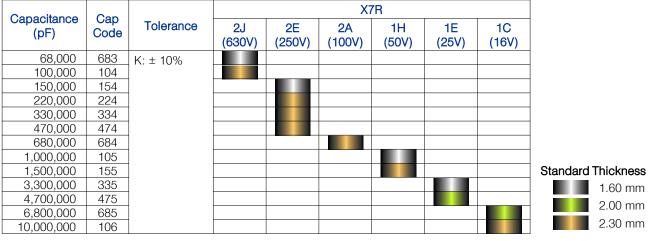
MULTILAYER CERAMIC CHIP CAPACITORS



C4532 [EIA CC1812]

Capacitance Range Chart

Temperature Characteristics: X7R, (± 15%) Rated Voltage: 630V (2J), 250V (2E), 100V (2A), 50V (1H), 25V (1E), 16V (1C)





Capacitance Range Table

C4532 [EIA CC1812]

Class 2 (Temperature Stable)

Temperature Characteristics X7R (-55 to +125°C, ±15%)

TDK Part Number (Ordering Code)	Temperature Characteristics	Rated Voltage	Capacitance (pF)	Capacitance Tolerance	Thickness (mm)
C4532X7R1C685KT5	X7R	16V	6,800,000	± 10%	2.00 ± 0.20
C4532X7R1C106KT5	X7R	16V	10,000,000	± 10%	2.30 ± 0.20
C4532X7R1E335KT5	X7R	25V	3,300,000	± 10%	1.60 ± 0.30
C4532X7R1E475KT5	X7R	25V	4,700,000	± 10%	2.00 ± 0.20
C4532X7R1H105KT5	X7R	50V	1,000,000	± 10%	1.60 ± 0.30
C4532X7R1H155KT5	X7R	50V	1,500,000	± 10%	2.30 ± 0.20
C4532X7R2A684KT5	X7R	100V	680,000	± 10%	2.30 ± 0.20
C4532X7R2E154KT5	X7R	250V	150,000	± 10%	1.60 ± 0.30
C4532X7R2E224KT5	X7R	250V	220,000	± 10%	2.30 ± 0.20
C4532X7R2E334KT5	X7R	250V	330,000	± 10%	2.30 ± 0.20
C4532X7R2E474KT5	X7R	250V	470,000	± 10%	2.30 ± 0.20
C4532X7R2J683KT5	X7R	630V	68,000	± 10%	1.60 ± 0.30
C4532X7R2J104KT5	X7R	630V	100,000	± 10%	2.30 ± 0.20

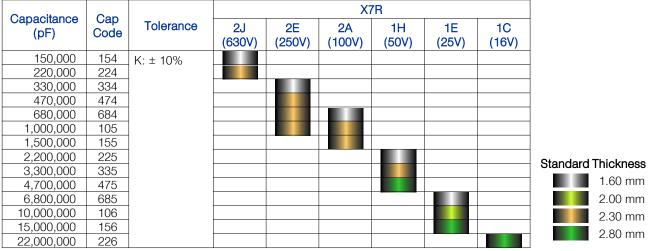
MULTILAYER CERAMIC CHIP CAPACITORS



C5750 [EIA CC2220]

Capacitance Range Chart

Temperature Characteristics: X7R, (± 15%) Rated Voltage: 630V (2J), 250V (2E), 100V (2A), 50V (1H), 25V (1E), 16V (1C)





Capacitance Range Table

C5750 [EIA CC2220]

Class 2 (Temperature Stable)

Temperature Characteristics X7R (-55 to +125°C, ±15%)

TDK Part Number (Ordering Code)	Temperature Characteristics	Rated Voltage	Capacitance (pF)	Capacitance Tolerance	Thickness (mm)
C5750X7R1C226MT5	X7R	16V	22,000,000	± 20%	2.80 ± 0.20
C5750X7R1E685KT5	X7R	25V	6,800,000	± 10%	1.60 ± 0.30
C5750X7R1E106KT5	X7R	25V	10,000,000	± 10%	2.00 ± 0.20
C5750X7R1E156MT5	X7R	25V	15,000,000	± 20%	2.80 ± 0.20
C5750X7R1H225KT5	X7R	50V	2,200,000	± 10%	1.60 ± 0.30
C5750X7R1H335KT5	X7R	50V	3,300,000	± 10%	2.30 ± 0.20
C5750X7R1H475KT5	X7R	50V	4,700,000	± 10%	2.80 ± 0.20
C5750X7R2A684KT5	X7R	100V	680,000	± 10%	1.60 ± 0.30
C5750X7R2A105KT5	X7R	100V	1,000,000	± 10%	2.30 ± 0.20
C5750X7R2A155KT5	X7R	100V	1,500,000	± 10%	2.30 ± 0.20
C5750X7R2E334KT5	X7R	250V	330,000	± 10%	1.60 ± 0.30
C5750X7R2E474KT5	X7R	250V	470,000	± 10%	2.30 ± 0.20
C5750X7R2E684KT5	X7R	250V	680,000	± 10%	2.30 ± 0.20
C5750X7R2E105KT5	X7R	250V	1,000,000	± 10%	2.30 ± 0.20
C5750X7R2J154KT5	X7R	630V	150,000	± 10%	1.60 ± 0.30
C5750X7R2J224KT5	X7R	630V	220,000	± 10%	2.30 ± 0.20

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MULTILAYER CERAMIC CHIP CAPACITORS



General Specifications

C Series – Open Mode Design

No.	ltem	Per	formance		Test or Inspection Method				
1	External Appearance		defects which may af ormance.	fect	Inspect with magnifying glass (3 $ imes$).				
2	Insulation Resistance	whic capa	000MΩ or 500MΩ•μF chever smaller. (As fo acitors of rated voltag 000 MΩ or 100MΩ•μF	or the ge 16V DC,	Apply rated voltage for 60s. As for the rated voltage 630V DC, apply 500V DC.				
3	Voltage Proof	With	nstand test voltage w	ithout	Rat	ed Voltage	Apply volta	ade	
-			lation breakdown or			V ≤ 100V	2.5 × rated vo		
					R	V > 100V	1.5 × rated vo		
						-	be applied for not exceed 50n	1 to 5s. Charge / nA.	
4	Capacitance	Within the specified tolerance.		Class	Rated Capacitance	Measuring Frequency	Measuring voltage		
					Class 2	C ≤ 10uF	1kHz±10%	1.0±0.2V _{rms}	
						C > 10uF	120Hz±20%	0.5 ± 0.2 V _{rms}	
5	Dissipation	T.C.	Rated Voltage (DC)	D.F.	See No.4	4 in this table fo	or measuring co	ndition.	
	Factor	X7R	RV = 25V& 50V	3% max.			Ū.		
	(Class 2)	X8R	RV ≤ 16V	5% max.					
6	Temperature Characteristics of Capacitance	Capacitance Change (%) No Voltage Applied		•	wing table after	•	steps shown in rium is obtained		
	(Class 2)		X7R: ± 15%		ΔC be calculated ref. STEP 3 reading				
	, ,		X8R: ± 15%		Step	Temperature (°C)	-	
					 1	Reference temp	-		
					2	Min. operating 1		-	
					3	Reference temp	-	-	
					4	Max. operating	temp. \pm 2		
7	Robustness of Terminations	No sign of termination coming off, breakage of ceramic, or other abnormal signs.		Appendi	x 1a or Append 5N for 10±1s.	citors on P.C. b lix 1b) and appl	y a pushing		
8	Bending	No r	No mechanical damage.			solder the capacity $(x 2)$ and bend is $50 + \frac{20}{50}$	citor on P.C. bo t for 1mm. F	ard (shown in	

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Unit: mm

Version B11

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MULTILAYER CERAMIC CHIP CAPACITORS



General Specifications

C Series – Open Mode Design

No.	Item	Performance		Test or Inspection Method		
9	Solderability	New solder to contermination.	ver over 75% of	Completely soak both terminations in solder at $235\pm5^{\circ}$ C for 2 ± 0.5 s.		
		25% may have pi	inholes or rough spots	Solder: H63A (JIS Z 3282)		
		but not concentra		Flux: Isopropyl alcohol (JIS K 8839)		
		Ceramic surface not be exposed d shifting of termina		Rosin (JIS K 5902) 25% solid solution.		
		A section				
10	Resistance to so	older heat		Completely soak both terminations in solder at		
	External appearance		owed and terminations at least 60% with new	260±5°C for 5±1s. Preheating condition Temp.: 150±10°C		
	Capacitance	Characteristics	Change from the value before test	Time : 1 to 2min. Flux: Isopropyl alcohol (JIS K 8839) Rosin (JIS K 5902) 25% solid solution. Solder: H63A (JIS Z 3282) Leave the capacitor in ambient conditions for 6 to 24h		
		Class 2 X7R X8R	± 7.5%			
	D.F. (Class 2)	Meet the initial sp	Dec.			
	Insulation Resistance	Meet the initial sp	Dec.	before measurement.		
	Voltage Proof	No insulation bread	akdown or other			
11	Vibration			Reflow solder the capacitor on P.C. board (shown in		
	External	No mechanical da	amage.	Appendix 1a or Appendix 1b) before testing.		
	appearance			Vibrate the capacitor with amplitude of 1.5mm P-P sweeping the frequencies from 10Hz to 55Hz and back		
	Capacitance	Characteristics	Change from the value before test	to 10Hz after 1min.		
		Class 2 X7R X8R	± 7.5%	 Repeat this for 2h each in 3 perpendicular directions. 		
	D.F. (Class 2)	Meet the initial sp	Dec.	_		

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MULTILAYER CERAMIC CHIP CAPACITORS



General Specifications

C Series – Open Mode Design

No.	ltem	Performance		Test o	r Inspection Method			
12	Temperature cyc External appearance	Sle No mechanical damage.		 Reflow solder the capacitors on a P.C. board (shown in Appendix 1a or Appendix 1b) before testing. Expose the capacitor in the conditions in step 1 through step 4, and repeat 5 times consecutively. 				
	Capacitance	Characteristics	Change from the value before test	Leave t	he capacitor in ambient con- measurement.	2		
		Class 2 X7R X8R	± 7.5%	Step	Temperature (°C)	Time (min.)		
	D.F. (Class 2)	Meet the initial	spec.	- <u>1</u> 2	Min. operating temp. ± 3 Reference Temp.	30 ± 3 $2 - 5$		
	Insulation Resistance	Meet the initial spec.		3 4	Max. operating temp. ± 2Reference Temp.	30 ± 2 2 - 5		
	Voltage Proof	No insulation breakdown or other damage.		_				
13	Moisture Resista External appearance	ance (Steady State No mechanical	-	Reflow solder the capacitor on P.C. board (shown in Appendix 1a or Appendix 1b) before testing. Leave at temperature 40±2°C, 90 to 95%RH for 500				
	Capacitance	Characteristics	Change from the value before test		+24,0h. Leave the capacitor in ambient condition for $24\pm 2h$			
		Class 2 X7R X8R	± 12.5%	before measurement.				
	D.F. (Class 2) Characteristics X7R: 200% of initial spec. max. X8R: 200% of initial spec. max.		_					
	Insulation Resistance	1,000MΩ or 50MΩ• μ F min., whichever smaller. (As for the capacitors of rated voltage 16V DC, 1,000 MΩ or 10MΩ• μ F min.,)						

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General Specifications

C Series – Open Mode Design

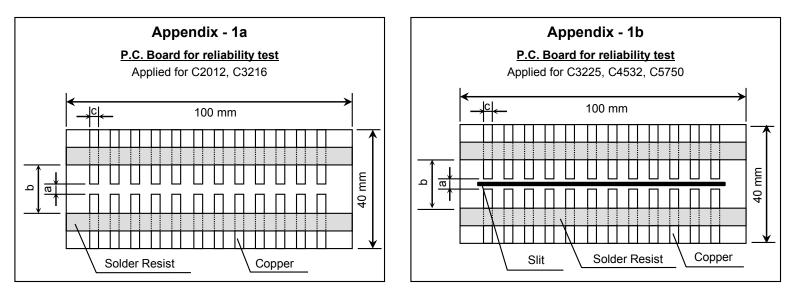
No.	ltem	Performance		Test or Inspection Method	
14	Moisture Resista	ance		Reflow solder the capacitors on P.C. board (shown in Appendix 1a or Appendix 1b) before testing.	
	External appearance	5		Appendix Ta of Appendix Tb) before testing. Apply the rated voltage at temperature $40\pm2^{\circ}$ C and 90 to 95%RH for 500 +24,0h.	
	Capacitance	Characteristics	Change from the value before test	Charge/discharge current shall not exceed 50mA.	
		Class 2 X7R X8R	± 12.5%	Leave the capacitor in ambient conditions for 24 \pm 2h before measurement.	
	D.F. (Class 2)	Characteristics		Voltage conditioning:	
		X7R: 200% of in X8R: 200% of in		Voltage treat the capacitors under testing temperature and voltage for 1 hour.	
	Insulation 500MΩ or 25MΩ•μF min., whichever smaller. (As for the capacitors of rated voltage 16V DC, 500 MΩ or 5MΩ•μF min.,)			 Leave the capacitors in ambient condition for 24±2h before measurement. 	
			•	Use this measurement for initial value.	
15	Life			Reflow solder the capacitors on P.C. board (shown in	
	External appearance	No mechanical o	damage.	Appendix 1a or Appendix 1b) before testing. Apply rated voltage at maximum operating temperature	
	Capacitance	Characteristics	Change from the value before test	$\pm 2^{\circ}$ C for 1,000 +48, 0h. Some items may be tested at higher voltage (1.2x, 1.5x or 2xRV).	
		Class 2 X7R X8R	± 15%	Charge/discharge current shall not exceed 50mA.	
	D.F. (Class 2)	Characteristics		Leave the capacitor in ambient conditions for $24\pm 2h$ before measurement.	
		X7R: 200% of in	•	Voltage conditioning:	
		X8R: 200% of in	•	Voltage treat the capacitors under testing temperature and voltage for 1 hour.	
	Insulation Resistance	smaller. (As for	/Ω•μF min., whichever the capacitors of rated , 1,000 MΩ or 10MΩ•μF	Leave the capacitors in ambient condition for $24\pm 2h$ before measurement.	
		min.,)		Use this measurement for initial value.	

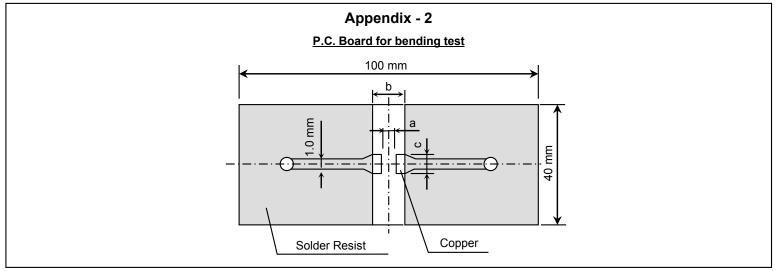
*As for the initial measurement of capacitors (Class 2) on number 6, 10, 11, 12 and 13, leave capacitor at 150 -10, 0°C for 1 hour and measure the value after leaving capacitor for 24±2h in ambient condition.

MULTILAYER CERAMIC CHIP CAPACITORS



C Series – Open Mode Design





Material : Glass Epoxy (As per JIS C6484 GE4)

P.C. Board thickness: 1.6mm



Copper (thickness 0.035mm) Solder resist

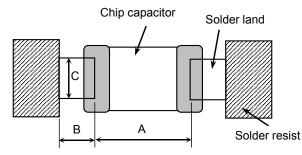
Case	Code	Dimensions (mm)				
JIS	EIA	а	b	С		
C2012	CC0805	1.2	4.0	1.65		
C3216	CC1206	2.2	5.0	2.0		
C3225	CC1210	2.2	5.0	2.9		
C4532	CC1812	3.5	7.0	3.7		
C5750	CC2220	4.5	8.0	5.6		

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MULTILAYER CERAMIC CHIP CAPACITORS



Recommended Soldering Land Pattern



Wave Solderi	Unit: mm		
Туре	C2012	C3216	
Symbol	[CC0805]	[CC1206]	
А	1.0 - 1.3	2.1 - 2.5	
В	1.0 - 1.2	1.1 - 1.3	
С	0.8 - 1.1	1.0 - 1.3	

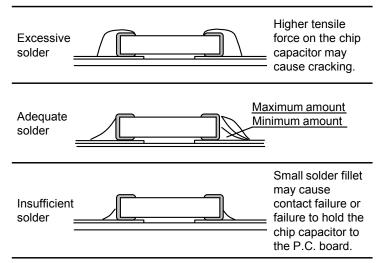
Reflow Solde	Reflow Soldering Unit: mn	
Туре	C2012	C3216
Symbol	[CC0805]	[CC1206]
А	0.9 - 1.2	2.0 - 2.4
В	0.7 - 0.9	1.0 - 1.2
С	0.9 - 1.2	1.1 - 1.6

Reflow Soldering

Unit: mm

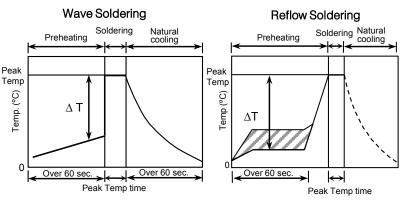
Туре	C3225	C4532	C5750
Symbol	[CC1210]	[CC1812]	[CC2220]
A	2.0 - 2.4	3.1 - 3.7	4.1 - 4.8
В	1.0 - 1.2	1.2 - 1.4	1.2 - 1.4
С	1.9 - 2.5	2.4 - 3.2	4.0 - 5.0

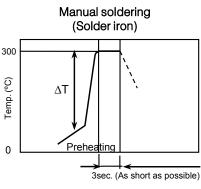
Recommended Solder Amount



C Series – Open Mode Design

Recommended Soldering Profile





Recommended soldering duration

Temp./	Wave Soldering		Reflow Soldering		
Dura.	Peak temp	Duration	Peak temp	Duration	
Solder	(°C)	(sec.)	(°C)	(sec.)	
Sn-Pb Solder	250 max.	3 max.	230 max.	20 max.	
Lead-Free Solder	260 max.	5 max.	260 max.	10 max.	

Recommended solder compositions

Sn-37Pb (Sn-Pb solder)

Sn-3.0Ag-0.5Cu (Lead Free Solder)

Preheating Condition

Soldering	Case Size - JIS (EIA)	Temp. (°C)
Wave soldering	C2012(CC0805), C3216(CC1206)	∆T ≤ 150
Reflow	C2012(CC0805), C3216(CC1206)	∆T ≤ 150
soldering	C3225(CC1210), C4532(CC1812), C5750(CC2220)	∆T ≤ 130
Manual	C2012(CC0805), C3216(CC1206)	∆T ≤ 150
Manual soldering	C3225(CC1210), C4532(CC1812), C5750(CC2220)	∆T ≤ 130

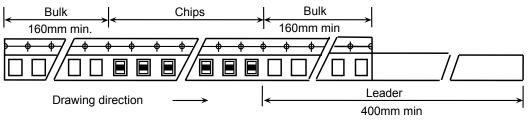
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MULTILAYER CERAMIC CHIP CAPACITORS

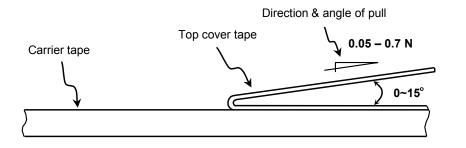


C Series – Open Mode Design

Carrier Tape Configuration



• Peel Back Force (Top Tape)



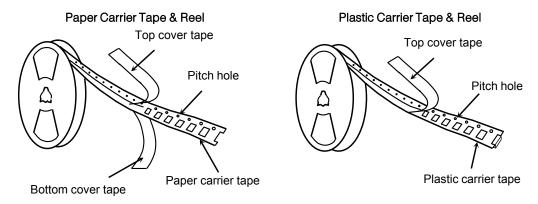
• Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.

 \bullet The missing of components shall be less than 0.1%

· Components shall not stick to the cover tape.

• The cover tape shall not protrude beyond the edges of the carrier tape and shall not cover the sprocket holes.

• Chip Quantity Per Reel and Structure of Reel (Paper & Plastic)



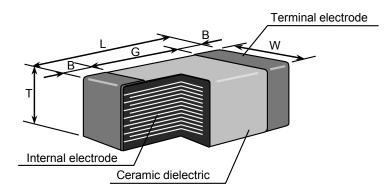
Case	e Code	Chip Taping Material		Chip quantity (pcs.)	
JIS	EIA	Thickness	Taping Material	φ178mm (7") reel	φ330mm (13") reel
C2012	CC0805	0.85 mm	Paper/Plastic	4,000	10,000
02012	CC0805	1.25 mm	Plastic	2,000	10,000
		1.15 mm			10.000
C3216	CC1206	1.30 mm	Plastic	2,000	10,000
		1.60 mm			8,000
		1.15 mm		2.000	10,000
		1.60 mm		2,000	8,000
C3225	CC1210	2.00 mm	Plastic		
		2.30 mm		1,000	5,000
		2.50 mm			
		1.60 mm		1 000	
C4532	CC1812	2.00 mm	Plastic	1,000	3,000
		2.30 mm		500	-
		1.60 mm		1,000	
05750	000000	2.00 mm	Diactia		3,000
C5750	CC2220	2.30 mm	Plastic	500	
		2.80 mm			2,000

MULTILAYER CERAMIC CHIP CAPACITORS



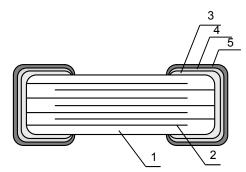
C Series – Open Mode Design

Shape & Dimensions



Case Code		Dimensions (mm)				
JIS	EIA	L	W	Т	В	G
C2012	CC0805	2.00	1.20	0.85	0.20 min.	0.50 min.
62012	CC0805	2.00	1.20	1.25	0.20 mm.	0.50 mm.
				1.15		
C3216	CC1206	3.20	1.60	1.30	0.20 min.	1.00 min.
				1.60		
				1.15		
				1.60	0.20 min.	
C3225	CC1210	3.20	2.50	2.00		1.00 min.
				2.30	0.30 min.	
				2.50	0.30 mm.	
				1.60		
C4532	CC1812	4.50	3.20	2.00	0.20 min.	2.00 min.
				2.30		
				1.60		
C5750	CC2220	5.70	5.00	2.00	0.20 min.	2.00 min.
05750	002220	5.70	5.00	2.30	0.20 11111.	2.00 11111.
				2.80		

• Inside Structure & Material System



No.	NAME	MATERIAL		
		Class 1	Class 2	
(1)	Ceramic Dielectric	CaZrO ₃	BaTiO ₃	
(2)	Internal Electrode	Nickel (Ni)		
(3)		Coppe	er (Cu)	
(4)	Termination	Nickel (Ni)		
(5)		Tin (Sn)		

• Environmental Information

TDK Corporation established internal product environmental assurance standards that include the six hazardous substances banned by the EU RoHS Directive¹ enforced on July 1, 2006 along with additional substances independently banned by TDK and has successfully completed making general purpose electronic components conform to the RoHS Directive².

- Abbreviation for Restriction on Hazardous Substances, which refers to the regulation EU Directive 2002/95/EC on hazardous substances by the European Union (EU) effective from July 1, 2006. The Directive bans the use of six specific hazardous substances in electric and electronic devices and products handled within the EU. The six substances are lead, mercury, cadmium, hexavalent chromium, PBB (polybrominated biphenyls), and PBDE (polybrominated diphenyl ethers).
- 2. This means that, in conformity with the EU Directive 2002/95/EC, lead, cadmium, mercury, hexavalent chromium, and specific bromine-based flame retardants, PBB and PBDE, have not been used, except for exempted applications.
- For REACH (SVHC : 15 substances according to ECHA / October 2008) : All TDK MLCC do not contain these 15 substances.
- For European Directive 2000/53/CE and 2005/673/CE : Cadmium, Hexavalent Chromium, Mercury, Lead are not contained in all TDK MLCC.
- For European Directive 2003/11/CE : Pentabromodiphenylether, Octabromodiphenyl-ether are not contained in all TDK MLCC.