

OKI semiconductor

MSC2340-XXYS9/KS9

7-46-23-15

4,194,304 Word x 9 Bit DYNAMIC RAM MODULE: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2340-XXYS9/KS9 is a fully decoded, 4,194,304 word by 9 bit CMOS dynamic random access memory composed of nine 4Mb DRAMs in SOJ (MSM514100JS). The mounting of nine SOJs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2340-XXYS9/KS9 are quite same as the original MSM514100 JS; each timing requirements are noncritical, and power supply tolerance is very wide.

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FEATURES

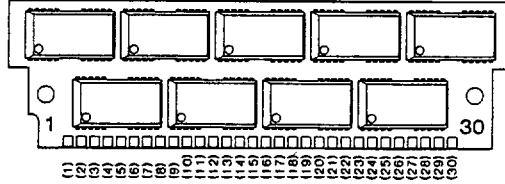
- 4,194,304 word x 9 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}		Operating (MAX)	Standby (MAX)
MSC2340-8 YS9/KS9	80 ns	40 ns	20 ns	160 ns	4455 mW	49.5 mW (MOS level)
MSC2340-8A YS9/KS9	80 ns	40 ns	25 ns	160 ns	4455 mW	
MSC2340-10 YS9/KS9	100 ns	50 ns	25 ns	190 ns	3960 mW	

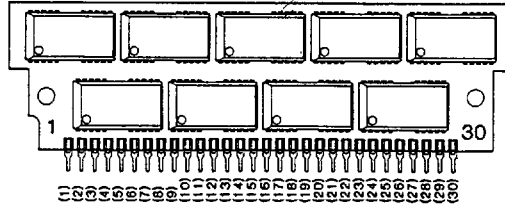
- Single + 5 V supply, ± 10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- Common $\overline{\text{CAS}}$ control for eight common Data-in and Data-out lines
- Separate $\overline{\text{CAS}}$ control for one separate pair of Data-in and Data-out lines
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$ only refresh capability
- Multi bit test mode capability

PIN ASSIGNMENT

MSC2340-XXYS9



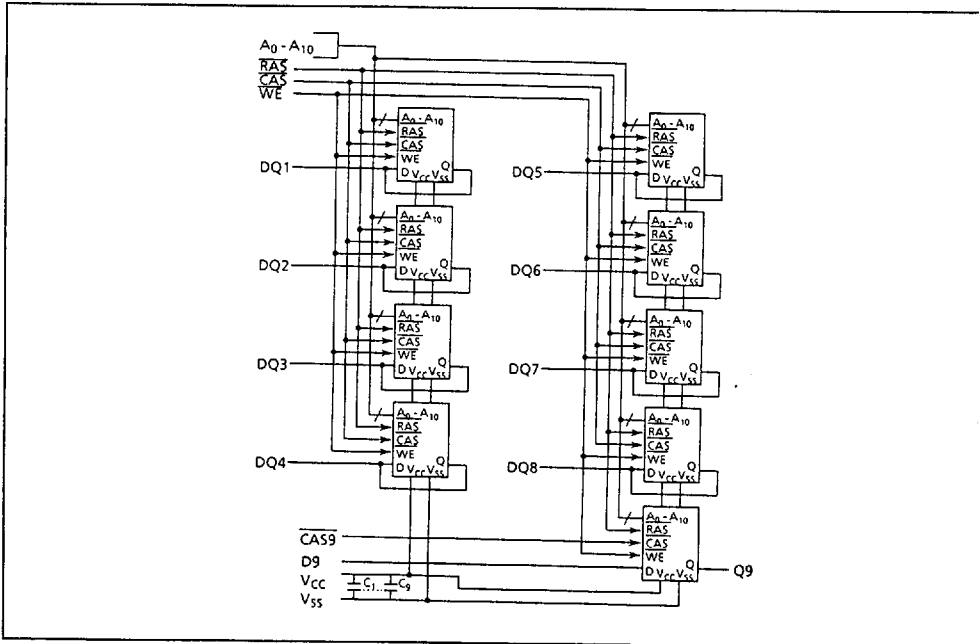
MSC2340-XXKS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	VCC	11	A4	21	WE
2	CAS	12	A5	22	VSS
3	DQ1	13	DO4	23	DO7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DO8
6	DQ2	16	DO5	26	DO9
7	A2	17	A8	27	RAS
8	A3	18	A9	28	CAS
9	VSS	19	A10	29	D9
10	DO3	20	DO6	30	VCC

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FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	$T_a = 25^\circ\text{C}$	- 1.0 to + 7.0	V	1
Short circuit output current	I_{OS}	$T_a = 25^\circ\text{C}$	50	mA	1
Power dissipation	P_D	$T_a = 25^\circ\text{C}$	9	W	1
Operating temperature	T_{opr}	-	0 to + 70	$^\circ\text{C}$	1
Storage temperature	T_{stg}	-	- 40 to + 125	$^\circ\text{C}$	1

RECOMMENDED OPERATING CONDITIONS

 $(T_a = 0 \text{ to } +70^\circ\text{C})$

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	-	6.5	V	2
Input low voltage	V_{IL}	- 1.0	-	0.8	V	2

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. All voltages are referenced to V_{SS} .

CAPACITANCE

 $(T_a = 25^\circ\text{C}, f = 1 \text{ MHz})$

Parameter	Symbol	TYP	MAX	Unit
Input Capacitance (A_0 to A_{10})	C_{IN1}	55	70	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{WE})	C_{IN2}	55	75	pF
Data Input/Output Capacitance (DQ1 to DQ8)	C_{DQ}	12	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{IN3}	7	15	pF
Input Capacitance (D9)	C_{IN4}	7	15	pF
Output Capacitance (Q9)	C_{OUT}	8	15	pF

Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

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 $(V_{CC} = 5V \pm 10\%, T_a = 0 \text{ to } +70^\circ\text{C})$

Parameter	Symbol	Conditions	MSC2340-8 YS9/KS9		MSC2340-8A YS9/KS9		MSC2340-10 YS9/KS9		Unit	Note	
			MIN	MAX	MIN	MAX	MIN	MAX			
Output high voltage	V_{OH}	$I_{OH} = -5.0 \text{ mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V		
Output low voltage	V_{OL}	$I_{OL} = 4.2 \text{ mA}$	0	0.4	0	0.4	0	0.4	V		
Input leakage current	I_{LI}	$0V \leq V_I \leq 6.5V$; all other pins not under test = 0V	90	90	90	90	90	90	μA		
Output leakage current	I_{LO}	DQ1-8, Q9 = disable $0V < V_O \leq 5.5V$	-10	10	-10	10	-10	10	μA		
Average power supply current (Operating)	I_{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{CAS9}}$ cycling, $t_{RC} = \text{min}$	-	810	-	810	-	720	mA	1, 2	
Power supply current (Standby)	I_{CC2}	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}}$, $\overline{\text{CAS9}}$ = V_{IH}	TTL	-	18	-	18	-	18	mA	
		DQ1-8, Q9 = Hz	MOS	-	9	-	9	-	9		
Average power supply current (RAS only refresh)	I_{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$, $\overline{\text{CAS9}} = V_{IH}$ $t_{RC} = \text{min}$	-	810	-	810	-	720	mA	1, 2	
Power supply current (Standby)	I_{CC5}	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}}$, $\overline{\text{CAS9}} = V_{IL}$, DQ1-8, Q9 = enable	-	45	-	45	-	45	mA	1	
Average power supply current (CAS before RAS refresh)	I_{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	-	810	-	810	-	720	mA	1	
Average power supply current (Fast page mode)	I_{CC7}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$, $\overline{\text{CAS9}}$ cycling $t_{PC} = \text{min}$	-	720	-	720	-	630	mA	1, 3	

Notes: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.

2. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

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AC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, T_a = 0 to +70°C)

Note 1, 2, 3, 9, 10

Parameter	Symbol	MSC2340-8 YS9 / KS9		MSC2340-8A YS9 / KS9		MSC2340-10 YS9 / KS9		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t _{RC}	160	—	160	—	190	—	ns	
Fast page mode cycle time	t _{PC}	55	—	55	—	65	—	ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}	—	80	—	80	—	100	ns	4, 5
Access time from $\overline{\text{CAS}}$	t _{CAC}	—	20	—	25	—	25	ns	4, 5
Access time from column address	t _{AA}	—	40	—	40	—	50	ns	4, 6
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	45	—	45	—	55	ns	4
Output low impedance time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
Output buffer turn-off delay time	t _{OFF}	0	20	0	20	0	25	ns	7
Transition time	t _T	3	50	3	50	3	50	ns	3
Refresh period	t _{REF}	—	16	—	16	—	16	ms	
$\overline{\text{RAS}}$ precharge time	t _{RP}	70	—	70	—	80	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	80	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	t _{RASP}	80	100,000	80	100,000	100	100,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	20	—	25	—	25	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	80	—	80	—	100	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	22	60	25	55	25	75	ns	5
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	17	40	20	40	20	50	ns	6
Row address set-up time	t _{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t _{RAH}	12	—	15	—	15	—	ns	
Column address set-up time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	15	—	15	—	20	—	ns	
Column address hold time from $\overline{\text{RAS}}$	t _{AR}	60	—	60	—	75	—	ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	40	—	40	—	50	—	ns	

AC CHARACTERISTICS (Continued)

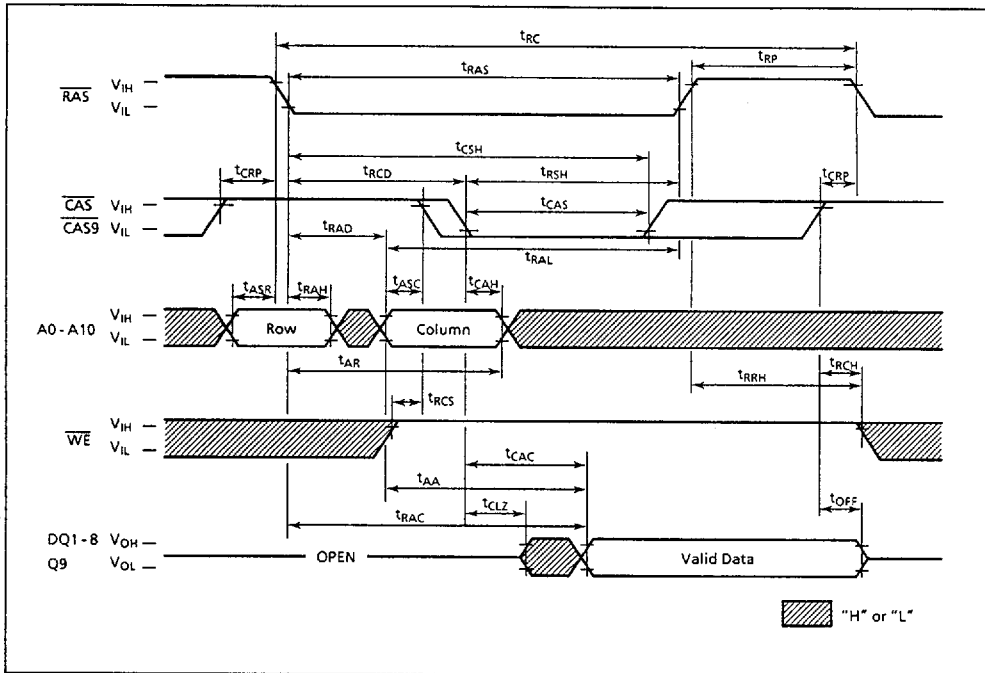
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Parameter	Symbol	MSC2340-8 YS9 / KS9		MSC2340-8A YS9 / KS9		MSC2340-10 YS9 / KS9		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Read command hold time	t_{RCH}	0	-	0	-	0	-	ns	8
Read command hold time reference to \overline{RAS}	t_{RRH}	10	-	10	-	10	-	ns	8
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	
Write command hold time	t_{WCH}	15	-	15	-	20	-	ns	
Write command hold time from \overline{RAS}	t_{WCR}	60	-	60	-	75	-	ns	
Write command pulse width	t_{WCP}	15	-	15	-	20	-	ns	
Write command to \overline{RAS} lead time	t_{RWL}	20	-	25	-	25	-	ns	
Write command to \overline{CAS} lead time	t_{CWL}	20	-	25	-	25	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	0	-	ns	
Data-in hold time	t_{DH}	15	-	15	-	20	-	ns	
Data-in hold time from \overline{RAS}	t_{DHR}	60	-	60	-	75	-	ns	
\overline{CAS} active delay time from \overline{RAS} precharge	t_{RPC}	10	-	10	-	10	-	ns	
\overline{RAS} to \overline{CAS} set-up time (\overline{CAS} before \overline{RAS})	t_{CSR}	10	-	10	-	10	-	ns	
\overline{RAS} to \overline{CAS} hold time (\overline{CAS} before \overline{RAS})	t_{CHR}	20	-	20	-	20	-	ns	
\overline{CAS} precharge time (Refresh counter test)	t_{CPT}	40	-	40	-	50	-	ns	
\overline{WE} to \overline{RAS} precharge time (\overline{CAS} before \overline{RAS})	t_{WRP}	10	-	10	-	10	-	ns	
\overline{WE} hold time from \overline{RAS} (\overline{CAS} before \overline{RAS})	t_{WRH}	20	-	20	-	20	-	ns	
\overline{RAS} to \overline{WE} set-up time (Test mode)	t_{WSR}	10	-	10	-	10	-	ns	
\overline{RAS} to \overline{WE} hold time (Test mode)	t_{WHR}	20	-	20	-	20	-	ns	

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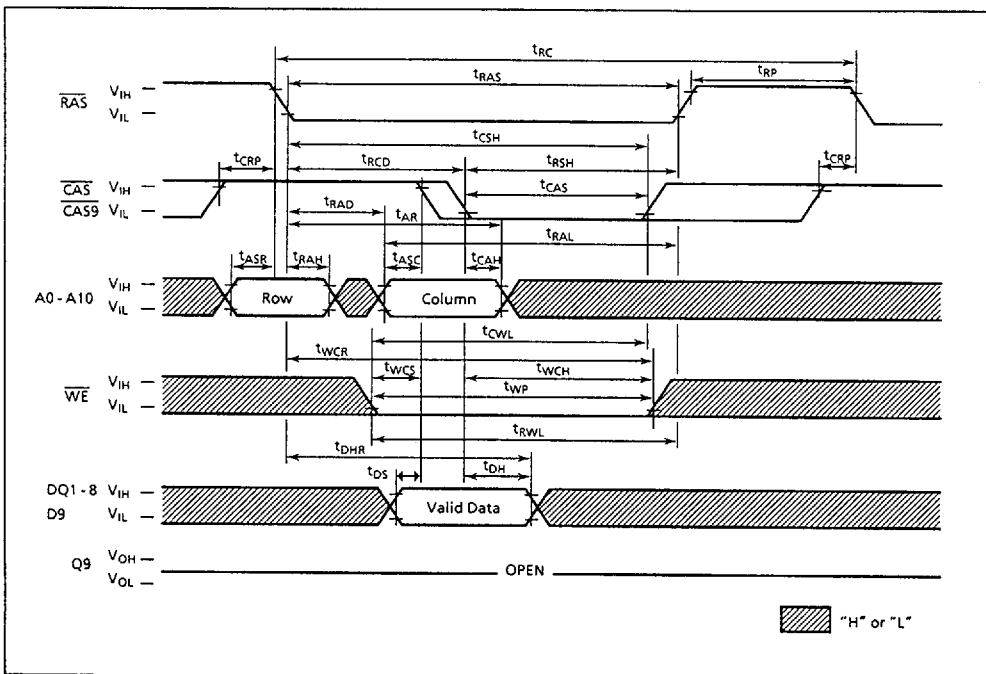
- Notes: 1. An initial pause of 200 μ s is required after power-up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, a minimum of eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ initialization cycles is required.
2. The AC characteristics assume $t_T = 5$ ns.
 3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 4. Measured with a load circuit equivalent to 2TTL loads and 100pF.
 5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC} .
 6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA} .
 7. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
 9. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated. The test mode specified in this data sheet is 8-bit parallel test function. RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are equal, the data output pin will indicate a high level. If any internal bits are not equal, then data output pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{\text{RAS}}$ only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 10. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

READ CYCLE



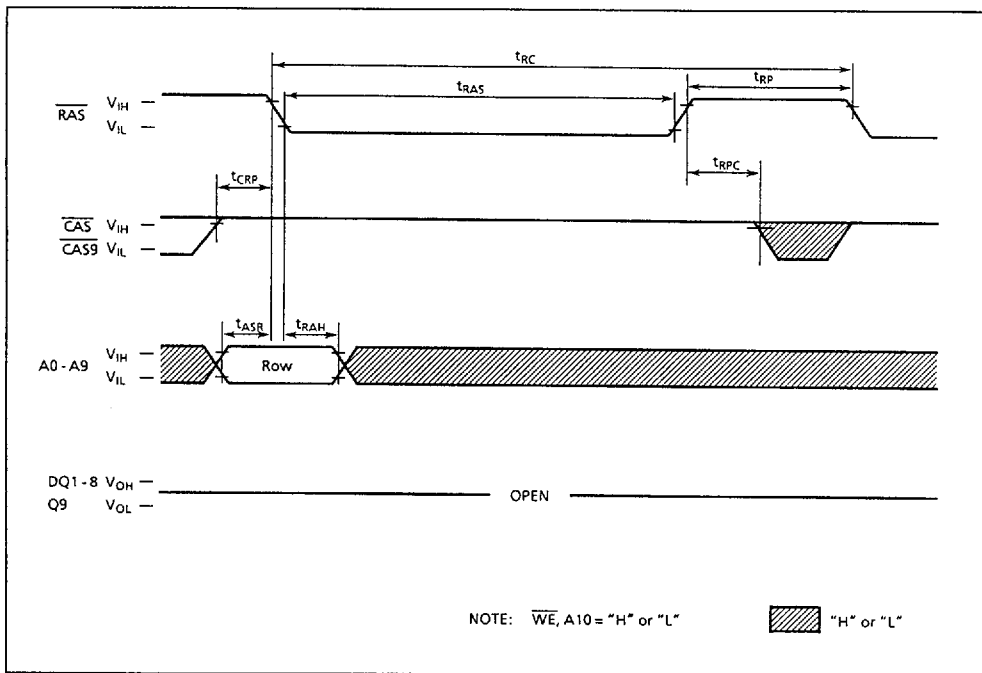
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WRITE CYCLE (EARLY WRITE)



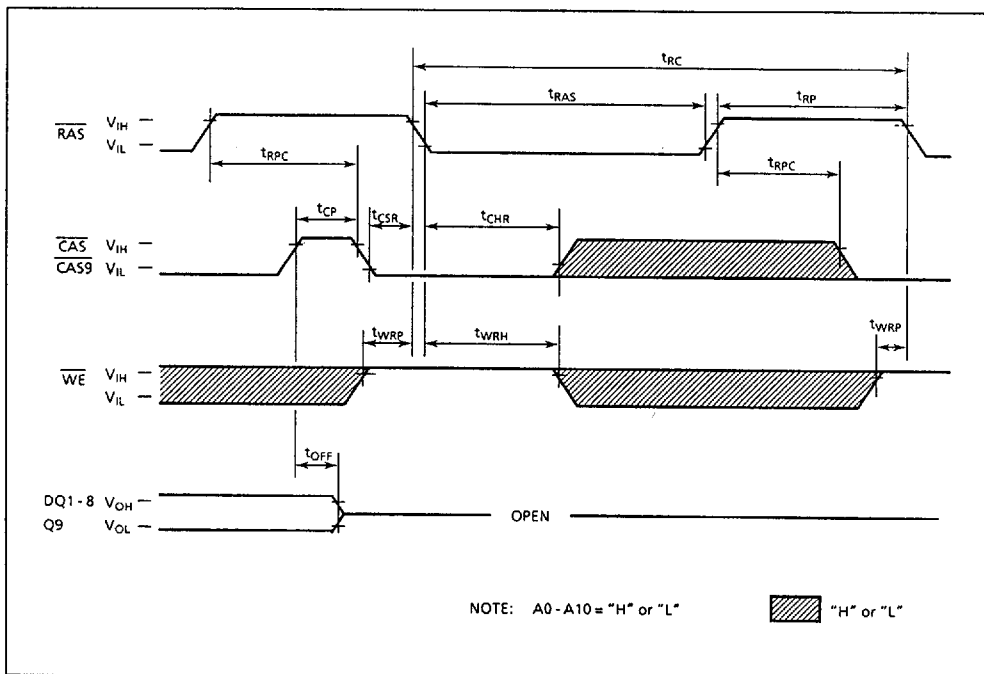
RAS ONLY REFRESH CYCLE

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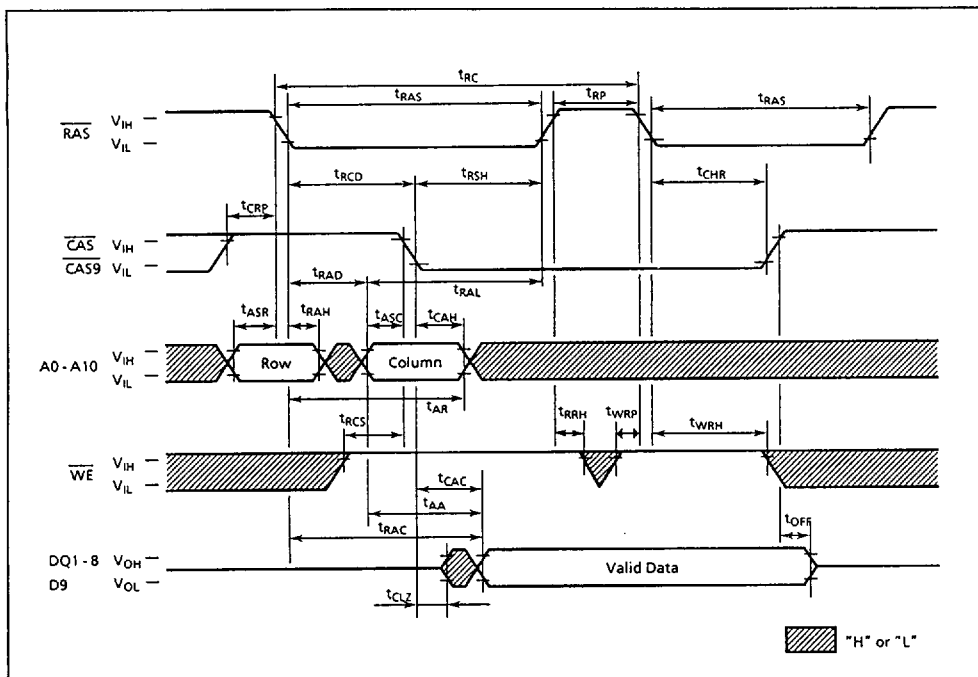
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CAS BEFORE RAS AUTO REFRESH CYCLE

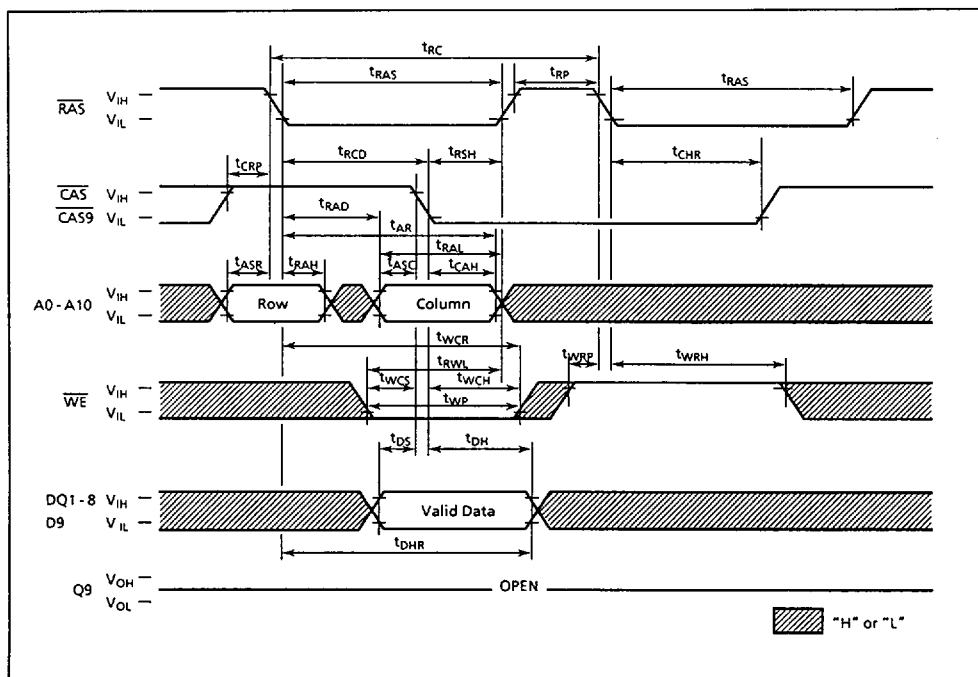


HIDDEN REFRESH READ CYCLE

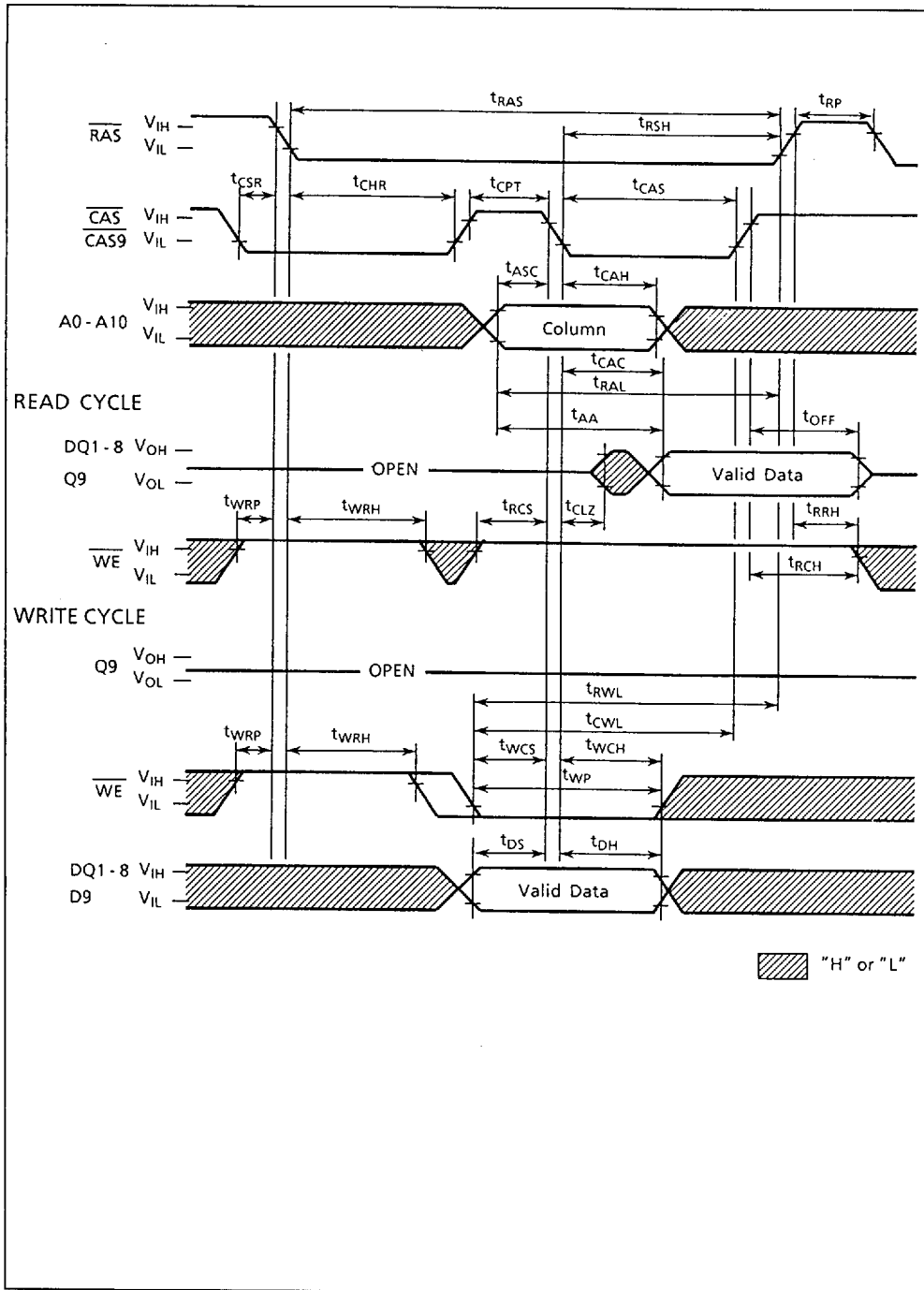
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HIDDEN REFRESH WRITE CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST

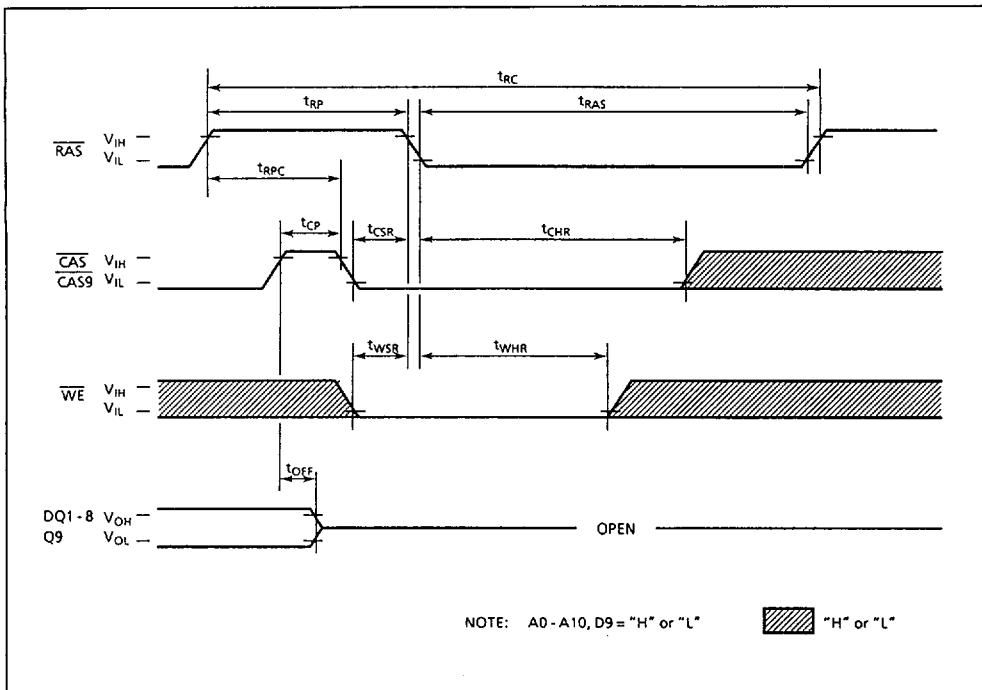


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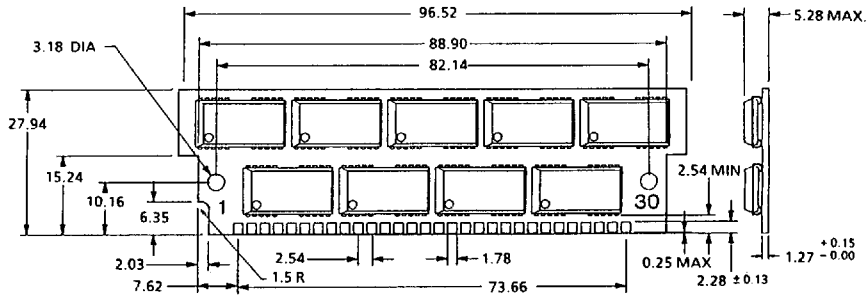
TEST MODE INITIATE CYCLE

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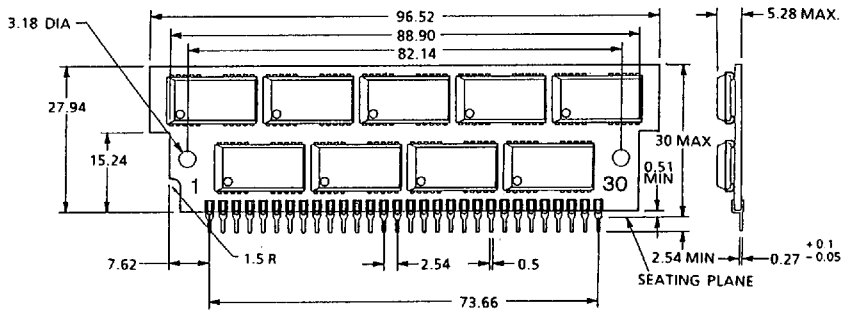


MSC2340YS9



- NOTE 1) SUBSTRATE GLASS EPOXY (FR-4)
 2) CONTACT PADS Pb/Sn or Au PLATING
 3) 4M x 1 DRAM x 9 pcs

MSC2340KS9



- NOTE 1) SUBSTRATE GLASS EPOXY (FR-4)
 2) CONTACT LEAD Pb/Sn SOLDER
 3) SEATING PLANE (PAI 0.83, PITCH 2.54)
 4) 4M x 1 DRAM x 9 pcs

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