4,194,304 Word x 9 Bit DYNAMIC RAM MODULE: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2340-xxYS9/KS9 is a fully decoded, 4,194,304 word by 9 bit CMOS dynamic random access memory composed of nine 4Mb DRAMs in SOJ (MSM514100JS). The mounting of nine SOJs together with nine 0.2µF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2340-xxYS9/KS9 are same as the original MSM514100JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

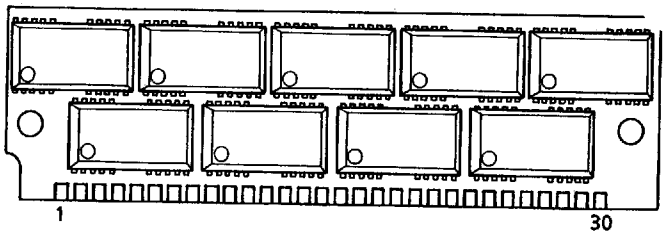
- 4,194,304 word x 9 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (MAX)	Standby (MAX)
MSC2340-80YS9/KS9	80 ns	40 ns	20 ns	160 ns	4455 mW	50 mW (MOS level)
MSC2340-10YS9/KS9	100 ns	50 ns	25 ns	190 ns	3960 mW	

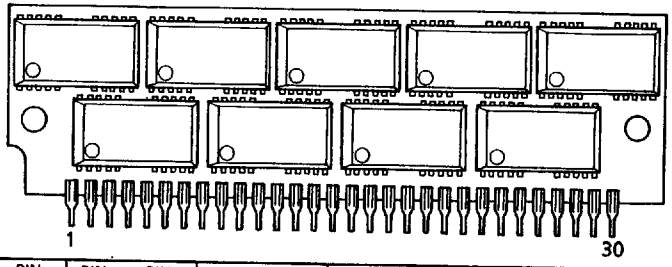
- Single + 5 V supply, ± 10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- Common $\overline{CAS}$ control for eight common Data-in and Data-out lines
- Separate $\overline{CAS}$ control for one separate pair of Data-in and Data-out lines
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi-bit test mode capability

PIN CONFIGURATION

MSC2340-xxYS9

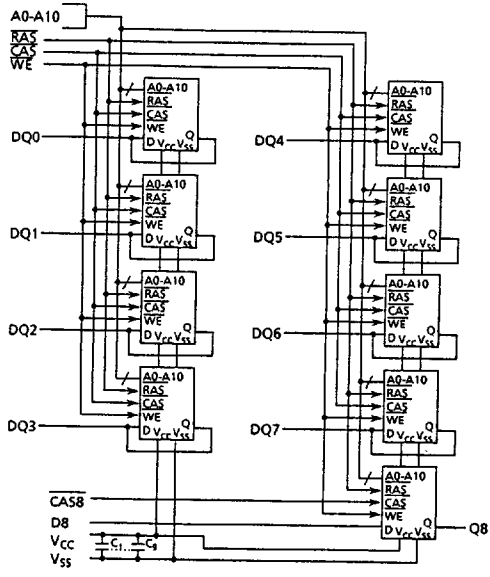


MSC2340-xxKS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	6	DQ1	11	A4	16	DQ4	21	$\overline{WE}$	26	Q8
2	$\overline{CAS}$	7	A2	12	A5	17	A8	22	VSS	27	$\overline{RAS}$
3	DQ0	8	A3	13	DQ3	18	A9	23	DQ6	28	$\overline{CAS8}$
4	A0	9	VSS	14	A6	19	A10	24	NC	29	D8
5	A1	10	DQ2	15	A7	20	DQ5	25	DQ7	30	V_{CC}

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	Ta = 25 °C	− 1.0 ~ + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	Ta = 25 °C	− 1.0 ~ + 7.0	V
Short circuit output current	Ios	Ta = 25 °C	50	mA
Power dissipation	P_D	Ta = 25 °C	9	W
Operating temperature	Topr	−	0 ~ + 70	°C
Storage temperature	Tstg	−	− 40 ~ + 125	°C

Notes: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	MIN	TYP	MAX	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C ~ + 70°C
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	−	6.5	V	
Input low voltage	V_{IL}	− 1.0	−	0.8	V	

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	TYP	MAX	Unit
Input Capacitance (A0 - A10)	C_{IN1}	55	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	55	75	pF
Data Input/Output Capacitance (DQ0 - DQ7)	C_{DQ}	12	20	pF
Input Capacitance ($\overline{CAS8}$)	C_{IN3}	7	15	pF
Input Capacitance (D8)	C_{IN4}	7	15	pF
Output Capacitance (Q8)	C_{OUT}	8	15	pF

Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 ~ + 70°C)

Parameter	Symbol	Conditions		MSC2340-80 YS9/KS9 MIN	MSC2340-80 YS9/KS9 MAX	MSC2340-10 YS9/KS9 MIN	MSC2340-10 YS9/KS9 MAX	Unit	Note
Input leakage current	I_{LI}	0 V ≦ V_{IN} ≦ 6.5V; all other pins not under test = 0 V		– 90	90	– 90	90	µA	
Output leakage current	I_{LO}	DQ0 - 7,Q8 = disable 0 V ≦ V_{OUT} ≦ 5.5 V		– 10	10	– 10	10	µA	
Output high voltage	V_{OH}	I_{OH} = – 5.0 mA		2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$, $\overline{CAS8}$ cycling, t_{RC} = min		–	810	–	720	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$, $\overline{CAS8}$ = V_{IH} DQ0~7, Q8 = Hz	TTL	–	18	–	18	mA	
			MOS	–	9	–	9		
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$ = V_{IH} t_{RC} = min		–	810	–	720	mA	1, 2
Power supply current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$, $\overline{CAS8}$ = V_{IL} DQ0~7, Q8 = enable		–	45	–	45	mA	1
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling,		–	810	–	720	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$, $\overline{CAS8}$ cycling t_{PC} = min		–	720	–	630	mA	1, 3

Note: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 ~ +70°C)

Note 1, 2, 3, 9, 10

Parameter	Symbol	MSC2340-80 YS9/KS9		MSC2340-10 YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	–	190	–	ns	
Fast page mode cycle time	t_{PC}	55	–	65	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4, 5
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4, 5
Access time from column address	t_{AA}	–	40	–	50	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	55	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay time	t_{OFF}	0	20	0	25	ns	7
Transition time	t_T	3	50	3	50	ns	3
Refresh period	t_{REF}	–	16	–	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	

AC CHARACTERISTICS (Continued)

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Parameter	Symbol	MSC2340-80 YS9/KS9		MSC2340-10 YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	15	–	20	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	ns	
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	–	20	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	50	–	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	–	10	–	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	20	–	20	–	ns	
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test mode)	t_{WSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (Test mode)	t_{WHR}	20	–	20	–	ns	

Notes: 1. An initial pause of 200μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.

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2. The AC characteristics assume $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL loads and 100pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect untill the exit cycle is generated.
The test mode specified in this data sheet is 8-bit parallel test function.
RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are not equal, then the data output pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
10. In a test mode read cycle, the value of an access time parameters is delayed by 5ns from the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

READ CYCLE

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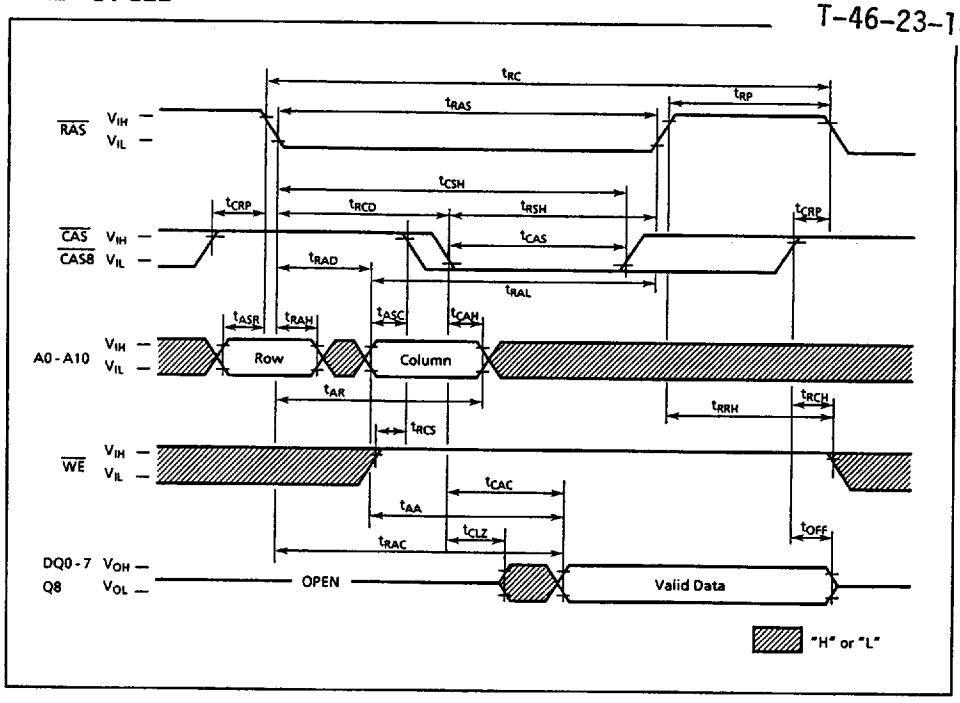
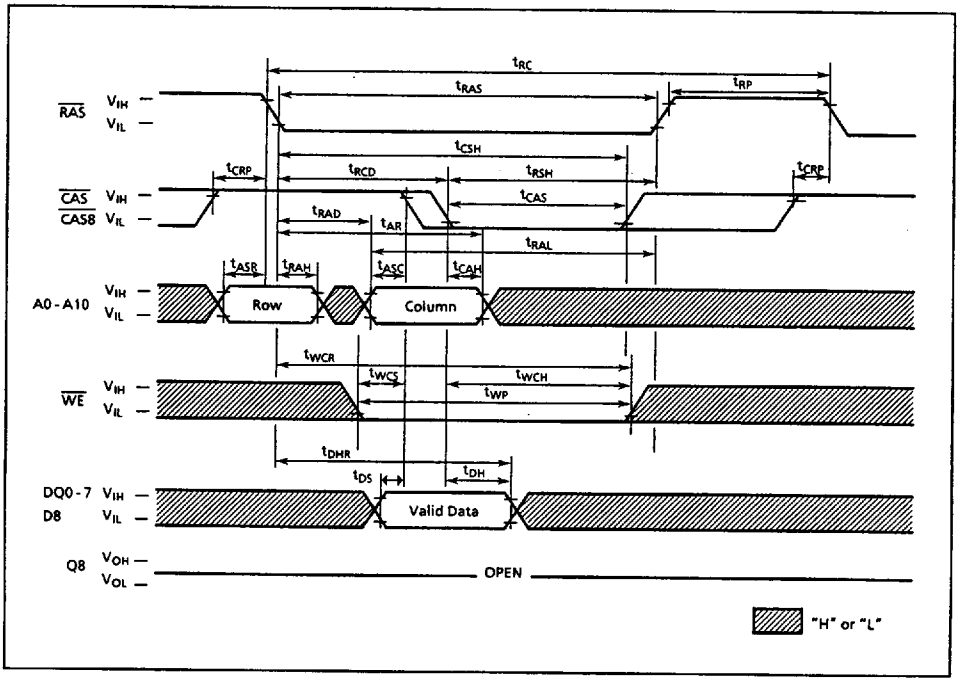


WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ CYCLE

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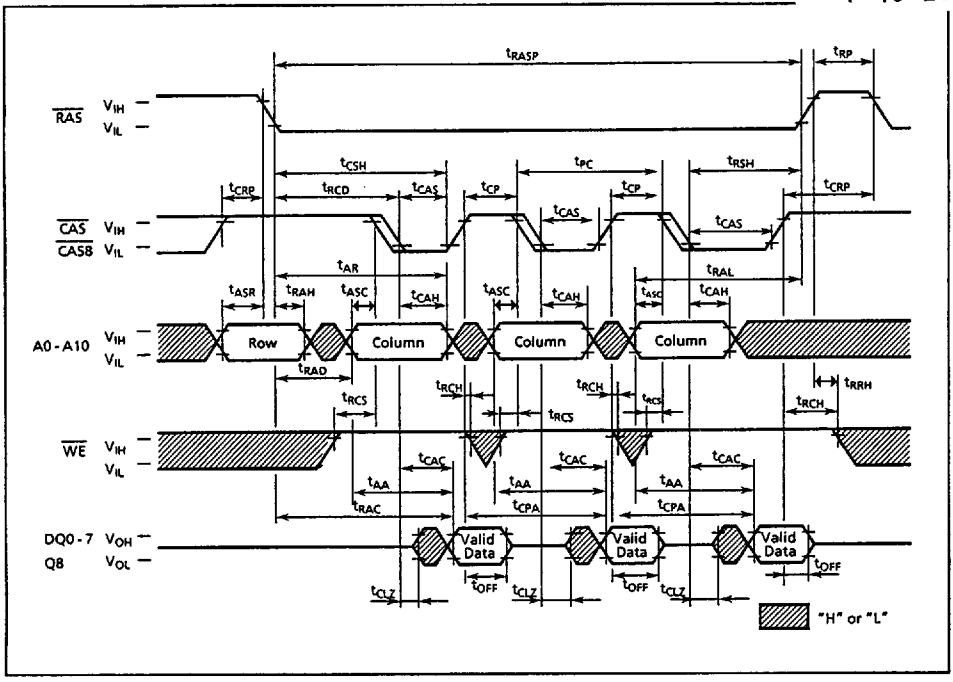
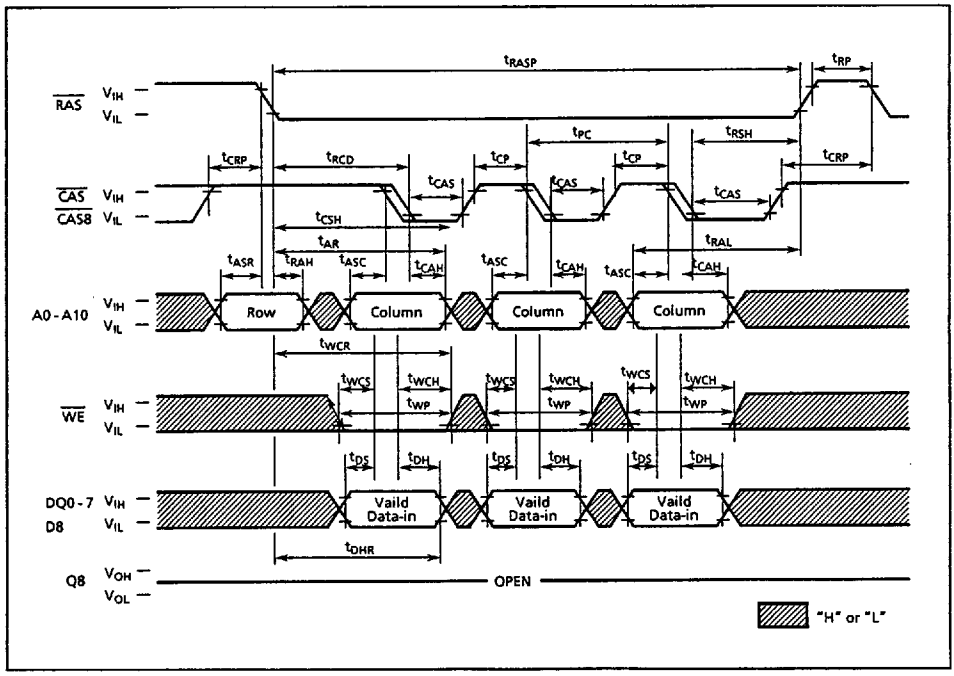
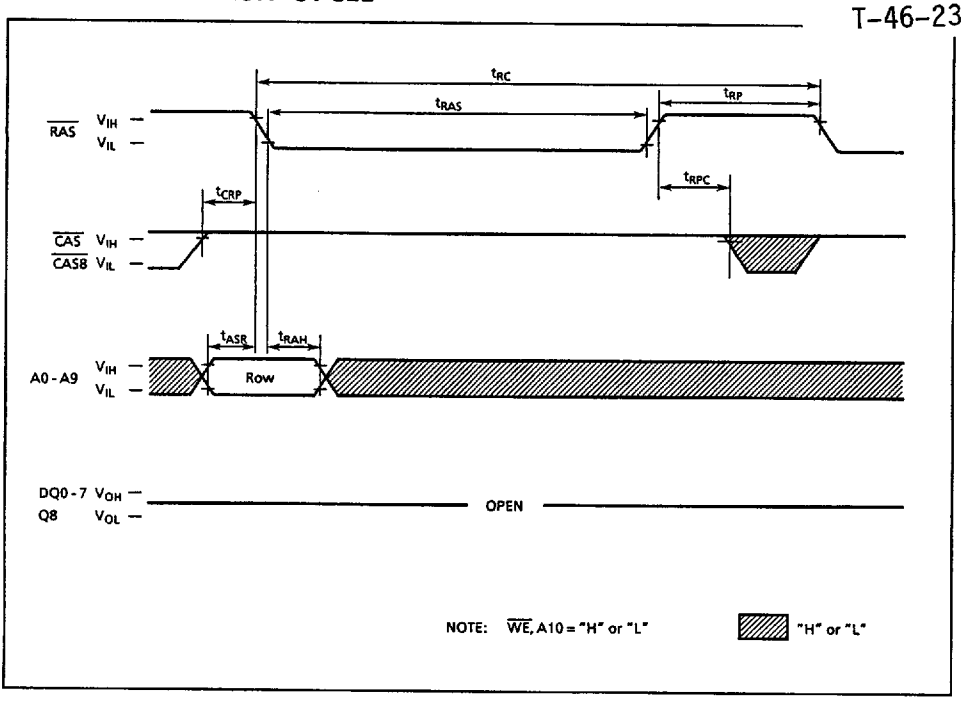


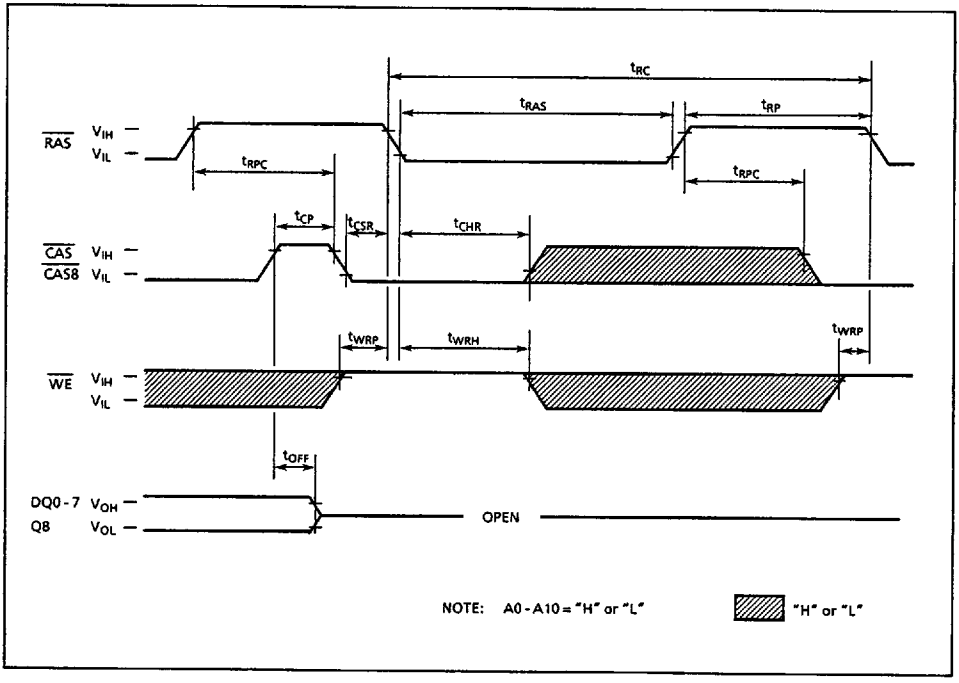
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE

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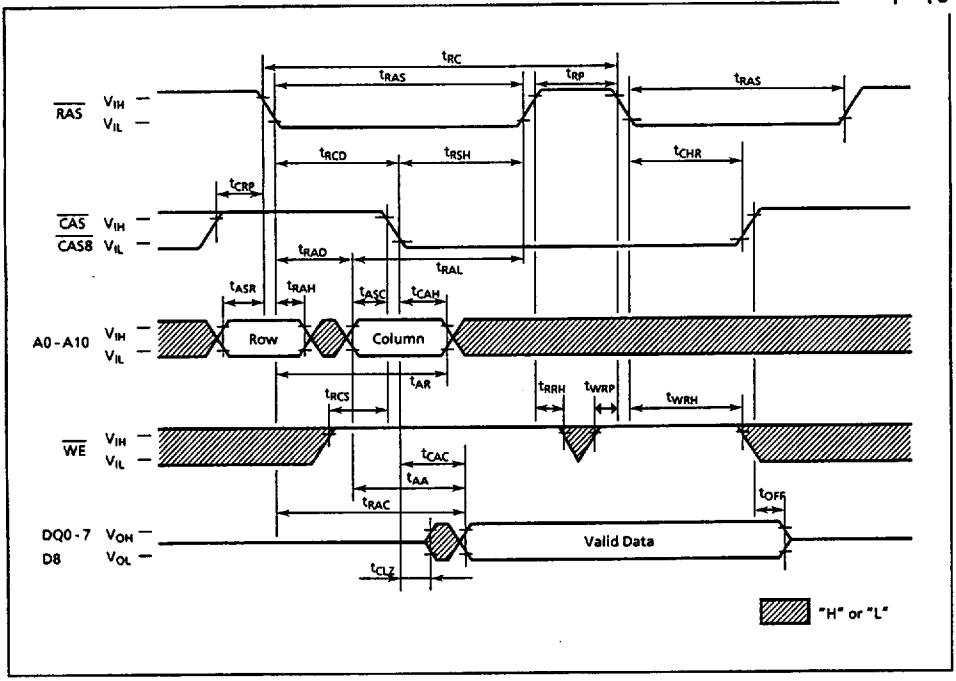
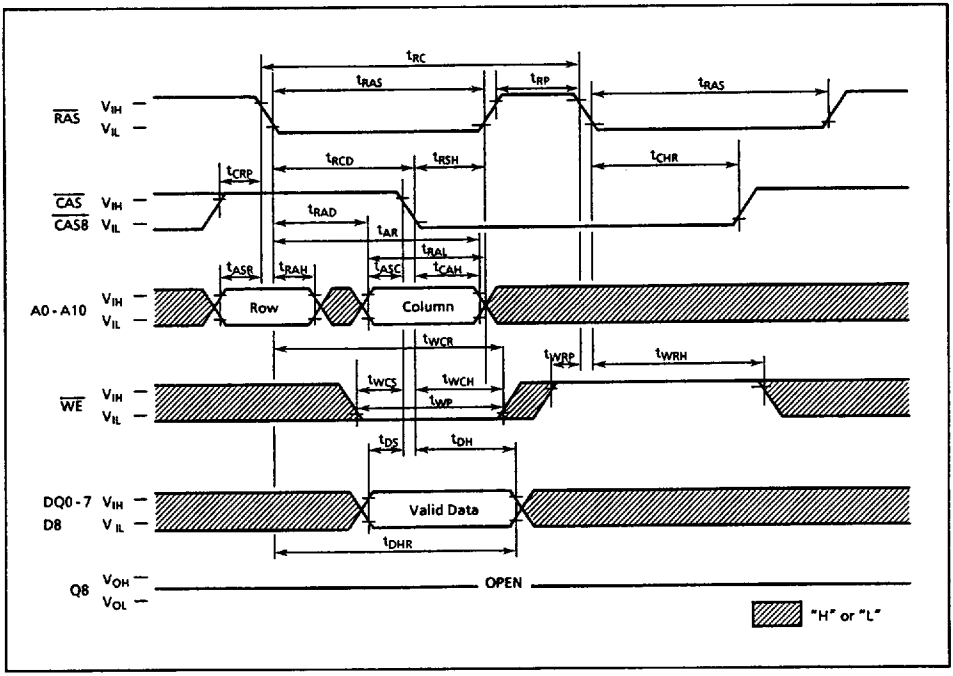


HIDDEN REFRESH WRITE CYCLE



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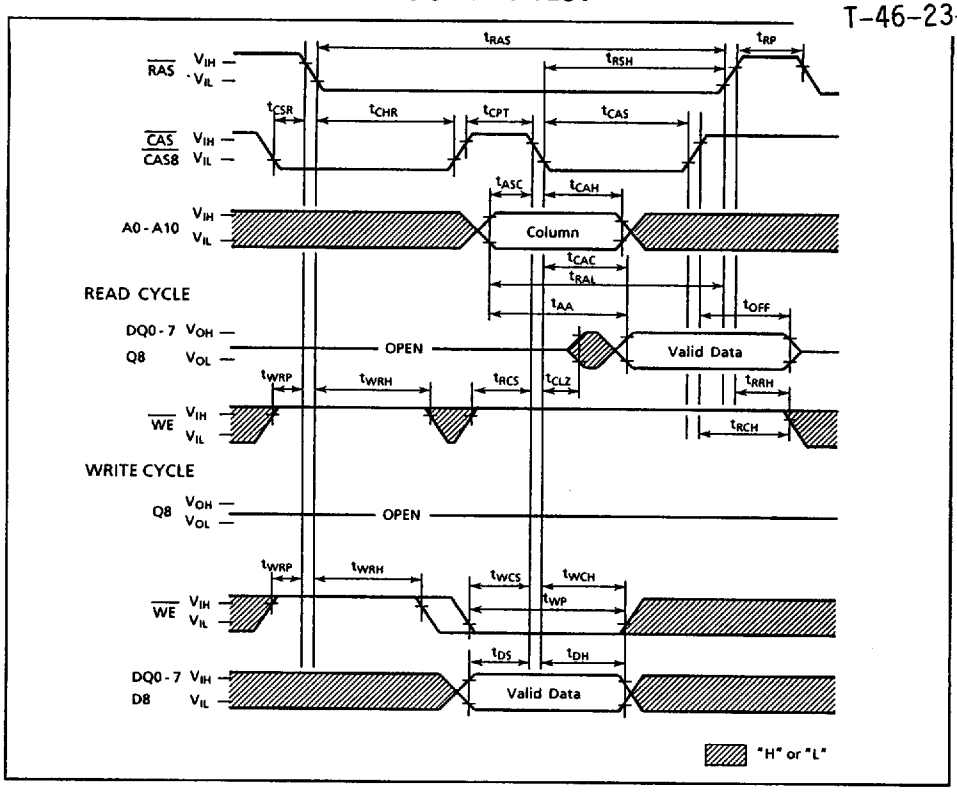
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST



TEST MODE INITIATE CYCLE