OKI semiconductor T-46-23-17

MSC2329-xxYS3/KS3

262,144 Word BY 9 Bit DYNAMIC RAM MODULE : PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2329-xxYS3/KS3 is a fully decoded, 262,144 word × 9 bit dynamic random access memory composed of two 1 Mb DRAMs in SOJ (MSM514256AJS) and one 256Kb DRAM in PLCC (MSM41256AJS). The mounting of two SOJs and one PLCC together with three 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2329-xxYS3/KS3 are same as the original MSM41256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

- 262,144 word × 9 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)		Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2329-10YS3/KS3	100ns	50ns	200ns	1155mW	50mW
MSC2329-12YS3/KS3	120ns	60ns	220ns	1073mW	

- Single + 5V supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8 ms
- Common $\overline{CAS}$ Control for eight Common Data-in and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-in and Data-Out Lines

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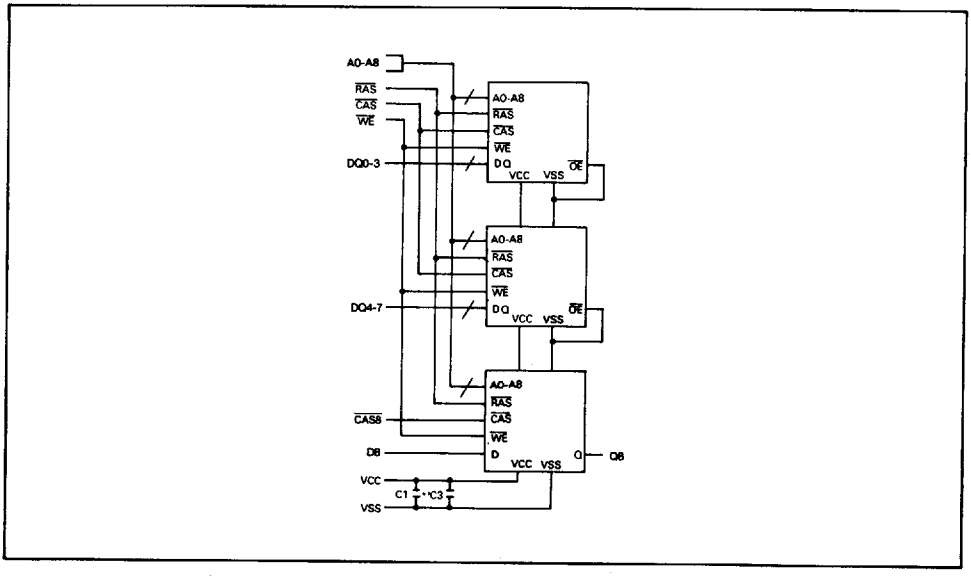
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

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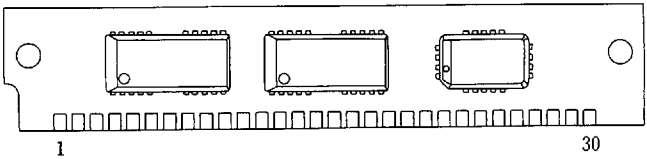
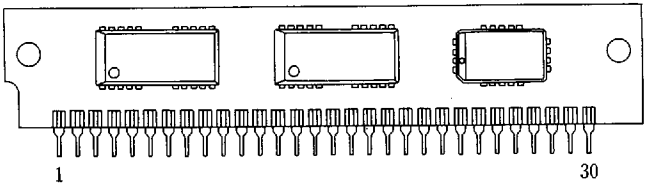


MSC2329-xxKS3



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	Vcc	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	Q8
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	$\overline{CAS8}$
9	VSS	19	NC	29	D8
10	DQ2	20	DQ5	30	Vcc

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ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ +125	°C
Power dissipation	P_D	4	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±10%, Ta=0~+70°C)

Parameter	Symbol	Condition	MSC2329-10YS3/KS3		MSC2329-12YS3/KS3		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0V≤V_{IN}≤6.5V : All other pins not under test=0V	−30	30	−30	30	μA	
Output Leakage Current	I_{LO}	DQ0-7, Q8=disable 0V≤V_{OUT}≤5.5V	−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA	2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA	—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$, $\overline{CAS8}$ cycling, t_{RC}=min	—	210	—	195	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CAS}$, $\overline{CAS8}$=V_{IH}	—	9	—	9	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$=V_{IH} t_{RC}=min	—	205	—	190	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.	—	205	—	190	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$=V_{IL} $\overline{CAS}$, $\overline{CAS8}$ cycling t_{PC}=min.	—	150	—	135	mA	1, 3

Note : 1. I_{CC} in dependent on out put loading and cycle rates. Specified value are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

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CAPACITANCE

(Ta = 25°C, f = 1 MHz)

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Parameter	Symbol	Max.	Unit
Input Capacitance (A0 – A8)	C_{IN1}	40	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	pF
Data Input/Output Capacitance (DQ0 — DQ7)	C_{DQ}	20	pF
Input Capacitance ($\overline{CAS8}$)	C_{IN3}	10	pF
Input Capacitance (D8)	C_{IN4}	10	pF
Output Capacitance (Q8)	C_{OUT}	15	pF

Capacitance measured with Boonton Meter.

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AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 ~ +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2329-10YS3/KS3		MSC2329-12YS3/KS3		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	4	–	4	ms	
Random read or write cycle time	t_{RC}	200	–	220	–	ns	
Page mode cycle time	t_{PC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 5
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	4. 5
Output buffer turn-off delay	t_{OFF}	0	30	0	30	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	90	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10K	120	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10K	60	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	ns	5
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	20	–	25	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	75	–	90	–	ns	

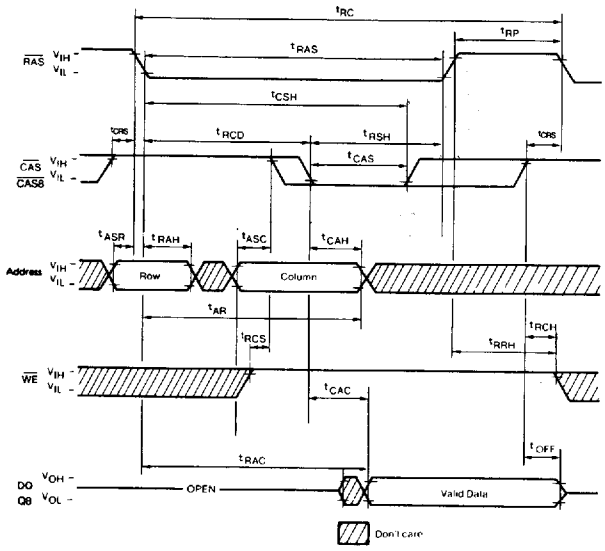
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSC2329-10YS3/KS3		MSC2329-12YS3/KS3		Unit	Note
		MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	6
Write command hold time from $\overline{RAS}$	t_{WCR}	75	–	90	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	20	–	20	–	ns	
Write command pulse width	t_{WP}	20	–	20	–	ns	
Date-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	75	–	90	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20	–	20	–	ns	6
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$	t_{FCH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	ns	

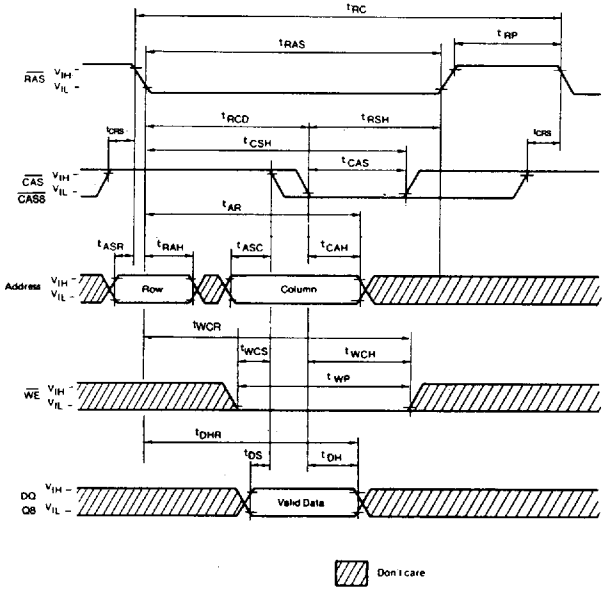
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example : $\overline{RAS}$ only refresh cycle) before proper device operation is acieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2 TTL loads and 100pF
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

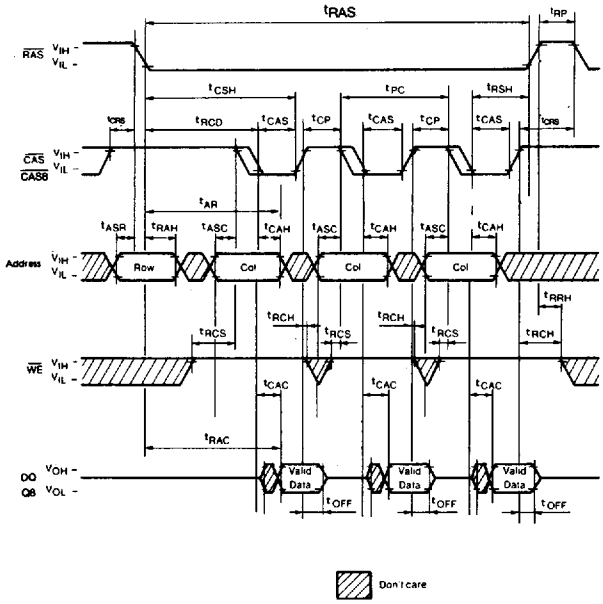
READ CYCLE



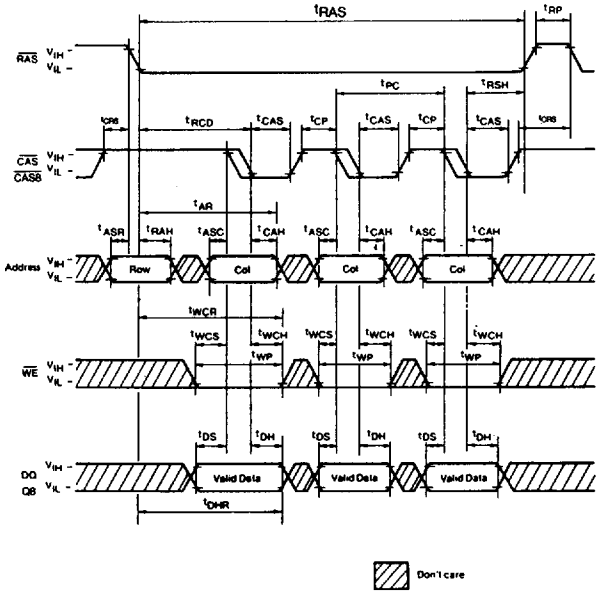
WRITE CYCLE (EARLY WRITE)



PAGE MODE READ CYCLE



PAGE MODE CYCLE (EARLY WRITE)



$\overline{RAS}$ ONLY REFRESH CYCLE

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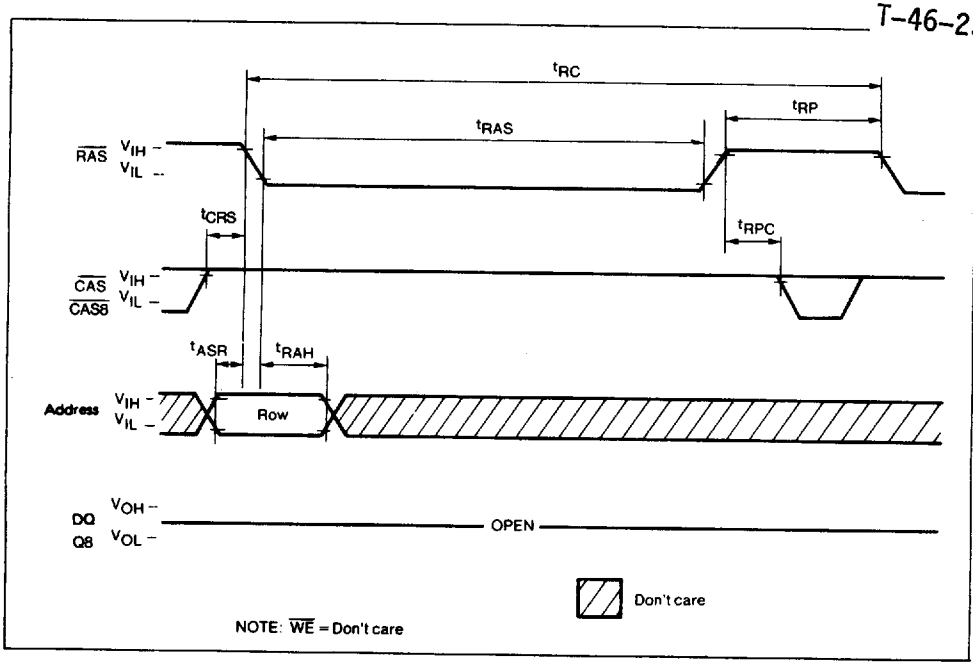
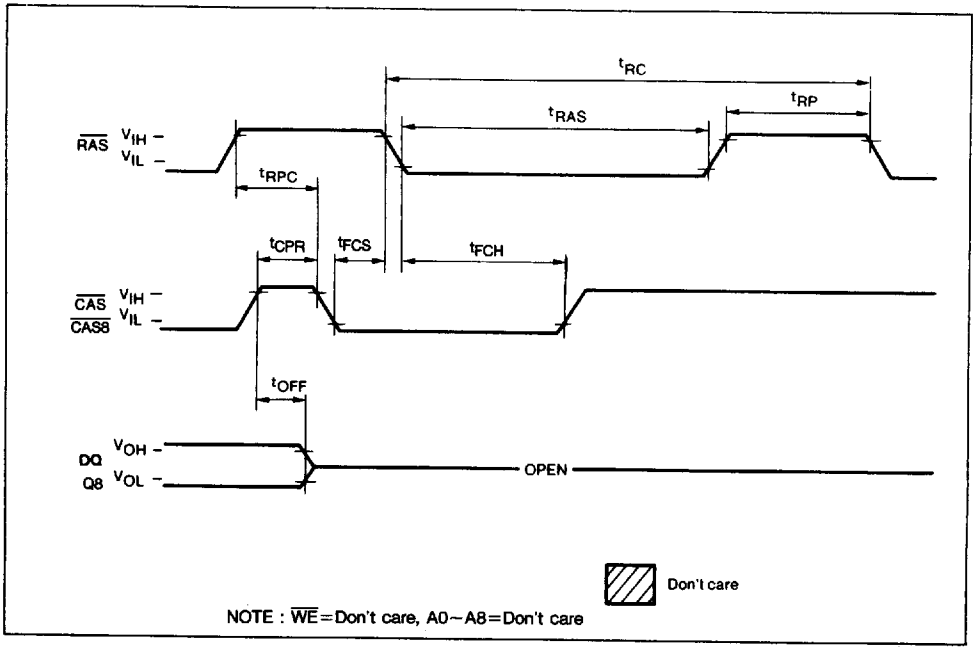


$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE