OKI semiconductor

MSC2328A-XX YS2/KS2

T-46-23-17

262,144 BY 8 BIT DYNAMIC RAM MODULE

O K I SEMICONDUCTOR GROUP

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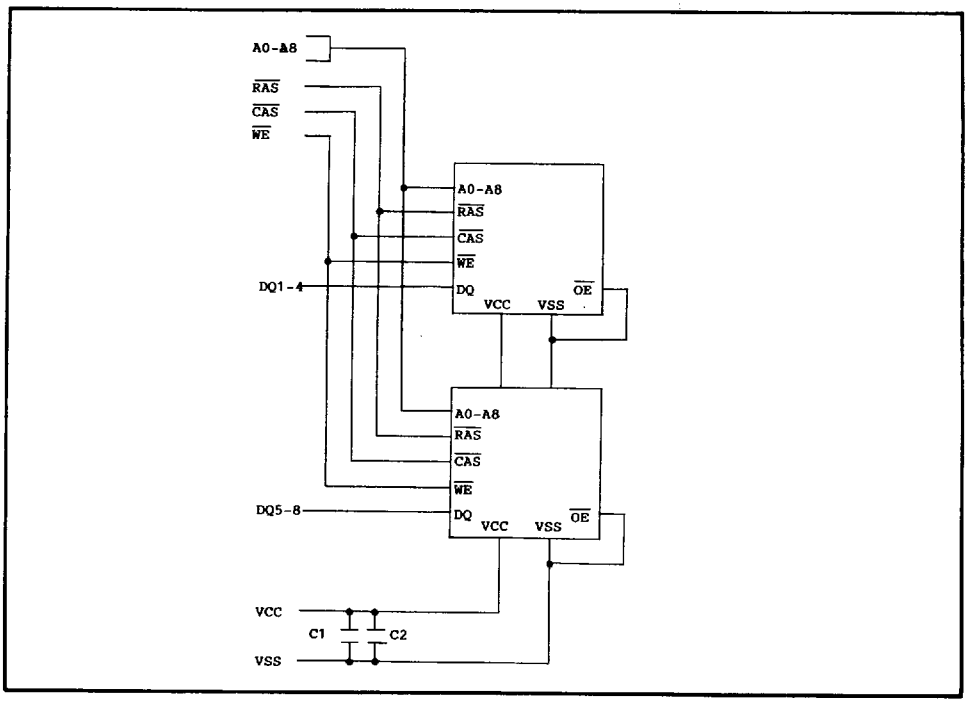
GENERAL DESCRIPTION

The Oki MSC2328A-XX YS2/KS2 is a fully decoded, 262,144 words×8 bit CMOS dynamic random access memory composed of two 1Mb DRAMs in SOJ (MSM514256AJS). The mounting of two SOJs together with two 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2328A-XX YS2/KS2are quite same as the original MSM514256A JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

- 262,144 word × 8 bit Organization
- Single =5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common $\overline{CAS}$ Control for two Common Data-In and Data-Out Lines
- Row Access Time;
  80ns max. (MSC2328A-8A/80 YS2/KS2)
  100ns max. (MSC2328A-1A/10 YS2/KS2)
- Low Power Dissipation;
  825mW max. (MSC2328A-8A/80 YS2/KS2)
  715mW max. (MSC2328A-1A/10 YS2/KS2)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT

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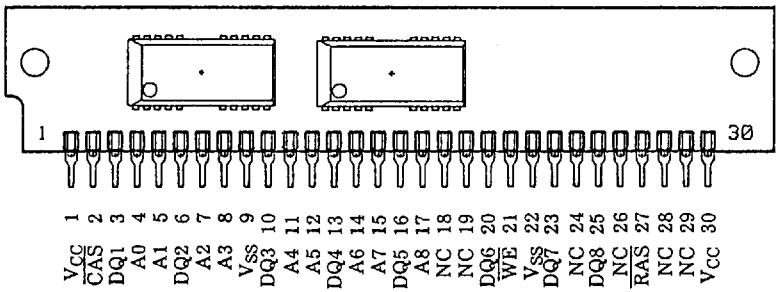

PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	NC
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	NC
9	VSS	19	NC	29	NC
10	DQ3	20	DQ6	30	V_{CC}

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ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to 150	°C
Power dissipation	P_D	2	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2328A-8AYS2/KS2		MSC2328A-1AYS2/KS2		MSC2328A-80YS2/KS2		MSC2328A-10YS2/KS2		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}	—	150	—	130	—	150	—	130	mA
Standby Current* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2} (TTL)	—	4	—	4	—	4	—	4	mA
	I_{CC2} (MOS)	—	2	—	2	—	2	—	2	mA
REfresh Current 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} =min.)	I_{CC3}	—	150	—	130	—	150	—	130	mA
Refresh Current 2* Average power supply current (CAS before RAS; t_{RC} = min)	I_{CC6}	—	150	—	130	—	150	—	130	mA
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} =min.)	I_{CC7}	—	120	—	120	—	130	—	120	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−20	20	−20	20	−20	20	−20	20	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	30	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	30	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	20	pF

Capacitance measured with Boonton Meter.

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AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2328A-8AYS2/KS2		MSC2328A-1AYS2/ KS2		MSC2328A-80YS2/KS2		MSC2328A-10YS2/KS2		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
Random read or write cycle time	t_{RC}	160	—	190	—	160	—	190	—	ns	
Fast page mode cycle time	t_{PC}	55	—	55	—	50	—	55	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	80	—	100	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	30	—	20	—	25	ns	4,5
Access time from column address	t_{AA}	—	40	—	50	—	40	—	50	ns	4,6
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	50	—	50	—	45	—	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	0	—	n_s	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100000	100	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	—	30	—	20	—	25	—	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	30	10000	20	10000	25	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	80	—	100	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	55	25	70	25	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Row address set-up time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	12	—	15	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	15	—	20	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	—	75	—	60	—	75	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	50	—	40	—	50	—	ns	

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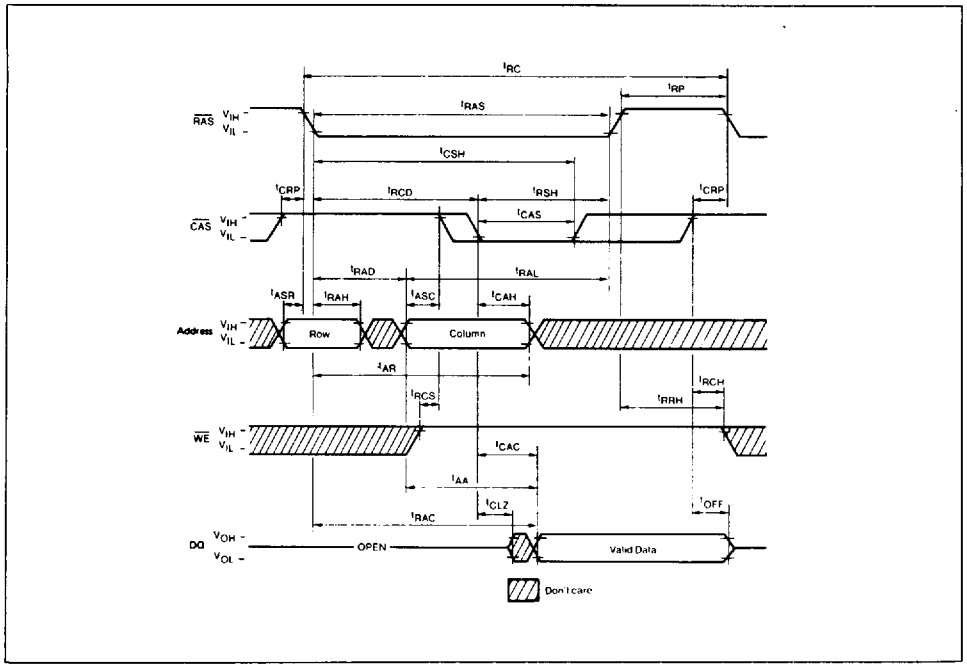
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSC2328A-8AYS2/KS2		MSC2328A--1AYS2/ KS2		MSC2328A-80YS2/KS2		MSC2328A-10YS2/KS2		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	7
Write command hold time from $\overline{RAS}$	t_{WCR}	60	—	75	—	60	—	75	—	ns	
Write command set-up time	t_{WCS}	0	—	0	—	0	—	0	—	ns	
Write command hold time	t_{WCH}	15	—	20	—	15	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	15	—	20	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	0	—	0	—	ns	
Data-in hold time	t_{DH}	15	—	20	—	15	—	20	—	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	—	75	—	60	—	75	—	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	7
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	—	30	—	30	—	30	—	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	10	—	15	—	ns	

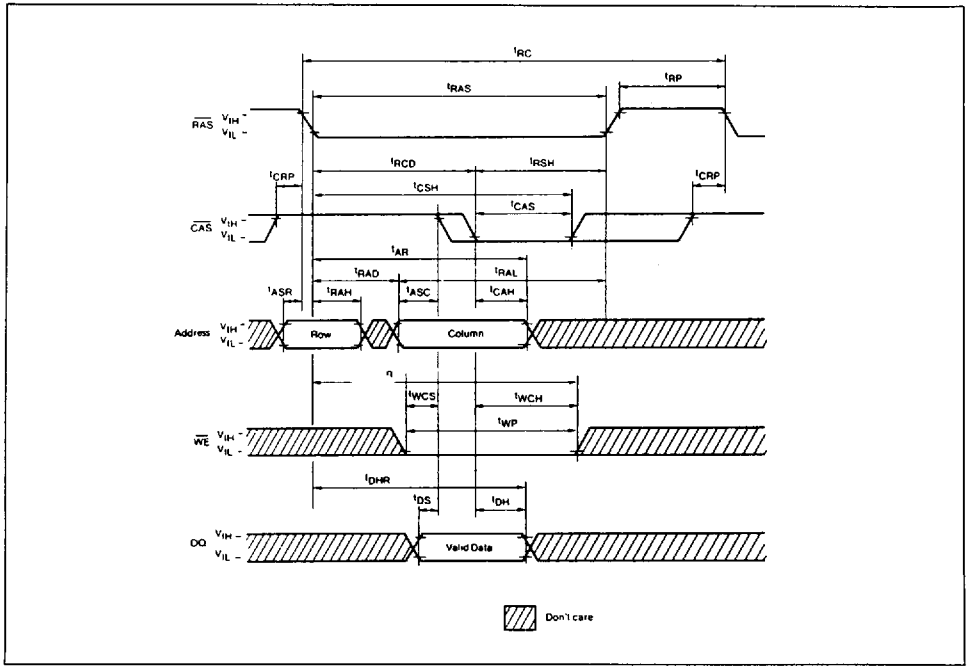
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

READ CYCLE



WRITE CYCLE(EARLY WRITE)



FAST PAGE MODE READ CYCLE

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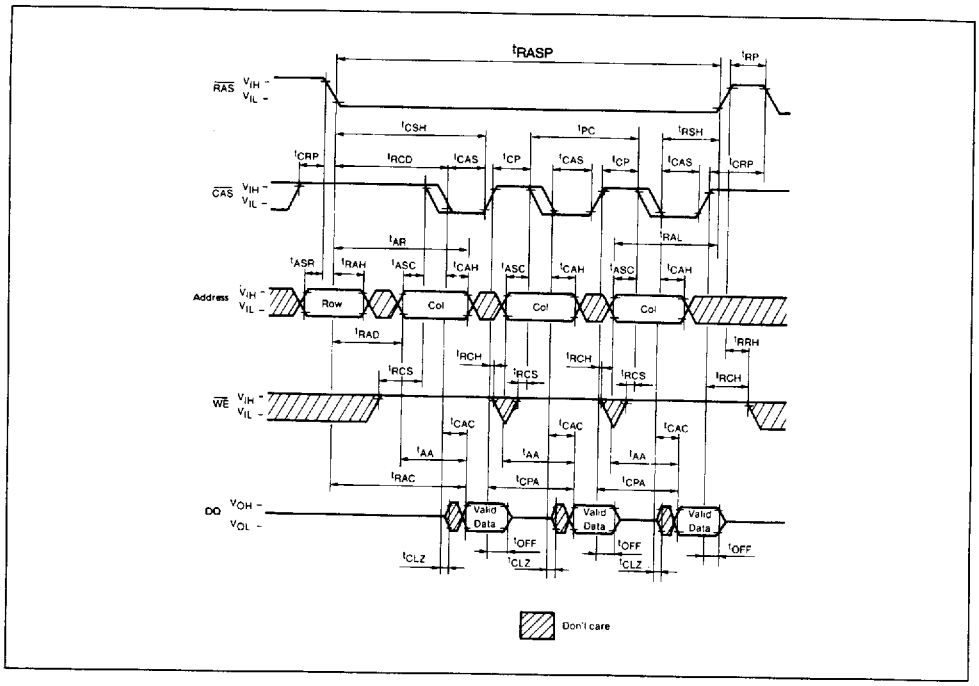
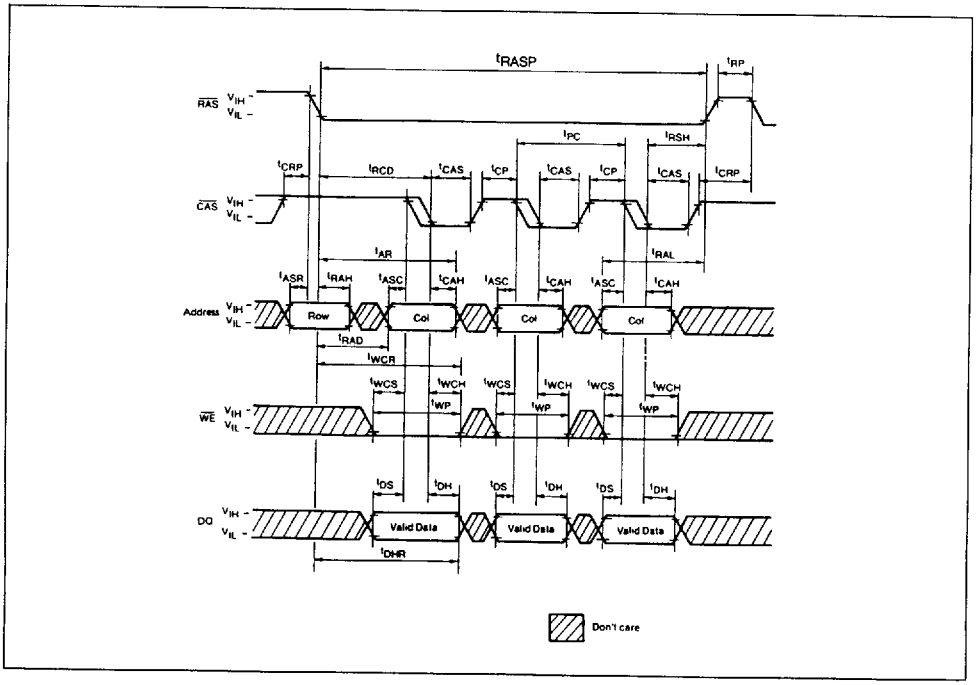
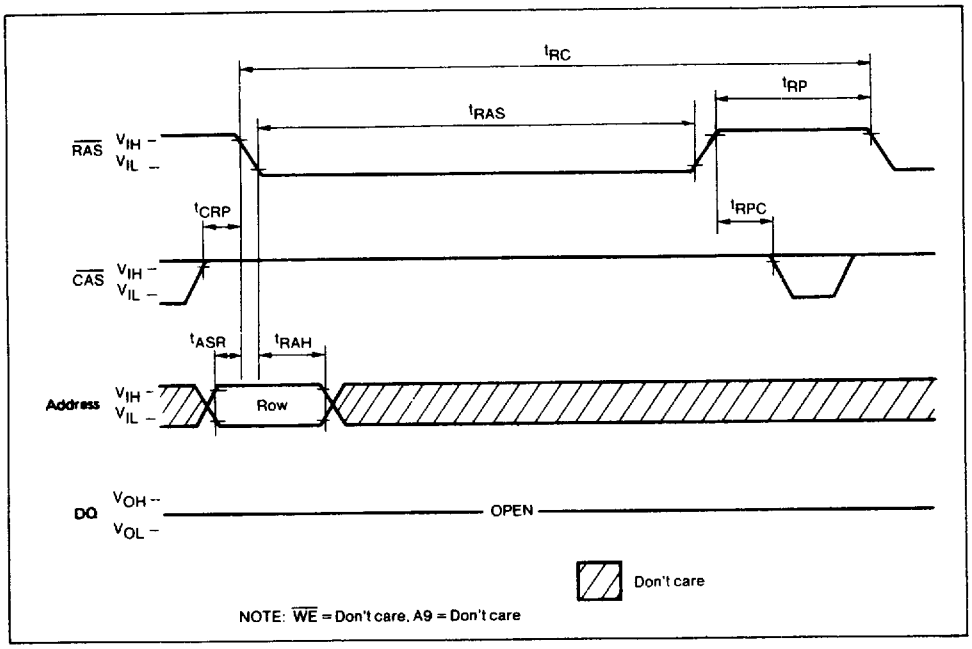


FAST PAGE MODE CYCLE (EARLY WRITE)

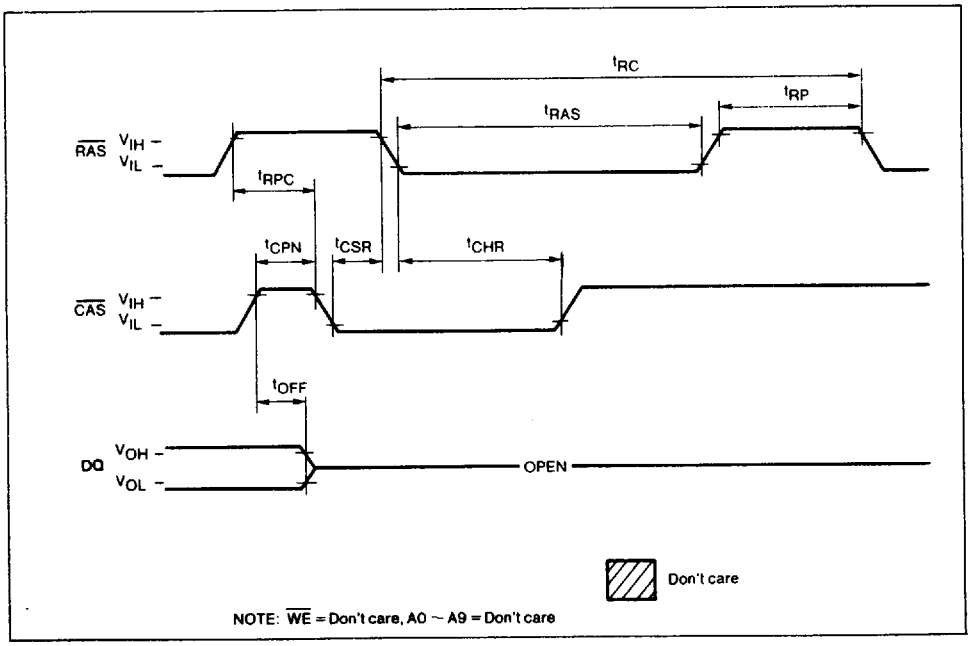


RAS ONLY REFRESH CYCLE



NOTE: $\overline{WE}$ = Don't care, A9 = Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



NOTE: $\overline{WE}$ = Don't care, A0 ~ A9 = Don't care

HIDDEN REFRESH READ CYCLE

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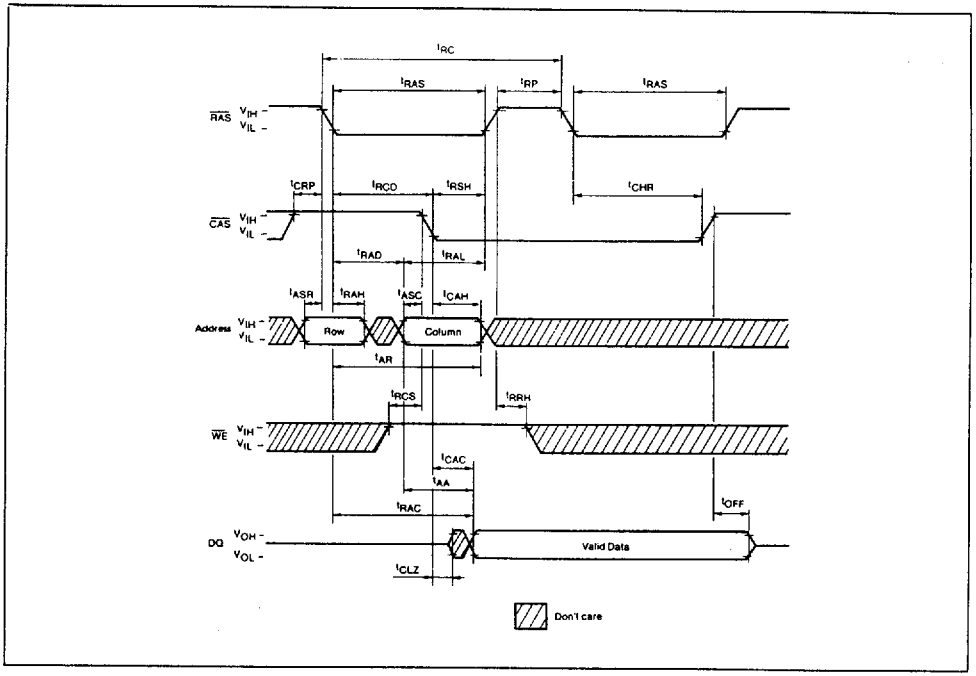
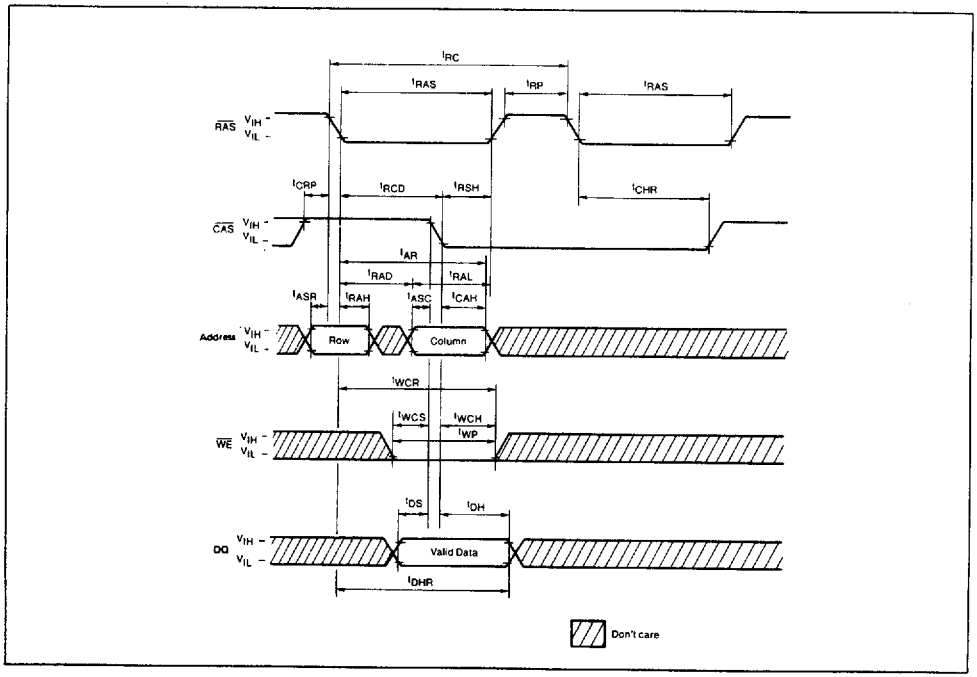


HIDDEN REFRESH WRITE CYCLE



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