OKI semiconductor

MSC2310YS9/KS9

1,048,576 BY 9 BIT DYNAMIC RAM MODULE

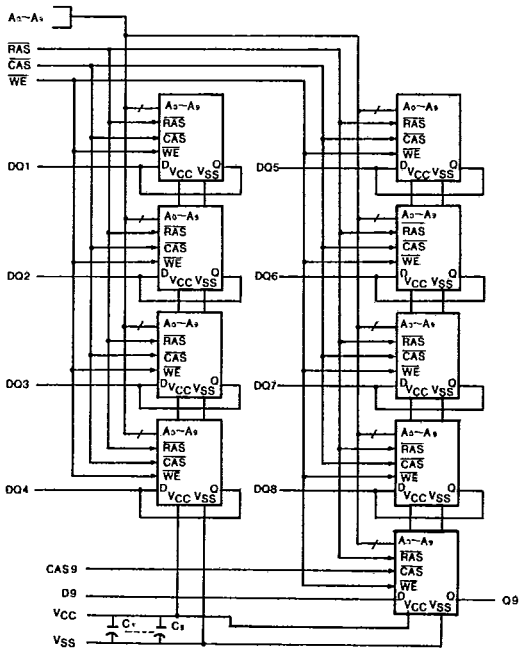
GENERAL DESCRIPTION

The Oki MSC2310YS9/KS9 is a fully decoded, 1,048,576 words × 9 bit NMOS dynamic random access memory composed of nine 1 Mb DRAMs in SOJ (MSM411000JS). The mounting of nine SOJs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2310YS9/KS9 are quite same as the original MSM411000JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

- 1,048,576 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Linens
- Access Time;
  100ns max. (MSC2310-10YS9/KS9)
  120ns max. (MSC2310-12YS9/KS9)
- Low Power Dissipation;
  3713mW max. (MSC2310-10YS9/KS9)
  3465mW max. (MSC2310-12YS9/KS9)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT

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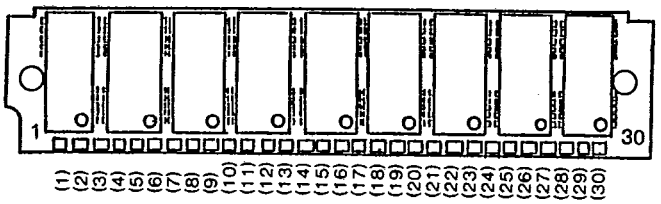
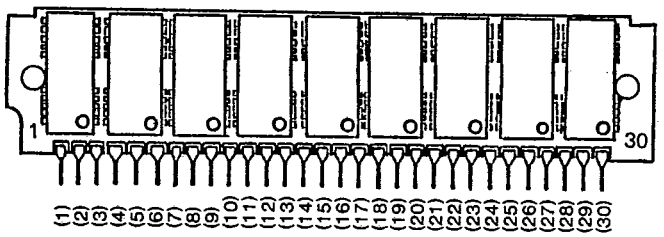
MSC2310YS9



MSC2310KS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	$\overline{CAS9}$
9	VSS	19	NC	29	D9
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	9	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2310-10YS9/KS9		MSC2310-12YS9/KS9		Unit
		Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		675		630	mA
Standby Current* Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}		45		45	mA
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} =min.)	I_{CC3}		585		540	mA
Page Mode Current* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} =min.)	I_{CC4}		495		450	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−90	90	−90	90	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

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CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_9$)	C_{IN1}	40	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	75	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{IN3}	5	10	pF
Input Capacitance (D9)	C_{IN4}	4	10	pF
Output Capacitance (Q9)	C_{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

Note 1, 2, 3 (V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	MSC2310-10YS9/KS9		MSC2310-12YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read/write cycle time	t_{RC}	200	–	230	–	ns	
Page mode cycle time	t_{PC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	5, 6
Output buffer turn-off delay	t_{OFF}	0	25	0	25	ns	
Transition time	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90	–	100	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	ns	7, 8
$\overline{CAS}$ and $\overline{RAS}$ set-up time	t_{CRS}	15	–	20	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	70	–	80	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	9
Write command hold time from $\overline{RAS}$	t_{WCR}	70	–	85	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	20	–	25	–	ns	

AC CHARACTERISTICS (CONT.) 89D 02739 D T-46-23-17

Parameter	Symbol	MSC2310-10YS9/KS9		MSC2310-12YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX		
Write command pulse width	t_{WP}	20	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40	–	40	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40	–	40	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	25	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	70	–	85	–	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	20	–	20	–	ns	9
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	ns	

Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL + 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

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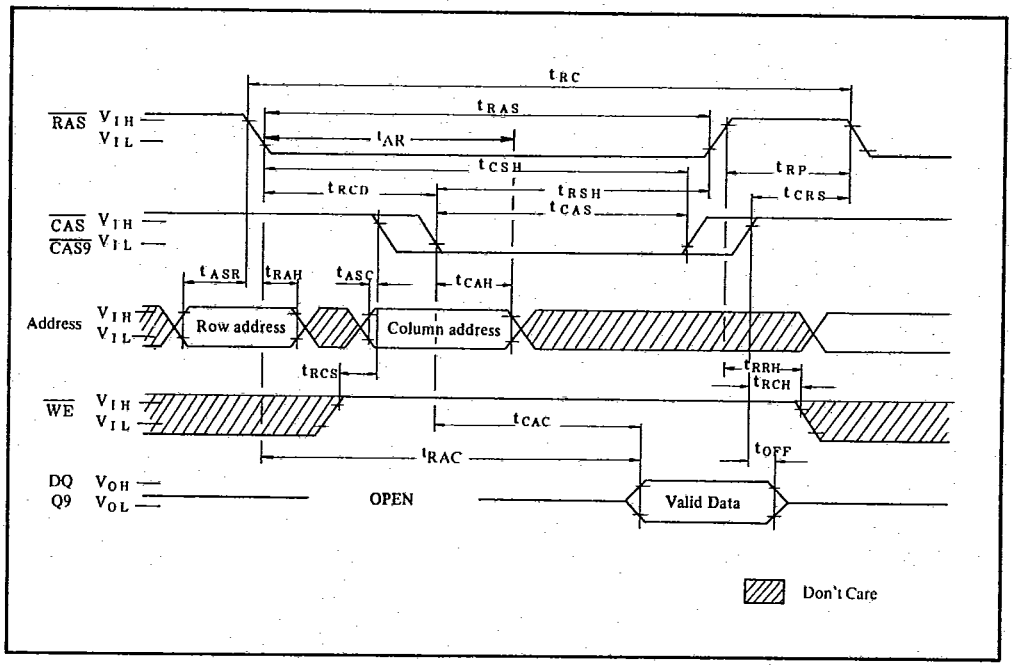
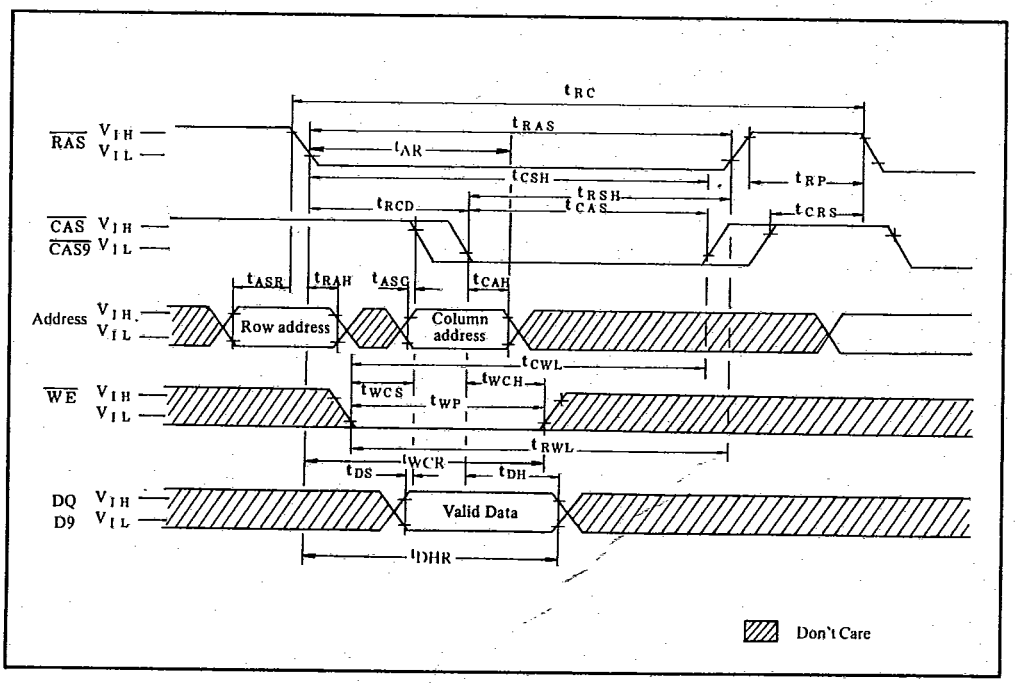
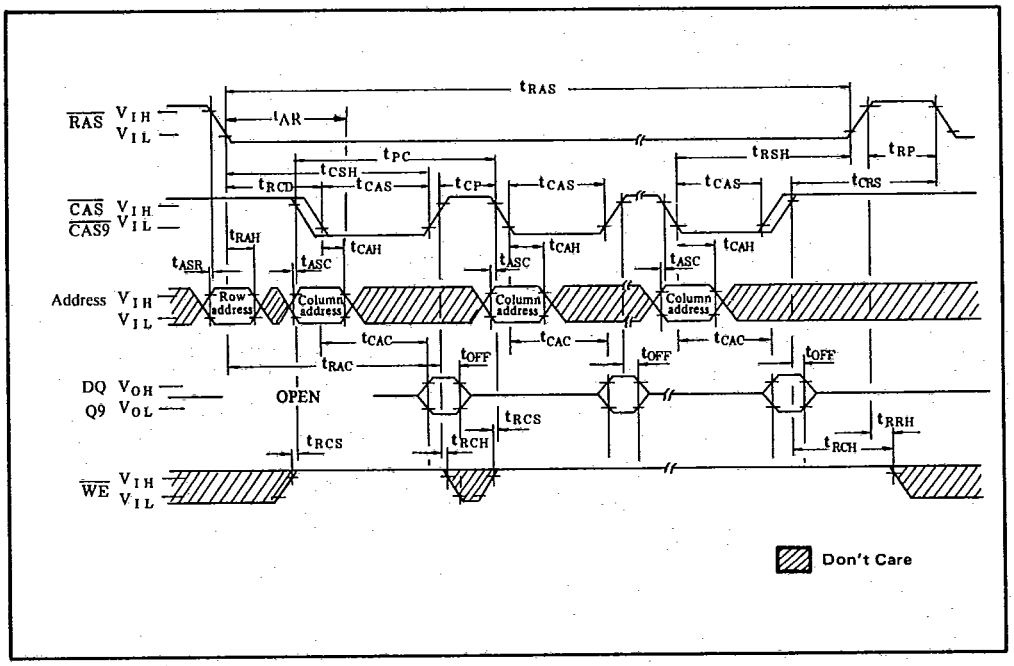
READ CYCLE



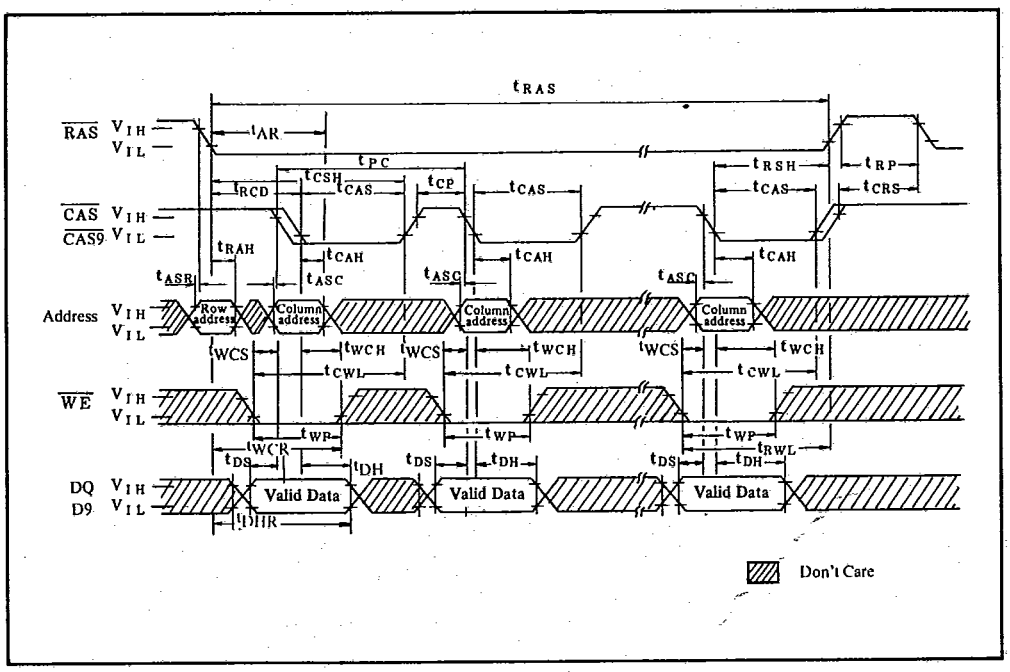
WRITE CYCLE (EARLY WRITE)



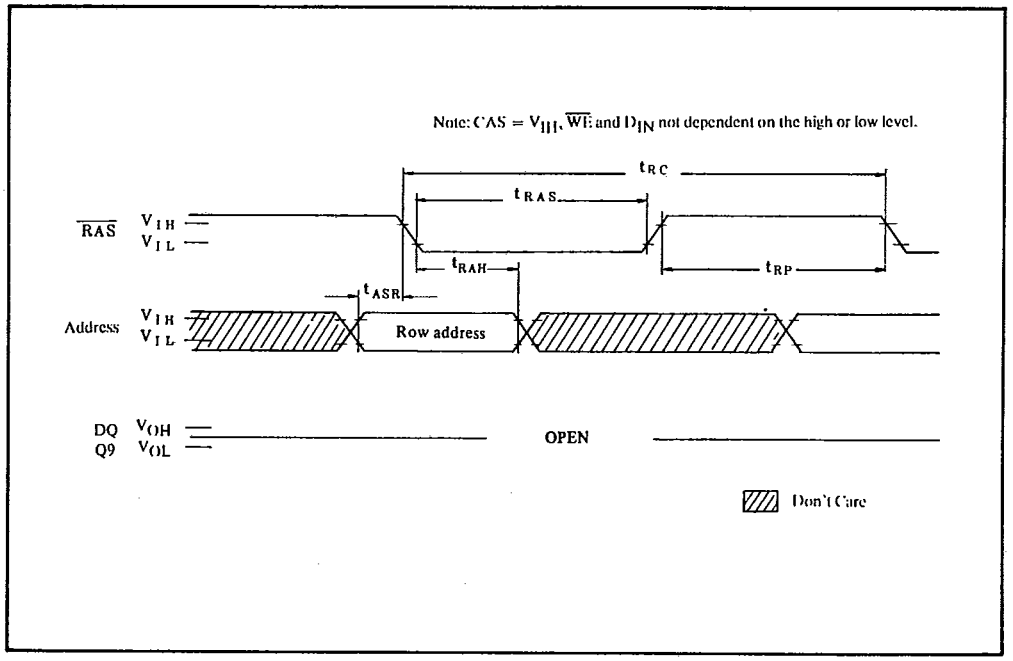
PAGE MODE READ CYCLE



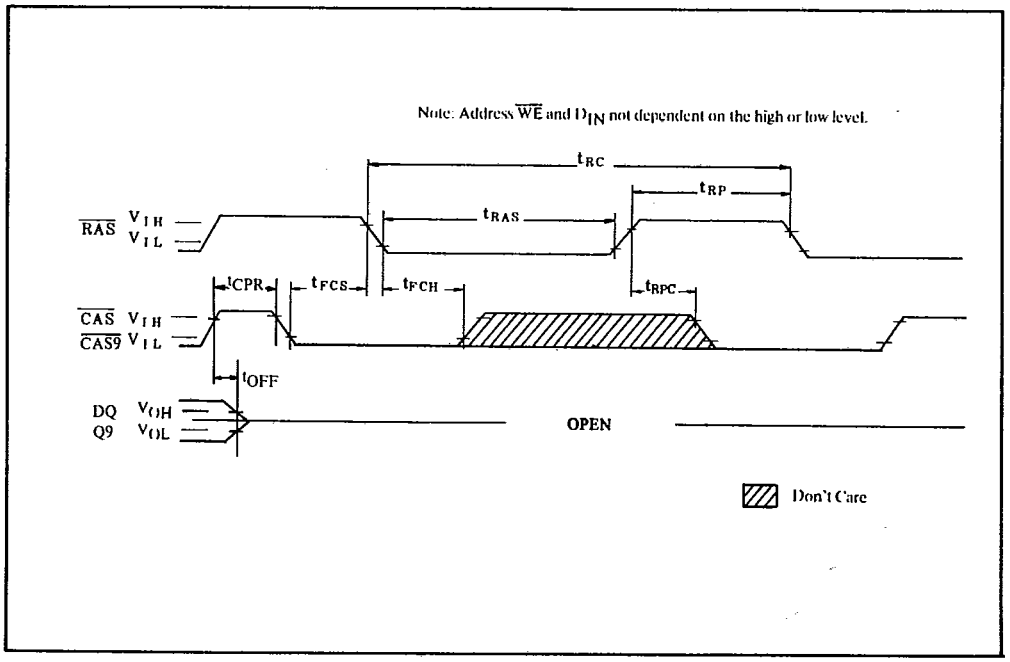
PAGE MODE WRITE CYCLE (EARLY WRITE)



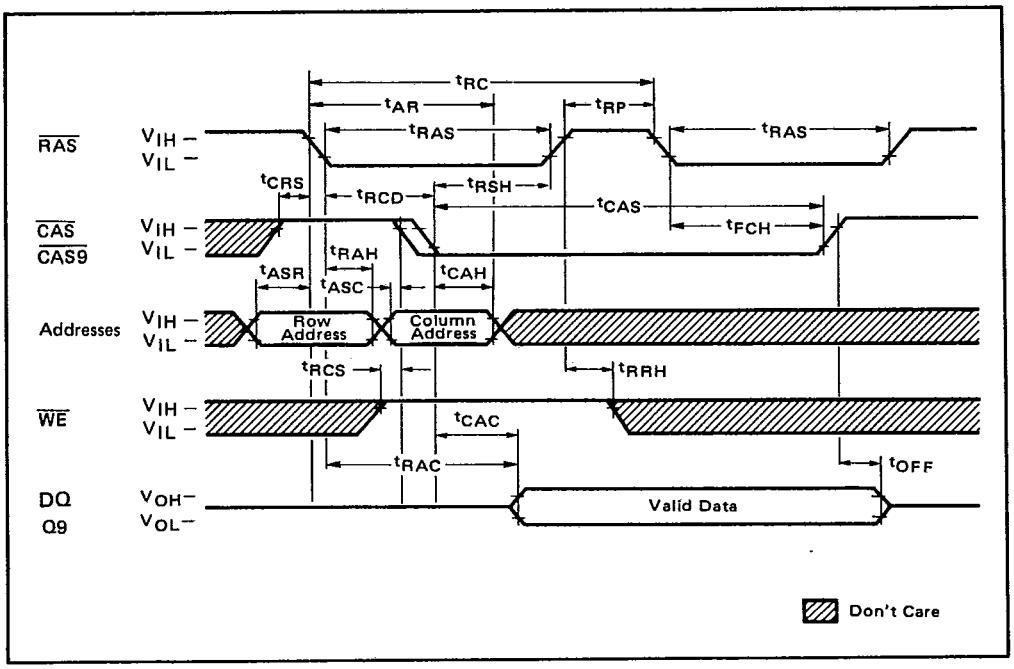
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

20 bits of binary address input are required to decode any one of the 1,048,576 words by 1 bit storage cell locations.

10 row-address bits are set up on address input pins A0 through A9 and latched onto the chip by the row address strobe ($\overline{RAS}$). Then 10 column-address bits are set up on pins A0 through A9 and latched onto the chip by the column address strobe ($\overline{CAS}$).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In a write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0 to A_8) at least every 8 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 512 (A_0 to A_8) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.