

# Quad-Channel Digital Isolators ADuM1400/ADuM1401/ADuM1402

#### **FEATURES**

Low power operation 5 V operation: 1.0 mA per channel max @ 0 Mbps to 2 Mbps 3.5 mA per channel max @ 10 Mbps 31 mA per channel max @ 100 Mbps 3 V operation: 0.7 mA per channel max @ 0 Mbps to 2 Mbps 2.1 mA per channel max @ 10 Mbps 20 mA per channel max @ 100 Mbps **Bidirectional communication** 3 V/5 V level translation High temperature operation: 105°C High data rate: dc to 100 Mbps (NRZ) Precise timing characteristics: 2 ns max pulse width distortion 2 ns max channel-to-channel matching High common-mode transient immunity: >25 kV/µs **Output enable function** Wide body 16-lead SOIC package, Pb-free models available Safety and regulatory approvals UL recognition: 2500 V rms for 1 minute per UL 1577 CSA component acceptance notice #5A VDE certificate of conformity DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01 DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000  $V_{IORM} = 560 V peak$ 

#### **APPLICATIONS**

General-purpose multichannel isolation SPI® interface/data converter isolation RS-232/422/485 transceiver Industrial fieldbus isolation

### **GENERAL DESCRIPTION**

The ADuM140x are four-channel digital isolators based on Analog Devices' *i*Coupler<sup>®</sup> technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discretes is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices run at one-tenth to one-sixth the power consumption of optocouplers at comparable signal data rates.

The ADuM140x isolators provide four independent isolation channels in a variety of channel configurations and data rates (see Ordering Guide). All ADuM140x models operate with the supply voltage of either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the ADuM140x provides low pulse width distortion (<2 ns for CRW grade), and tight channel-to-channel matching (<2 ns for CRW grade). Unlike other optocoupler alternatives, the ADuM140x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

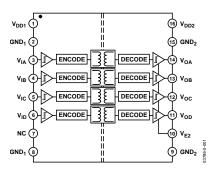


Figure 1. ADuM1400 Functional Block Diagram

#### FUNCTIONAL BLOCK DIAGRAMS

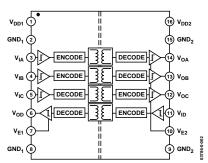


Figure 2. ADuM1401 Functional Block Diagram

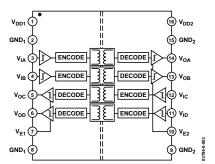


Figure 3. ADuM1402 Functional Block Diagram

#### Rev. A

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#### **REVISION HISTORY**

5/04—Data Sheet Changed from Rev. 0 to Rev. A.
Updated FormatUniversal
Changes to the Features 1
Changes to Table 7 and Table 814
Changes to Table 9 15
Changes to the DC Correctness and Magnetic Field Immunity
Section
Changes to the Power Consumption Section
Changes to the Ordering Guide

9/03—Revision 0: Initial Version.

### **SPECIFICATIONS**

### **ELECTRICAL CHARACTERISTICS—5 V OPERATION<sup>1</sup>**

 $4.5 \text{ V} \le V_{DD1} \le 5.5 \text{ V}, 4.5 \text{ V} \le V_{DD2} \le 5.5 \text{ V}; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at <math>T_A = 25^{\circ}\text{C}, V_{DD1} = V_{DD2} = 5 \text{ V}.$ 

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
DC SPECIFICATIONS			71			
Input Supply Current, per Channel, Quiescent	I <sub>DDI (Q)</sub>		0.50	0.53	mA	
Output Supply Current, per Channel, Quiescent			0.19	0.21	mA	
ADuM1400, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (Q)</sub>		2.2	2.8	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	IDD2 (Q)		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
VDD1 Supply Current	IDD1 (10)		8.6	10.6	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (10)</sub>		2.6	3.5	mA	5 MHz logic signal freq.
100 Mbps (CRW Grade Only)						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (100)</sub>		76	100	mA	50 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	IDD2 (100)		21	25	mA	50 MHz logic signal freq.
ADuM1401, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
VDD1 Supply Current	IDD1 (Q)		1.8	2.4	mA	DC to 1 MHz logic signal freq.
VDD2 Supply Current	IDD2 (Q)		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
VDD1 Supply Current	IDD1 (10)		7.1	9.0	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	IDD2 (10)		4.1	5.0	mA	5 MHz logic signal freq.
100 Mbps (CRW Grade Only)						
VDD1 Supply Current	IDD1 (100)		62	82	mA	50 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	IDD2 (100)		35	43	mA	50 MHz logic signal freq.
ADuM1402, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
VDD1 or VDD2 Supply Current	IDD1 (Q), IDD2 (Q)		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V <sub>DD1</sub> or V <sub>DD2</sub> Supply Current	IDD1 (10), IDD2 (10)		5.6	7.0	mA	5 MHz logic signal freq.
100 Mbps (CRW Grade Only)						
VDD1 or VDD2 Supply Current	IDD1 (100), IDD2 (100)		49	62	mA	50 MHz logic signal freq.
For All Models						
Input Currents	Iia, Iib, Iic, Iid, Ie1, Ie2	-10	+0.01	+10	μΑ	$ \begin{array}{l} 0 \leq V_{\text{IA}}, V_{\text{IB}}, V_{\text{IC}}, V_{\text{ID}} \leq V_{\text{DD1}} \text{ or } V_{\text{DD2}}, \\ 0 \leq V_{\text{E1}}, V_{\text{E2}} \leq V_{\text{DD1}} \text{ or } V_{\text{DD2}} \end{array} $
Logic High Input Threshold	$V_{\text{IH}}, V_{\text{EH}}$	2.0			V	
Logic Low Input Threshold	VIL, VEL			0.8	V	
Logic High Output Voltages	Vоан, Vовн,	$V_{\text{DD1},}V_{\text{DD2}}-0.1$	5.0		V	$I_{\text{Ox}} = -20 \ \mu\text{A}, \ V_{\text{Ix}} = V_{\text{IxH}}$
	Voch, Vodh	V <sub>DD1</sub> , V <sub>DD2</sub> - 0.4	4.8		V	$I_{Ox} = -4 \text{ mA}, V_{Ix} = V_{IxH}$
Logic Low Output Voltages	VOAL, VOBL,		0.0	0.1	V	$I_{Ox} = 20 \ \mu A$ , $V_{Ix} = V_{IxL}$
	Vocl, Vodl		0.04	0.1	V	$I_{Ox} = 400 \ \mu A$ , $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4 \text{ mA}, V_{Ix} = V_{IxL}$
SWITCHING SPECIFICATIONS			-			
ADuM140xARW						
Minimum Pulse Width <sup>3</sup>	PW			1000	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Maximum Data Rate <sup>4</sup>		1			Mbps	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay <sup>5</sup>	tphl, tplh	50	65	100	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> −t <sub>PHL</sub>   <sup>5</sup>	PWD			40	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels

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ParameterSymbolMinTypMaxUnitTest ConditionsPropagation Delay Skew <sup>6</sup> trax50ns $C_i = 15 pF_i$ CMOS signal levelsChannel-to-Channel Matching <sup>7</sup> traxcoo100ns $C_i = 15 pF_i$ CMOS signal levelsADUM140xBRWPW10ns $C_i = 15 pF_i$ CMOS signal levelsMinimum Pulse Width <sup>3</sup> PW10ns $C_i = 15 pF_i$ CMOS signal levelsPulse Width Distortion, [hur-trax] <sup>2</sup> trui, trui203250ns $C_i = 15 pF_i$ CMOS signal levelsPulse Width Distortion, [hur-trax] <sup>2</sup> trui, trui203ns $C_i = 15 pF_i$ CMOS signal levelsChange versus Temperaturetrax15ns $C_i = 15 pF_i$ CMOS signal levelsPropagation Delay Skew <sup>6</sup> traxtrax15ns $C_i = 15 pF_i$ CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels <sup>7</sup> trax6ns $C_i = 15 pF_i$ CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels <sup>7</sup> true, trui182732ns $C_i = 15 pF_i$ CMOS signal levelsPulse Width Distortion, [hur-trax] <sup>2</sup> true, trui182732ns $C_i = 15 pF_i$ CMOS signal levelsPulse Width Distortion, [hur-trax] <sup>2</sup> true, trui182732ns $C_i = 15 pF_i$ CMOS signal levelsChange versus Temperaturetrue, trui182732ns $C_i = 15 pF_i$ CMOS signal levelsPropagation Delay'true, trui18 <t< th=""><th></th><th>1</th><th></th><th></th><th></th><th>1</th><th></th></t<>		1				1	
Channel-to-Channel Matching?trace.com50ns $C_{L} = 15 \text{ pF}, CMOS signal levelsADUM140x8RWPW10nsC_{L} = 15 \text{ pF}, CMOS signal levelsMaximum Data Rate410nsC_{L} = 15 \text{ pF}, CMOS signal levelsPropagation Delay2totu, teu203250nsC_{L} = 15 \text{ pF}, CMOS signal levelsPulse Width Distortion, [Bur-thet]3PWD5ps/CC_{L} = 15 \text{ pF}, CMOS signal levelssignal levelsChange versus Temperaturetrsk15nsC_{L} = 15 \text{ pF}, CMOS signal levelssignal levelsPropagation Delay Skew4trsk15nsC_{L} = 15 \text{ pF}, CMOS signal levelsChannel-to-Channel Matching, Opposing-Directional Channels7trsk10nsC_{L} = 15 \text{ pF}, CMOS signal levelsADUM140xCRWPW6.710nsC_{L} = 15 \text{ pF}, CMOS signal levelsADuM140xCRWPW6.710nsC_{L} = 15 \text{ pF}, CMOS signal levelsPropagation Delay3Evelt100150MbpsC_{L} = 15 \text{ pF}, CMOS signal levelsPulse Width Distortion, [bur-thet]3PWD0.52nsC_{L} = 15 \text{ pF}, CMOS signal levelsPropagation Delay3Evelt100150msS_{L} = 15 \text{ pF}, CMOS signal levelsPropagation Delay3Evelt100nsC_{L} = 15 \text{ pF}, CMOS signal levelsPropagation Delay3Evelt100nsC_{L} = 15 \text{ pF}, CMOS signal levelsPropagation Delay3Evelt100ns$	Parameter	Symbol	Min	Тур	Мах	Unit	Test Conditions
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Minimum Pulse Width <sup>3</sup> Maximum Data Rate <sup>4</sup> PW100ns Mbps $C_{L} = 15 pF, CMOS signal levelsC_ = 15 pF, CMOS signal levelsPropagation Delay5Pulse Width Distortion, [t111-t114]5PWDPWD3nsC_ = 15 pF, CMOS signal levelsChange versus TemperaturePropagation Delay Skew6Channel-to-Channel Matching, Co-Directional Channels7trsk15nsC_ = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Co-Directional Channels7trsk10nsC_ = 15 pF, CMOS signal levelsADuM140xCRWMinimum Pulse Width3Propagation Delay8Channel-to-Channel Matching, Opposing-Directional Channels7PW6.710nsC_ = 15 pF, CMOS signal levelsPulse Width Distortion, [t111-t114]8Pulse Width Distortion, [t111-t114]8PW6.710nsC_ = 15 pF, CMOS signal levelsPropagation Delay8Channel-to-Channel Matching, Co-Directional Channels7trsk, trutPWD182.732nsC_ = 15 pF, CMOS signal levelsPulse Width Distortion, [t111-t114]8PWDPWD0.52nsC_ = 15 pF, CMOS signal levelsPropagation Delay8Channel-to-Channel Matching, Co-Directional Channels7trsk10nsC_ = 15 pF, CMOS signal levelsPropagation Delay8(High/Low-to-High Impedance)trsk10nsC_ = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Co-Directional Channels7trsk10nsC_ = 15 pF, CMOS signal levelsOutput Disable Propagation Delay(High/Invedance to High/Low)trsk$	Channel-to-Channel Matching <sup>7</sup>	t <sub>PSKCD/OD</sub>			50	ns	$C_{L} = 15 \text{ pF}$ , CMOS signal levels
Maximum Data Rate410Mbps $C_{i} = 15 pF, CMOS signal levelsPropagation Delay5true, true203250nsC_{i} = 15 pF, CMOS signal levelsPulse Width Distortion, [tuu-true]5PWD3nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay Skew4trsx15nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay Skew4trsx15nsC_{i} = 15 pF, CMOS signal levelsChannel+to-Channel Matching, Opposing-Directional Channels7trsx3nsC_{i} = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing-Directional Channels7trsx6nsC_{i} = 15 pF, CMOS signal levelsADUM 140xCRWtrsx100150MbpsC_{i} = 15 pF, CMOS signal levelsMaximum Data Rate4trsx100150MbpsC_{i} = 15 pF, CMOS signal levelsPropagation Delay6trsutruetrsx10nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay6trsx100150MbpsC_{i} = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Co-Directional Channels7trsx10nsC_{i} = 15 pF, CMOS signal levelsPropagation Delay Skew6trsx100nsC_{i} = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Oposing-Directional Channels7trsx10nsC_{i} = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Oposing-Directional Channels7trsx5nsC_{i} = 15 pF, CMOS signal levels$	ADuM140xBRW						
Propagation Delays $t_{HL}, t_{PLH}$ 203250ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Pulse Width Distortion, $ t_{HL}-t_{PLH} ^{5}$ PWD3ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Change versus Temperaturetrsk5ps/°C $c_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Propagation Delay Skew <sup>6</sup> trsktsk3ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Directional Channels'tsktsk3ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Directional Channels'tsktsk6ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ ADUM140xCRWtsk100150mbps $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Minimum Data Rate <sup>6</sup> tws.100150Mbps $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Propagation Delay'tws.100150mbps $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Pulse Width Distortion, $ t_{PL-t_{PH} ^{5}$ PWD0.52ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Propagation Delay'stsktsk10ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Propagation Delay Skew <sup>6</sup> tsktsk10ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Channel-to-Channel Matching, Co-tsk10ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Directional Channels'tsktsk2ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Output Disable Propagation Delaytsktsk<	Minimum Pulse Width <sup>3</sup>	PW			100	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Pulse Width Distortion, $ t_{PV-trant,I} ^3$ PWD3nsC <sub>i</sub> = 15 pF, CMOS signal levelsChange versus Temperaturetrack5ps/°CC <sub>i</sub> = 15 pF, CMOS signal levelsPropagation Delay Skew <sup>6</sup> track15nsC <sub>i</sub> = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Co- Directional Channels'track6nsC <sub>i</sub> = 15 pF, CMOS signal levelsADuM140xCRWFrom Data Rate*100150MbpsC <sub>i</sub> = 15 pF, CMOS signal levelsMaximum Data Rate*100150MbpsC <sub>i</sub> = 15 pF, CMOS signal levelsPropagation Delay5trant, trant182732nsC <sub>i</sub> = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{PV-trant]^3}$ PWD0.52nsC <sub>i</sub> = 15 pF, CMOS signal levelsPulse Width Distortion, $ t_{PV-trant]^3}$ PWD0.52nsC <sub>i</sub> = 15 pF, CMOS signal levelsPropagation Delay5trant, trant182732nsC <sub>i</sub> = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Co- Directional Channels7trask0nsC <sub>i</sub> = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7trask2nsC <sub>i</sub> = 15 pF, CMOS signal levelsOutput Disable Propagation Delay (High/Low+to-High Impedance)tratk, trask68nsC <sub>i</sub> = 15 pF, CMOS signal levelsOutput Disable Propagation Delay (High/Low+to-High Impedance)tratk, trask2nsC <sub>i</sub> = 15 pF, CMOS signal levelsOutput Disable Propagation	Maximum Data Rate <sup>4</sup>		10			Mbps	$C_L = 15 \text{ pF}$ , CMOS signal levels
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Propagation Delay <sup>5</sup>	tphl, tplh	20	32	50	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay Skew <sup>6</sup> tesk15ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Channel-to-Channel Matching, Co- Directional Channels'teskco3ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Channel-to-Channel Matching, Opposing- Directional Channels'teskco6ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ ADUM140xCRWfsico100150ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Minimum Data Rate <sup>6</sup> 100150MbpsC_{L} = 15 \text{ pF}, CMOS \text{ signal levels}Propagation Delay <sup>5</sup> tesk, tesk100150nsC_{L} = 15 \text{ pF}, CMOS \text{ signal levels}Pulse Width Distortion, [touthet] <sup>5</sup> PWD0.52nsC_{L} = 15 \text{ pF}, CMOS \text{ signal levels}Propagation Delay <sup>5</sup> tesk, teskco2nsC_{L} = 15 \text{ pF}, CMOS \text{ signal levels}Propagation Delay Skew <sup>6</sup> tesk10nsC_{L} = 15 \text{ pF}, CMOS \text{ signal levels}Channel-to-Channel Matching, Co- Directional Channels'teskco2nsC_{L} = 15 \text{ pF}, CMOS \text{ signal levels}Channel-to-Channel Matching, Opposing- Directional Channels'teskco5nsC_{L} = 15 \text{ pF}, CMOS \text{ signal levels}Output Disable Propagation Delay (High Inpedance)tesk, tesk2.5nsC_{L} = 15 \text{ pF}, CMOS signal levelsOutput Rise/Fall Time (10% to 90%) Common-Mode Transient Immunity at Logic High Output*tesk2.5nsC_L = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output*[CML]2.5	Pulse Width Distortion,  t <sub>PLH</sub> -t <sub>PHL</sub>   <sup>5</sup>	PWD			3	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Change versus Temperature			5		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Directional Channels7 Channel-to-Channel Matching, Opposing- Directional Channels7 $t_{FSKOD}$ $t_{FSKOD}$ $c_{R}$ $n_{S}$ $C_{L} = 15 \text{ pF}$ , CMOS signal levelsMaximum Data Rate4 Propagation Delay5PW $6.7$ 10ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsPulse Width Distortion, $ t_{DU}-t_{FHL} ^{S}$ $t_{FHL}$ , $t_{ELH}$ 182732ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsPulse Width Distortion, $ t_{DU}-t_{FHL} ^{S}$ $t_{FHL}$ , $t_{ELH}$ 182732ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsPulse Width Distortion, $ t_{DU}-t_{FHL} ^{S}$ $t_{FHL}$ , $t_{ELH}$ 182732ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsChange versus Temperature Propagation Delay Skew <sup>4</sup> $t_{FSK}$ 10ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsChannel-to-Channel Matching, Co- Directional Channels7 $t_{FSKOD}$ $t_{FSKOD}$ $s_{SKOD}$ $s_{SKOD}$ $s_{SKOD}$ Output Disable Propagation Delay (High/Low-to-High Impedance) $t_{H2R}$ , $t_{FLH}$ $6$ $8$ ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsOutput Rise/Fall Time (10% to 90%) Common-Mode Transient Immunity at Logic Low Output <sup>4</sup> $t_{H2R}$ , $t_{FL}$ $6$ $8$ ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output <sup>4</sup> $t_{H2R}$ , $t_{FLH}$ $6$ $8$ ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output <sup>4</sup> $t_{H2R}$ , $t_{FLH}$ $6$ $8$ ns $C_{L} = 15 \text{ pF}$ ,	Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			15	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Directional Channels?Directional Channels?PW6.710ns $C_L = 15 \text{ pF}, CMOS \text{ signal levels}ADuM140xCRWMinimum Pulse Width3PW6.7100150MbpsC_L = 15 \text{ pF}, CMOS \text{ signal levels}Maximum Data Rate4100150MbpsC_L = 15 \text{ pF}, CMOS \text{ signal levels}100Propagation Delay5tertu, trut182732nsC_L = 15 \text{ pF}, CMOS \text{ signal levels}Pulse Width Distortion, [trut-tert]5PWD0.52nsC_L = 15 \text{ pF}, CMOS \text{ signal levels}Change versus TemperaturePWD0.52nsC_L = 15 \text{ pF}, CMOS \text{ signal levels}Propagation Delay Skew6tesk100nsC_L = 15 \text{ pF}, CMOS \text{ signal levels}Channel-to-Channel Matching, Co-teskc2nsC_L = 15 \text{ pF}, CMOS \text{ signal levels}Directional Channels7teskcD5nsC_L = 15 \text{ pF}, CMOS \text{ signal levels}Portput Disable Propagation Delaytertz, trut68nsC_L = 15 \text{ pF}, CMOS \text{ signal levels}Output Disable Propagation Delaytertz, trut68nsC_L = 15 \text{ pF}, CMOS \text{ signal levels}Output Bise/Fall Time (10% to 90%)ta/tr2.5nsC_L = 15 \text{ pF}, CMOS \text{ signal levels}Common-Mode Transient Immunity at Logic[CMi]2535kV/µsV_{ix} = V_{ix}, V_{ixy} = 1000 V,High Output8fr1.2MbpsNbpsNc = 0.0, V_{ixy} = 1000 V,Common-Mode Transient Immuni$		<b>t</b> pskcd			3	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Minimum Pulse Width3 Maximum Data Rate4PW6.710nsCL = 15 pF, CMOS signal levels CL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7tPskcD2nsCL = 15 pF, CMOS signal levelsFor All ModelstPskcDtPskcD5nsCL = 15 pF, CMOS signal levelsOutput Disable Propagation Delay (High/Low-to-High Impedance)tPskt, tPzL68nsCL = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%) Low Output8tr/tr2.5nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output8[CML]2535kV/µsV <sub>in</sub> = V <sub>DDI</sub> /V <sub>DDZ</sub> , V <sub>GM</sub> = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channel9fr1.2MbpsMbpsMaximum PAMbps		t <sub>PSKOD</sub>			6	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Maximum Data Rate4100150Mbps $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Propagation Delay5tPHL, tPLH182732ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Pulse Width Distortion,  tPLH-tPHL]5PWD0.52ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Change versus TemperaturePWD0.52ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Propagation Delay Skew6trsk10ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Channel-to-Channel Matching, Co-trskcD2ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Directional Channels7trskcD5ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ For All Models0utput Disable Propagation Delay (High/Low-to-High Impedance)trskcD5ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Output Rise/Fall Time (10% to 90%) Common-Mode Transient Immunity at Logic Low Output <sup>8</sup> tr/tr2.5ns $C_{L} = 15 \text{ pF}, CMOS \text{ signal levels}$ Common-Mode Transient Immunity at Logic Low Output <sup>8</sup> fr,2535kV/µs $V_{hx} = V_{DDI}/D_{D2}, V_{CM} = 1000 V,$ transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channel <sup>9</sup> fr,1.2MbpsNsV_{L} = 0V, V_{CM} = 1000 V, transient magnitude = 800 V	ADuM140xCRW						
Propagation Delays $t_{PHL}$ , $t_{PLH}$ 182732ns $C_L = 15 \text{ pF}$ , CMOS signal levelsPulse Width Distortion, $ t_{PLH-t_{PHL}} ^5$ PWD0.52ns $C_L = 15 \text{ pF}$ , CMOS signal levelsChange versus Temperature3ps/°C $C_L = 15 \text{ pF}$ , CMOS signal levels $C_L = 15 \text{ pF}$ , CMOS signal levelsPropagation Delay Skew <sup>6</sup> tpsk10ns $C_L = 15 \text{ pF}$ , CMOS signal levelsChannel-to-Channel Matching, Co- Directional Channels7tpskCD2ns $C_L = 15 \text{ pF}$ , CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7tpskCD5ns $C_L = 15 \text{ pF}$ , CMOS signal levelsFor All ModelstpskcDtpskcD5ns $C_L = 15 \text{ pF}$ , CMOS signal levelsOutput Disable Propagation Delay (High Impedance)tpstz, tpzL68ns $C_L = 15 \text{ pF}$ , CMOS signal levelsOutput Rise/Fall Time (10% to 90%)tp/tz, tpzL68ns $C_L = 15 \text{ pF}$ , CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output <sup>8</sup> [CML]2535kV/µs $V_{Ix} = V_{DDI}/V_{DDZ}, V_{CM} = 1000 V, transienttransient magnitude = 800 VRefresh RateInput Dynamic Supply Current, per Channel9fr1.2MbpsMps$	Minimum Pulse Width <sup>3</sup>	PW		6.7	10	ns	C∟ = 15 pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH-tPH_{i}} ^{5}$ PWD0.52ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsChange versus Temperature310ns $C_{L} = 15 \text{ pF}$ , CMOS signal levels $C_{L} = 15 \text{ pF}$ , CMOS signal levelsPropagation Delay Skew <sup>6</sup> t <sub>PSK</sub> 10ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsChannel-to-Channel Matching, Co- Directional Channels7t <sub>PSKD</sub> 2ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7t <sub>PSKD</sub> 5ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsFor All Modelst <sub>PHZ</sub> , t <sub>PLH</sub> 68ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsOutput Disable Propagation Delay (High/Low-to-High Impedance)t <sub>PHZ</sub> , t <sub>PLH</sub> 68ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsOutput Rise/Fall Time (10% to 90%)t <sub>R</sub> /tr2.5ns $C_{L} = 15 \text{ pF}$ , CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output <sup>8</sup> [CM <sub>H</sub> ]2535kV/µs $V_{Ix} = 0 \text{ V}, V_{CM} = 1000 \text{ V},$ transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channel <sup>9</sup> fr1.2MbpsMbps	Maximum Data Rate⁴		100	150		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Change versus Temperature3 $ps/°C$ $C_L = 15 pF, CMOS signal levelsPropagation Delay Skew6t_{PSK}10nsC_L = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Co-Directional Channels7t_{PSKCD}2nsC_L = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing-Directional Channels7t_{PSKCD}5nsC_L = 15 pF, CMOS signal levelsFor All Modelst_{PHZ}, t_{PLH}68nsC_L = 15 pF, CMOS signal levelsOutput Disable Propagation Delay(High/Low-to-High Impedance)t_{PHZ}, t_{PLH}68nsC_L = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%)High Output6t_{R}/t_F2.5nsC_L = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at LogicLow Output8[CM_H]2535kV/\mu sV_{Ix} = 0 V, V_{CM} = 1000 V,Common-Mode Transient Immunity at LogicLow Output8f_r1.2MbpsV_{Ix} = 0 V, V_{CM} = 1000 V,Refresh RateInput Dynamic Supply Current, per Channel9I_{DD(D)}0.19mA/MbpsV_{Ix} = 0 V, V_{CM} = 1000 V,$	Propagation Delay <sup>5</sup>	tphl, tplh	18	27	32	ns	$C_{L} = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay Skew6trsk10nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Co- Directional Channels7trskcD2nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7trskoD5nsCL = 15 pF, CMOS signal levelsFor All ModelsOutput Disable Propagation Delay (High/Low-to-High Impedance)tretz, tPLH68nsCL = 15 pF, CMOS signal levelsOutput Bise/Fall Time (10% to 90%)tretzH, tPzL68nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output8[CMH]2535nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output8[CML]2535kV/µsVix = V_DDI/VDD2, VCM = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channel9fr1.2MbpsMpsNot Dutput Supply Current, per Channel9IpDI(D)0.19mA/MbpsNs	Pulse Width Distortion,  t <sub>PLH</sub> -t <sub>PHL</sub>   <sup>5</sup>	PWD		0.5	2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Co- Directional Channels?teskcD2nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels?teskoD5nsCL = 15 pF, CMOS signal levelsFor All Models0utput Disable Propagation Delay (High/Low-to-High Impedance)teskoD5nsCL = 15 pF, CMOS signal levelsOutput Enable Propagation Delay (High Impedance to High/Low)tesk, tesk68nsCL = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%) High Outputtrk/tr2.5nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output[CML]2535kV/µsVix = VpDi/VDD2, VcM = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channelfr1.2MbpsMbps	Change versus Temperature			3		ps/°C	$C_{L} = 15 \text{ pF}$ , CMOS signal levels
Directional Channels7trescop5nsCL = 15 pF, CMOS signal levelsChannel-to-Channel Matching, Opposing- Directional Channels7trescop5nsCL = 15 pF, CMOS signal levelsFor All ModelsOutput Disable Propagation Delay (High/Low-to-High Impedance)trescop68nsCL = 15 pF, CMOS signal levelsOutput Enable Propagation Delay (High Impedance to High/Low)trescop68nsCL = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%) High Output <sup>8</sup> tre/trescop2.5nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output <sup>8</sup> [CML]2535kV/µsVix = V_DD1/VDD2, VCM = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channel <sup>9</sup> fr1.2MbpsMbps	Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			10	ns	$C_{L} = 15 \text{ pF}$ , CMOS signal levels
Directional Channels7Directional Channels7Directional Channels7For All ModelsOutput Disable Propagation Delay (High/Low-to-High Impedance)tPHZ, tPLH68nsCL = 15 pF, CMOS signal levelsOutput Enable Propagation Delay (High Impedance to High/Low)tPZH, tPZL68nsCL = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%) (High Output 8tR/tF2.5nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic Low Output8[CMH]2535kV/µsVIx = V_DDI,V_DD2, V_CM = 1000 V, transient magnitude = 800 VCommon-Mode Transient Immunity at Logic Low Output8[CML]2535kV/µsVIx = 0 V, V_CM = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channel9fr1.2MbpsMbps		t <sub>PSKCD</sub>			2	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Output Disable Propagation Delay (High/Low-to-High Impedance)t_{PHZ}, t_{PLH}68nsCL = 15 pF, CMOS signal levelsOutput Enable Propagation Delay (High Impedance to High/Low)t_{PZH, t_PZL}68nsCL = 15 pF, CMOS signal levelsOutput Rise/Fall Time (10% to 90%)t_R/t_F2.5nsCL = 15 pF, CMOS signal levelsCommon-Mode Transient Immunity at Logic High Output <sup>8</sup> I/CMH2535kV/µsVIx = V_DD1/V_DD2, V_CM = 1000 V, transient magnitude = 800 VCommon-Mode Transient Immunity at Logic Low Output <sup>8</sup> I/CML2535kV/µsVIx = 0 V, V_CM = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channel <sup>9</sup> fr1.2MbpsMbps		<b>t</b> pskod			5	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
(High/Low-to-High Impedance)transfer to High/Low)transfer to H	For All Models						
(High Impedance to High/Low) $t_R/t_F$ 2.5ns $C_L = 15 \text{ pF}, \text{CMOS signal levels}$ Output Rise/Fall Time (10% to 90%) $t_R/t_F$ 2.5ns $C_L = 15 \text{ pF}, \text{CMOS signal levels}$ Common-Mode Transient Immunity at Logic High Output <sup>8</sup> $ CM_H $ 2535 $kV/\mu s$ $V_{1x} = V_{DD1}/V_{DD2}, V_{CM} = 1000 V,$ transient magnitude = 800 VCommon-Mode Transient Immunity at Logic Low Output <sup>8</sup> $ CM_L $ 2535 $kV/\mu s$ $V_{1x} = 0 V, V_{CM} = 1000 V,$ transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channel <sup>9</sup> $f_r$ 1.2MbpsMaps		t <sub>PHZ</sub> , t <sub>PLH</sub>		6	8	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Common-Mode Transient Immunity at Logic High Output8ICMH2535kV/µsVIx = V_DD1/V_DD2, V_CM = 1000 V, transient magnitude = 800 VCommon-Mode Transient Immunity at Logic Low Output8ICML2535kV/µsVIx = 0 V, V_{CM} = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channel9fr1.2MbpsMaps		t <sub>PZH</sub> , t <sub>PZL</sub>		6	8	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
High Output8ICML2535transient magnitude = 800 VCommon-Mode Transient Immunity at Logic Low Output8ICML2535kV/µsVIx = 0 V, VCM = 1000 V, transient magnitude = 800 VRefresh Rate Input Dynamic Supply Current, per Channel9fr1.2MbpsMbps	Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> /t <sub>F</sub>		2.5		ns	C∟ = 15 pF, CMOS signal levels
Low Output8magnitude = 800 VRefresh Ratefr1.2Input Dynamic Supply Current, per Channel9IDDI (D)0.19Mbps		CM <sub>H</sub>	25	35		kV/μs	
Input Dynamic Supply Current, per Channel <sup>9</sup> I <sub>DDI (D)</sub> 0.19 mA/Mbps	Common-Mode Transient Immunity at Logic	CM∟	25	35		kV∕µs	$V_{lx} = 0 V$ , $V_{CM} = 1000 V$ , transient
	Refresh Rate	fr		1.2		Mbps	
Output Dynamic Supply Current, per Channel <sup>9</sup> I <sub>DDO (D)</sub> 0.05 mA/Mbps	Input Dynamic Supply Current, per Channel <sup>9</sup>	IDDI (D)		0.19		mA/Mbps	
		I <sub>DDO (D)</sub>		0.05			

<sup>&</sup>lt;sup>1</sup> All voltages are relative to their respective ground.

<sup>4</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>&</sup>lt;sup>2</sup> Supply current values are for all four channels combined running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section on Page 18. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 14 for total I<sub>DD1</sub> and I<sub>DD2</sub> supply currents as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

<sup>&</sup>lt;sup>3</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>&</sup>lt;sup>5</sup> t<sub>PHL</sub> propagation delay is measured from the 50% level of the falling edge of the V<sub>Ix</sub> signal to the 50% level of the falling edge of the V<sub>ox</sub> signal. t<sub>PLH</sub> propagation delay is measured from the 50% level of the rising edge of the V<sub>ix</sub> signal to the 50% level of the rising edge of the V<sub>ox</sub> signal.

<sup>&</sup>lt;sup>6</sup> t<sub>PSK</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> or t<sub>PLH</sub> that will be measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>&</sup>lt;sup>7</sup> Co-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>&</sup>lt;sup>8</sup> CM<sub>H</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_0 > 0.8 V_{DD2}$ . CM<sub>L</sub> is the maximum common-mode voltage slew rate than can be sustained while maintaining  $V_0 < 0.8 V$ . The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>&</sup>lt;sup>9</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section on Page 18 for guidance on calculating the per-channel supply current for a given data rate.

### **ELECTRICAL CHARACTERISTICS—3 V OPERATION<sup>1</sup>**

 $2.7 \text{ V} \le V_{DD1} \le 3.6 \text{ V}, 2.7 \text{ V} \le V_{DD2} \le 3.6 \text{ V};$  all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at  $T_A = 25^{\circ}\text{C}, V_{DD1} = V_{DD2} = 3.0 \text{ V}.$ 

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
DC SPECIFICATIONS	Symbol		194	IVIUX	Unit	
Input Supply Current, per Channel, Quiescent	IDDI (Q)		0.26	0.31	mA	
Output Supply Current, per Channel, Quiescent			0.20	0.14	mA	
ADuM1400, Total Supply Current, Four Channels <sup>2</sup>	IDDO (Q)		0.11	0.14	шл	
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	IDD1 (Q)		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current			0.5	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)	1DD2 (Q)		0.5	0.9	шл	De to Thing logic signal freq.
V <sub>DD1</sub> Supply Current	I <sub>DD1 (10)</sub>		4.5	6.5	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	IDD1 (10)		1.4	2.0	mA	5 MHz logic signal freq.
100 Mbps (CRW Grade Only)	1002 (10)		1.4	2.0	1103	o minz logic signal freq.
V <sub>DD1</sub> Supply Current	IDD1 (100)		42	65	mA	50 MHz logic signal freq.
V <sub>DD2</sub> Supply Current			72 11	15	mA	50 MHz logic signal freq.
ADuM1401, Total Supply Current, Four Channels <sup>2</sup>	DD2 (100)			15	шл	so winz logic signal freq.
DC to 2 Mbps						
	I <sub>DD1 (Q)</sub>		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current			0.7	1.0	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)	יטטע (ע)		0.7			
V <sub>DD1</sub> Supply Current	I <sub>DD1 (10)</sub>		3.7	5.4	mA	5 MHz logic signal freq.
V <sub>DD1</sub> Supply Current	IDD1 (10)		2.2	3.0	mA	5 MHz logic signal freq.
100 Mbps (CRW Grade Only)	1002 (10)		2.2	5.0	1103	s with logic signal freq.
V <sub>DD1</sub> Supply Current	IDD1 (100)		34	52	mA	50 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	IDD1 (100)		19	27	mA	50 MHz logic signal freq.
ADuM1402, Total Supply Current, Four Channels <sup>2</sup>	1002 (100)		15	27		so winz logic signarrieq.
DC to 2 Mbps						
V <sub>DD1</sub> or V <sub>DD2</sub> Supply Current	IDD1 (Q), IDD2 (Q)		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)			0.5	1.5		
$V_{DD1}$ or $V_{DD2}$ Supply Current	IDD1 (10), IDD2(10)		3.0	4.2	mA	5 MHz logic signal freq.
100 Mbps (CRW Grade Only)			5.0			s milz logic signal freq.
V <sub>DD1</sub> or V <sub>DD2</sub> Supply Current	IDD1 (100), IDD2 (100)		27	39	mA	50 MHz logic signal freq.
For All Models	1001 (100) 1002 (100)		-	57		so miliz logic signal ricq.
Input Currents	I <sub>IA</sub> , I <sub>IB</sub> , I <sub>IC</sub>	-10	+0.01	+10	μA	$0 \leq V_{IA}$ , $V_{IB}$ , $V_{IC}$ , $V_{ID} \leq V_{DD1}$ or $V_{DD2}$ ,
	lid, le1, le2				P	$0 \le V_{E1}, V_{E2} \le V_{DD1} \text{ or } V_{DD2}$
Logic High Input Threshold	VIH, VEH	1.6			V	
Logic Low Input Threshold	VIL, VEL			0.4	V	
Logic High Output Voltages	Voah, Vobh,	V <sub>DD1</sub> , V <sub>DD2</sub> – 0.1	3.0		V	$I_{Ox} = -20 \ \mu A$ , $V_{Ix} = V_{IxH}$
	Voch, Vodh	$V_{DD1}, V_{DD2} - 0.4$	2.8		V	$I_{Ox} = -4 \text{ mA}, V_{Ix} = V_{IxH}$
Logic Low Output Voltages	VOAL, VOBL,		0.0	0.1	V	$I_{Ox} = 20 \ \mu A$ , $V_{Ix} = V_{IxL}$
	Vocl, Vodl		0.04	0.1	V	$I_{0x} = 400 \ \mu A$ , $V_{1x} = V_{1xL}$
			0.2	0.4	V	$I_{Ox} = 4 \text{ mA}, V_{Ix} = V_{IxL}$
WITCHING SPECIFICATIONS						
ADuM140xARW						
Minimum Pulse Width <sup>3</sup>	PW			1000	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		1			Mbps	$C_{L} = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay <sup>5</sup>	tphl, tplh	50	75	100	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> -t <sub>PHL</sub>   <sup>5</sup>	PWD			40	ns	$C_{L} = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay Skew <sup>6</sup>	tрsк			50	ns	$C_{L} = 15 \text{ pF}$ , CMOS signal levels
Channel-to-Channel Matching <sup>7</sup>	tpskcd/od			50	ns	$C_{L} = 15 \text{ pF}$ , CMOS signal levels

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
ADuM140xBRW						
Minimum Pulse Width <sup>3</sup>	PW			100	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		10			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	tphl, tplh	20	38	50	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse Width Distortion,  tplh-tphl  <sup>5</sup>	PWD			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change versus Temperature			5		ps/°C	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			22	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Channel-to-Channel Matching, Co- Directional Channels <sup>7</sup>	<b>t</b> pskcd			3	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels <sup>7</sup>	t <sub>PSKOD</sub>			6	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
ADuM140xCRW						
Minimum Pulse Width <sup>3</sup>	PW		6.7	10	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Maximum Data Rate <sup>4</sup>		100	150		Mbps	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay <sup>5</sup>	tphl, tplh	20	34	45	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Pulse Width Distortion, $ t_{PLH}-t_{PHL} ^5$	PWD		0.5	2	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Change versus Temperature			3		ps/°C	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay Skew <sup>6</sup>	tрsк			16	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Channel-to-Channel Matching, Co- Directional Channels <sup>7</sup>	<b>t</b> pskcd			2	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels <sup>7</sup>	<b>t</b> pskod			5	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low-to-High Impedance)	tphz, tplh		6	8	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	tpzh, tpzl		6	8	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> /t <sub>F</sub>		3		ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Common Mode Transient Immunity at Logic High Output <sup>8</sup>	CM <sub>H</sub>	25	35		kV∕µs	$V_{lx} = V_{DD1}/V_{DD2}$ , $V_{CM} = 1000$ V,transient magnitude = 800 V
Common Mode Transient Immunity at Logic Low Output <sup>8</sup>	CM∟	25	35		kV∕µs	$V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V$
Refresh Rate	fr		1.1		Mbps	
Input Dynamic Supply Current, per Channel <sup>9</sup>	IDDI (D)		0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel <sup>9</sup>	IDDO (D)		0.03		mA/Mbps	

<sup>&</sup>lt;sup>1</sup> All voltages are relative to their respective ground.

<sup>3</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>&</sup>lt;sup>2</sup> Supply current values are for all four channels combined running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section on Page 18. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 14 for total lop: and loz2 supply currents as a function of ADUM1400/ADUM1401/ADUM1402 channel configurations.

<sup>&</sup>lt;sup>4</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>&</sup>lt;sup>5</sup> t<sub>PHL</sub> propagation delay is measured from the 50% level of the falling edge of the V<sub>Ix</sub> signal to the 50% level of the falling edge of the V<sub>Ox</sub> signal. t<sub>PLH</sub> propagation delay is measured from the 50% level of the rising edge of the V<sub>Ix</sub> signal to the 50% level of the rising edge of the V<sub>Ox</sub> signal.

<sup>&</sup>lt;sup>6</sup> t<sub>PSK</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> or t<sub>PLH</sub> that will be measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>&</sup>lt;sup>7</sup> Co-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

 $<sup>^{8}</sup>$  CM<sub>H</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>0</sub> > 0.8 V<sub>DD2</sub>. CM<sub>L</sub> is the maximum common-mode voltage slew rate than can be sustained while maintaining V<sub>0</sub> < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

<sup>&</sup>lt;sup>9</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section on Page 18 for guidance on calculating the per-channel supply current for a given data rate.

### ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION<sup>1</sup>

5 V/3 V operation:  $4.5 \text{ V} \le \text{V}_{\text{DD1}} \le 5.5 \text{ V}$ ,  $2.7 \text{ V} \le \text{V}_{\text{DD2}} \le 3.6 \text{ V}$ ; 3 V/5 V operation:  $2.7 \text{ V} \le \text{V}_{\text{DD1}} \le 3.6 \text{ V}$ ,  $4.5 \text{ V} \le \text{V}_{\text{DD2}} \le 5.5 \text{ V}$ ; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at  $T_A = 25^{\circ}\text{C}$ ;  $V_{\text{DD1}} = 3.0 \text{ V}$ ,  $V_{\text{DD2}} = 5 \text{ V}$ ; or  $V_{\text{DD1}} = 5 \text{ V}$ ,  $V_{\text{DD2}} = 3.0 \text{ V}$ .

Table 3. Parameter	Symbol	Min	Ture	Max	Unit	Test Conditions
DC SPECIFICATIONS	Symbol	MIN	Тур	IVIdX	Unit	Test Conditions
Input Supply Current, per Channel, Quiescent	DDI (Q)			0.50		
5 V/3 V Operation			0.50	0.53	mA	
3 V/5 V Operation			0.26	0.31	mA	
Output Supply Current, per Channel, Quiescent	DDO (Q)					
5 V/3 V Operation			0.11	0.14	mA	
3 V/5 V Operation			0.19	0.21	mA	
ADuM1400, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	DD1 (Q)					
5 V/3 V Operation			2.2	2.8	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.9	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (Q)</sub>					
5 V/3 V Operation			0.5	0.9	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
VDD1 Supply Current	I <sub>DD1 (10)</sub>					
5 V/3 V Operation			8.6	10.6	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.5	6.5	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (10)</sub>					
5 V/3 V Operation			1.4	2.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.6	3.5	mA	5 MHz logic signal freq.
100 Mbps (CRW Grade Only)						
VDD1 Supply Current	IDD1 (100)					
5 V/3 V Operation			76	100	mA	50 MHz logic signal freq.
3 V/5 V Operation			42	65	mA	50 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (100)</sub>					5 5 1
5 V/3 V Operation			11	15	mA	50 MHz logic signal freq.
3 V/5 V Operation			21	25	mA	50 MHz logic signal freq.
ADuM1401, Total Supply Current, Four Channels <sup>2</sup>						5 5 1
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	DD1 (Q)					
5 V/3 V Operation			1.8	2.4	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.0	1.6	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (Q)</sub>			1.0		
5 V/3 V Operation	1002 (Q)		0.7	1.2	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)			1.2	1.0		
V <sub>DD1</sub> Supply Current	IDD1 (10)					
5 V/3 V Operation			7.1	9.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.7	5.4	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current			5.7	э.т		
5 V/3 V Operation	DD2 (10)		2.2	3.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.2 4.1	5.0	mA	5 MHz logic signal freq.
-			4.1	5.0	IIIA	5 INITZ IOGIC SIGNAL HEQ.
100 Mbps (CRW Grade Only)	.					
V <sub>DD1</sub> Supply Current	DD1 (100)		()	02		
5 V/3 V Operation	I		62	82	mA	50 MHz logic signal freq.

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Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
3 V/5 V Operation			34	52	mA	50 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	IDD2 (100)					5 5 .
5 V/3 V Operation			19	27	mA	50 MHz logic signal freq.
3 V/5 V Operation			35	43	mA	50 MHz logic signal freq.
, ADuM1402, Total Supply Current, Four Channels <sup>2</sup>						
DC to 2 Mbps						
V <sub>DD1</sub> Supply Current	I <sub>DD1 (Q)</sub>					
5 V/3 V Operation	551(2)		1.5	2.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	DD2 (Q)					
5 V/3 V Operation	1002 (Q)		0.9	1.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						2 e to 1
V <sub>DD1</sub> Supply Current	DD1 (10)					
5 V/3 V Operation	1001 (10)		5.6	7.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.0	4.2	mA	5 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	I <sub>DD2 (10)</sub>		5.0	1.2	110 (	s with logic signal freq.
5 V/3 V Operation	1002 (10)		3.0	4.2	mA	5 MHz logic signal freq.
3 V/5 V Operation			5.6	7.0	mA	5 MHz logic signal freq.
100 Mbps (CRW Grade Only)			5.0	7.0	1107	5 Miliz logic signal req.
V <sub>DD1</sub> Supply Current	DD1 (100)					
5 V/3 V Operation	1001 (100)		49	62	mA	50 MHz logic signal freq.
3 V/5 V Operation			49 27	02 39	mA	50 MHz logic signal freq.
V <sub>DD2</sub> Supply Current	1		27	29	IIIA	So MHZ logic signal freq.
5 V/3 V Operation	DD2 (100)		27	39		
·			27 49	59 62	mA	50 MHz logic signal freq.
3 V/5 V Operation For All Models			49	02	mA	50 MHz logic signal freq.
		10	10.01	10		
Input Currents	IIA, IIB, IIC, IID, IE1, IE2	-10	+0.01	+10	μΑ	$ \begin{array}{l} 0 \leq V_{IA}, V_{IB},  V_{IC}, V_{ID} \leq V_{DD1} \text{ or} \\ V_{DD2},  0 \leq V_{E1}, V_{E2} \leq V_{DD1} \text{ or } V_{DD2} \end{array} $
Logic High Input Threshold	VIH, VEH					
5 V/3 V Operation	VIH, VEH	2.0			v	
3 V/5 V Operation		1.6			v	
Logic Low Input Threshold	VIL, VEL	1.0			v	
5 V/3 V Operation	VIL, VEL			0.8	v	
3 V/5 V Operation				0.0 0.4	v	
Logic High Output Voltages	Vоан, Vовн,	V <sub>DD1</sub> /V <sub>DD2</sub> – 0.1	Var Var	0.4	v	$I_{0x} = -20 \ \mu A, V_{1x} = V_{1xH}$
Logic High Output voltages	Voah, Vobh, Voch, Vodh		$V_{DD1}/V_{DD2} = 0.2$		v	$I_{0x} = -20 \ \mu A, \ V_{1x} = V_{1xH}$ $I_{0x} = -4 \ mA, \ V_{1x} = V_{1xH}$
Logic Low Output Voltages	VOAL VOBL	V DD1/ V DD2 - 0.4	0.0	0.1	v	$I_{0x} = -4 \text{ IIA}, V_{1x} = V_{1xH}$ $I_{0x} = 20 \mu\text{A}, V_{1x} = V_{1xL}$
Logic Low Output Voltages	VOAL, VOBL, Vocl <b>,</b> Vodl		0.04	0.1	v	$I_{0x} = 20 \ \mu A, \ V_{1x} = V_{1xL}$ $I_{0x} = 400 \ \mu A, \ V_{1x} = V_{1xL}$
	· OCL) · ODL		0.04	0.1	v	$I_{Ox} = 4 \text{ mA}, V_{Ix} = V_{IxL}$ $I_{Ox} = 4 \text{ mA}, V_{Ix} = V_{IxL}$
			0.2	0.4	v	$IO_X = 4 IIIA, VI_X = VI_{XL}$
SWITCHING SPECIFICATIONS ADuM140xARW						
Minimum Pulse Width <sup>3</sup>	PW			1000		
	PVV	1		1000	_	$C_L = 15 \text{ pF}$ , CMOS signal levels
Maximum Data Rate <sup>4</sup>		1	70	100	Mbps	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay <sup>5</sup>	tphl, tplh	50	70	100	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> -t <sub>PHL</sub>   <sup>5</sup>	PWD			40	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay Skew <sup>6</sup>	t <sub>PSK</sub>			50	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Channel-to-Channel Matching <sup>7</sup>	tpskcd/od			50	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
ADuM140xBRW	DW			100		
Minimum Pulse Width <sup>3</sup>	PW			100	ns	$C_L = 15 \text{ pF,CMOS signal levels}$
Maximum Data Rate <sup>4</sup>		10			Mbps	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay <sup>5</sup>	tphl, tplh	15	35	50	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Pulse Width Distortion,  t <sub>PLH</sub> -t <sub>PHL</sub>   <sup>5</sup>	PWD			3	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels

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Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
Change versus Temperature			5		ps/°C	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay Skew <sup>6</sup>	tрsк			22	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Co- Directional Channels <sup>7</sup>	<b>t</b> pskcd			3	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels <sup>7</sup>	<b>t</b> pskod			6	ns	C∟ = 15 pF, CMOS signal levels
ADuM140xCRW						
Minimum Pulse Width <sup>3</sup>	PW		6.7	10	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Maximum Data Rate <sup>4</sup>		100	150		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay <sup>5</sup>	tphl, tplh	20	30	40	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Pulse Width Distortion,  tplh-tphl  <sup>5</sup>	PWD		0.5	2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change versus Temperature			3		ps/°C	$C_L = 15 \text{ pF}$ , CMOS signal levels
Propagation Delay Skew <sup>6</sup>	tрsк			14	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Co- Directional Channels <sup>7</sup>	<b>t</b> pskcd			2	ns	C∟ = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing- Directional Channels <sup>7</sup>	<b>t</b> pskod			5	ns	C∟ = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	tphz, tplh		6	8	ns	C∟ = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t <sub>PZH</sub> , t <sub>PZL</sub>		6	8	ns	$C_L = 15 \text{ pF}$ , CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> /t <sub>f</sub>					C <sub>L</sub> = 15 pF, CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output <sup>8</sup>	CM <sub>H</sub>	25	35		kV/μs	$V_{lx} = V_{DD1}/V_{DD2}, V_{CM} = 1000 V,$ transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output <sup>8</sup>	CM⊾	25	35		kV/μs	$V_{Ix} = 0 V, V_{CM} = 1000 V,$ transient magnitude = 800 V
Refresh Rate	fr					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current, per Channel <sup>9</sup>	I <sub>DDI (D)</sub>					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel <sup>9</sup>	I <sub>DDI (D)</sub>					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

<sup>&</sup>lt;sup>1</sup> All voltages are relative to their respective ground.

<sup>8</sup> CM<sub>H</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>0</sub> > 0.8 V<sub>DD2</sub>. CM<sub>L</sub> is the maximum common-mode voltage slew rate than can be sustained while maintaining V<sub>0</sub> < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.</p>

<sup>&</sup>lt;sup>2</sup> Supply current values are for all four channels combined running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section on Page 18. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 14 for total I<sub>DD1</sub> and I<sub>DD2</sub> supply currents as a function of data rate for ADuM1400/ADuM1402 channel configurations.

<sup>&</sup>lt;sup>3</sup> The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

<sup>&</sup>lt;sup>4</sup> The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

<sup>&</sup>lt;sup>5</sup> t<sub>PHL</sub> propagation delay is measured from the 50% level of the falling edge of the V<sub>Ix</sub> signal to the 50% level of the falling edge of the V<sub>ox</sub> signal. t<sub>PLH</sub> propagation delay is measured from the 50% level of the rising edge of the V<sub>Ix</sub> signal to the 50% level of the rising edge of the V<sub>ox</sub> signal.

<sup>&</sup>lt;sup>6</sup> t<sub>PSK</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> or t<sub>PLH</sub> that will be measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>&</sup>lt;sup>7</sup> Co-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

<sup>&</sup>lt;sup>9</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on perchannel supply current for unloaded and loaded conditions. See the Power Consumption section on Page 18 for guidance on calculating the per-channel supply current for a given data rate.

### PACKAGE CHARACTERISTICS

Table 4.						
Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
Resistance (Input-Output) <sup>1</sup>	RI-O		10 <sup>12</sup>		Ω	
Capacitance (Input-Output) <sup>1</sup>	CI-O		2.2		pF	f = 1 MHz
Input Capacitance <sup>2</sup>	Ci		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ」		33		°C/W	Thermocouple located
IC Junction-to-Case Thermal Resistance, Side 2	θιςο		28		°C/W	at center of package underside

<sup>1</sup> Device considered a 2-terminal device: Pins 1, 2, 3, 4, 5, 6, 7, and 8 shorted together and Pins 9, 10, 11, 12, 13, 14, 15, and 16 shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

#### **REGULATORY INFORMATION**

The ADuM140x has been approved by the organizations listed in Table 5.

Table 5.

UL <sup>1</sup>	CSA	VDE <sup>2</sup>
Recognized under 1577 component recognition program <sup>1</sup>	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01 <sup>2</sup>
Double insulation, 2500 V rms isolation voltage	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms maximum working voltage	Basic insulation, 560 V peak Complies with DIN EN 60747-5-2 (VDE 0884 Part 2): 2003 01, DIN EN 60950 (VDE 0805): 2001-12; EN 60950:2000 Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

<sup>1</sup> In accordance with UL1577, each ADuM140x is proof tested by applying an insulation test voltage  $\geq$  3000 V rms for 1 second (current leakage detection limit = 5  $\mu$ A). <sup>2</sup> In accordance with DIN EN 60747-5-2, each ADuM140x is proof tested by applying an insulation test voltage  $\geq$  1050 V peak for 1 second (partial discharge detection limit = 5  $\mu$ C). A "\*" mark branded on the component designates DIN EN 60747-5-2 approval.

#### **INSULATION AND SAFETY-RELATED SPECIFICATIONS** Table 6.

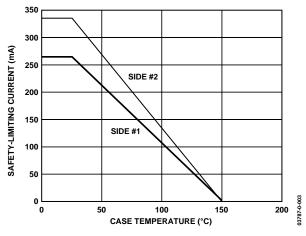
Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.40 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.10 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	v	DIN IEC 112/VDE 0303 Part 1
Isolation Group		Illa		Material Group (DIN VDE 0110, 1/89, Table 1)

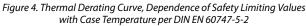
Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110			
For Rated Mains Voltage ≤ 150 V rms		I–IV	
For Rated Mains Voltage ≤ 300 V rms		1–111	
For Rated Mains Voltage ≤ 400 V rms		1–11	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)		2	
Maximum Working Insulation Voltage	VIORM	560	V peak
Input to Output Test Voltage, Method b1	V <sub>PR</sub>	1050	V peak
$V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test, t <sub>m</sub> = 1 sec, Partial Discharge < 5 pC			
Input to Output Test Voltage, Method a	V <sub>PR</sub>		
After Environmental Tests Subgroup 1			
$V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge < 5 pC		896	V peak
After Input and/or Safety Test Subgroup 2/3		672	V peak
$V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge < 5 pC		072	v peak
Highest Allowable Overvoltage	V <sub>TR</sub>	4000	V peak
(Transient Overvoltage, $t_{TR} = 10$ sec)			
Safety-Limiting Values (Maximum value allowed in the event of a failure, also see Thermal Derating Curve, Figure 4)			
Case Temperature	Ts	150	°C
Side 1 Current	Is1	265	mA
Side 2 Current	ls2	335	mA
Insulation Resistance at $T_s$ , $V_{IO} = 500 V$	Rs	>109	Ω

### DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

The \* marking on packages denotes DIN EN 60747-5-2 approval for 560 V peak working voltage.





#### **RECOMMENDED OPERATING CONDITIONS** Table 8.

14010 01				
Parameter	Symbol	Min	Max	Unit
Operating Temperature	TA	-40	+105	°C
Supply Voltages <sup>1</sup>	$V_{DD1,}V_{DD2}$	2.7	5.5	V
Input Signal Rise and Fall Times			1.0	ms

<sup>1</sup> All voltages are relative to their respective ground.

Immunity section on Page 17 for information on immunity to external magnetic fields.

See the DC Correctness and Magnetic Field

### **ABSOLUTE MAXIMUM RATINGS**

Table 9.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T <sub>st</sub>	-65	+150	°C
Ambient Operating Temperature	T <sub>A</sub>	-40	+105	°C
Supply Voltages <sup>1</sup>	V <sub>DD1</sub> , V <sub>DD2</sub>	-0.5	+7.0	V
Input Voltage <sup>1, 2</sup>	VIA, VIB, VIC, VID, VE1, VE2	-0.5	V <sub>DDI</sub> + 0.5	V
Output Voltage <sup>1, 2</sup>	V <sub>OA</sub> , V <sub>OB</sub> , V <sub>OC</sub> , V <sub>OD</sub>	-0.5	$V_{DDO} + 0.5$	V
Average Output Current, Per Pin <sup>3</sup>				
Side 1	loı	-18	+18	mA
Side 2	l <sub>02</sub>	-22	+22	mA
Common-Mode Transients <sup>4</sup>		-100	+100	kV/μs

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> V<sub>DDI</sub> and V<sub>DDO</sub> refer to the supply voltages on the input and output sides of a given channel, respectively. See PC Board Layout section.

<sup>3</sup> See Figure 4 for maximum rated current values for various temperatures.

<sup>4</sup> Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. Ambient temperature = 25°C, unless otherwise noted.

#### **ESD CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table 10.	Truth	Table	(Positive	Logic)
			(10010100	

	V <sub>EX</sub> Input <sup>2</sup>	V <sub>DDI</sub> State <sup>1</sup>	V <sub>DDO</sub> State <sup>1</sup>		Note
Н	H or NC	Powered	Powered	Н	
L	H or NC	Powered	Powered	L	
Х	L	Powered	Powered	Z	
Х	H or NC	Unpowered	Powered	н	Outputs returns to input state within 1 $\mu$ s of V <sub>DDI</sub> power restoration.
Х	L	Unpowered	Powered	Z	
x	x	Powered	Unpowered	Indeterminate	Outputs returns to input state within 1 $\mu$ s of V <sub>DDO</sub> power restoration if V <sub>EX</sub> state is H or NC. Outputs returns to high impedance state within 8 ns of V <sub>DDO</sub> power restoration if V <sub>EX</sub> state is L.

<sup>1</sup> V<sub>IX</sub> and V<sub>OX</sub> refer to the input and output signals of a given channel (A, B, C, or D). V<sub>EX</sub> refers to the output enable signal on the same side as the V<sub>OX</sub> outputs. V<sub>DDI</sub> and V<sub>DDD</sub> refer to the supply voltages on the input and output sides of the given channel, respectively.

 $<sup>^{2}</sup>$  In noisy environments, connecting  $V_{\text{EX}}$  to an external logic high or low is recommended.

### **PIN CONFIGURATIONS AND PIN FUNCTION DESCRIPTIONS**

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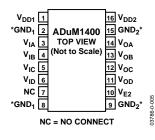


Figure 5. ADuM1400 Pin Configuration

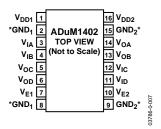


Figure 7. ADuM1402 Pin Configuration

Figure 6. ADuM1401 Pin Configuration

\*Pins 2 and 8 are internally connected. Connecting both to GND<sub>1</sub> is recommended. Pins 9 and 15 are internally connected. Connecting both to GND<sub>2</sub> is recommended. Output enable Pin 10 on the ADuM1400 may be left disconnected, if outputs are to be always enabled. Output enable Pins 7 and 10 on the ADuM1401/ADuM1402 may be left disconnected, if outputs are to be always enabled. In noisy environments, connecting Pin 7 (for ADuM1401 and ADuM1402) and Pin 10 (for all models) to an external logic high or low is recommended.

Pin		
No.	Mnemonic	Function
1	V <sub>DD1</sub>	Supply voltage for isolator Side 1, 2.7 V to 5.5 V.
2	GND1	Ground 1. Ground reference for isolator Side 1.
3	VIA	Logic Input A.
4	VIB	Logic Input B.
5	VIC	Logic Input C.
6	VID	Logic Input D.
7	NC	No Connect.
8	GND <sub>1</sub>	Ground 1. Ground reference for isolator Side 1.
9	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
10	V <sub>E2</sub>	Output Enable 2. Active high logic input. $V_{OA}$ , $V_{OB}$ , $V_{OC}$ , and $V_{OD}$ outputs are enabled when $V_{E2}$ is high or disconnected. $V_{OA}$ , $V_{OB}$ , $V_{OC}$ , and $V_{OD}$ outputs are disabled when $V_{E2}$ is low. In noisy environments, connecting $V_{E2}$ to an external logic high or low is recommended.
11	Vod	Logic Output D.
12	Voc	Logic Output C.
13	Vob	Logic Output B.
14	Voa	Logic Output A.
15	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
16	V <sub>DD2</sub>	Supply voltage for isolator Side 2, 2.7 V to 5.5 V.

#### Table 12. ADuM1401 Pin Function Descriptions

Pin		
No.	Mnemonic	Function
1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND <sub>1</sub>	Ground 1. Ground reference for isolator Side 1.
3	VIA	Logic Input A.
4	V <sub>IB</sub>	Logic Input B.
5	Vic	Logic Input C.
6	V <sub>OD</sub>	Logic Output D.
7	V <sub>E1</sub>	Output Enable 1. Active high logic input. $V_{OD}$ output is enabled when $V_{E1}$ is high or disconnected. $V_{OD}$ is disabled when $V_{E1}$ is low. In noisy environments, connecting $V_{E1}$ to an external logic high or low is recommended.
8	GND1	Ground 1. Ground reference for isolator Side 1.
9	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
10	V <sub>E2</sub>	Output Enable 2. Active high logic input. $V_{OA}$ , $V_{OB}$ , and $V_{OC}$ outputs are enabled when $V_{E2}$ is high or disconnected. $V_{OA}$ , $V_{OB}$ , and $V_{OC}$ outputs are disabled when $V_{E2}$ is low. In noisy environments, connecting $V_{E2}$ to an external logic high or low is recommended.
11	VID	Logic Input D.
12	Voc	Logic Output C.
13	Vob	Logic Output B.
14	V <sub>OA</sub>	Logic Output A.
15	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
16	V <sub>DD2</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.

	гш		
	No.	Mnemonic	Function
V.	1	V <sub>DD1</sub>	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
	2	GND1	Ground 1. Ground reference for isolator Side 1.
	3	VIA	Logic Input A.
	4	VIB	Logic Input B.
	5	Voc	Logic Output C.
	6	Vod	Logic Output D.
	7	V <sub>E1</sub>	Output Enable 1. Active high logic input. $V_{OC}$ and $V_{OD}$ outputs are enabled when $V_{E1}$ is high or disconnected. $V_{OC}$ and $V_{OD}$ outputs are disabled when $V_{E1}$ is low. In noisy environments, connecting $V_{E1}$ to an external logic high or low is recommended.
	8	GND <sub>1</sub>	Ground 1. Ground reference for isolator Side 1.
	9	GND <sub>2</sub>	Ground 2. Ground reference for isolator Side 2.
	10	V <sub>E2</sub>	Output Enable 2. Active high logic input. $V_{OA}$ and $V_{OB}$ outputs are enabled when $V_{E2}$ is high or disconnected. $V_{OA}$ and $V_{OB}$ outputs are disabled when $V_{E2}$ is low. In noisy environments, connecting $V_{E2}$ to an external logic high or low is recommended.
	11	V <sub>ID</sub>	Logic Input D.
V	12	VIC	Logic Input C.
	13	V <sub>OB</sub>	Logic Output B.

Logic Output A.

Ground 2. Ground Reference for Isolator Side 2.

Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

#### Table 13. ADuM1402 Pin Function Descriptions

Pin

14 V<sub>OA</sub>

15

 $\mathsf{GND}_2$ 

16 V<sub>DD2</sub>

### **TYPICAL PERFORMANCE CHARACTERISTICS**

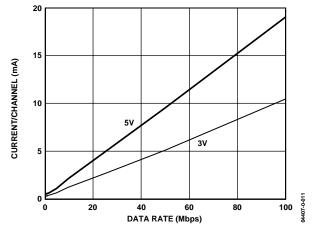


Figure 8. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

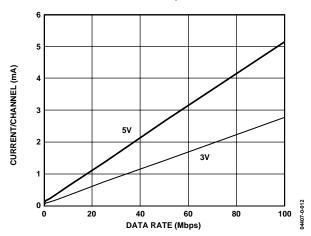


Figure 9. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

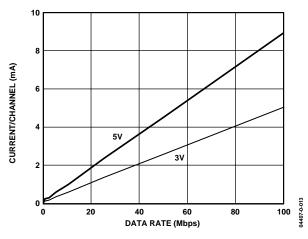


Figure 10. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

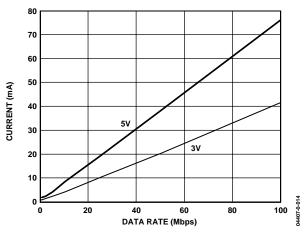


Figure 11. Typical ADuM1400 VDD1 Supply Current vs. Data Rate for 5 V and 3 V Operation

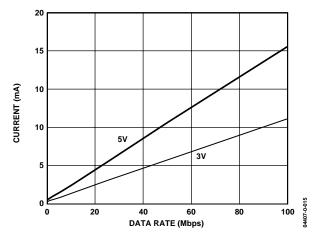


Figure 12. Typical ADuM1400  $V_{DD2}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

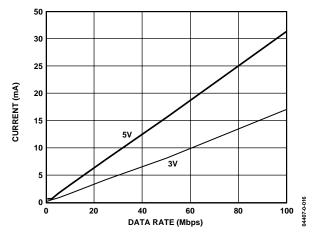


Figure 13. Typical ADuM1401 V<sub>DD1</sub> Supply Current vs. Data Rate for 5 V and 3 V Operation

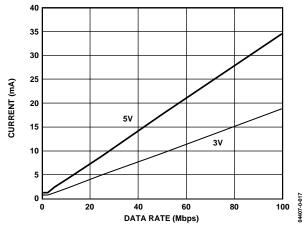


Figure 14. Typical ADuM1401  $V_{\mbox{\scriptsize DD2}}$  Supply Current vs. Data Rate for 5 V and 3 V Operation

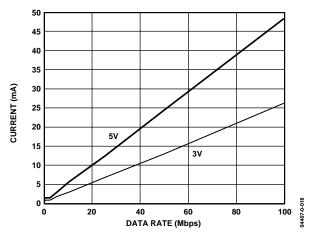


Figure 15. Typical ADuM1402 VDD1 or VDD2 Supply Current vs. Data Rate for 5 V and 3 V Operation

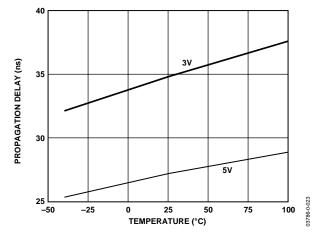


Figure 16. Propagation Delay vs. Temperature, C Grade

### APPLICATION INFORMATION PC BOARD LAYOUT

The ADuM140x digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (Figure 17). Bypass capacitors are most conveniently connected between Pins 1 and 2 for  $V_{DD1}$  and between Pins 15 and 16 for  $V_{DD2}$ . The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pins 1 and 8 and between Pins 9 and 16 should also be considered unless the ground pair on each package side are connected close to the package.

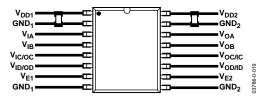


Figure 17. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's Absolute Maximum Ratings, thereby leading to latch-up or permanent damage.

### **PROPAGATION DELAY-RELATED PARAMETERS**

Propagation delay is a parameter that describes the time it takes for a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high.

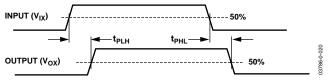


Figure 18. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs among channels within a single ADuM140x component.

Propagation delay skew refers to the maximum amount the propagation delay differs among multiple ADuM140x components operated under the same conditions.

### DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is, therefore, either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than 2  $\mu$ s, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5  $\mu$ s, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 10) by the watchdog timer circuit.

The limitation on the ADuM140x's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The analysis below defines the conditions under which this may occur. The 3 V operating condition of the ADuM140x is examined, because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \prod r_n^2; n = 1, 2, \dots, N$$

where:

β is magnetic flux density (gauss). *N* is the number of turns in the receiving coil. *r<sub>n</sub>* is the radius of the n<sup>th</sup> turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM140x and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 19.

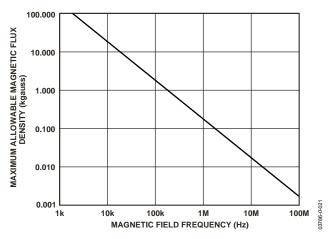
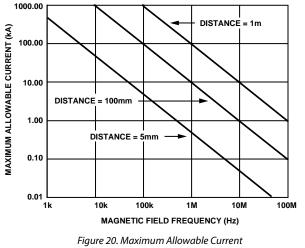


Figure 19. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and will not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst case polarity), it would reduce the received pulse from > 1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM140x transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As can be seen, the ADuM140x is extremely immune and can be affected only by extremely large currents operated at high frequency, very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM140x to affect the component's operation.



for Various Current-to-ADuM140x Spacings

Note that at combinations of strong magnetic field and high

frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

### **POWER CONSUMPTION**

The supply current at a given channel of the ADuM140x isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)}$$
  $f \le 0.5 f_r$ 

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by:

$$I_{DDO} = I_{DDO(Q)} \qquad \qquad f \le 0.5 f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \text{ x } 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO(Q)}$$
  
f > 0.5f\_r

where:

*I*<sub>DDI(D)</sub>, *I*<sub>DDO(D)</sub> are the input and output dynamic supply currents per channel (mA/Mbps).

 $C_L$  is output load capacitance (pF).

 $V_{DDO}$  is the output supply voltage (V).

*f* is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

 $f_r$  is the input stage refresh rate (Mbps).

 $I_{DDI(Q)}$ ,  $I_{DDO(Q)}$  are the specified input and output quiescent supply currents (mA).

To calculate the total  $I_{DD1}$  and  $I_{DD2}$  supply current, the supply currents for each input and output channel corresponding to  $I_{DD1}$  and  $I_{DD2}$  are calculated and totaled. Figure 8 and Figure 9 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 10 provides perchannel supply current as a function of data rate for a 15 pF output condition. Figure 11 through Figure 14 provide total  $I_{DD1}$  and  $I_{DD2}$  supply current as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

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### **OUTLINE DIMENSIONS**

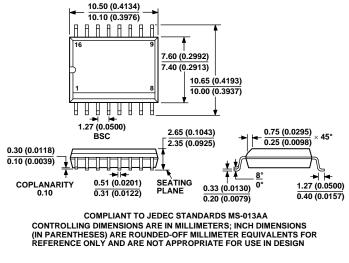


Figure 21. 16-Lead Standard Small Outline Package [SOIC] Wide Body (RW-16) Dimension shown in millimeters (inches)

#### **ORDERING GUIDE**

Models	Number of Inputs, V <sub>DD1</sub> Side	Number of Inputs, V <sub>DD2</sub> Side	Maximum Data Rate (Mbps)	Maximum Popagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range (°C)	Package Option <sup>1</sup>
ADuM1400ARW <sup>2</sup>	4	0	1	100	40	–40 to +105	RW-16
ADuM1400BRW <sup>2</sup>	4	0	10	50	3	–40 to +105	RW-16
ADuM1400CRW <sup>2</sup>	4	0	100	32	2	–40 to +105	RW-16
ADuM1400ARWZ <sup>2, 3</sup>	4	0	1	100	40	–40 to +105	RW-16
ADuM1400BRWZ <sup>2, 3</sup>	4	0	10	50	3	–40 to +105	RW-16
ADuM1400CRWZ <sup>2, 3</sup>	4	0	100	32	2	–40 to +105	RW-16
ADuM1401ARW <sup>2</sup>	3	1	1	100	40	–40 to +105	RW-16
ADuM1401BRW <sup>2</sup>	3	1	10	50	3	–40 to +105	RW-16
ADuM1401CRW <sup>2</sup>	3	1	100	32	2	–40 to +105	RW-16
ADuM1401ARWZ <sup>2, 3</sup>	3	1	1	100	40	–40 to +105	RW-16
ADuM1401BRWZ <sup>2, 3</sup>	3	1	10	50	3	–40 to +105	RW-16
ADuM1401CRWZ <sup>2, 3</sup>	3	1	100	32	2	–40 to +105	RW-16
ADuM1402ARW <sup>2</sup>	2	2	1	100	40	–40 to +105	RW-16
ADuM1402BRW <sup>2</sup>	2	2	10	50	3	–40 to +105	RW-16
ADuM1402CRW <sup>2</sup>	2	2	100	32	2	–40 to +105	RW-16
ADuM1402ARWZ <sup>2, 3</sup>	2	2	1	100	40	–40 to +105	RW-16
ADuM1402BRWZ <sup>2, 3</sup>	2	2	10	50	3	–40 to +105	RW-16
ADuM1402CRWZ <sup>2, 3</sup>	2	2	100	32	2	–40 to +105	RW-16

 $^{1}$  RW-16 = 16-lead wide body SOIC.

<sup>2</sup> Tape and reel are available. The addition of an "-RL" suffix designates a 13" (1,000 units) tape and reel option.

 $^{3}$  Z = Pb-free part.

### NOTES

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