

### FEATURES

**+1.8 V to +5.5 V Single Supply**  
**2.5  $\Omega$  (Typ) On Resistance**  
**Low On-Resistance Flatness**  
**-3 dB Bandwidth >200 MHz**  
**Rail-to-Rail Operation**  
**10-Lead  $\mu$ SOIC Package**  
**Fast Switching Times**  
 $t_{ON}$  16 ns  
 $t_{OFF}$  8 ns  
**Typical Power Consumption (<0.01  $\mu$ W)**  
**TTL/CMOS Compatible**

### APPLICATIONS

**Battery Powered Systems**  
**Communication Systems**  
**Sample-and-Hold Systems**  
**Audio Signal Routing**  
**Audio and Video Switching**  
**Mechanical Reed Relay Replacement**

### GENERAL DESCRIPTION

The ADG736 is a monolithic device comprising two independently selectable CMOS SPDT switches. These switches are designed on a submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents and wide input signal bandwidth.

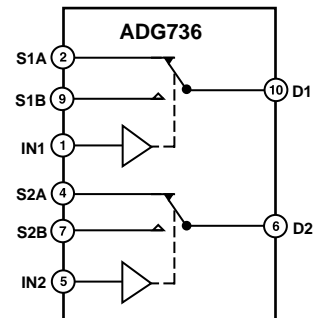
The on resistance profile is very flat over the full analog signal range. This ensures excellent linearity and low distortion when switching audio signals. Fast switching speed also makes the part suitable for video signal switching.

The ADG736 can operate from a single +1.8 V to +5.5 V supply, making it ideally suited to portable and battery powered instruments.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the power supplies. The ADG736 exhibits break-before-make switching action.

The ADG736 is available in a 10-lead  $\mu$ SOIC package.

### FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

### PRODUCT HIGHLIGHTS

- +1.8 V to +5.5 V Single Supply Operation.  
The ADG736 offers high performance, including low on resistance and fast switching times and is fully specified and guaranteed with +3 V and +5 V supply rails.
- Very Low  $R_{ON}$  (4.5  $\Omega$  Max at 5 V, 8  $\Omega$  Max at 3 V).  
At supply voltage of +1.8 V,  $R_{ON}$  is typically 35  $\Omega$  over the temperature range.
- Low On-Resistance Flatness.
- 3 dB Bandwidth >200 MHz.
- Low Power Dissipation.  
CMOS construction ensures low power dissipation.
- Fast  $t_{ON}/t_{OFF}$ .
- Break-Before-Make Switching Action.
- 10-Lead  $\mu$ SOIC Package.

### REV. 0

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**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**  
**Tel: 781/329-4700 World Wide Web Site: <http://www.analog.com>**  
**Fax: 781/326-8703 © Analog Devices, Inc., 1998**

# ADG736—SPECIFICATIONS<sup>1</sup> ( $V_{DD} = +5\text{ V} \pm 10\%$ , $GND = 0\text{ V}$ . All Specifications $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , unless otherwise noted.)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	
On-Resistance ( $R_{ON}$ )	2.5 4	4.5	$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -10\text{ mA}$ ; Test Circuit 1
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )		0.1 0.4	$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -10\text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.5	1.2	$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$ $\pm 0.1$	$\pm 0.3$	nA typ nA max	$V_{DD} = +5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$ $\pm 0.1$	$\pm 0.3$	nA typ nA max	$V_S = V_D = 1\text{ V}$ or $4.5\text{ V}$ ; Test Circuit 3
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005	$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	12	16	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ , Test Circuit 4
$t_{OFF}$	5	8	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ , Test Circuit 4
Break-Before-Make Time Delay, $t_D$	7	1	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 3\text{ V}$ , Test Circuit 5
Off Isolation	-62 -82		dB typ dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 6
Channel-to-Channel Crosstalk	-62 -82		dB typ dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
Bandwidth -3 dB	200		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 8
$C_S$ (OFF)	9		pF typ	
$C_D$ , $C_S$ (ON)	32		pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001	1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +5.5\text{ V}$ Digital Inputs = 0 V or 5 V

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# SPECIFICATIONS<sup>1</sup> ( $V_{DD} = +3\text{ V} \pm 10\%$ , $GND = 0\text{ V}$ . All Specifications $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , unless otherwise noted.)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	
On-Resistance ( $R_{ON}$ )	5	5.5 8	$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -10\text{ mA}$ ; Test Circuit 1
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.1		$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -10\text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )		0.4 2.5	$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$ $\pm 0.1$	$\pm 0.3$	nA typ nA max	$V_{DD} = +3.3\text{ V}$ $V_S = 3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3\text{ V}$ ; Test Circuit 2
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$ $\pm 0.1$	$\pm 0.3$	nA typ nA max	$V_S = V_D = 1\text{ V}$ or $3\text{ V}$ ; Test Circuit 3
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.0	V min	
Input Low Voltage, $V_{INL}$		0.4	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005	$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	14	20	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$ ; Test Circuit 4
$t_{OFF}$	6	10	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$ ; Test Circuit 4
Break-Before-Make Time Delay, $t_D$	7	1	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 2\text{ V}$ ; Test Circuit 5
Off Isolation	-62 -82		dB typ dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 6
Channel-to-Channel Crosstalk	-62 -82		dB typ dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
Bandwidth -3 dB	200		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 8
$C_S$ (OFF)	9		pF typ	
$C_D$ , $C_S$ (ON)	32		pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001	1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +3.3\text{ V}$ Digital Inputs = 0 V or 3 V

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG736

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to GND	.....	-0.3 V to +6 V
Analog, Digital Inputs <sup>2</sup>	.....	-0.3 V to V <sub>DD</sub> +0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	.....	30 mA
Peak Current, S or D	.....	100 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range		
Industrial (B Version)	.....	-40°C to +85°C
Storage Temperature Range	.....	-65°C to +150°C
Junction Temperature	.....	+150°C
μSOIC Package, Power Dissipation	.....	315 mW
θ <sub>JA</sub> Thermal Impedance	.....	205°C/W
Lead Temperature, Soldering		
Vapor Phase (60 sec)	.....	+215°C
Infrared (15 sec)	.....	+220°C
ESD	.....	2 kV

### NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overtolerances at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## ORDERING GUIDE

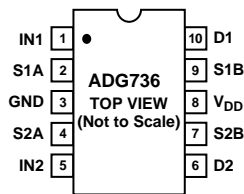
Model	Temperature Range	Brand <sup>1</sup>	Package Option <sup>2</sup>
ADG736BRM	-40°C to +85°C	SAB	RM-10

### NOTES

<sup>1</sup>Brand = Due to small package size, these three characters represent the part number.

<sup>2</sup>RM = μSOIC.

## PIN CONFIGURATION (10-Lead μSOIC)



## TERMINOLOGY

V <sub>DD</sub>	Most positive power supply potential.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
R <sub>ON</sub>	Ohmic resistance between D and S.
ΔR <sub>ON</sub>	On resistance match between any two channels i.e., R <sub>ONmax</sub> -R <sub>ONmin</sub> .
R <sub>FLAT(ON)</sub>	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I <sub>S</sub> (OFF)	Source leakage current with the switch "OFF."
I <sub>D</sub> , I <sub>S</sub> (ON)	Channel leakage current with the switch "ON."
V <sub>D</sub> (V <sub>S</sub> )	Analog voltage on terminals D, S.
C <sub>S</sub> (OFF)	"OFF" switch source capacitance.
C <sub>D</sub> , C <sub>S</sub> (ON)	"ON" switch capacitance.
t <sub>ON</sub>	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
t <sub>OFF</sub>	Delay between applying the digital control input and the output switching off.
t <sub>D</sub>	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Bandwidth	The frequency at which the output is attenuated by -3 dBs.
On Response	The frequency response of the "ON" switch.
On Loss	The voltage drop across the "ON" switch, seen on the On Response versus frequency plot as how many dBs the signal is away from 0 dB at very low frequencies.

Table I. Truth Table

Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG736 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# Typical Performance Characteristics—ADG736

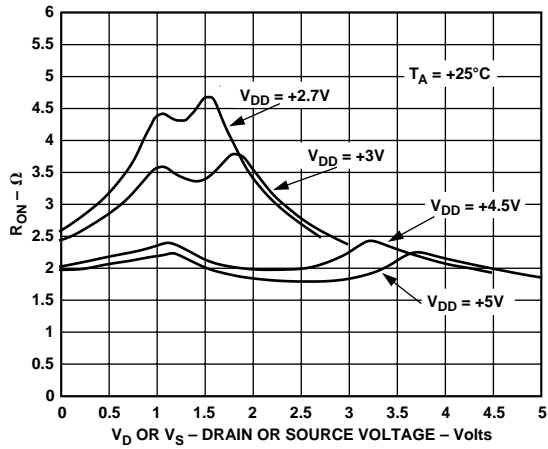


Figure 1. On Resistance as a Function of  $V_D$  ( $V_S$ ) Single Supplies

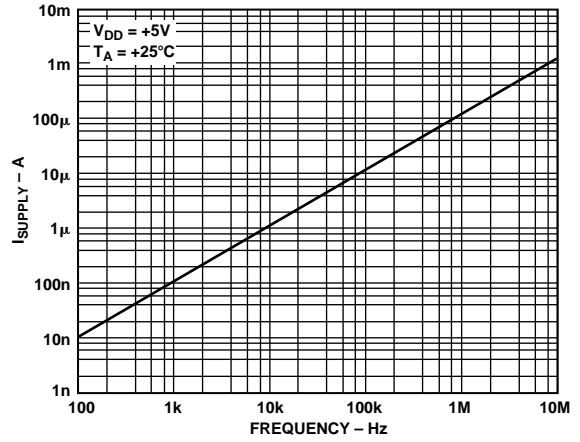


Figure 4. Supply Current vs. Input Switching Frequency

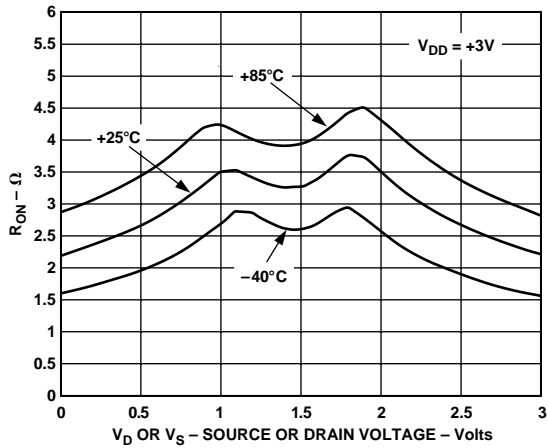


Figure 2. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures  $V_{DD} = 3V$

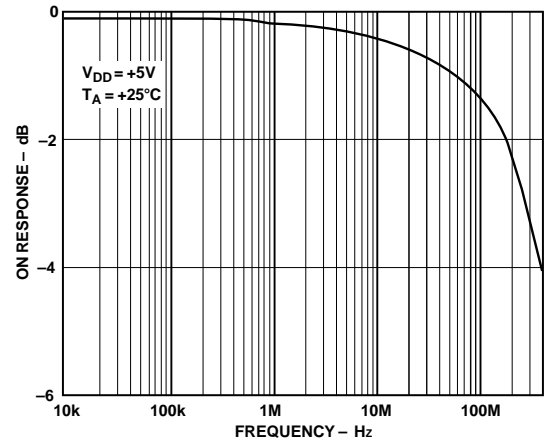


Figure 5. On Response vs. Frequency

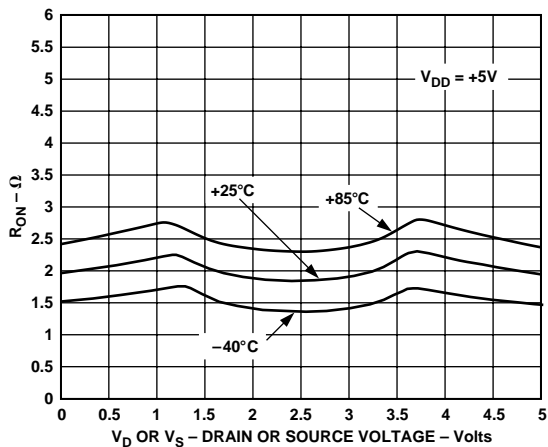


Figure 3. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures  $V_{DD} = 5V$

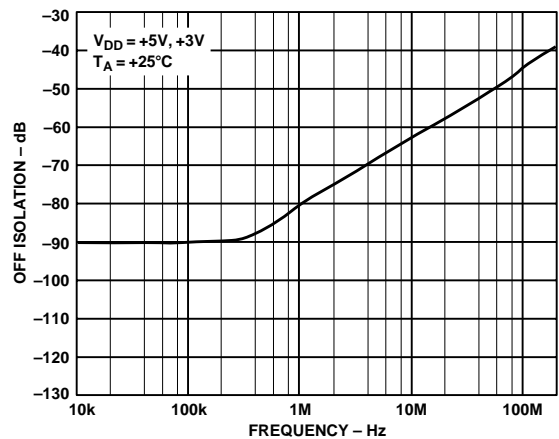


Figure 6. Off Isolation vs. Frequency

# ADG736

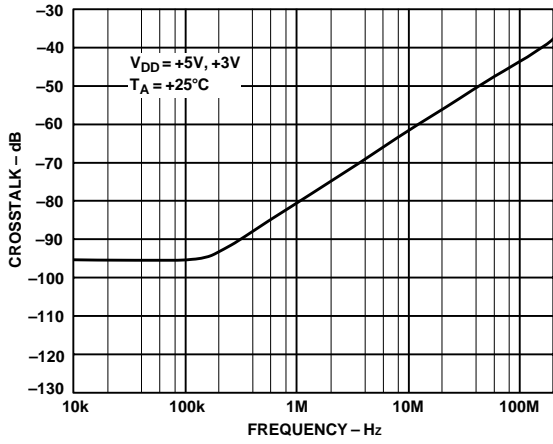


Figure 7. Crosstalk vs. Frequency

## APPLICATIONS

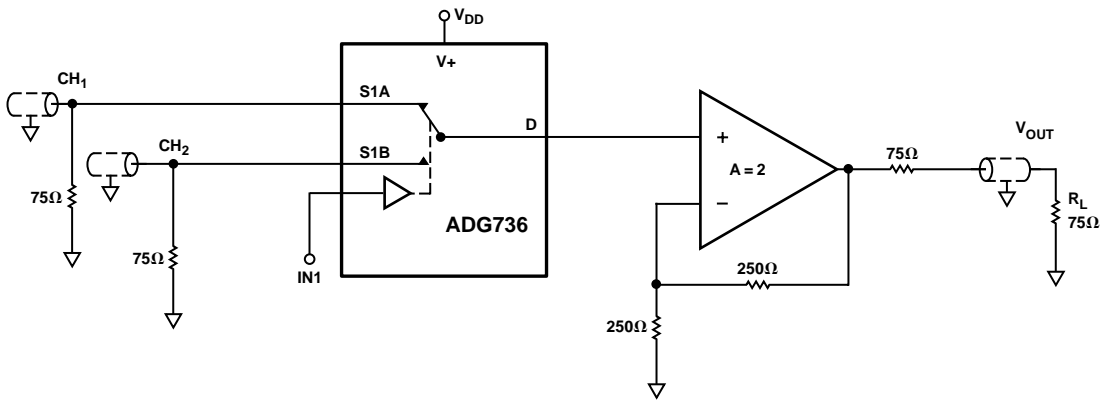
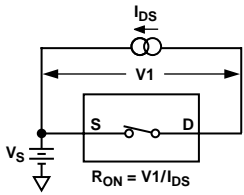
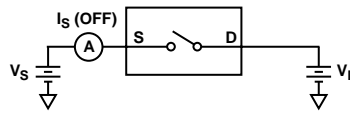


Figure 8. Using the ADG736 to Select Between Two Video Signals

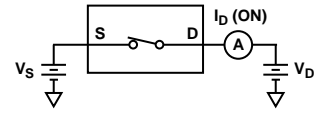
## Test Circuits



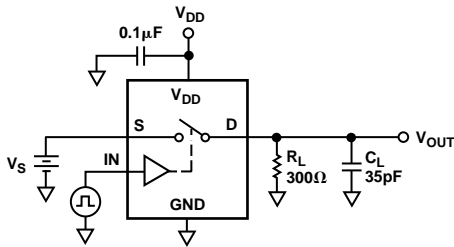
Test Circuit 1. On Resistance



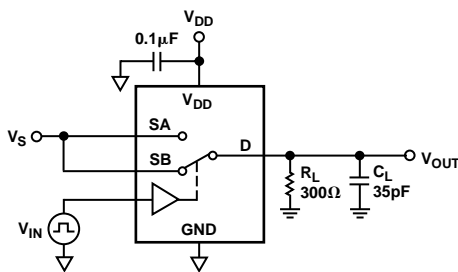
Test Circuit 2. Off Leakage



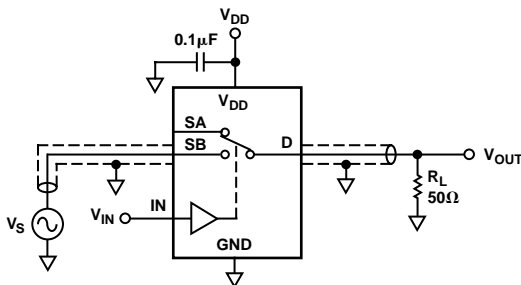
Test Circuit 3. On Leakage



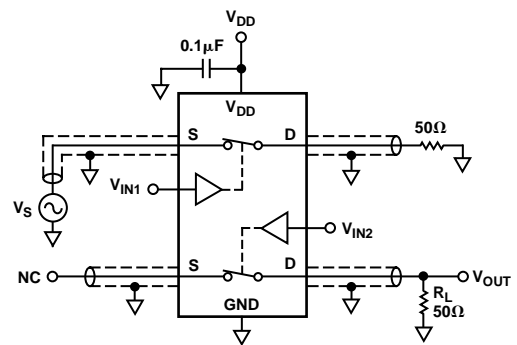
Test Circuit 4. Switching Times



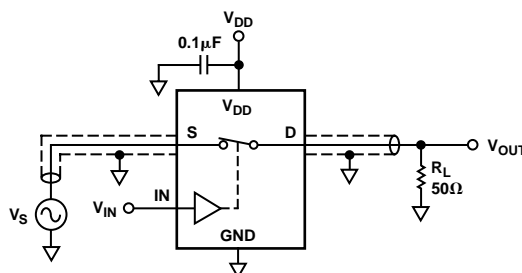
Test Circuit 5. Break-Before-Make Time Delay,  $t_D$



Test Circuit 6. Off Isolation



Test Circuit 7. Channel-to-Channel Crosstalk



Test Circuit 8. Bandwidth

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 10-Lead $\mu$ SOIC (RM-10)

