Dual High Speed PECL Comparators

Preliminary Technical Data

ADCMP561/ADCMP562

FEATURES

Differential PECL compatible outputs
1 ns propagation delay input to output
100 ps propagation delay dispersion
Input common-mode range: –2.0 V to +3.0 V
Input differential range
Robust input protection
Differential latch control
Power supply rejection greater than 70 dB
700 ps minimum pulse width
1.5 GHz equivalent input rise time bandwidth
Typical output rise/fall time of 500 ps
Programmable hysteresis

APPLICATIONS

Automatic test equipment
High speed instrumentation
Scope and logic analyzer front ends
Window comparators
High speed line receivers
Threshold detection
Peak detection
High speed triggers
Patient diagnostics
Disk drive read channel detection
Hand-held test instruments
Zero crossing detectors
Line receivers and signal restoration
Clock drivers

FUNCTIONAL BLOCK DIAGRAM

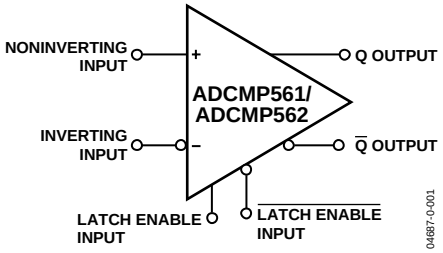

Figure 1.

GENERAL DESCRIPTION

The ADCMP561/ADCMP562 are high speed comparators fabricated on Analog Devices' proprietary XFCB process. The devices feature a 1 ns propagation delay with less than 150 ps overdrive dispersion. Dispersion, a measure of the difference in propagation delay under differing overdrive conditions, is a particularly important characteristic of high speed comparators. A separate programmable hysteresis pin is available on the ADCMP562.

A differential input stage permits consistent propagation delay with a wide variety of signals in the common-mode range from −2.0 V to +3.0 V. Outputs are complementary digital signals that are fully compatible with PECL 10 K and 10 KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50 Ω to V_{DD} − 2 V. A latch input, which is included, permits tracking, track-and-hold, or sample-and-hold modes of operation.

The ADCMP561/ADCMP562 are specified over the industrial temperature range (−40°C to +85°C). The ADCMP561 is available in a 16-lead QSOP package. The ADCMP562 is available in a 20-lead QSOP package.

Rev. PrA

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REVISION HISTORY

Revision PrA: Initial Version

SPECIFICATIONS

ADCMP561/ADCMP562 Electrical Characteristics (V_{CC} = +5.0 V, V_{EE} = −5.2 V, V_{DD} = +3.3 V, T_A = 25°C, unless otherwise noted.)

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS[1]						
Input Common-Mode Range	V_{CM}		−2.0		3.0	V
Input Differential Voltage			−5		+5	V
Input Offset Voltage	V_{OS}	−IN = 0 V, +IN = 0 V	−10.0	±3.0	+10.0	mV
Input Offset Voltage Channel Matching				±3.0		mV
Offset Voltage Tempco	DV_{OS}/d_T			10.0		µV/°C
Input Bias Current	I_{BC}	@ −IN = −2 V, +IN = +3 V	−10.0	±5	+10.0	µA
Input Bias Current Tempco				0.5		nA/°C
Input Offset Current			−3.0	±1.0	+3.0	µA
Input Capacitance	C_{IN}			1.75		pF
Input Resistance, Differential Mode				100		kΩ
Input Resistance, Common Mode				600		kΩ
Open-Loop Gain				60		dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = −2.0 V to +3.0 V		70		dB
Hysteresis				±0.5		mV
LATCH ENABLE CHARACTERISTICS						
Latch Enable Voltage Range	V_{LCM}		V_{DD} − 2.0		V_{DD}	V
Latch Enable Differential Input Voltage	V_{LD}		0.4		2.0	V
Input High Current		@ 0.0 V	−150		+150	µA
Input Low Current		@ −2.0 V	−150		+150	µA
Latch Setup Time	t_S	250 mV overdrive		500		ps
Latch to Output Delay	t_{PLOH}, t_{PLOL}	250 mV overdrive		750		ps
Latch Minimum Pulse Width	t_{PL}	250 mV overdrive		750		ps
Latch Hold Time	t_H	250 mV overdrive		500		ps
DC OUTPUT CHARACTERISTICS						
Output Voltage—High Level	V_{OH}	PECL 50 Ω to V_{DD} − 2.0 V	V_{DD} − 1.05		V_{DD} − 0.81	V
Output Voltage—Low Level	V_{OL}	PECL 50 Ω to V_{DD} − 2.0 V	V_{DD} − 1.95		V_{DD} − 1.54	V
Rise Time	t_R	10% to 90%		500		ps
Fall Time	t_F	10% to 90%		500		ps
AC PERFORMANCE						
Propagation Delay	t_{PD}	1 V overdrive		750		ps
Propagation Delay	t_{PD}	20 mV overdrive		850		ps
Propagation Delay Tempco				0.5		ps/°C
Prop Delay Skew—Rising Transition to Falling Transition				100		ps
Within Device Propagation Delay Skew—Channel-to-Channel				100		ps
Propagation Delay Dispersion vs. Duty Cycle		1 MHz, 1 ns t_R, t_F		50		ps
Propagation Delay Dispersion vs. Overdrive		50 mV to 1.5 V		100		ps
Propagation Delay Dispersion vs. Overdrive		20 mV to 100 mV		100		ps
Propagation Delay Dispersion vs. Slew Rate		0 V to 1 V swing, 20% to 80%, 600 ps and 2 ns		100		ps
Propagation Delay Dispersion vs. Common-Mode Voltage		1 V swing, $-1.5V_{CM}$ to $+2.5V_{CM}$		100		ps

[1] Under no circumstances should the input voltages exceed the supply voltages.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Equivalent Bandwidth	BW	0 V to 1 V swing, 20% to 80%, 50 ps tr, tf		1500		MHz
Toggle Rate		>50% Output Swing		650		MHz
Minimum Pulse Width	PW	Δt_{PD} from 10 ns to 750 ps		750		ps
Unit-to-Unit Propagation Delay Skew		< ±25 ps		100		ps
POWER SUPPLY						
Positive Supply Current	I_{VCC}	@ +5.0 V		3.2	5	mA
Negative Supply Current	I_{VEE}	@ −5.2 V		22	28	mA
Logic Supply Current	I_{VDD}	@ 3.3 V without load		9	13	mA
Logic Supply Current	I_{VDD}	@ 3.3 V with load		60	70	mA
Positive Supply Voltage	V_{CC}	Dual	4.75	5.0	5.25	V
Negative Supply Voltage	V_{EE}	Dual	−4.96	−5.2	−5.45	V
Logic Supply Voltage	V_{DD}	Dual	2.5	3.3	5.0	V
Power Dissipation		Dual, without load		160	190	mW
Power Dissipation		Dual, with load		220	250	mW
Power Supply Sensitivity—V_{CC}	PSS_{VCC}			68		dB
Power Supply Sensitivity—V_{EE}	PSS_{VEE}			80		dB
Power Supply Sensitivity—V_{DD}	PSS_{VDD}			70		dB
HYSTERESIS (ADCMP562 Only)						
Hysteresis			0		40	mV

ABSOLUTE MAXIMUM RATINGS

Table 2. ADCMP561/ADCMP562 Stress Ratings

Parameter	Rating
Supply Voltages	
Positive Supply Voltage (V_{CC} to GND)	−0.5 V to +6.0 V
Negative Supply Voltage (V_{EE} to GND)	−6.0 V to +0.5 V
Logic Supply Voltage (V_{DD} to GND)	−0.5 V to +6.0 V
Ground Voltage Differential	−0.5 V to +0.5 V
Input Voltages	
Input Common-Mode Voltage	−3.0 V to +4.0 V
Differential Input Voltage	−7.0 V to +7.0 V
Input Voltage, Latch Controls	−0.5 V to +5.5 V
Output	
Output Current	30 mA
Temperature	
Operating Temperature, Ambient	−40°C to +85°C
Operating Temperature, Junction	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CONSIDERATIONS

The ADCMP562 QSOP 20-lead package option has a θ_{JA} (junction-to-ambient thermal resistance) of TBD°C/W in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

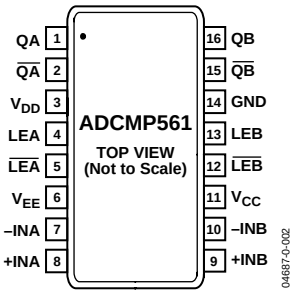

Figure 2. ADCMP561 16-Lead QSOP Pin Configuration

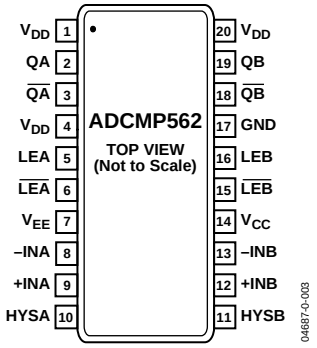

Figure 3. ADCMP562 20-Lead QSOP Pin Configuration

Pin No.			
ADCMP561	**ADCMP562**	**Mnemonic**	**Function**
	1	V_{DD}	Logic Supply Terminal.
1	2	QA	One of Two Complementary Outputs for Channel A. QA is logic high if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in the compare mode). See the description of Pin LES for more information.
2	3	$\overline{QA}$	One of Two Complementary Outputs for Channel A. $\overline{QA}$ is logic low if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in the compare mode). See the description of Pin LEA for more information.
3	4	V_{DD}	Logic Supply Terminal.
4	5	LEA	One of Two Complementary Inputs for Channel A Latch Enable. In the compare mode (logic high), the output tracks changes at the input of the comparator. In the latch mode (logic low), the output reflects the input state just prior to the comparator's being placed in the latch mode. $\overline{LEA}$ must be driven in conjunction with LEA.
5	6	$\overline{LEA}$	One of Two Complementary Inputs for Channel A Latch Enable. In the compare mode (logic low), the output tracks changes at the input of the comparator. In the latch mode (logic high), the output reflects the input state just prior to the comparator's being placed in the latch mode. LEA must be driven in conjunction with $\overline{LEA}$.
6	7	V_{EE}	Negative Supply Terminal.
7	8	–INA	Inverting Analog Input of the Differential Input Stage for Channel A. The inverting A input must be driven in conjunction with the noninverting A input.
8	9	+INA	Noninverting Analog Input of the Differential Input Stage for Channel A. The noninverting A input must be driven in conjunction with the inverting A input.
	10	HYSA	Programmable Hysteresis.
	11	HYSB	Programmable Hysteresis.
9	12	+INB	Noninverting Analog Input of the Differential Input Stage for Channel B. The noninverting B input must be driven in conjunction with the inverting B input.
10	13	–INB	Inverting Analog Input of the Differential Input Stage for Channel B. The inverting B input must be driven in conjunction with the noninverting B input.
11	14	V_{CC}	Positive Supply Terminal.
12	15	$\overline{LEB}$	One of Two Complementary Inputs for Channel B Latch Enable. In the compare mode (logic low), the output tracks changes at the input of the comparator. In the latch mode (logic high), the output reflects the input state just prior to the comparator's being placed in the latch mode. LEB must be driven in conjunction with $\overline{LEB}$.

Pin No.			
ADCMP561	**ADCMP562**	**Mnemonic**	**Function**
13	16	LEB	One of Two Complementary Inputs for Channel B Latch Enable. In the compare mode (logic high), the output tracks changes at the input of the comparator. In the latch mode (logic low), the output reflects the input state just prior to the comparator's being placed in the latch mode. $\overline{LEB}$ must be driven in conjunction with LEB.
14	17	GND	Analog Ground.
15	18	$\overline{QB}$	One of Two Complementary Inputs for Channel B. $\overline{QB}$ is logic low if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in the compare mode). See the description of PIN LEB for more information.
16	19	QB	One of Two Complementary Inputs for Channel B. QB is logic high if the analog voltage at the noninverting input is greater than the analog voltage at the inverting input (provided the comparator is in the compare mode). See the description of Pin LEB for more information.
	20	V_{DD}	Logic Supply Terminal.

TIMING INFORMATION

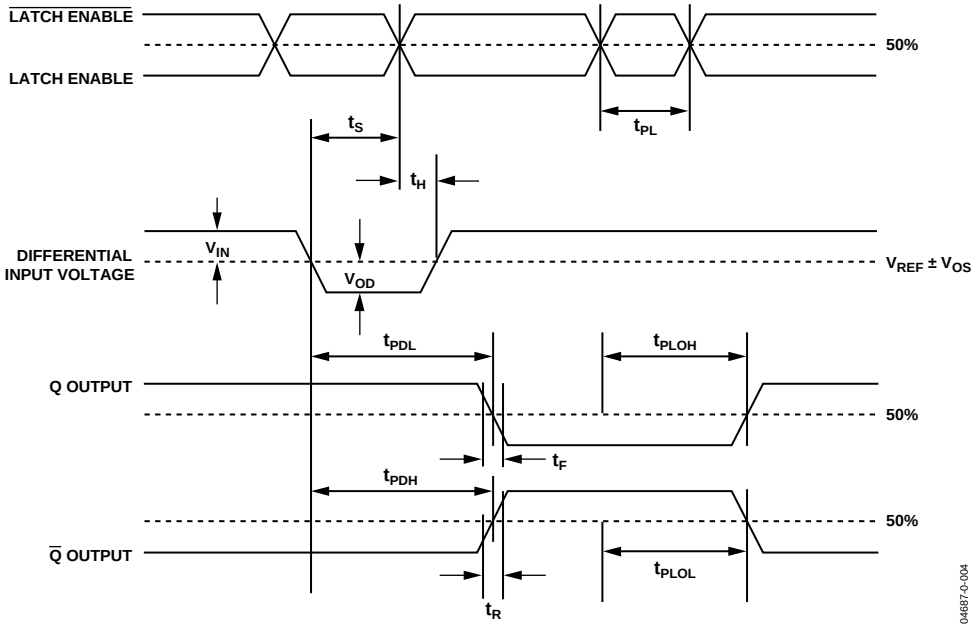

Figure 4. System Timing Diagram

Figure 4 shows the compare and latch features of the ADCMP561/ADCMP562. Table 3 describes the terms in the diagram.

Table 3. Timing Descriptions

Symbol	Timing	Description
t_{PDH}	Input to Output High Delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition
t_{PDL}	Input to Output Low Delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition
t_{PLOH}	Latch Enable to Output High Delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition
t_{PLOL}	Latch Enable to Output Low Delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition
t_H	Minimum Hold Time	Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs
t_{PL}	Minimum Latch Enable Pulse Width	Minimum time the latch enable signal must be high to acquire an input signal change
t_S	Minimum Setup Time	Minimum time before the negative transition of the latch enable signal that an input signal change must be present to be acquired and held at the outputs
t_R	Output Rise Time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points
t_F	Output Fall Time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points
V_{OD}	Voltage Overdrive	Difference between the differential input and reference input voltages

APPLICATION INFORMATION

The ADCMP561/ADCMP562 comparators are very high speed devices. Consequently, high speed design techniques must be employed to achieve the best performance. The most critical aspect of any ADCMP561/ADCMP562 design is the use of a low impedance ground plane. A ground plane, as part of a multilayer board, is recommended for proper high speed performance. Using a continuous conductive plane over the surface of the circuit board can create this, allowing breaks in the plane only for necessary signal paths. The ground plane provides a low inductance ground, eliminating any potential differences at different ground points throughout the circuit board caused by ground bounce. A proper ground plane also minimizes the effects of stray capacitance on the circuit board.

It is also important to provide bypass capacitors for the power supply in a high speed application. A 1 µF electrolytic bypass capacitor should be placed within 0.5 inches of each power supply pin to ground. These capacitors reduce any potential voltage ripples from the power supply. In addition, a 10 nF ceramic capacitor should be placed as close as possible from the power supply pins on the ADCMP561/ADCMP562 to ground. These capacitors act as a charge reservoir for the device during high frequency switching.

The LATCH ENABLE input is active low (latched). If the latching function is not used, the LATCH ENABLE input should be attached to V_{DD} (V_{DD} is a PECL logic high), and the complementary input, $\overline{\text{LATCH ENABLE}}$, should be tied to V_{DD} − 2.0 V. This disables the latching function.

Occasionally, one of the two comparator stages within the ADCMP561/ADCMP562 is not used. The inputs of the unused comparator should not be allowed to float. The high internal gain may cause the output to oscillate (possibly affecting the comparator that is being used) unless the output is forced into a fixed state. This is easily accomplished by ensuring that the two inputs are at least one diode drop apart, while also appropriately connecting the LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ inputs as described above.

The best performance is achieved with the use of proper PECL terminations. The open emitter outputs of the ADCMP561/ADCMP562 are designed to be terminated through 50 Ω resistors to V_{DD} − 2.0 V, or any other equivalent PECL termination. If high speed PECL signals must be routed more than a centimeter, microstrip or stripline techniques may be required to ensure proper transition times and prevent output ringing.

CLOCK TIMING RECOVERY

Comparators are often used in digital systems to recover clock timing signals. High speed square waves transmitted over a distance, even tens of centimeters, can become distorted due to stray capacitance and inductance. Poor layout or improper termination can also cause reflections on the transmission line, further distorting the signal waveform. A high speed comparator can be used to recover the distorted waveform while maintaining a minimum of delay.

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator amplifier, proper design and layout techniques should be used to ensure optimal performance from the ADCMP561/ADCMP562. The performance limits of high speed circuitry can easily be a result of stray capacitance, improper ground impedance, or other layout issues.

Minimizing resistance from source to the input is an important consideration in maximizing the high speed operation of the ADCMP561/ADCMP562. Source resistance in combination with equivalent input capacitance could cause a lagged response at the input, thus delaying the output. The input capacitance of the ADCMP561/ADCMP562, in combination with stray capacitance from an input pin to ground, could result in several picofarads of equivalent capacitance. A combination of 3 kΩ source resistance and 5 pF of input capacitance yields a time constant of 15 ns, which is significantly slower than the 750 ps capability of the ADCMP561/ADCMP562. Source impedances should be significantly less than 100 Ω for best performance.

Sockets should be avoided due to stray capacitance and inductance. If proper high speed techniques are used, the ADCMP561/ADCMP562 should be free from oscillation when the comparator input signal passes through the switching threshold.

COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP561/ADCMP562 has been specifically designed to reduce propagation delay dispersion over an input overdrive range of 100 mV to 1 V. Propagation delay overdrive dispersion is the change in propagation delay that results from a change in the degree of overdrive (how far the switching point is exceeded by the input). The overall result is a higher degree of timing accuracy since the ADCMP561/ADCMP562 is far less sensitive to input variations than most comparator designs.

Propagation delay dispersion is a specification that is important in critical timing applications such as ATE, bench instruments, and nuclear instrumentation. Overdrive dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed (Figure 5). For the ADCMP561/ADCMP562, overdrive dispersion is typically 100 ps as the overdrive is changed from 100 mV to 1 V. This specification applies for both positive and negative overdrive since the ADCMP561/ADCMP562 has equal delays for positive and negative going inputs.

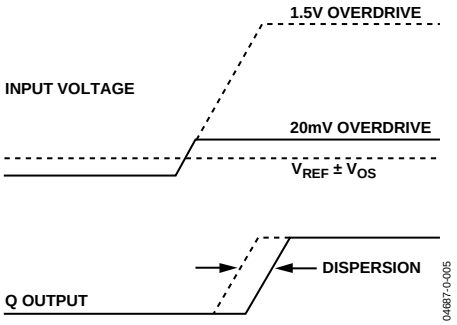

Figure 5. Propagation Delay Dispersion

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often useful in a noisy environment, or where it is not desirable for the comparator to toggle between states when the input signal is at the switching threshold. The transfer function for a comparator with hysteresis is shown in Figure 6. If the input voltage approaches the threshold from the negative direction, the comparator switches from a 0 to a 1 when the input crosses $+V_H/2$. The new switching threshold becomes $-V_H/2$. The comparator remains in a 1 state until the threshold $-V_H/2$ is crossed coming from the positive direction. In this manner, noise centered on 0 V input does not cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

Positive feedback from the output to the input is often used to produce hysteresis in a comparator (Figure 10). The major problem with this approach is that the amount of hysteresis varies with the output logic levels, resulting in a hysteresis that is not symmetrical around zero.

In the ADCMP562, hysteresis is generated through the programmable hysteresis pin. A resistor from the HYS pin to GND creates a current into the part that is used to generate hysteresis. Hysteresis generated in this manner is independent of output swing and is symmetrical around the trip point. The hysteresis versus resistance curve is shown in Figure 7.

Another method to implement hysteresis is generated by introducing a differential voltage between the LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ inputs (Figure 11).

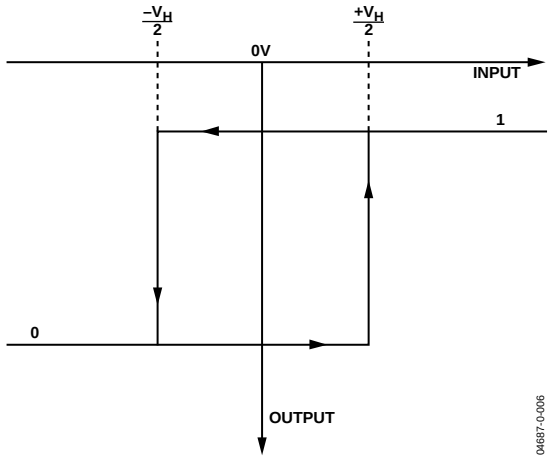

Figure 6. Comparator Hysteresis Transfer Function

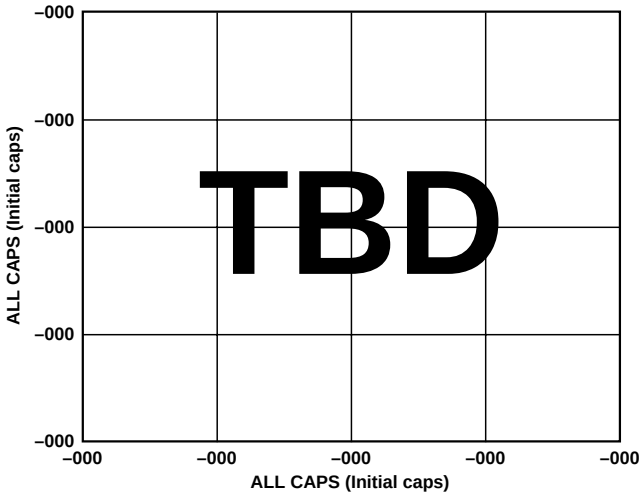

Figure 7. Comparator Hysteresis Transfer Function

MINIMUM INPUT SLEW RATE REQUIREMENT

As for all high speed comparators, a minimum slew rate must be met to ensure that the device does not oscillate when the input crosses the threshold. This oscillation is due in part to the high input bandwidth of the comparator and the parasitics of the package. Analog Devices recommends a slew rate of 1 V/µs or faster to ensure a clean output transition. If slew rates less than 1 V/µs are used, hysteresis should be added to reduce the oscillation.

TYPICAL APPLICATION CIRCUITS

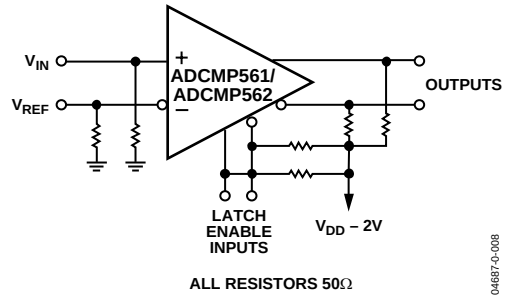

Figure 8. High Speed Sampling Circuits

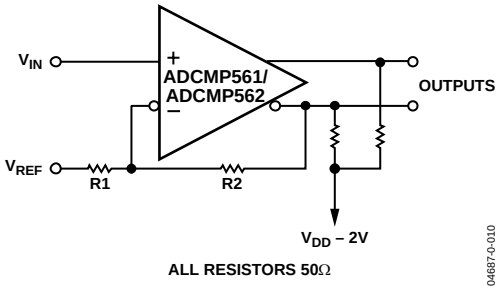

Figure 10. Hysteresis Using Positive Feedback

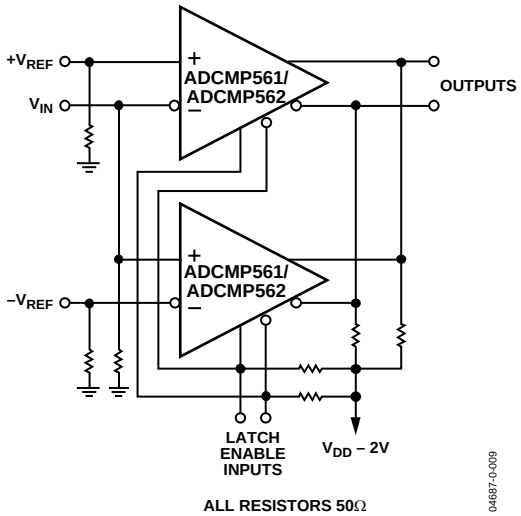

Figure 9. High Speed Window Comparator

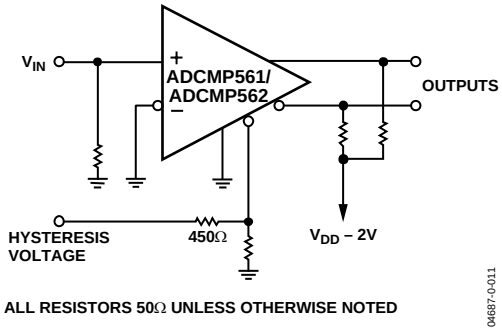

Figure 11. Hysteresis Using Latch Enable Input

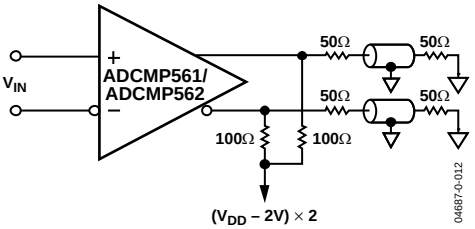

Figure 12. How to Interface a PECL Output to an Instrument with a 50 Ω to Ground Input

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = +5.0 V, V_{EE} = −5.2 V, V_{DD} = +3.3 V, T_A = 25°C, unless otherwise noted.

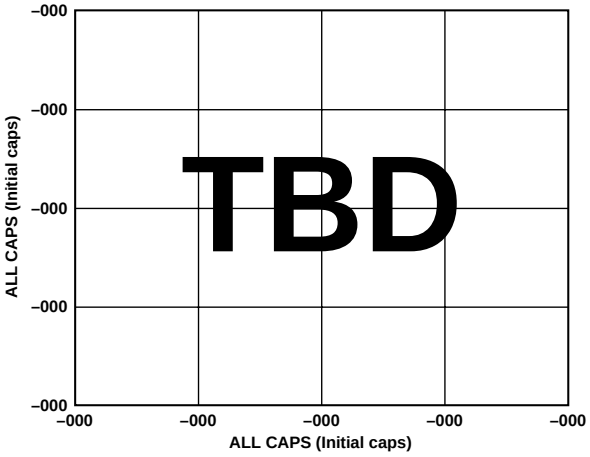

Figure 13. Input Bias Current vs. Input Voltage

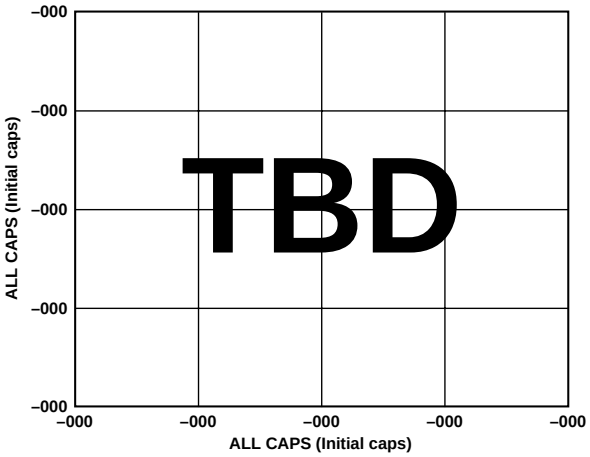

Figure 14. Input Offset Voltage vs. Temperature

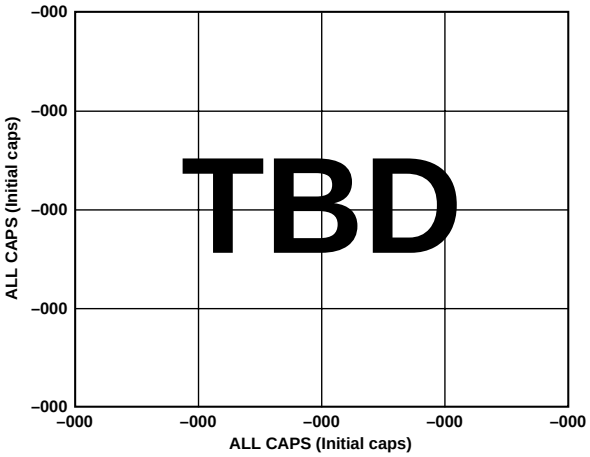

Figure 15. Rise Time vs. Temperature

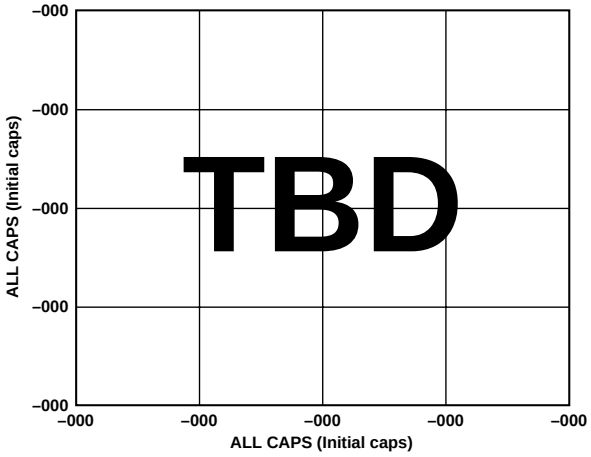

Figure 16. Input Bias Current vs. Temperature

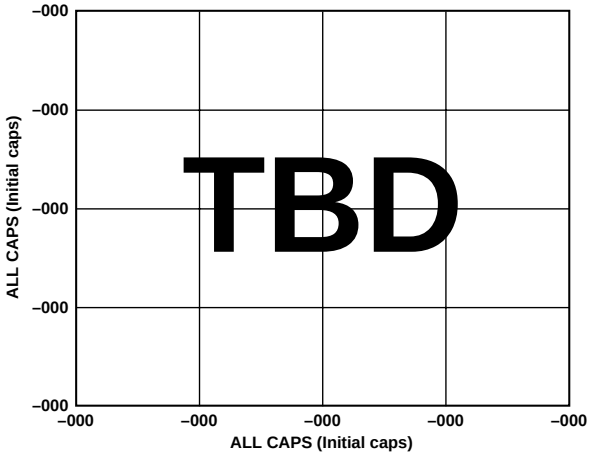

Figure 17. Hysteresis vs. ΔLatch

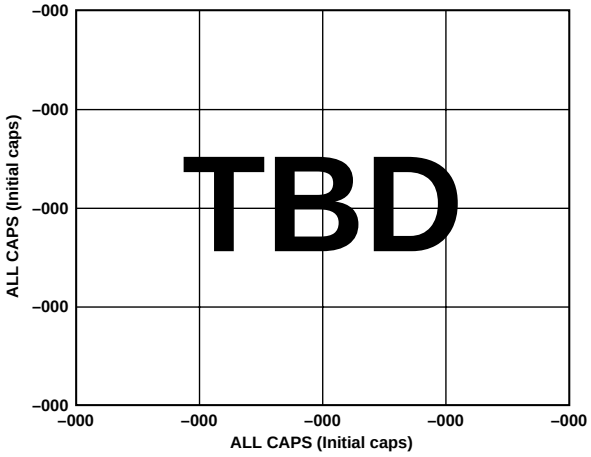

Figure 18. Fall Time vs. Temperature

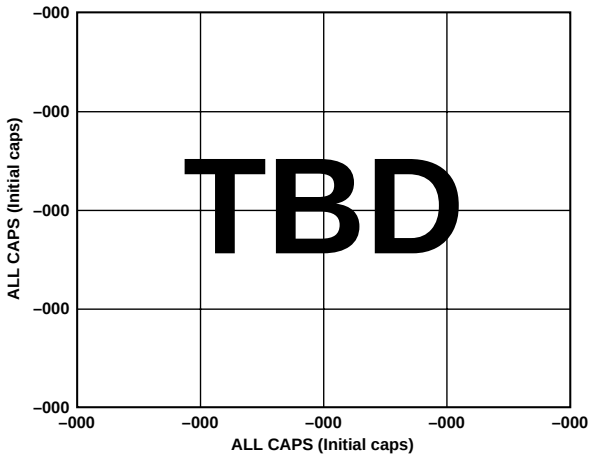

Figure 19. Propagation Delay vs. Temperature

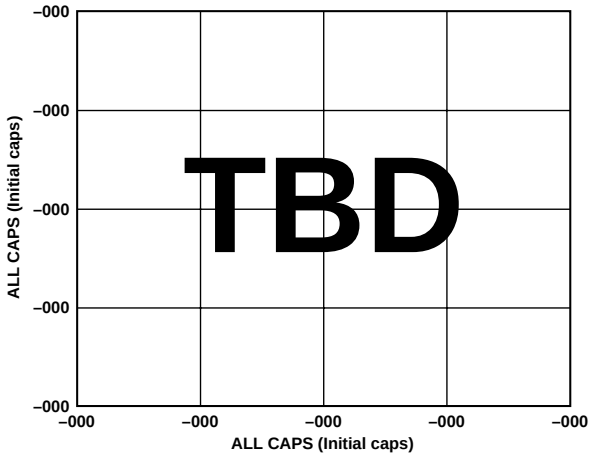

Figure 20. Propagation Delay vs. Overdrive Voltage

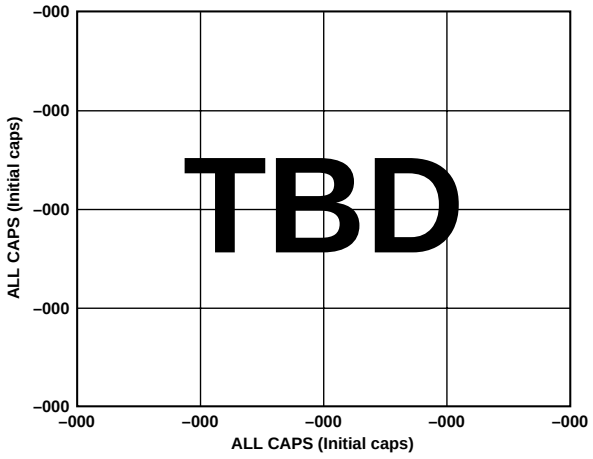

Figure 21. Rise and Fall of Outputs vs. Time

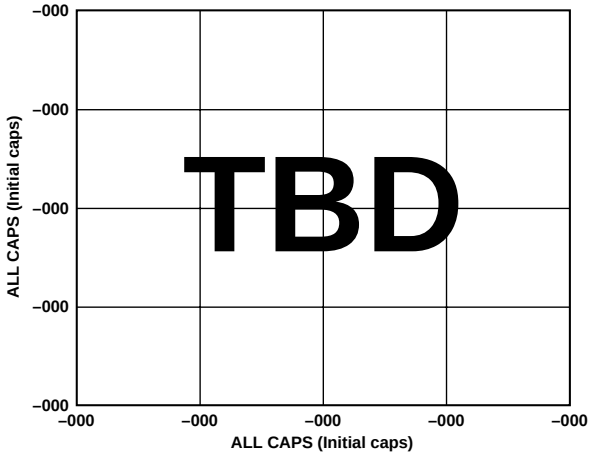

Figure 22. Propagation Delay vs. Common-Mode Voltage

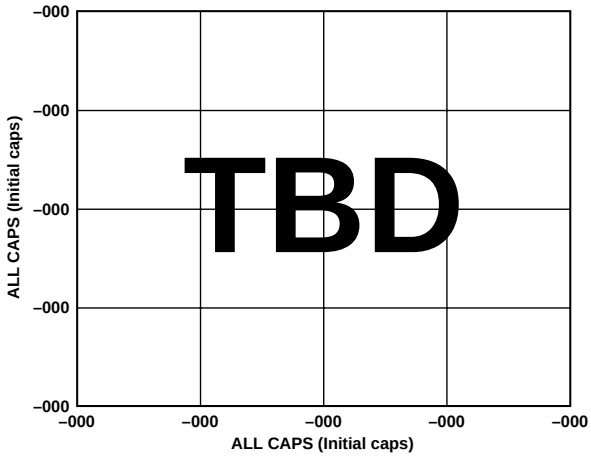

Figure 23. Propagation Delay Error vs. Pulse Width

OUTLINE DIMENSIONS

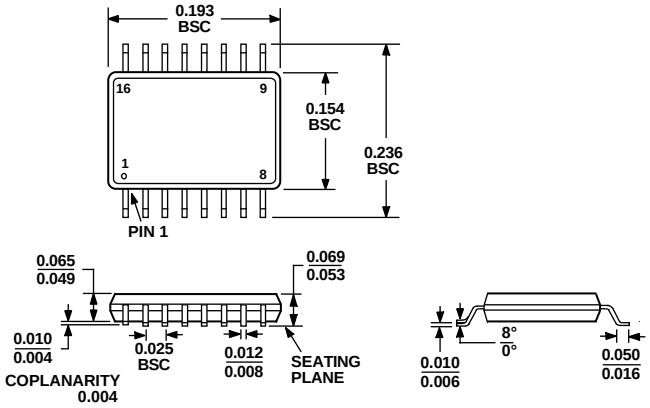

Figure 24. 16-Lead Shrink Small Outline Package[QSOP]
(RQ-16)
Dimensions shown in inches

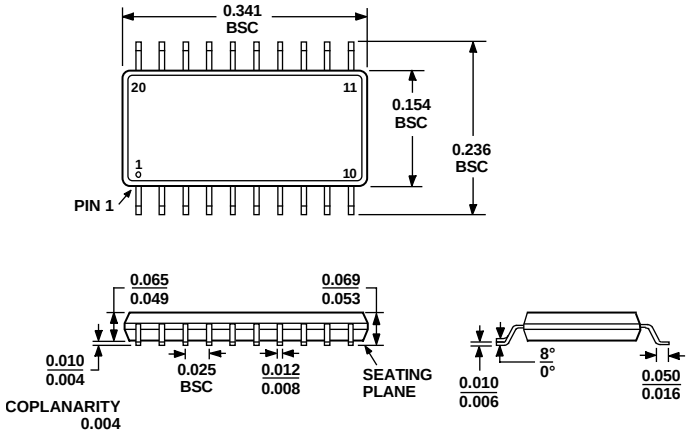

Figure 25. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADCMP561BRQ	–40°C to +85°C	16-Lead QSOP	RQ-16
ADCMP562BRQ	–40°C to +85°C	20-Lead QSOP	RQ-20

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