

AD8057/AD8058

FEATURES

Low Cost Single (AD8057) and Dual (AD8058)

High Speed

325 MHz, -3 dB Bandwidth (G = +1)

1000 V/ μ s Slew Rate

Gain Flatness 0.1 dB to 28 MHz

Low Noise

7 nV/ $\sqrt{\text{Hz}}$

Low Power

5.4 mA/Amplifier Typical Supply Current @ +5 V

Low Distortion

-85 dBc @ 5 MHz, $R_L = 1 \text{ k}\Omega$

Wide Supply Range from 3 V to 12 V

Small Packaging

AD8057 Available in SOIC-8 and SOT-23-5

AD8058 Available in SOIC-8 and μ SOIC

APPLICATIONS

Imaging

DVD/CD

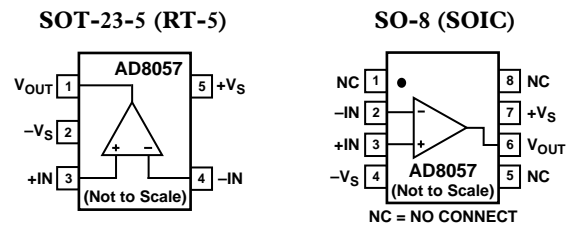
Photodiode Preamp

A-to-D Driver

Professional Cameras

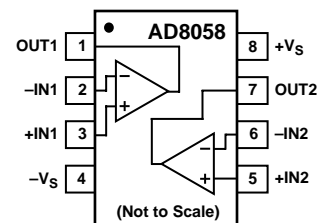
Filters

CONNECTION DIAGRAMS (TOP VIEWS)



RM-8 (μ SOIC)

SO-8 (SOIC)



PRODUCT DESCRIPTION

The AD8057 (single) and AD8058 (dual) are very high performance amplifiers with a very low cost. The balance between cost and performance make them ideal for many applications. The AD8057 and AD8058 will reduce the need to qualify a variety of specialty amplifiers.

The AD8057 and AD8058 are voltage feedback amplifiers with the bandwidth and slew rate normally found in current feedback amplifiers. The AD8057 and AD8058 are low power amplifiers having low quiescent current and a wide supply range from 3 V to 12 V. They have noise and distortion performance required for high-end video systems as well as dc performance parameters rarely found in high speed amplifiers.

The AD8057 and AD8058 are available in standard SOIC packaging as well as tiny SOT-23-5 (AD8057) and μ SOIC (AD8058). These amplifiers are available in the industrial temperature range of -40°C to +85°C.

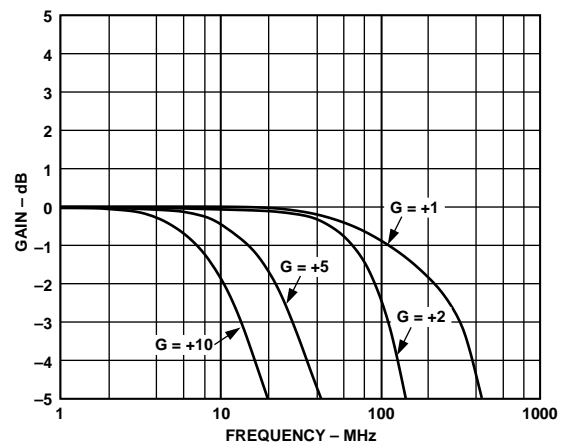


Figure 1. Small Signal Frequency Response

REV. A

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AD8057/AD8058—SPECIFICATIONS (@ $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{ V}$, $R_L = 100\ \Omega$, $R_F = 0\ \Omega$, Gain = +1, unless otherwise noted)

Parameter	Conditions	AD8057/AD8058			Units
		Min	Typ	Max	
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	$G = +1$, $V_O = 0.2\text{ V p-p}$		325		MHz
	$G = -1$, $V_O = 0.2\text{ V p-p}$		95		MHz
	$G = +1$, $V_O = 2\text{ V p-p}$		175		MHz
Bandwidth for 0.1 dB Flatness	$G = +1$, $V_O = 0.2\text{ V p-p}$		30		MHz
Slew Rate	$G = +1$, $V_O = 2\text{ V Step}$, $R_L = 2\text{ k}\Omega$		850		V/ μs
	$G = +1$, $V_O = 4\text{ V Step}$, $R_L = 2\text{ k}\Omega$		1150		V/ μs
Settling Time to 0.1%	$G = +2$, $V_O = 2\text{ V Step}$		30		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	$f_C = 5\text{ MHz}$, $V_O = 2\text{ V p-p}$, $R_L = 1\text{ k}\Omega$		-85		dBc
	$f_C = 20\text{ MHz}$, $V_O = 2\text{ V p-p}$, $R_L = 1\text{ k}\Omega$		-62		dBc
SFDR	$f = 5\text{ MHz}$, $V_O = 2\text{ V p-p}$, $R_L = 150\ \Omega$		-68		dB
Third Order Intercept	$f = 5\text{ MHz}$, $V_O = \pm 2.0\text{ V p-p}$		-35		dBm
Crosstalk, Output to Output	$f = 5\text{ MHz}$, $G = +2$		-60		dB
Input Voltage Noise	$f = 100\text{ kHz}$		7		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		0.7		pA/ $\sqrt{\text{Hz}}$
Differential Gain Error	NTSC, $G = +2$, $R_L = 150\ \Omega$		0.01		%
	NTSC, $G = +2$, $R_L = 1\text{ k}\Omega$		0.02		%
Differential Phase Error	NTSC, $G = +2$, $R_L = 150\ \Omega$		0.15		Degree
	NTSC, $G = +2$, $R_L = 1\text{ k}\Omega$		0.01		Degree
Overload Recovery	$V_{IN} = 200\text{ mV p-p}$, $G = +1$		30		ns
DC PERFORMANCE					
Input Offset Voltage			1	5	mV
	$T_{MIN} - T_{MAX}$		2.5		mV
Input Offset Voltage Drift			3		$\mu\text{V}/^\circ\text{C}$
Input Bias Current			0.5	2.5	μA
	$T_{MIN} - T_{MAX}$		3.0		μA
Input Offset Current				0.75	$\pm\mu\text{A}$
Open-Loop Gain	$V_O = \pm 2.5\text{ V}$, $R_L = 2\text{ k}\Omega$	50	55		dB
	$V_O = \pm 2.5\text{ V}$, $R_L = 150\ \Omega$	50	52		dB
INPUT CHARACTERISTICS					
Input Resistance			10		M Ω
Input Capacitance	+Input		2		pF
Input Common-Mode Voltage Range	$R_L = 1\text{ k}\Omega$	-4.0		+4.0	$\pm\text{V}$
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5\text{ V}$	48	60		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	$R_L = 2\text{ k}\Omega$	-4.0		+4.0	$\pm\text{V}$
	$R_L = 150\ \Omega$		± 3.9		$\pm\text{V}$
Capacitive Load Drive	30% Overshoot		30		pF
POWER SUPPLY					
Operating Range		± 1.5	± 6.0	± 2.5	V
Quiescent Current for AD8057			6.0	7.5	mA
Quiescent Current for AD8058			14.0	15	mA
Power Supply Rejection Ratio	$V_S = \pm 5\text{ V to } \pm 1.5\text{ V}$	54	59		dB

Specifications subject to change without notice.

SPECIFICATIONS

(@ $T_A = +25^\circ\text{C}$, $V_S = +5\text{ V}$, $R_L = 100\ \Omega$, $R_F = 0\ \Omega$, Gain = +1, unless otherwise noted)

Parameter	Conditions	AD8057/AD8058			Units
		Min	Typ	Max	
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	$G = +1$, $V_O = 0.2\text{ V p-p}$		300		MHz
	$G = +1$, $V_O = 2\text{ V p-p}$		155		MHz
Bandwidth for 0.1 dB Flatness	$V_O = 0.2\text{ V p-p}$		28		MHz
Slew Rate	$G = +1$, $V_O = 2\text{ V Step}$, $R_L = 2\text{ k}\Omega$		700		V/ μs
Settling Time to 0.1%	$G = +2$, $V_O = 2\text{ V Step}$		35		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	$f_C = 5\text{ MHz}$, $V_O = 2\text{ V p-p}$, $R_L = 1\text{ k}\Omega$		-75		dBc
	$f_C = 20\text{ MHz}$, $V_O = 2\text{ V p-p}$, $R_L = 1\text{ k}\Omega$		-54		dBc
Crosstalk, Output to Output	$f = 5\text{ MHz}$, $G = +2$		-60		dB
Input Voltage Noise	$f = 100\text{ kHz}$		7		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		0.7		pA/ $\sqrt{\text{Hz}}$
Differential Gain Error	NTSC, $G = +2$, $R_L = 150\ \Omega$		0.05		%
	NTSC, $G = +2$, $R_L = 1\text{ k}\Omega$		0.05		%
Differential Phase Error	NTSC, $G = +2$, $R_L = 150\ \Omega$		0.10		Degree
	NTSC, $G = +2$, $R_L = 1\text{ k}\Omega$		0.02		Degree
DC PERFORMANCE					
Input Offset Voltage			1	5	mV
	$T_{\text{MIN}}-T_{\text{MAX}}$		2.5		mV
Input Offset Voltage Drift			3		$\mu\text{V}/^\circ\text{C}$
Input Bias Current			0.5	2.5	μA
	$T_{\text{MIN}}-T_{\text{MAX}}$		3.0		μA
Input Offset Current				0.75	μA
Open-Loop Gain	$V_O = \pm 1.25\text{ V}$, $R_L = 2\text{ k}\Omega$	50	55		dB
	$V_O = \pm 1.25\text{ V}$, $R_L = 150\ \Omega$	45	52		dB
INPUT CHARACTERISTICS					
Input Resistance			10		M Ω
Input Capacitance	+Input		2		pF
Input Common-Mode Voltage Range	$R_L = 1\text{ k}\Omega$		0.9 to 3.4		$\pm\text{V}$
Common-Mode Rejection Ratio	$V_{\text{CM}} = \pm 2.5\text{ V}$	48	60		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	$R_L = 2\text{ k}\Omega$		0.9 to 4.1		V
	$R_L = 150\ \Omega$		1.2 to 3.8		V
Capacitive Load Drive	30% Overshoot		30		pF
POWER SUPPLY					
Operating Range		3.0	6.0	10.0	V
Quiescent Current for AD8057			5.4	7.0	mA
Quiescent Current for AD8058			13.5	14	mA
Power Supply Rejection Ratio	$V_S = \pm 2.5\text{ V to } \pm 1.5\text{ V}$	54	58		dB

Specifications subject to change without notice.

AD8057/AD8058

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	12.6 V
Internal Power Dissipation ²	
Small Outline Package (R)	0.8 W
SOT-23-5 Package	0.5 W
μ SOIC Package	0.6 W
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	± 4.0 V
Output Short Circuit Duration	Observe Power Derating Curves
Storage Temperature Range (R)	-65°C to +125°C
Operating Temperature Range (A Grade)	-40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	+300°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Specification is for device in free air:
 8-Lead SOIC Package: $\theta_{JA} = 160^\circ\text{C}/\text{W}$
 5-Lead SOT-23-5 Package: $\theta_{JA} = 240^\circ\text{C}/\text{W}$
 8-Lead μ SOIC Package: $\theta_{JA} = 200^\circ\text{C}/\text{W}$

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8057/AD8058 is limited by the associated rise in junction temperature. Exceeding a junction temperature of +175°C for an extended period can result in device failure. While the AD8057/AD8058 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions.

To ensure proper operation, it is necessary to observe the maximum power derating curves.

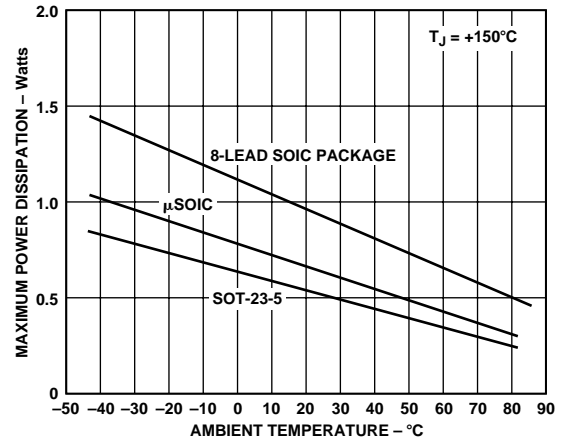


Figure 2. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Options	Brand Code
AD8057AR	-40°C to +85°C	8-Lead Narrow Body SOIC Die	SO-8 Waffle Pak	Standard N/A
AD8057ACHIPS	-40°C to +85°C	8-Lead SOIC, 13" Reel	SO-8	Standard
AD8057AR-REEL	-40°C to +85°C	8-Lead SOIC, 7" Reel	SO-8	Standard
AD8057ART-REEL	-40°C to +85°C	5-Lead SOT-23, 13" Reel	RT-5	H7A
AD8057ART-REEL7	-40°C to +85°C	5-Lead SOT-23, 7" Reel	RT-5	H7A
AD8058AR	-40°C to +85°C	8-Lead Narrow Body SOIC Die	SO-8 Waffle Pak	Standard N/A
AD8058ACHIPS	-40°C to +85°C	8-Lead SOIC, 13" Reel	SO-8	Standard
AD8058AR-REEL	-40°C to +85°C	8-Lead SOIC, 7" Reel	SO-8	Standard
AD8058ARM	-40°C to +85°C	8-Lead μ SOIC	RM-8	H8A
AD8058ARM-REEL	-40°C to +85°C	8-Lead μ SOIC, 13" Reel	RM-8	H8A
AD8058ARM-REEL7	-40°C to +85°C	8-Lead μ SOIC, 7" Reel	RM-8	H8A

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8057/AD8058 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Typical Performance Characteristics—AD8057/AD8058

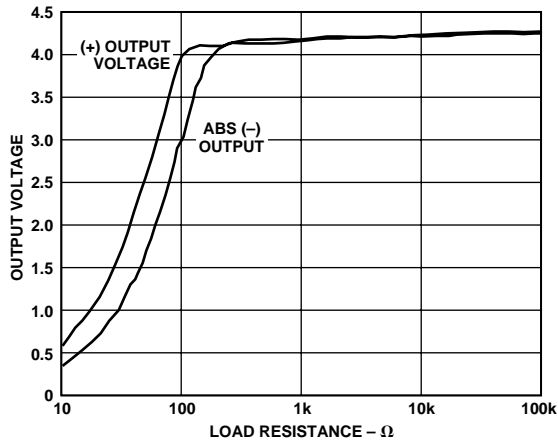


Figure 3. Output Swing vs. Load Resistance

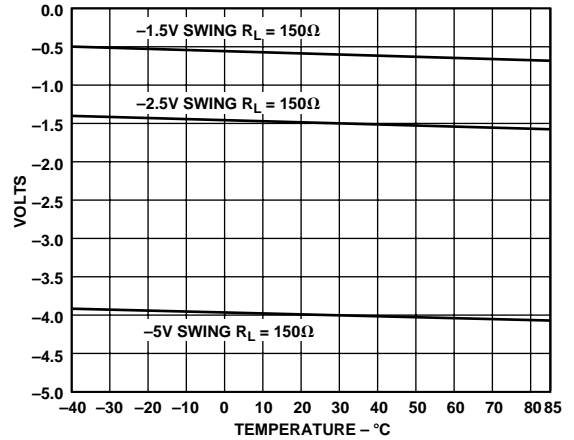


Figure 6. Negative Output Voltage Swing vs. Temperature

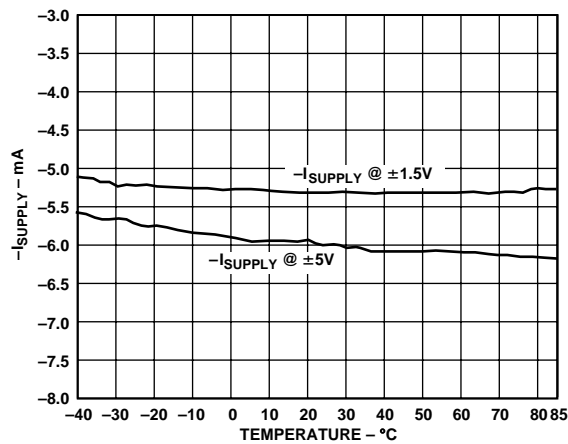


Figure 4. $-I_{SUPPLY}$ vs. Temperature

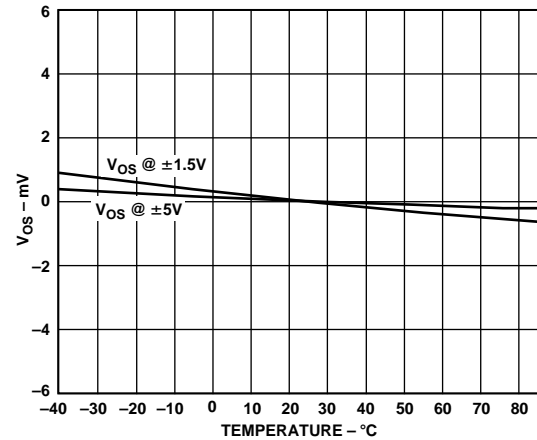


Figure 7. V_{OS} vs. Temperature

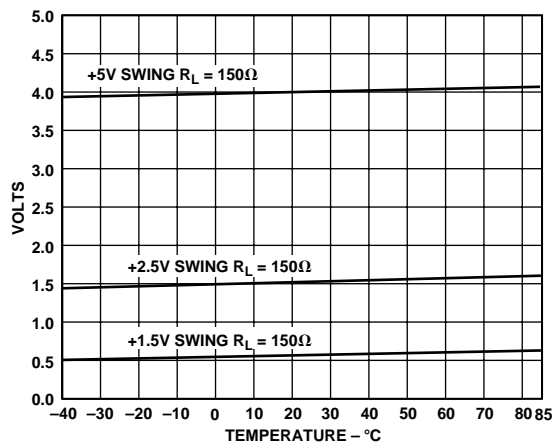


Figure 5. Positive Output Voltage Swing vs. Temperature

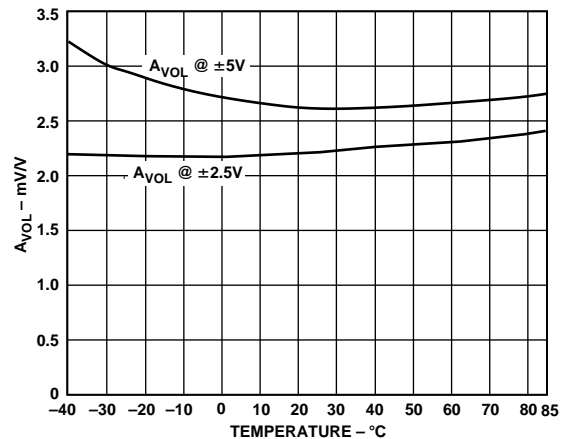


Figure 8. Open-Loop Gain vs. Temperature

AD8057/AD8058 – Typical Performance Characteristics

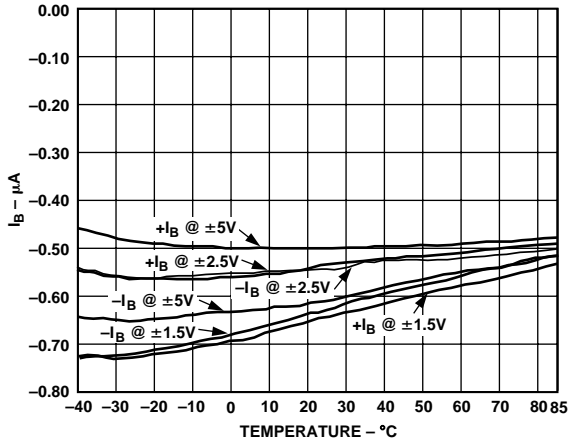


Figure 9. Input Bias Current vs. Temperature

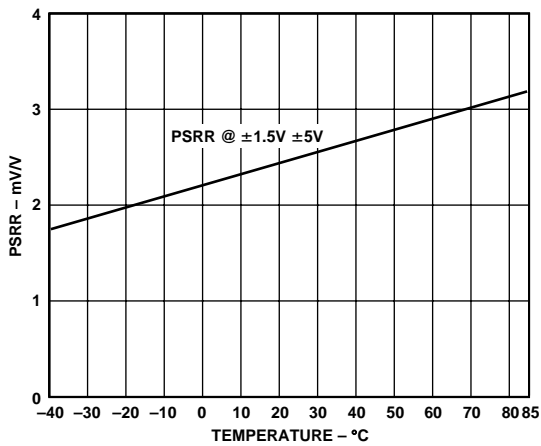


Figure 10. PSRR vs. Temperature

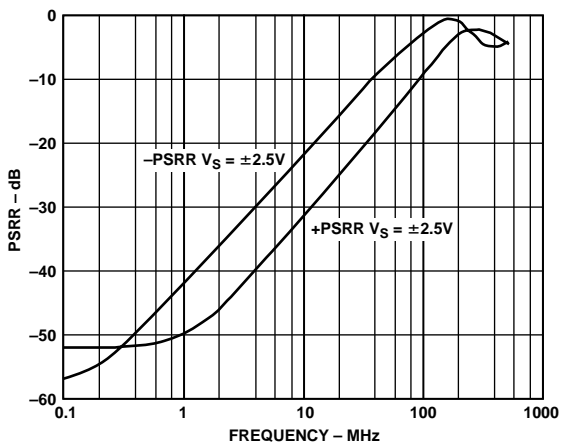


Figure 11. \pm PSRR vs. Frequency

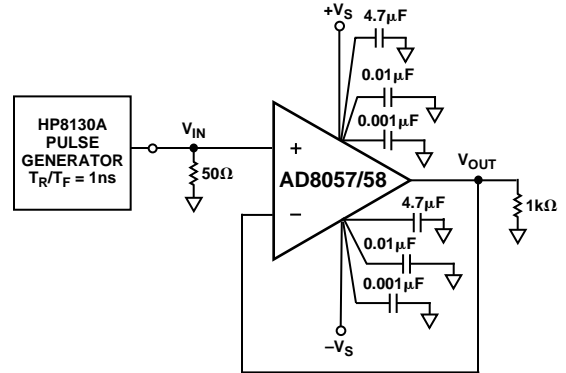


Figure 12. Test Circuit $G = +1$, $R_L = 1 \text{ k}\Omega$ for Figures 13 and 14

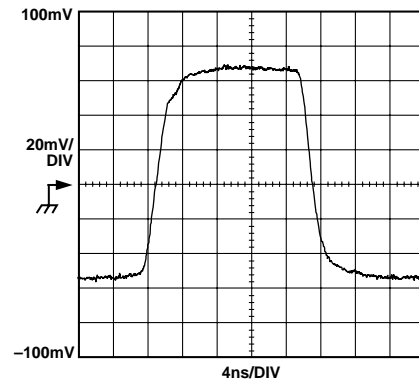


Figure 13. Small Signal Step Response $G = +1$, $R_L = 1 \text{ k}\Omega$, $V_S = \pm 5 \text{ V}$

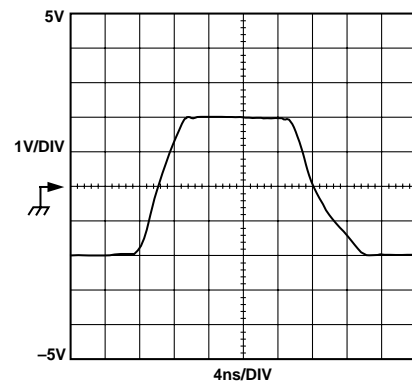


Figure 14. Large Signal Step Response $G = +1$, $R_L = 1 \text{ k}\Omega$, $V_S = \pm 5.0 \text{ V}$

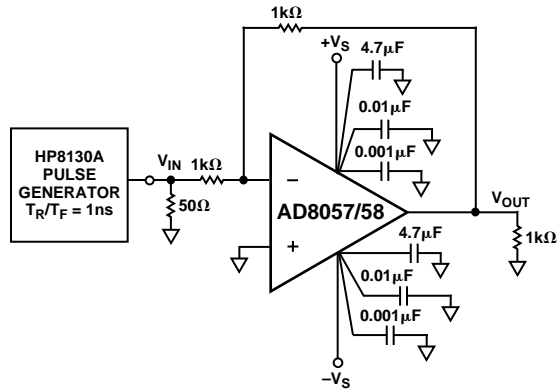


Figure 15. Test Circuit $G = -1$, $R_L = 1\text{ k}\Omega$ for Figures 16 and 17

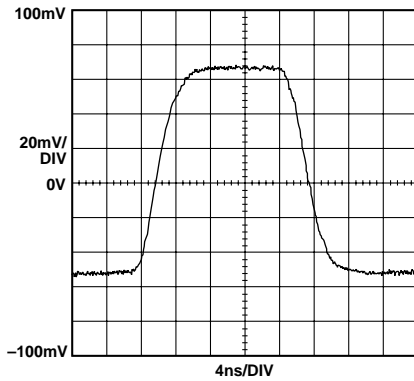


Figure 16. Small Signal Step Response $G = -1$, $R_L = 1\text{ k}\Omega$

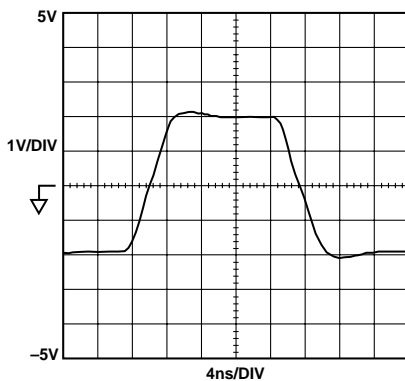


Figure 17. Large Signal Step Response $G = -1$, $R_L = 1\text{ k}\Omega$

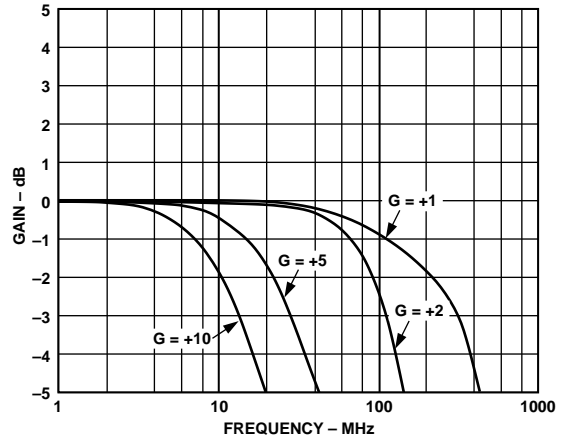


Figure 18. Small Signal Frequency Response, $V_{OUT} = 0.2\text{ V p-p}$

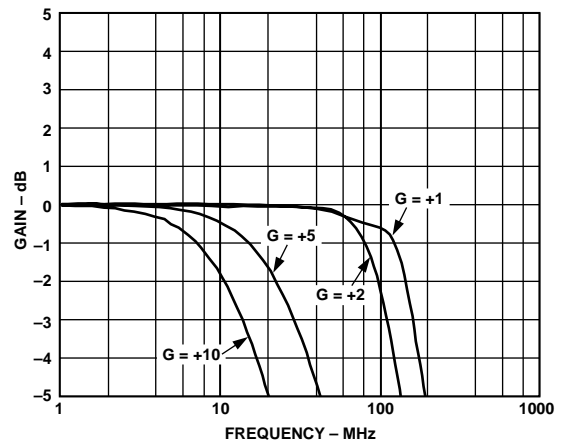


Figure 19. Large Signal Frequency Response, $V_{OUT} = 2\text{ V p-p}$

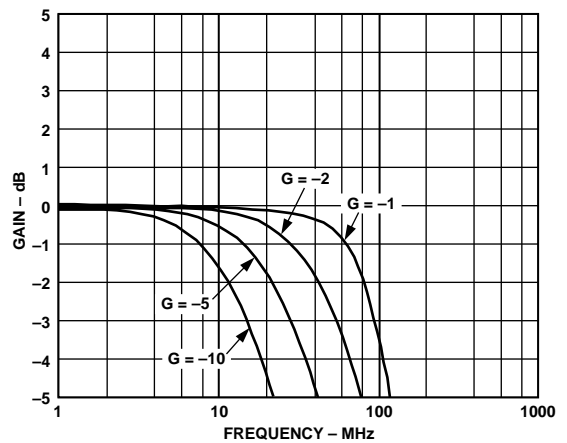


Figure 20. Large Signal Frequency Response

AD8057/AD8058

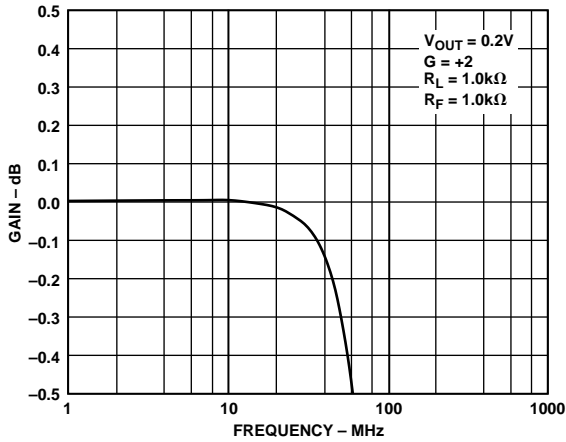


Figure 21. 0.1 dB Flatness $G = +2$

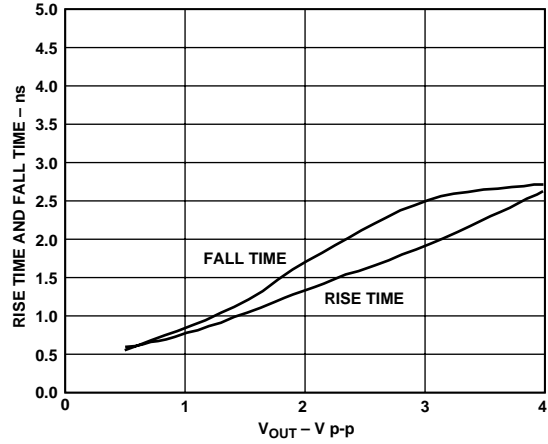


Figure 24. Rise Time and Fall Time vs. V_{OUT} . $G = +1$, $R_L = 1\text{ k}\Omega$, $R_F = 0\ \Omega$

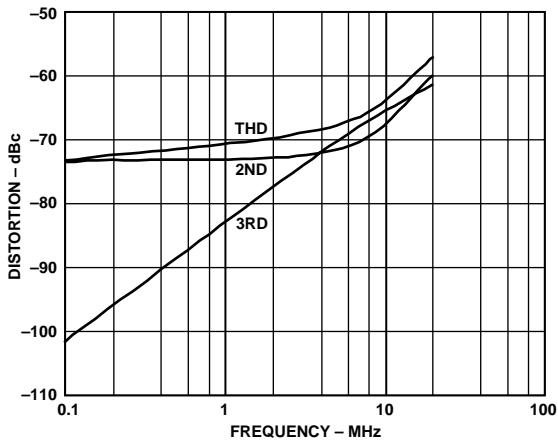


Figure 22. Distortion vs. Frequency, $R_L = 150\ \Omega$

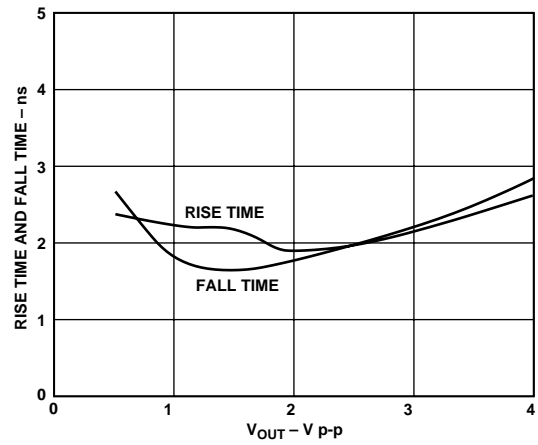


Figure 25. Rise Time and Fall Time vs. V_{OUT} . $G = +2$, $R_L = 100\ \Omega$, $R_F = 402\ \Omega$

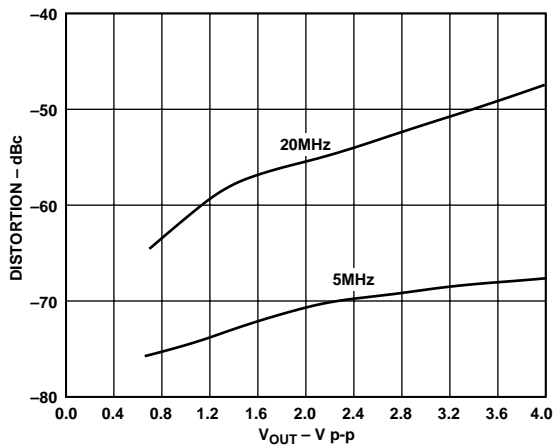


Figure 23. Distortion vs. V_{OUT} @ 20 MHz, 5 MHz, $R_L = 150\ \Omega$, $V_S = \pm 5.0\text{ V}$

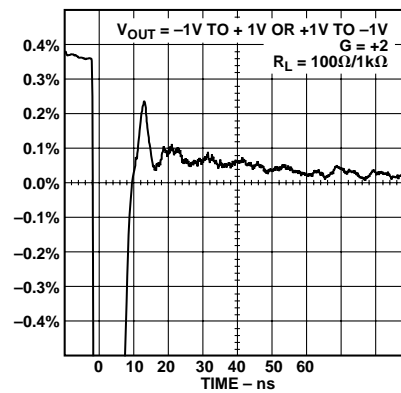


Figure 26. Settling Time

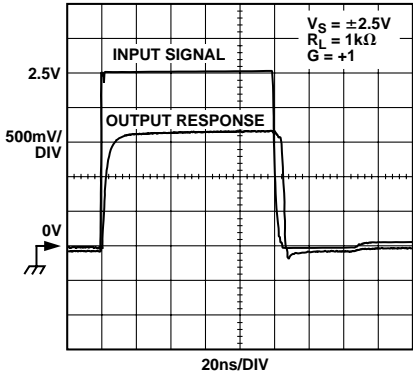


Figure 27. Input Overload Recovery, $V_S = \pm 2.5\text{ V}$

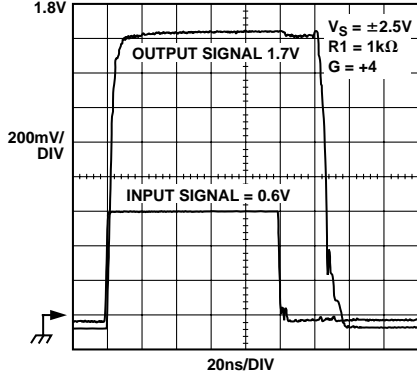


Figure 30. Output Overload Recovery, $V_S = \pm 2.5\text{ V}$

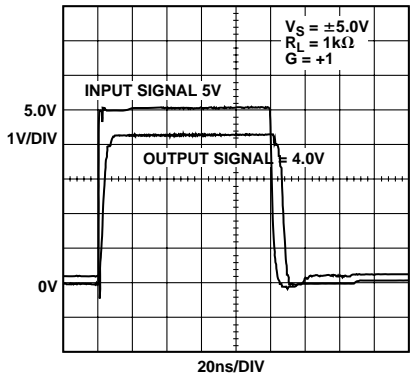


Figure 28. Output Overload Recovery, $V_S = \pm 5.0\text{ V}$

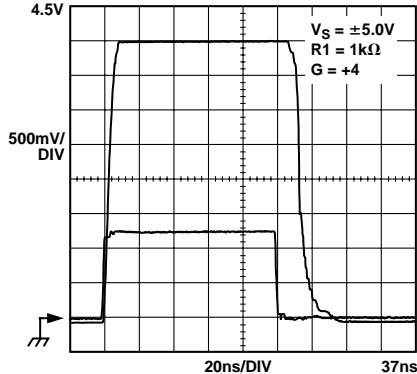


Figure 31. Output Overload Recovery, $V_S = \pm 5.0\text{ V}$

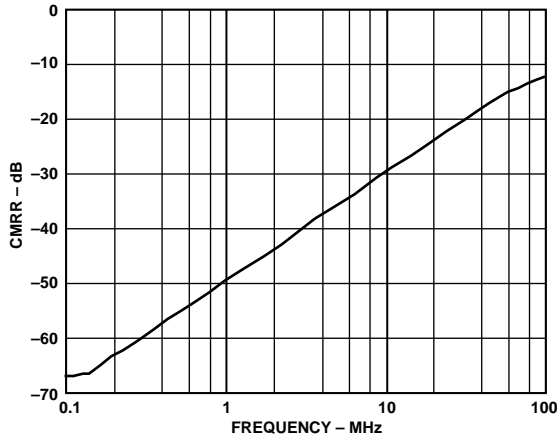


Figure 29. CMRR vs. Frequency

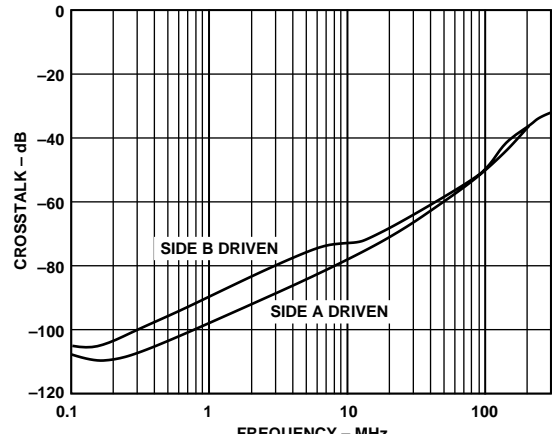
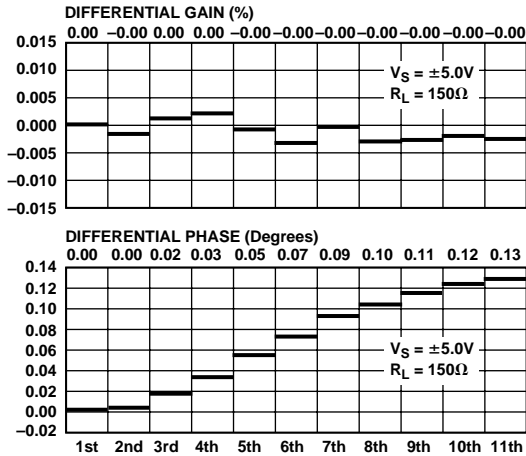
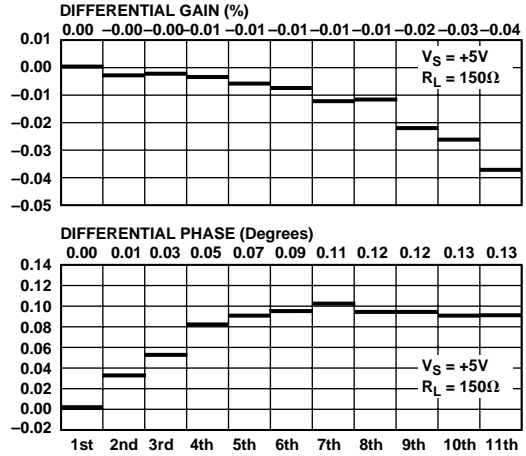


Figure 32. Crosstalk (Output-to-Output) vs. Frequency

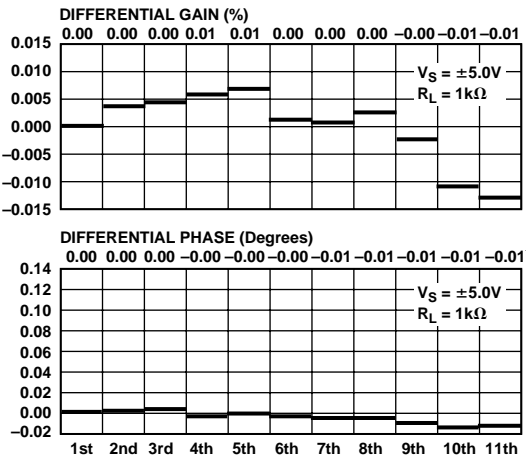
AD8057/AD8058



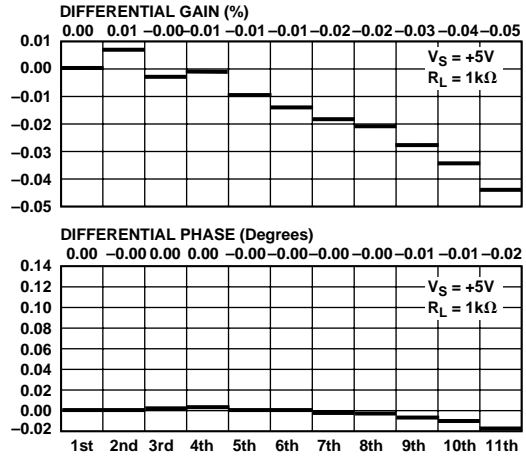
a.



a.



b.



b.

Figure 33. Differential Gain and Differential Phase One Back Terminated Load (150 Ω) (Video Op Amps Only)

Figure 35. Differential Gain and Differential Phase
a. $R_L = 150\Omega$, b. $R_L = 1k\Omega$

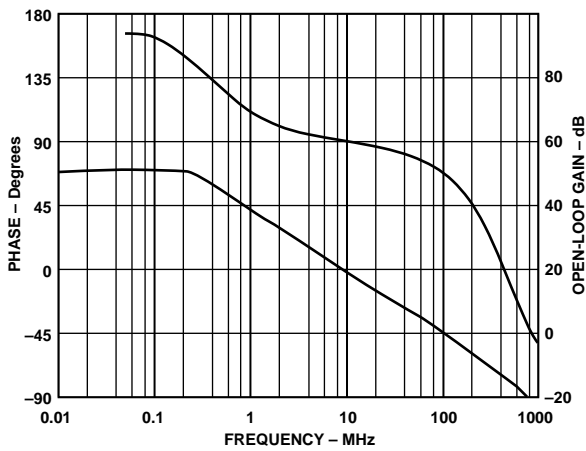


Figure 34. Open-Loop Gain and Phase vs. Frequency

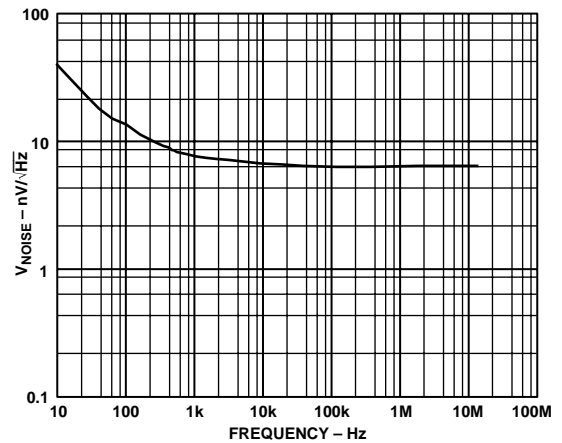


Figure 36. Voltage Noise vs. Frequency

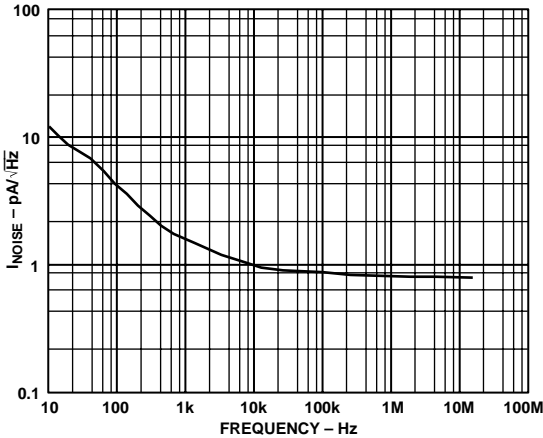


Figure 37. Current Noise vs. Frequency

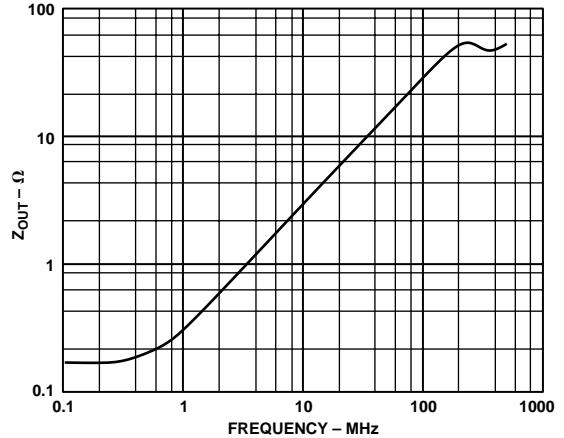


Figure 38. Output Impedance vs. Frequency

APPLICATIONS

Driving Capacitive Loads

When driving a capacitive load, most op amps will exhibit overshoot in their pulse response.

Figure 39 shows the relationship between the capacitive load that results in 30% overshoot and closed loop gain of an AD8058. It can be seen that, under the Gain = +2 condition, the device is stable with capacitive loads of up to 69 pF.

In general, to minimize peaking or to ensure device stability for larger values of capacitive loads, a small series resistor, R_S , can be added between the op amp output and the load capacitor, C_L , as shown in Figure 40.

For the setup shown in Figure 40, the relationship between R_S and C_L was empirically derived and is shown in Table I.

Table I. Recommended Value for Resistors R_S , R_F , R_G vs. Capacitive Load, C_L , Which Results in 30% Overshoot

Gain	R_F	R_G	C_L w/ $R_S = 0 \Omega$	C_L w/ $R_S = 2.4 \Omega$
1	100		11	13
2	100	100	51	69
3	100	50	104	153
4	100	33.2	186	270
5	100	25	245	500
10	100	11	870	1580

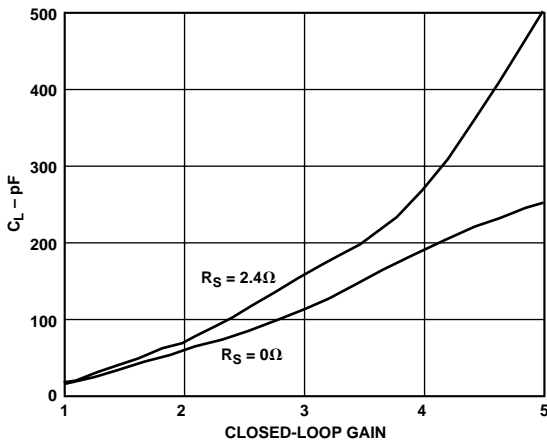


Figure 39. Capacitive Load Drive vs. Closed-Loop Gain

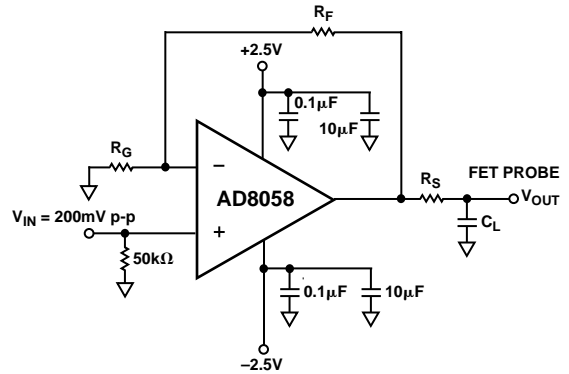


Figure 40. Capacitive Load Drive Circuit

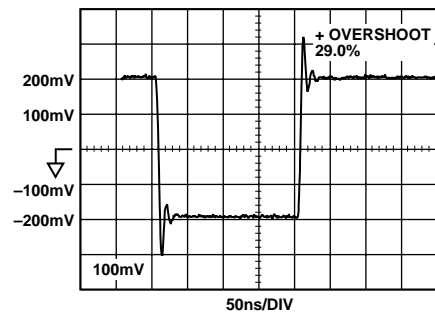


Figure 41. Typical Pulse Response with $C_L = 65 \text{ pF}$, Gain = +2, and $V_S = \pm 2.5 \text{ V}$

AD8057/AD8058

Video Filter

Some composite video signals that are derived from a digital source contain some clock feedthrough that can cause problems with downstream circuitry. This clock feedthrough is usually at 27 MHz, which is a standard clock frequency for both NTSC and PAL video systems. A filter that passes the video band and rejects frequencies at 27 MHz can be used to remove these frequencies from the video signal.

Figure 42 shows a circuit that uses an AD8057 to create a single +5 V supply, three-pole Sallen-Key filter. This circuit uses a single RC pole in front of a standard two-pole active section. To shift the dc operating point to midsupply, ac coupling is provided by R4, R5 and C4.

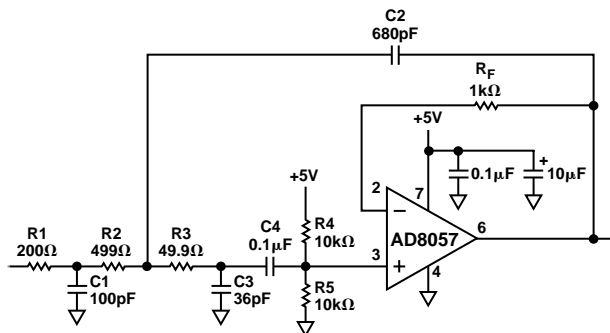


Figure 42. Low-Pass Filter for Video

Figure 43 shows a frequency sweep of this filter. The response is down 3 dB at 5.7 MHz, so it passes the video band with little attenuation. The rejection at 27 MHz is 42 dB, which provides more than a factor of 100 in suppression of the clock components at this frequency.

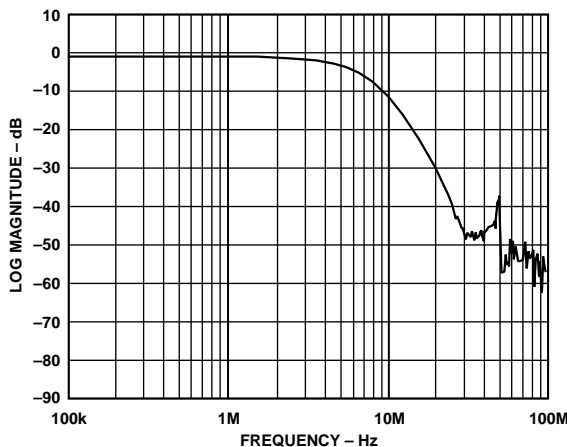


Figure 43. Video Filter Response

Differential A-to-D Driver

As system supply voltages are dropping, many A-to-D converters provide differential analog inputs to increase the dynamic range of the input signal, while still operating on a low supply voltage. Differential driving can also reduce second and other even-order distortion products.

Analog Devices offers an assortment of 12- and 14-bit high speed converters that have differential inputs and can be run from a single +5 V supply. These include the AD9220, AD9221, AD9223, AD9224 and AD9225 at 12 bits, and the AD9240, AD9241, and AD9243 at 14 bits. Although these devices can operate over a range of common-mode voltages at their analog inputs, they work best when the common-mode voltage at the input is at the midsupply or 2.5 V.

Op amp architectures that require upwards of 2 V of headroom at the output have significant problems when trying to drive such A-to-Ds while operating with a +5 V positive supply. The low headroom output design of the AD8057 and AD8058 make them ideal for driving these types of A-to-D converters.

The AD8058 can be used to make a dc-coupled, single-ended-to-differential driver for one of these A-to-Ds. Figure 44 is a schematic of such a circuit for driving an AD9225, a 12-bit, 25 MSPS A-to-D converter.

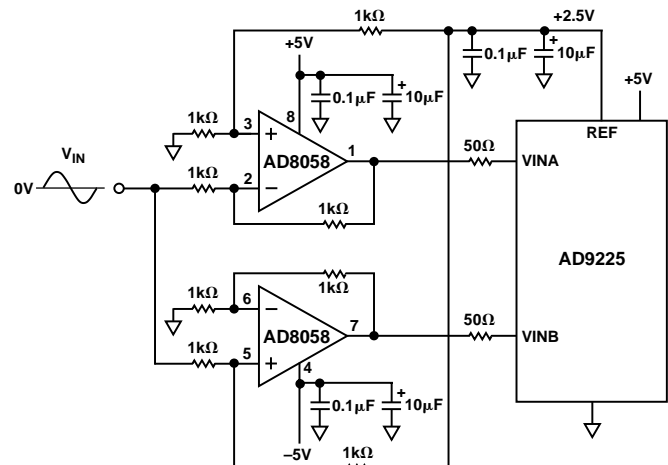


Figure 44. Schematic Circuit for Driving AD9225

In this circuit, one of the op amps is configured in the inverting mode, while the other is in the noninverting mode. However, to provide better bandwidth matching, each op amp is configured for a noise gain of 2. The inverting op amp is configured for a gain of -1 , while the noninverting op amp is configured for a gain of $+2$. Each of these produces a noise gain of 2, which is only determined by the inverse of the feedback ratio. The input signal to the noninverting op amp is divided by 2 in order to normalize its level and make it equal to the inverting output.

For zero volts input, the outputs of the op amps want to be at 2.5 V, which is the midsupply level of the A-to-D. This is accomplished by first taking the 2.5 V reference output of the A-to-D and dividing it by two by a pair of 1 k Ω resistors. The resulting 1.25 V is applied to each op amp's positive input. This voltage is then multiplied by the gain of 2 of the op amps to provide a 2.5 V level at each output.

The assumption for this circuit is that the input signal is bipolar with respect to ground and the circuit must be dc coupled. This implies the existence of a negative supply elsewhere in the system. This circuit uses -5 V as the negative supply for the AD8058.

If the AD8058 negative supply were tied to ground, there would be a problem at the input of the noninverting op amp. The input common-mode voltage can only go to within 1 V of the negative rail. Since this circuit requires that the positive inputs operate with a 1.25 V bias, there is not enough room to swing

this voltage in the negative direction. The inverting stage does not have this problem, because its common-mode input voltage remains fixed at 1.25 V. If dc-coupling is not required, various ac-coupling techniques can be used to eliminate this problem.

Layout

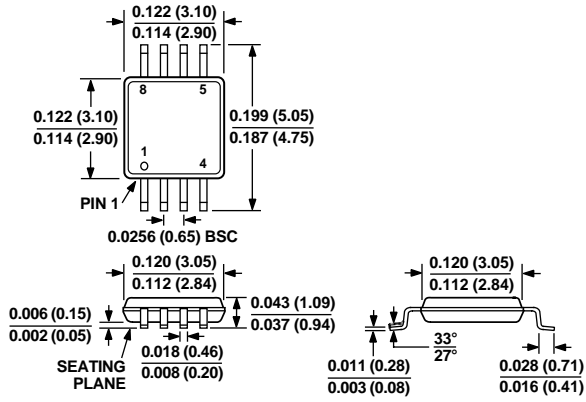
The AD8057 and AD8058 are high speed op amps and should be used in a board layout that follows standard high speed design rules. All the signal traces should be as short and direct as possible. In particular, the parasitic capacitance on the inverting input of each device should be kept to a minimum to avoid excessive peaking and other undesirable performance.

The power supplies should be bypassed very close to the power pins of the package with 0.1 μ F in parallel with a larger, approximately 10 μ F tantalum capacitor. These capacitors should be connected to a ground plane that is either on an inner layer, or fills the area of the board that is not used for other signals.

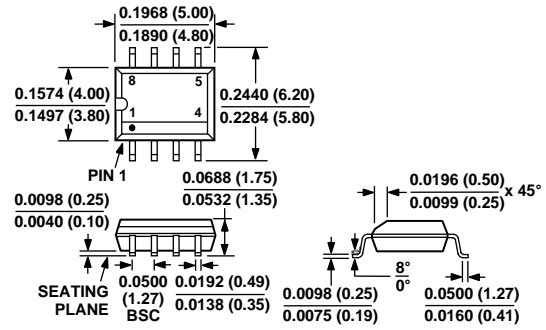
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead μ SOIC (RM-8)



8-Lead Narrow Body SOIC (SO-8)



5-Lead Surface Mount (SOT-23) (RT-5)

