Stereo Audio, 24-bit, 96 kHz, Multi-bit ΣΔ ADC

Preliminary Technical Data — AD1871

FEATURES

- 5.0V Stereo Audio ADC
  - with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates
- Supports 16/20/24-Bit Word Lengths
- Multibit Sigma Delta Modulators with
  - "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
- 105 dB (typ) Dynamic Range
- 95 dB (typ) S/(THD+N)
- Supports 256/512 and 768 xFs Master Clocks
- Flexible Serial Data Port
  - Allows Right-Justified, Left-Justified, I^2S-Compatible and DSP Serial Port Modes
  - Cascadable (up to 4 devices) from a single DSP SPORT
- Device Control via SPI compatible serial port or optional control pins
- On-Chip Reference
- 28-Lead SSOP Package.

APPLICATIONS

- Professional Audio
- Mixing Consoles
- Musical Instruments
- Digital Audio Recorders, Including
  - CD-R, MD, DVD-R, DAT, HDD
- Home Theatre Systems
- Automotive Audio Systems
- Multimedia

PRODUCT OVERVIEW

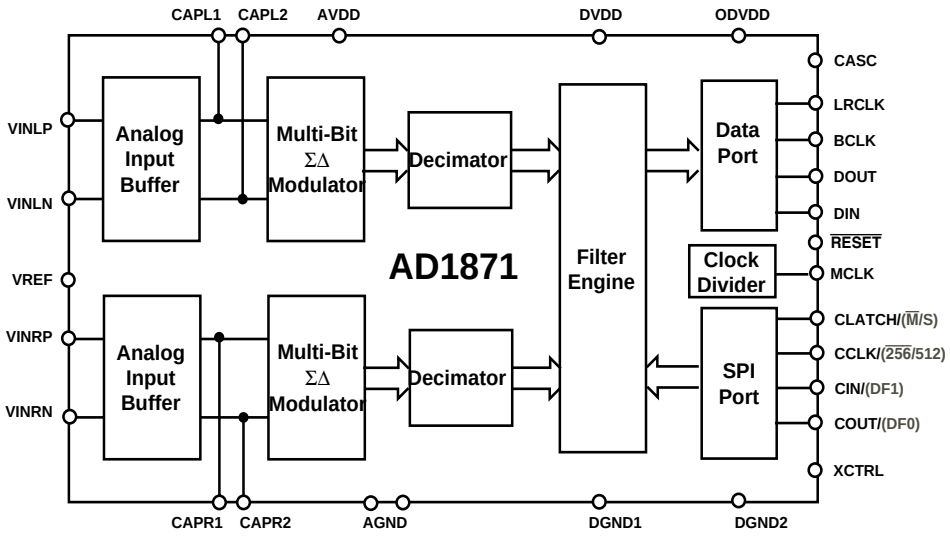
The AD1871 is a stereo audio ADC intended for digital audio applications requiring high performance analog-to-digital conversion. It features two 24-bit conversion channels each with programmable gain amplifier (PGA), multi-bit sigma-delta modulator and decimation filters. Each channel provides 95 dB of THD+N and 105 db of Dynamic Range making the AD1871 suitable for applications such as Digital Audio Recorders and Mixing Consoles.

Each of the AD1871's input channels (Left and Right) can be configured as either differential or single-ended (two inputs muxed with internal single-ended to differential conversion). The input PGA features a gain range of 0 dB to +12 dB in steps of 3 dB.The ΣΔ modulator features a proprietary multi-bit architecture which realises optimum performance over an audio bandwidth with standard audio sampling rates of 32 kHz up to 96 kHz. The decimation filter response features very-low passband ripple and excellent stopband attenuation.

The AD1871's audio data interface supports all common interface formats such as I^2S, Left-Justified, Right-Justified as well as other modes which allow for convenient hook-up to general purpose digital signal processors (DSPs). The AD1871 also features an SPI compatible serial control port which allows for convenient control of device parameters and functionality such as sample word-width, PGA-settings, interface-modes etc.

The AD1871 operates from a single +5V power supply - with optional digital interfacing capability of +3.3V. It is housed in a 28-lead SSOP package and is characterised for operation over the temperature range -40°C to 105°C.

FUNCTIONAL BLOCK DIAGRAM



REV. PrD 02/2002

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD1871–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages	+5.0	V
Ambient Temperature	25	°C
Input Clock (F_{CLKIN}) [256 ∞ F_S]	12.288	MHz
Input Signal	991.768	Hz
	–0.5	dB Full Scale (dBFS) (Differential - PGA/MUX Enabled)
Measurement Bandwidth	23.2 Hz to 19.998 kHz	
Word Width	24-bits	
Load Capacitance on Digital Outputs	100	pF
Input Voltage HI (V_{IH})	2.4	V
Input Voltage LO (V_{IL})	0.8	V

Master Mode, Data I2S-Justified.

ANALOG PERFORMANCE

	Min	Typ	Max	Unit
Resolution		24		Bits
Differential Input - PGA/MUX Enabled				
Dynamic Range (20 Hz to 20 kHz, –60 dB Input)				
Unweighted		101		dB
A-Weighted		105		dB
Signal to Noise Ratio		105		dB
Total Harmonic Distorton + Noise (THD+N)		-95		dB
Input = -20 dBFS		-100		dB
Single-Ended Input - PGA/MUX Enabled				
Dynamic Range (20 Hz to 20 kHz, –60 dB Input)				
Unweighted		101		dB
A-Weighted		105		dB
Signal to Noise Ratio		105		dB
Total Harmonic Distorton + Noise (THD+N)		-95		dB
Input = -20 dBFS		-100		dB
Differential Input - PGA/MUX Disabled				
Dynamic Range (20 Hz to 20 kHz, –60 dB Input)				
Unweighted		101		dB
A-Weighted		105		dB
Signal to Noise Ratio		105		dB
Total Harmonic Distorton + Noise (THD+N)		-95		dB
Input = -20 dBFS		-100		dB
Differential Input - PGA/MUX Enabled - Fs = 96 kHz (AMC = 1)				
Dynamic Range (20 Hz to 20 kHz, –60 dB Input)				
Unweighted		101		dB
A-Weighted		105		dB
Signal to Noise Ratio		105		dB
Total Harmonic Distorton + Noise (THD+N)		-95		dB
Input = -20 dBFS		-100		dB
Analog Inputs				
Differential Input Range (± Full Scale)	-2.828		+2.828	V
Input Impedance (PGA/MUX)		4		kΩ
V_{REF}		2.25		V
DC Accuracy				
Gain Error		TBD		%
Interchannel Gain Mismatch		0.01		dB
Gain Drift		100		ppm/°C
Crosstalk (EIAJ Method)		100		dB

LOW PASS DIGITAL FILTER CHARACTERISTICS

	Min	Typ	Max	Units
Decimation Factor				
- F_S = 48 kHz		128		
- F_S = 96 kHz		64		
Passband Frequency		20		kHz
Stopband Frequency		24		kHz
Passband Ripple		±0.0001		dB
Stopband Attenuation		120		dB
Group Delay		TBD		µs

HIGH PASS DIGITAL FILTER CHARACTERISTICS

	Min	Typ	Max	Units
Passband Frequency	TBD			Hz
Stopband Frequency			TBD	Hz
Passband Ripple			TBD	dB
Stopband Attenuation	TBD			dB
Group Delay			TBD	s

DATA INTERFACE TIMING

Mnemonic	Description	Min	Typ	Max	Unit
t_{DBH}	BCLK High Width		TBD		ns
t_{DBL}	BCLK Low Width		TBD		ns
t_{DBP}	BCLK Period		TBD		ns
t_{DLS}	Delay from LRCLK transition to BCLK high		TBD		ns
t_{DDS}	BCLK High Period		TBD		ns
t_{DDH}	BCLK High Period		TBD		ns

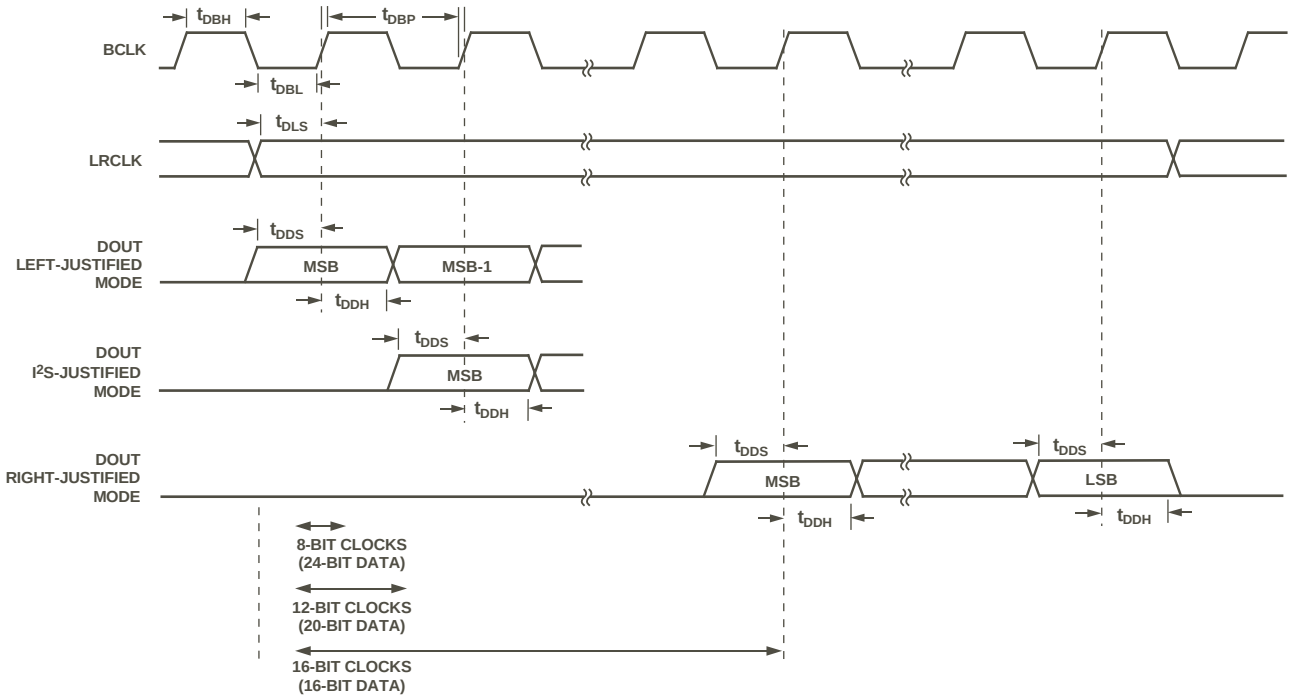


Figure <Serial_Data_Intf_Timing.eps> Data Interface Timing

CONTROL INTERFACE TIMING

Mnemonic	Description	Min	Typ	Max	Unit
t_{CCH}	CCLK High Width		TBD		ns
t_{CCL}	CCLK Low Width		TBD		ns
t_{CSU}	CDATA Setup Time		TBD		ns
t_{CHD}	CDATA Hold Time		TBD		ns
t_{CLL}	CLATCH Low Width		TBD		ns
t_{CLH}	CLATCH High Width		TBD		ns

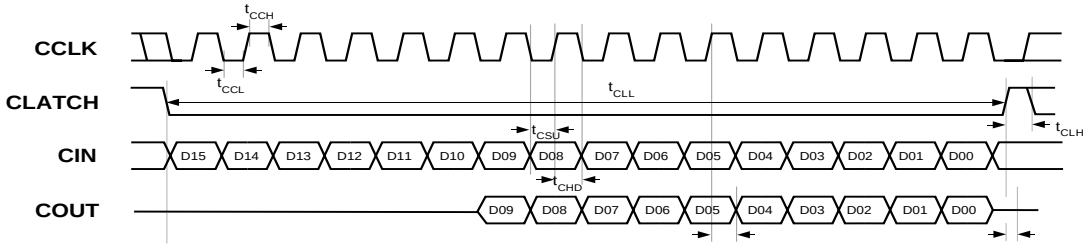


Figure <Control_Intf_Timing.eps> Control Interface Timing

DIGITAL I/O

	Min	Typ	Max	Unit
Input Voltage HI (V_{IH})	2.4			V
Input Voltage LO (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 5 V)			10	µA
Input Leakage (I_{IL} @ V_{IL} = 0 V)			10	µA
Output Voltage HI (V_{OH} @ I_{OH} = –2 mA)	ODVDD-0.4V			V
Output Voltage LO (V_{OL} @ I_{OL} = 2 mA)			0.4	V
Input Capacitance			15	pF

POWER

	Min	Typ	Max	Unit
Supplies				
Voltage, AVDD and DVDD	4.5	5	5.5	V
Voltage, ODVDD	2.7		5.5	V
Analog Current		34		mA
Analog Current—Power Down (MCLK Running)		TBD		µA
Digital Current, DVDD		16		mA
Digital Current, ODVDD		0.5		mA
Digital Current - Power Down (MCLK Running) DVDD		TBD		µA
Digital Current - Power Down (MCLK Running) ODVDD		TBD		µA
Power Supply Rejection (See Figure 11)				
1 kHz 300 mV p-p Signal at Analog Supply Pins		TBD		dB
20 kHz 300 mV p-p Signal at Analog Supply Pins		TBD		dB
Stopband (>0.55 * F_S)—any 300 mV p-p Signal		TBD		dB

TEMPERATURE RANGE

	Min	Typ	Max	Units
Specifications Guaranteed		25		°C
Functionality Guaranteed	-40		105	°C
Storage	–65		150	°C

NOTES

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

	Min	Typ	Max	Units
DVDD to DGND and ODVDD to DGND	0		6	V
AVDD to AGND	0		6	V
Digital Inputs	DGND – 0.3		DVDD + 0.3	V
Analog Inputs	AGND – 0.3		AVDD + 0.3	V
AGND to DGND	–0.3		0.3	V
Reference Voltage		Indefinite Short Circuit to Ground		
Soldering (10 sec)			+300	°C

ORDERING GUIDE

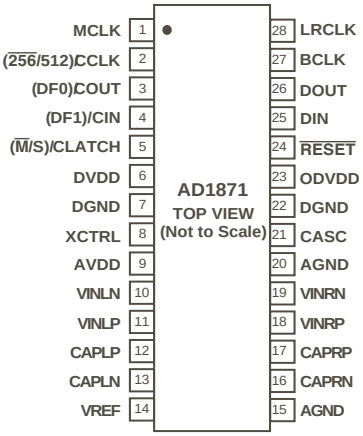
Model	Temperature	Package Description	Package Option
AD1871YRS	-40°C to +105°C	SSOP	RS-28
EVAL-AD1871EB		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1871 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Pin Configuration

28-Lead Shrink SSOP
(RS-28)



PIN FUNCTION DESCRIPTIONS

Pin	Input/ Output	Pin Name	Description
1	I	MCLK	Master Clock. The Master Clock input determines the sample rate of the device.MCLK can be 256, 512 or 768 times the sampling frequency.
2	I	CCLK/($\overline{256}$/512)	Control Port Bit Clock/Clock Rate Select - This pin has two functions which are determined by the level on pin XCTRL. When XCTRL is low, this pin is configured as the clock signal for control port data. If XCTRL is high, this pin is used to select between an MCLK of 256*fs (pin low) or 512*fs (pin high)..
3	I/O	COUT/(DF0)	Control Port Data Out/Data Format Select 0 - This pin has two functions which are determined by the level on pin XCTRL. When XCTRL is low, this pin is configured as the serial data output for control port data readback. If XCTRL is high, this pin is used as the low bit (DF0) of the Data Format Selection (See section on External Control).
4	I	CIN/(DF1)	Control Port Data Input - This pin has two functions which are determined by the level on pin XCTRL. When XCTRL is low, this pin is configured as the serial data input for control port data writing. If XCTRL is high, this pin is used as the high bit (DF1) of the Data Format Selection (See section on External Control).
5	I	CLATCH/($\overline{M}$/S)	Control Port Frame Sync/Data Format Select 1 - This pin has two functions which are determined by the level on pin XCTRL. When XCTRL is low, this pin is configured as the frame sync (framing signal) for control port data. If XCTRL is high, this pin is used to select between Master (pin low) or Slave (pin high) modes.
6	I	DVDD	+5 V Digital Core Supply
7	I	DGND	Digital Ground
8	I	XCTRL	External Control Enable - This pin is used to select the control mode for the device. When XCTRL is low, control is via the SPI compatible control port (pins CCLK, CLATCH, CIN and COUT). When XCTRL is enabled (high), control of several device functions is possible by hardware pin strapping (pins $\overline{256}$/512, $\overline{M}$/S, DF1 and DF0). In external control mode all other functions are in default state (please refer to control register descriptions and External Control section)
9	I	AVDD	+5 V Analog Supply
10	I	VINLN	Left Channel, Negative Input (via MUX/PGA)
11	I	VINLP	Left Channel Positive Input (via MUX/PGA)
12	I/O	CAPLP	Left External Filter Capacitor 1 (Direct Input to Modulator)
13	I/O	CAPLN	Left External Filter Capacitor 2 (Direct Input to Modulator)
14	O	VREF	Reference Voltage Output. It is recommended to connect a capacitor combination of 10 uF in parallel with 0.1 uF between VREF and AGND (pin 15). (See Layout Recommendations).
15	I	AGND	Analog Ground
16	I/O	CAPRN	Right External Filter Capacitor 2 (Direct Input to Modulator)
17	I/O	CAPRP	Right External Filter Capacitor 1 (Direct Input to Modulator)
18	I	VINRP	Right Channel Positive Input (via MUX/PGA)
19	I	VINRN	Right Channel Negative Input (via MUX/PGA)
20	I	AGND	Analog Ground
21	I	CASC	Cascade Enable - This pin enables cascading of up to 4 AD1871 devices to a single DSP serial port. (See Cascading section)
22	I	DGND	Digital Ground
23	I	ODVDD	Digital Interface Supply - The digital interface can operate from 3.3V to 5.0V (nominal).
24	I	RESET	Reset
25	I/O	DIN	Serial Data Input - This pin is used as a serial data input pin when cascading is enabled.
26	O	DOUT	Serial Data Output
27	I/O	BCLK	Bit Clock - The Bit Clock is the audio data serial clock and determines the rate of audio data transfer.
28	I/O	LRCLK	Left/Right Clock - This clock, also known as the word clock, determines the sampling rate. It is an output or input depending on the status of $\overline{Master}$/Slave.

DEFINITIONS

Dynamic Range
The ratio of a full-scale input signal to the integrated input noise in the passband (20 Hz to 20 kHz), expressed in decibels (dB). Dynamic range is measured with a –60 dB input signal and is equal to (S/[THD+N]) +60 dB. Note that spurious harmonics are below the noise with a –60 dB input, so the noise level establishes the dynamic range. The dynamic range is specified with and without an A-Weight filter applied.

Signal to (Total Harmonic Distortion + Noise) (S/(THD + N))
The ratio of the root-mean-square (rms) value of the fundamental input signal to the rms sum of all other spectral components in the passband, expressed in decibels (dB).

Passband
The region of the frequency spectrum unaffected by the attenuation of the digital decimator's filter.

Passband Ripple
The peak-to-peak variation in amplitude response from equal-amplitude input signal frequencies within the passband, expressed in decibels.

Stopband
The region of the frequency spectrum attenuated by the digital decimator's filter to the degree specified by "stopband attenuation."

Gain Error
With a near full-scale input, the ratio of actual output to expected output, expressed as a percentage.

Interchannel Gain Mismatch
With identical near full-scale inputs, the ratio of outputs of the two stereo channels, expressed in decibels.

Gain Drift
Change in response to a near full-scale input with a change in temperature, expressed as parts-per-million (ppm) per °C.

Midscale Offset Error
Output response to a midscale dc input, expressed in least-significant bits (LSBs).

Midscale Drift
Change in midscale offset error with a change in temperature, expressed as parts-per-million (ppm) per °C.

Crosstalk (EIAJ Method)
Ratio of response on one channel with a grounded input to a full-scale 1 kHz sine-wave input on the other channel, expressed in decibels.

Power Supply Rejection
With no analog input, signal present at the output when a 300 mV p-p signal is applied to power supply pins, expressed in decibels of full scale.

Group Delay
Intuitively, the time interval required for an input pulse to appear at the converter's output, expressed in milliseconds (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

Group Delay Variation
The difference in group delays at different input frequencies.
Specified as the difference between largest and the smallest group delays in the passband, expressed in microseconds (µs).

GLOSSARY

ADC - Analog to Digital Converter

DSP - Digital Signal Processor

IMCLK - Internal master clock signal, used to clock the decimating filter section (its frequency must be 256*fs).

MCLK - External master clock signal applied to the AD1871. Its frequency can be 256, 512 or 768 *fs. MCLK is divided internally to give an IMCLK frequency which must be 256*fs.

MODCLK - This is the ΣΔ modulator clock which determines the sample rate of the modulator. Ideally it should not exceed the lower of 6.144 MHz or 128*fs. The MODCLK is derived from the IMCLK by a divider which can be selected as /2 or /4.

MUX - Multiplexer

PGA - Programmable Gain Amplifier

FUNCTIONAL DESCRIPTION

Clocking Scheme

The MCLK pin is the input for the master clock frequency to the device. Nominally the MCLK frequency will be 256*fs for correct operation of the device. However, if the user's MCLK is a multiple of 256*fs (perhaps 512*fs or 768*fs) then it is possible to divide down the MCLK frequency to a suitable internal master clock frequency (IMCLK) using the MCLK Divider block as shown in Figure <Clock_Scheme.eps>. The divide options can be chosen from pass-through (/1), /2 or /3 corresponding with 256*fs, 512*fs or 768*fs MCLKs respectively. The MCLK divider can be controlled using the MCD1-0 bits of Control Register III (see Table <Master Clock Divider Settings>).

The resulting internal MCLK (IMCLK) is used to run the decimating and filtering engine and must be chosen to be at a ratio of 256*fs.

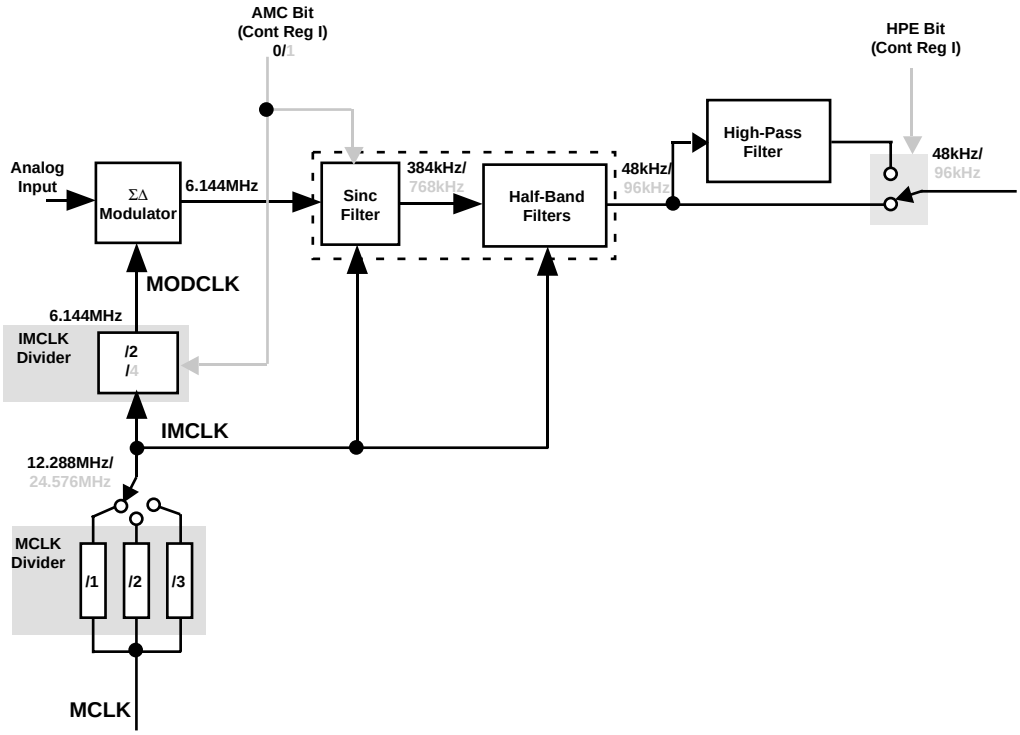


Figure <Clock_Scheme.eps> Clocking Scheme to Modulator and Filter Engine

Modulator

The AD1871's analog ΣΔ modulator section comprises a second-order multi-bit implementation using Analog Device's proprietary technology for best performance. As shown in Figure <Mod_FBD.eps>, the two analog integrator blocks are followed by a flash ADC section which generates the multi-bit samples. The output of the of the flash ADC, which is thermometer encoded, is decoded to binary for output to the filter sections and is scrambled for feedback to the two integrator stages.

The modulator is optimsed for operation at a sampling rate of 6.144 MHz (which is 128*fs at 48 kHz sampling and 64*fs at 96 kHz sampling). The modulator clock control (AMC bit in Control Register I) is used to select the modulator clock (MODCLK) as a ratio from the IMCLK. The modulator clock divider options are /2 (default) - for 48 kHz operation - and /4 - for 96 kHz operation.. When operating with an IMCLK of 12.288 MHz, the default divider setting (/2) gives a modulator clock of 6.144 MHz. When operating with an MCLK of 24.576 MHz, the alternate divider setting (/4) gives a modulator clock of 6.144 MHz. (See Figure <Clock_Scheme.eps>)

If it is required to operate the device at a different output sample rate than those detailed above - perhaps 44.1 kHz or 88.2 kHz - then the decimation filter cut-off characteristics can be determined from the normalised frequency response plot TPC <Comp_Resp_AMC_0_PB.eps>.

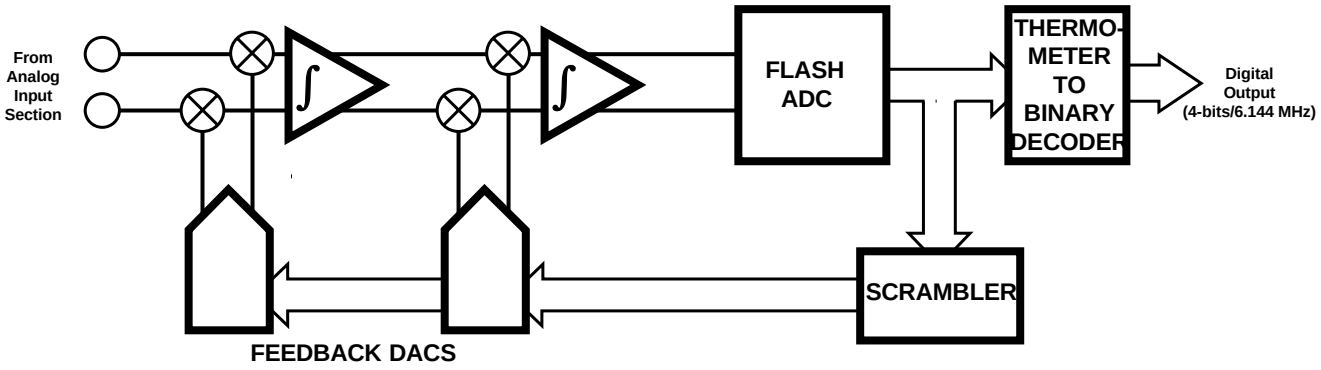


Figure <Mod_FBD.eps> Modulator Block Diagram

Digital Decimating Filters

The filtering and decimation of the AD1871's modulator datastream is implemented in an embedded DSP engine. The first stage of filtering is the Sinc filtering which has selectable decimation (selected by the modulator clock control bit (AMC - see modulator section above). The default decimation in the Sinc stage provides a sample rate reduction of 16 - this corresponds with a MODCLK rate of 128*fs. The alternate setting of the AMC bit gives a Sinc decimation factor of 8 - which corresponds with a MODCLK rate of 64*fs.. The output of the Sinc decimator stage is at a rate of 8*fs.

The filter engine implements two half-band FIR filter sections and a sinc compensation stage which together, give a further decimation factor of 8. Please refer to TPC 1 through 4 for details of the responses of the Sinc and FIR filter sections. TPC 5 gives the composite response of the sinc and FIR filters.

High Pass Filter

The AD1871 features an optional high-pass filter section which provides the ability of rejecting DC from the output datastream. The high-pass filter is enabled by setting bit 8 (HPE) of Control Register I to "1". Please refer to TPC <HPF.eps> and TPC <HPF96.eps> for details of the high-pass filter characteristic.

ADC Coding

The ADC's output data stream is in a two's complement encoded format. The word width can be selected from 16-bit, 20-bit or 24-bit (see Table <Cont_Reg_II> and Table <Word_width>). The coding scheme is detailed in Table <ADC Coding> below.

Table <ADC Coding>

Code	Level
011111.....1111	+FS
.....	
000000.....0000	0 (Ref Level)
.....	
100000.....0001	-FS

Analog Input Section

The analog input section comprises a differential PGA stage. It can also be configured for single-ended inputs, allowing two such inputs to be selected via a multiplex switch. The PGA has five gain settings (see Table <Analog Gain Settings>) ranging from 0 dB to 12 dB in 3 dB steps.

In differential mode, the VINxP and VINxN input pins are connected to a pair of inverting amplifiers whose outputs are connected to the CAPxP and CAPxN pins respectively (see Figure <Diff_Analog_Input_Select.eps>).

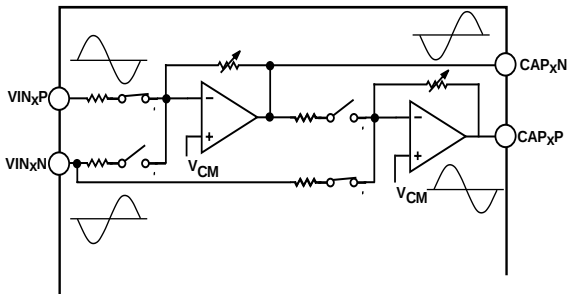


Figure <Diff_Analog_Input_Select.eps> Differential Analog Input

In single-ended mode, either VINxP or VINxN can be selected as input. The pair of input inverting amplifiers is reconfigured as a single-ended to differential conversion stage. Again the outputs of the differential section are connected to pins CAPxP and CAPxN (see Figure <SE_Analog_Input_Select.eps>).

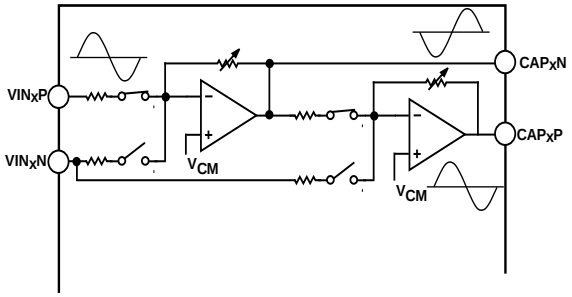


Figure <SE_Analog_Input_Select.eps> Single-ended Analog Input

The analog input section is enabled (powered on) by default on reset. If it is required to bypass the analog input section by using the modulator input pins (CAPxP and CAPxN) directly, then the analog input section must be powered down by setting bits MER and MEL in Control register III.

Serial Data Interface

The AD1871's serial data interface consists of three pins (LRCLK, BCLK and SDATA). LRCLK is the framing signal for Left and Right Channel samples and its frequency is equal to the sampling frequency (fs). BCLK is the serial clock used to clock the data samples from the AD1871 and its frequency is equal to 64*fs (giving 32 BCLK periods for each of the Left and Right Channels). SDATA outputs the Left and Right Channel sample data coincident with the rising/falling edge of BCLK.

The serial data interface supports all the popular audio interface standards such as I2S, Left-Justified (LJ) and Right-Justified (RJ) as well as the serial interfaces of modern DSPs.

The interface mode is selected by programming the bits DF1-0 of Control Register II (See Tables <Cont_Reg_II> and <Intf_Mode>).

The data sample width can be selected from 16, 20 or 24-bits by programming bits WW1-0 of Control Register II (See Tables <Cont_Reg_II> and <Word_Width>).

I^2S Mode

In I^2S mode the data is left-justified, MSB first, with the MSB placed in the second BCLK period following the transition of the LRCLK. A high to low transition of LRCLK signifies the begining of the Left channel data transfer while a low to high transition on LRCLK signifies the begining of the Right Channel data transfer (see Figure <I2S_Mode.eps>).

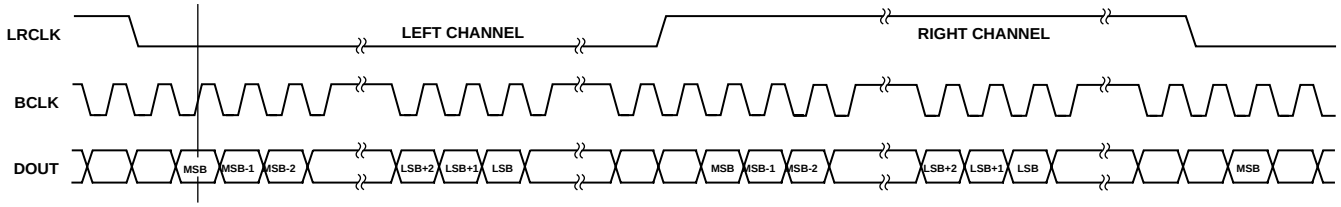


Figure <I2S_Mode.eps> I2S Mode

LJ Mode

In LJ mode the data is left-justified, MSB first, with the MSB placed in the first BCLK period following the transition of the LRCLK. A high to low transition of LRCLK signifies the begining of the Right channel data transfer while a low to high transition on LRCLK signifies the begining of the Left Channel data transfer (see Figure <LJ_Mode.eps>).

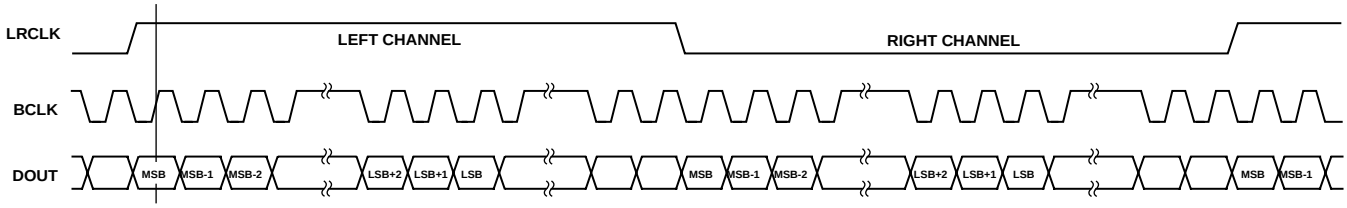


Figure <LJ_Mode.eps> LJ Mode

RJ Mode

In RJ mode the data is right-justified, LSB last, with the LSB placed in the last BCLK period preceding the transition of the LRCLK. A high to low transition of LRCLK signifies the begining of the Right channel data transfer while a low to high transition on LRCLK signifies the begining of the Left Channel data transfer (see Figure <RJ_Mode.eps>).

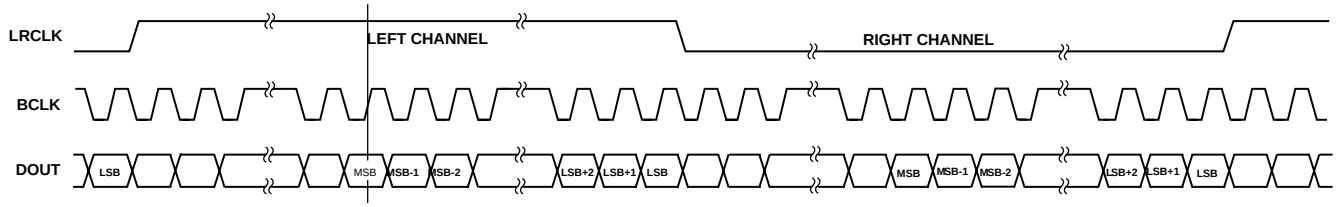


Figure <RJ_Mode.eps> RJ Mode

DSP Mode

In DSP mode tthe LRCLK signal becomes a Frame Sync signal which pulses high for the BCLK period prior to the MSB (or in the BCLK period of the previous LSB - 32 bits). The data is left-justified, MSB first, with the MSB placed in the BCLK period following the LRCLK.pulse (see Figure <DSP_Mode.eps>).

In I^2S and LJ modes, as the data is left-justified, differences in data word-width between the AD1871 and the controller are not catastrophic as the MSBs are guaranteed to be transferred. There may however, be a slight reduction in performance depending on the scale of the mismatch. In RJ mode however, differences in word-width between AD1871 and the controller have a catastrophic effect on signal performance as the MSBs of each sample may be lost due to the mismatch.

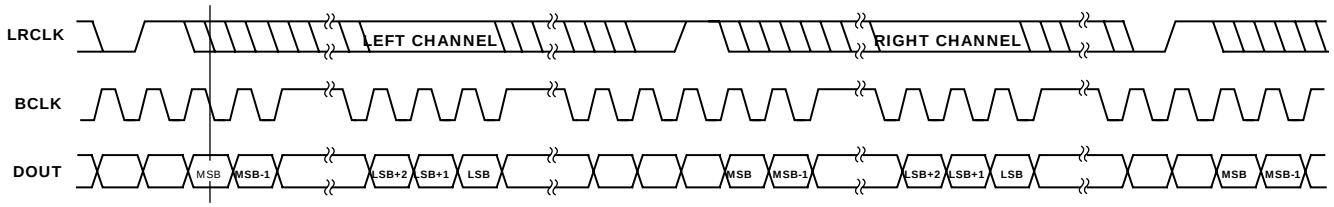


Figure <DSP_Mode.eps> DSP Mode

Cascade Mode

The AD1871 supports cascading of up to 4 devices in a daisy-chain configuration to the serial port of a DSP. In cascade mode, each device loads an internal 64-bit shift register with the results of the left and right channel conversions. The 64-bit register is split into two sub-frames of 32-bits each; the first for left channel data and the second for right-channel data. The results are left-justified, msb first within the sub-frames and the word-width setting in Control Register II applies. Remaining bits within the sub-frame, beyond the conversion word-width are set to zero. Please refer to Figure <cascade-frame.eps>.

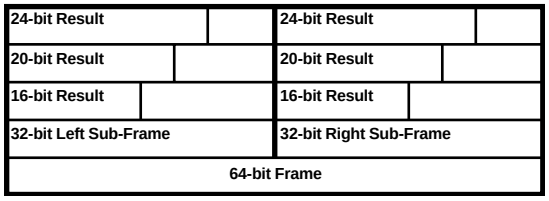


Figure <cascade-frame.eps> DSP Mode

Up to 4 devices can be connected in a daisy-chain as shown in Figure <Cascade.eps>. All devices must be set in cascade mode by tieing the CASC pin of each device to a logic high. The first device in the chain (device 4) has its DIN pin tied to either logic high or low. Its DOUT pin is connected to the DIN pin of device 3 whose DOUT is in turn connected to the DIN pin of device 2. This daisy chaining is continued until the DOUT of device 1 is connected to the DSP's serial port Rx data line (DR0). The DSP's RX serial clock (RXCLK0) is connected to the BCLK pin of all AD1871 devices and the DSP's RX frame sync (RFS0) is connected to the LRCLK pin of all AD1871 devices.

The DSP can be master and supply the frame sync and serial clock to the AD1871s or one of the AD1871s can be set as master with the DSP and all other AD1871s set to slave. Each sampling period begins with a frame sync being generated; either by the DSP or one of the AD1871s - depending on Master/Slave selection. The frame-sync pulse causes each device to load the 64-bit data I/O register with the left and right ADC results. These results are then clocked towards the DSP where they are received in the following order - Device 1 - Left, Device 1 - Right, Device 2 - Left, Device 2 - Right, Device 3 - Left, Device 3 - Right, Device 4 - Left, Device 4 - Right.

The DSP's serial port must be programmed to accept 32-bit word lengths regardless of the AD1871 word-length. The number of sample words to be accepted per sample interval will be determined by the number of AD1871 devices in cascade - up to a maximum of 8 words corresponding with the maximum number of 4 devices.

Figure <Cascade.eps> also shows the connection of a separate DSP serial port interface to the Control Port (SPI) interface of the cascaded AD1871s. Again this cascade is implemented as a daisy chain in this configuration, although it is possible to have individual read/write of the AD1871s using separate CLATCH controls for each device.

The timing relationships of the cascade mode is shown in Figure <Cascade_timing.eps>.

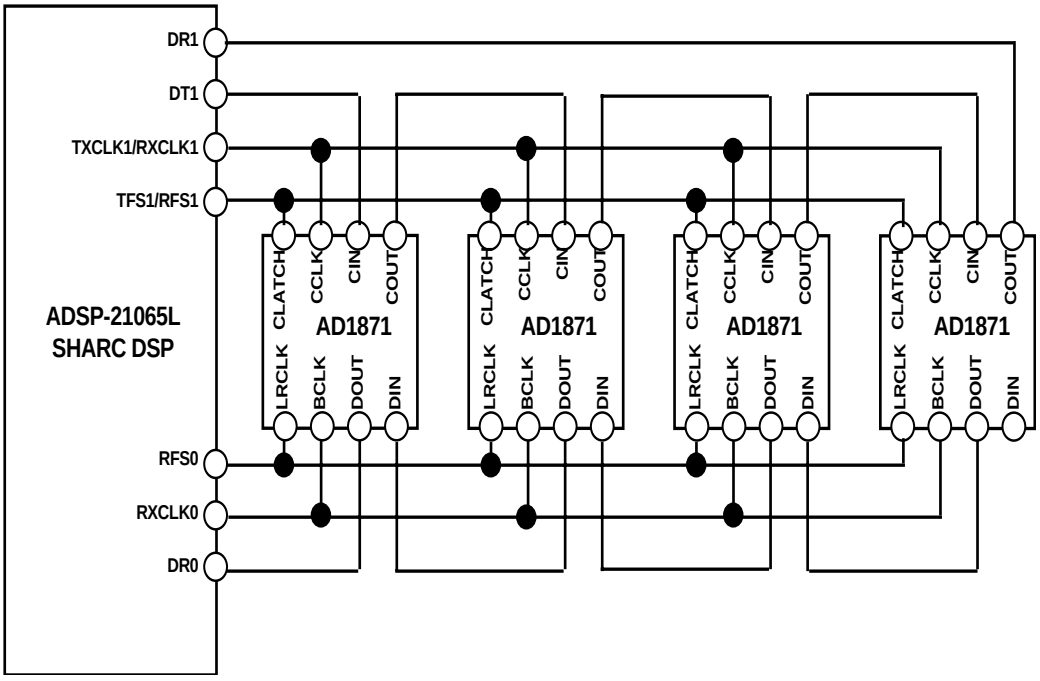


Figure <cascade.eps> DSP Mode

CONTROL/STATUS REGISTERS

The AD1871's operating mode is set by programming three, 10-bit control registers via an SPI compatible port. Figure <SPI_uC_Intf.eps> shows the typical connectivity between a microcontroller and the AD1871's Control Port. Table <Control/Status Word Format> details the format of the AD1871 control words, which are 16-bits wide with a 4-bit address field in positions 15 through 12, a Read/$\overline{\text{Write}}$ bit in position 11, a reserved bit in position 10 and ten bits of register data (corresponding to the control register width) in positions 9 through 0. The three control words occupy addresses 0000b through 0010b in the register map (see Table <Register Address Map>).

The AD1871 also features two readback (status) registers which can be enabled to track the peak reading on each of the channels (Left and Right). These 10-bit results are read back via the SPI compatible port in a 16-bit frame similar to that of the control words.

The SPI compatible control port features four signals (CCLK. CLATCH, CDATA and COUT). The CLATCH signal is an enable line which must be low to allow communication to or from the Control Port. The CCLK is the serial clock which clocks-in serial data via the CDATA pin and clocks-out serial data via the COUT pin. Figure <Control_Intf_Timing.eps> shows details of the Control Port timing.

Table <Register Address Map> Register Address Map

Address	Control Register
0000	Control Register I
0001	Control Register II
0010	Control Register III
0011	Peak Reading Register I
0100	Peak Reading Register II

Table <Control/Status Word Format> Control/Status Word Format

15-12	11	10	9	8	7	6	5	4	3	2	1	0
Address	R/W	Reserved	Control/Status Data Bits (9-0)									

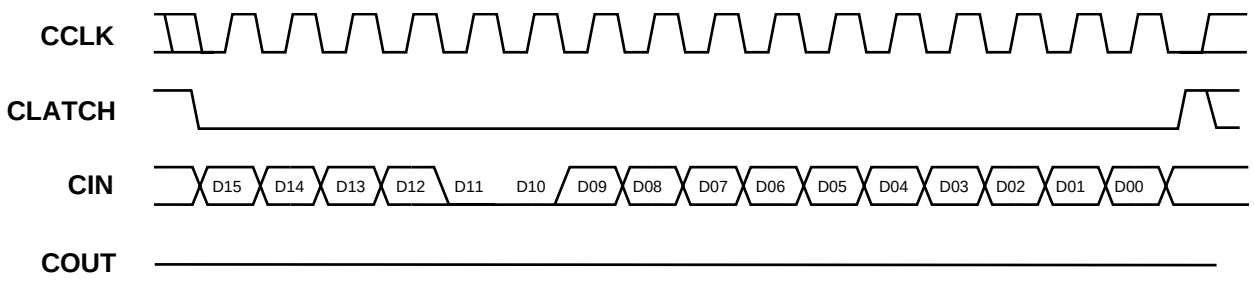


Figure <cont_intf_write.eps> Writing to register using Control Port

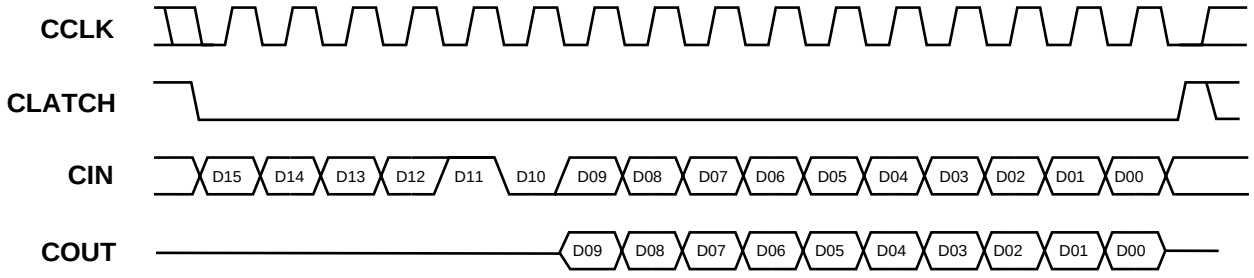


Figure <cont_intf_read.eps> Reading from register using Control Port

Table <Cont_Reg_I> Control Register I (Address 0000b - Write Only)

15-12	11	10	9	8	7	6	5	4	3	2	1	0
0000	0	0	PRE	HPE	PD	AMC	AGL2	AGL1	AGL0	AGR2	AGR1	AGR0

9	PRE	Peak Reading Enable (0 = Disabled; 1 = Enabled)
8	HPE	High Pass Filter Enable (0 = Disabled; 1 = Enabled)
7	PD	Powerdown Control (1 = Powerdown; 0 = Normal Operation)
6	AMC	ADC Modulator Clock (1 = 64*fs; 0 = 128*fs)
5-3	AGL2-0	Input Gain (Left Channel - See Table <Analog Gain Settings>)
2-0	AGR2-0	Input Gain (Right Channel - See Table <Analog Gain Settings>)

Control Register I

Control Register I contains bit settings for control of analog-front-end gain, modulator clock selection, powerdown control, high-pass filtering and peak hold.

Analog Gain Control

The AD1871 features an optional analog-front-end with selectable gain. Gain is selected using 3 control bits for each channel giving 5 separate and independent gain settings on each channel. Bits 2 through 0 (AGR2-0) set the analog gain for the Right Channel while bits 5 through 3 (AGL2-0) set the analog gain for the Left Channel. Table <Analog Gain Settings> shows the analog gain corresponding to the bit settings in AG_x2-0.

Table Analog Gain Settings

AG_x2	AG_x1	AG_x0	Gain (dB)
0	0	0	0
0	0	1	3
0	1	0	6
0	1	1	9
1	0	0	12
1	0	1	0
1	1	0	0
1	1	1	0

Modulator Clock

The modulator clock can be chosen to be either 128*fs or 64*fs. The AMC bit (bit 6) is used to select the modulator's clock rate. When AMC is set to 0 (default) the modulator clock is 128*fs. Otherwise, if set to 1, the modulator clock is 64*fs.. This bit is normally set depending on whether the desired sampling frequency is 48 kHz or 96 kHz and is also influenced by the selected MCLK frequency. Please refer to the Functional Description section for more information on MCLK selection and sampling rates.

Powerdown

Powerdown of the active clock signals within the AD1871 is effected by writing a logical 1 to bit 7 (PD).

High Pass Filter

The AD1871's digital filtering engine allows the insertion of a high pass filter (HPF) to effectively block DC signals from the output digital waveform. Setting bit 8 (HPE) enables the high-pass filter. For more details of the HPF, refer to the Functional Description.

Peak Reading Enable

The AD1871 has two readback registers which can be enabled to store the peak readings of the left and right channel ADC results. To enable the peak readings to be captured, the Peak Reading Enable bit (PRE), bit 9, must be set to logical 1. When set to logical 0, the peak reading capture is disabled.

Table <Cont_Reg_II> Control Register II (Address 0001b - Write Only)

15-12	11	10	9	8	7	6	5	4	3	2	1	0
0001	0	0	-	-	-	DF1	DF0	WW1	WW0	$\overline{M}$/S	MUR	MUL

9-7	-	Reserved
6-5	DF1-0	Data Format (See Table ___)
4-3	WW1-0	Word Width (See Table ___)
2	$\overline{M}$/S	Master/Slave Select (0 = Master Mode; 1 = Slave Mode)
1	MUR	Mute Control - Right Channel (0 = Disabled; 1 = Enabled)
0	MUL	Mute Control - Left Channel (0 = Disabled; 1 = Enabled)

Control Register II

Control Register II contains bit settings for control of left/ right channel muting, data sample word-width, data interface format, direct modulator bitstream output and modulator dither enable.

Mute Control

The left and right data channels can be muted to digital zero by setting the MUL and MUR bits (bits 0 and 1) respectively. If a channel is muted its output data stream will remain at digital zero, regardless of the amplitude of the input signal. Setting the bit to 1 mutes the channel while setting the bit to 0 restores normal operation.

Master/Slave Select

The AD1871 can operate as either a slave device or a master device. In slave mode, the controller must provide the LRCLK and BCLK to determine the sample rate and serial bit rate. In master mode, the AD1871 provides the LRCLK and BCLK as outputs which are applied to the controller. The AD1871 defaults to master mode ($\overline{M}$/S is low) on reset.

Word Width

The AD1871 allows the output sample word-width to be selected from 16, 20 and 24-bits wide. Compact Disc (CD) compatability may require 16-bits while many modern digital audio formats require 24-bit sample resolution. Bits WW1-0 are programmed to select the word-width. Table <Word_Width> details the control register bit settings corresponding to the various word-width selections.

Table <Word_Width> Word-Width Settings

WW1	WW0	Word-Width (No. of bits)
0	0	24
0	1	20
1	0	16
1	1	Reserved

Data Format

The AD1871's serial data interface can be configured from a choice of popular interface formats including I^2S, LJ, RJ or DSP modes. Bits DF1-0 are programmed to select the interface format (mode) as shown in Table <Data_Format>.

Table <Data_Format> Data Interface Format Settings

DF1	DF0	Interface Mode
0	0	I^2S
0	1	RJ
1	0	DSP
1	1	LJ

Please refer to the section on the Serial Interface in the Functional Description for more details on the various interface modes.

Table <Cont_Reg_III> Control Register III (Address 0010b - Write Only)

15-12	11	10	9	8	7	6	5	4	3	2	1	0
0010	0	0	-	-	MCD1	MCD0	SEL	SER	MEL	MXL	MER	MXR

9-8	Reserved	(Should be programmed to 0)
7-6	MCD1-0	Master Clock Divider (See Table <Master Clock Divider Settings>)
5	SEL	Single-Ended Enable - Left Channel (0 = Differential; 1 = Single-Ended)
4	SER	Single-Ended Enable - Right Channel (0 = Differential; 1=Single-Ended)
3	MEL	Mux/PGA Disable - Left Channel (0 = Enabled; 1 = Disabled)
2	MXL	Mux Select - Left Channel (0 = VINLP Selected; 1 = VINLN Selected)
1	MER	Mux/PGA Disable - Right Channel (0 = Enabled; 1 = Disabled)
0	MXR	Mux Select - Right Channel (0 = VINRP Selected; 1 = VINRN Selected)

Control Register III

Control register III contains bit settings for configuration of the analog input section (both Left and Right channels).

Mux Enable

The Mux Enable Left (MEL) and Mux Enable Right (MER) are used to enable the analog buffers.When these bits are set to 1, the analog input buffers are powered-down and input signals must be applied directly to the modulator inputs via the CAPxP and CAPxN pins. (See Figure <>). When MEL and MER are set to 0 (default condition after reset), the analog input section is enabled (See Table <Mux_Control>).

Table <Mux_Control> Mux Control Settings

MEL	MER	Input Setting
0	X	Left Channel Analog Buffer Enabled
1	X	Left Channel Analog Buffer Disabled
X	0	Right Channel Analog Buffer Enabled
X	1	Right Channel Analog Buffer Disabled

Mux Select

The Mux select bits (MXL and MXR for Left and Right channels respectively) are used to select the input from VINxP or VINxN when the input is configured as single-ended. When MXx is set to 0, the input is taken from VINxP. When MXx is set to 1, the input is taken from VINxN (See Table <Mux_Select>).

Table <Mux_Select> Mux Select Settings*

MXL	MXR	Input Setting
0	X	Left Channel Input from VINLP
1	X	Left Channel Input from VINLN
X	0	Right Channel Input from VINRP
X	1	Right Channel Input from VINRN

* Mux Select Settings are only valid when single-ended operation is enabled - SEL and SER are set to 1.

Single-Ended Mode Enable

The Single-Ended Mode Enable bits (SEL and SER for Left and Right channels respectively), when set to 1 are used to configure single-ended input on VINxP and VINxN (input is selected by state of MXL and MXR. In this mode, single-ended inputs taken from either VINxP or VINxN (selected using the Mux Select bits - MXL, MXR) are internally converted to a differential format to be applied to the modulator section.(See Table <SE_Enable>).

Table <SE_Enable> Differential/Single-Ended Select

SEL	SER	Input Setting
0	X	Left Channel Input -> Differential
1	X	Left Channel Input -> Single-Ended
X	0	Right Channel Input -> Differential
X	1	Right Channel Input -> Single-Ended

Master Clock Divider

The Master Clock Divider allows the division of the external MCLK frequency to a more suitable internal master clock frequency (IMCLK). IMCLK must be 256*fs, therefore if the available MCLK is not at 256*fs, but is a multiple of this, the MCD allows conversion of MCLK to a suitable IMCLK at 256*fs. (See Table <Master Clock Divider Settings>.)

Table <Master Clock Divider Settings> Master Clock Divider Settings

MCD1	MCD0	MCLK Division
0	0	IMCLK = MCLK (/1)
0	1	IMCLK = MCLK/2
1	0	IMCLK = MCLK/3
1	1	IMCLK = MCLK (/1)

Table <Peak_Rdg_I> Peak Reading Register I (Address 0011b - Read Only)

15-12	11	10	9	8	7	6	5	4	3	2	1	0
0011	1	0	-	-	-	-	A0P5	A0P4	A0P3	A0P2	A0P1	A0P0

9-6	Reserved	(Always set to zero)
5-0	A0P5-0	Left Channel Peak Reading (Valid only when PRE = 1)

Table <Peak_Rdg_II> Peak Reading Register II (Address 0100b - Read Only)

15-12	11	10	9	8	7	6	5	4	3	2	1	0
0100	1	0	-	-	-	-	A1P5	A1P4	A1P3	A1P2	A1P1	A1P0

9-6	Reserved	(Always set to zero)
5-0	A1P5-0	Right Channel Peak Reading (Valid only when PRE = 1)

Peak Reading Registers

The Peak Reading Registers are read-only registers which can be enabled to track and hold the peak ADC reading from each channel. The peak reading feature is enabled by setting bit PRE in Control Register I. The peak reading value is contained in the 6-LSBs of the 10-bit readback word. The result is binary coded where each LSB is equivalent to -1dbFS with all zeros corresponding to full-scale (0 dbFS) and all ones corresponding to -63 dBFS. (see Table <Peak_reading_format>).

Table <Peak_reading_format> Peak Reading Result Format

	Code						
AxP	**5**	**4**	**3**	**2**	**1**	**0**	**Level**
	0	0	0	0	0	0	0 dBFS
	0	0	0	0	0	1	-1 dBFS
	0	0	0	0	1	0	-2 dBFS
	…	…	…	…	…	…	…
	1	1	1	1	1	0	-62 dBFS
	1	1	1	1	1	1	-63 dBFS

A Peak Reading register read cycle is detailed in Figure <SPI_Read.eps>.

EXTERNAL CONTROL

The AD1871, can be configured for external hardware control of a subset of device functionality. This functionality includes Master/Slave mode select, MCLK select and serial Data Format select. External control is enabled by tieing the XCTRL pin high as shown in Figure <XCTRL.eps>.

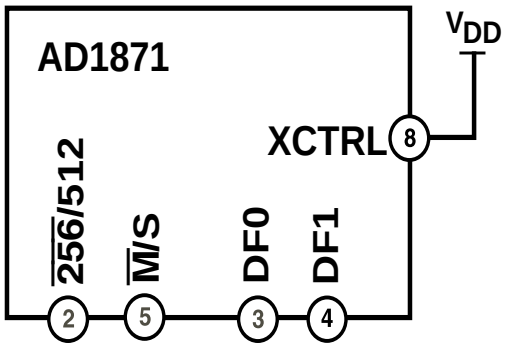


Figure <XCTRL.eps> External Control Configuration

Master/Slave Select

The Master/Slave hardware select (pin 27 - CIN/(M/S))is equivalent to setting the M/S bit of Control Register II. If set low, the device is placed in master mode, whereby the LRCLK and BCLK signals are outputs from the AD1871.

When M/S is set high, the device is in slave mode, whereby the LRCK and BCLK signals must be provided as inputs to the AD1871.

MCLK Mode Select

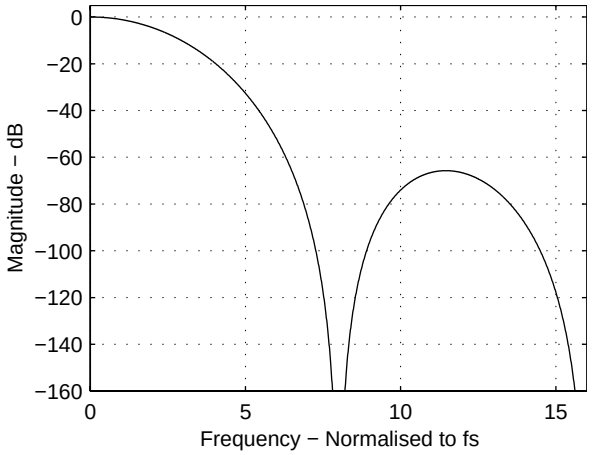
The MCLK Mode hardware select (pin 2 - CCLK/(256/512)) is a subset of the MCLK Mode selection which is determined by bits CM1-0 of Control Register II. When the hardware pin is low, the device operates with an MCLK which is 256*fs; while if the pin is set high, the device operates with an MCLK which is 512*fs.

Serial Data Format Select

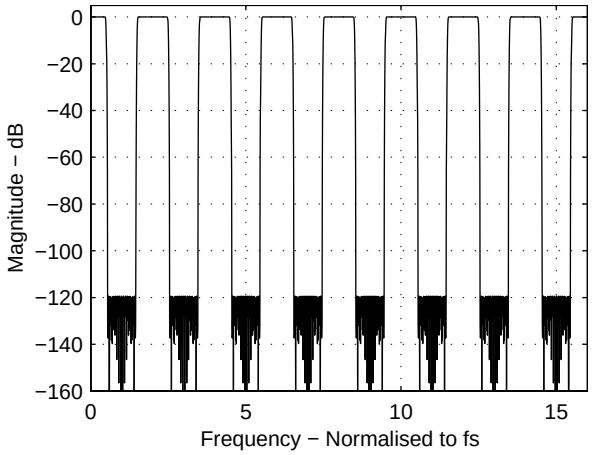
The Serial Data Format hardware select (pins 6,7 - CLATCH/(DF1),COUT/(DF0))is equivalent to setting the bits DF1-0 of Control Register II.

TYPICAL PERFORMANCE CURVES

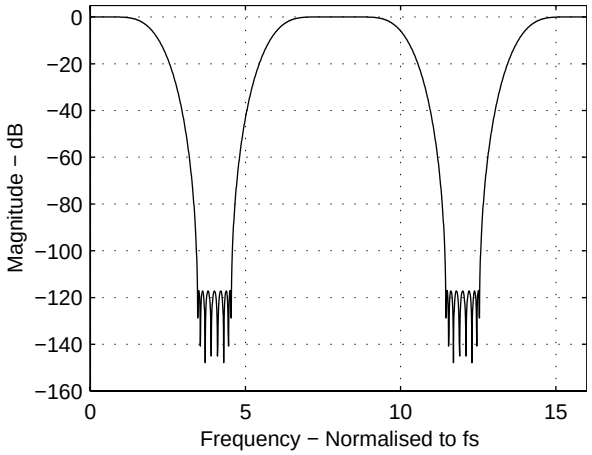
Filter Responses



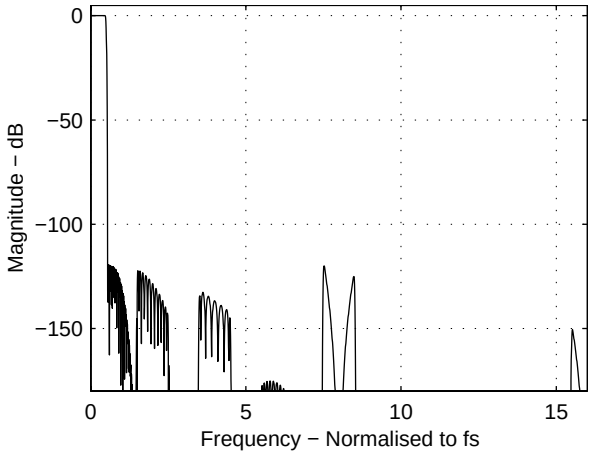
TPC <Sinc_AMC_0.eps> Sinc Filter Response (AMC = 0)



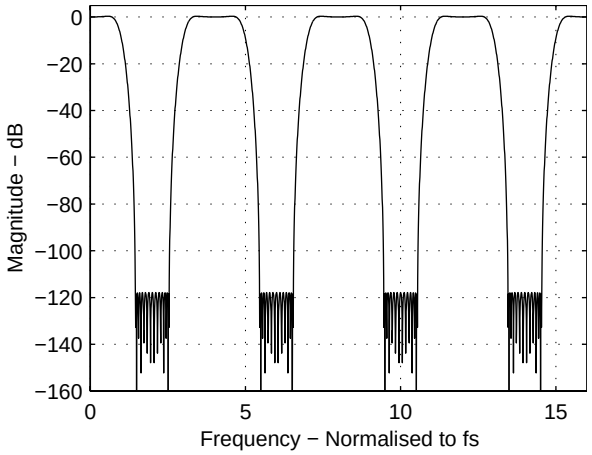
TPC <Second_HB_Filt.eps> Second Halfband Filter Response



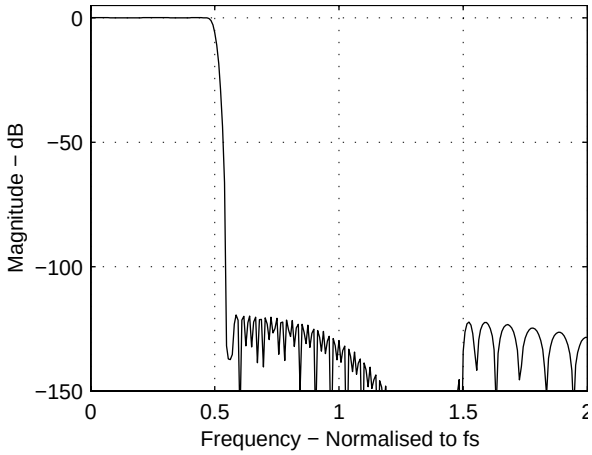
TPC <First_HB_Filt.eps> First Halfband Filter Response



TPC <Comp_resp_AMC_0.eps> Composite Filter Response (AMC = 0)

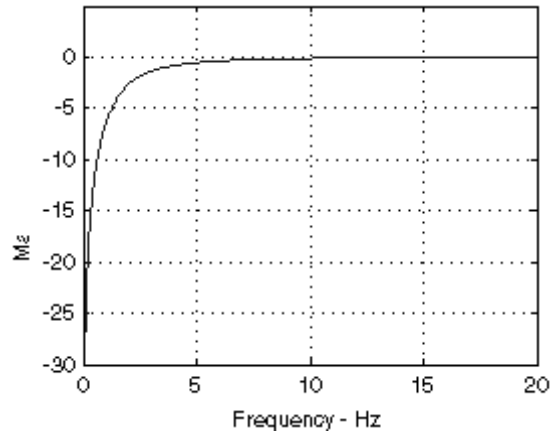


TPC <Comb_Comp_Filt.eps> Comb Compensation Filter Response

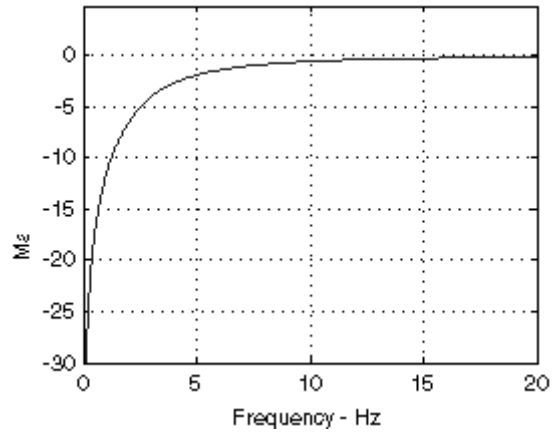


TPC <Comp_Resp_AMC_0_PB.eps> Composite Filter Response (Passband Section)(AMC = 0)

Device Performance Curves



TPC <HPF.eps> High Pass Filter Response - f_S = 48 kHz



TPC <HPF96.eps> High Pass Filter Response - f_S = 96 kHz

TPC <> 1 kHz Tone at -0.5 dBFS, (32k-point FFT), Fs = 48 kHz

TPC <> 1 kHz Tone at -20 dBFS, (32k-point FFT), Fs = 48 kHz

TPC <> 1 kHz Tone at -60 dBFS, (32k-point FFT), Fs = 48 kHz

TPC <> THD+N versus Input Amplitude at 1 kHz, Fs = 48 kHz

TPC <> THD+N versus Input Frequency at -0.5 dBFS, Fs = 48 kHz

TPC <> Channel Seperation versus Frequency at -0.5 dBFS, Fs = 48 kHz

INTERFACING

Analog Interfacing

The analog section of the AD1871 has been designed to offer flexibility as well as high performance. Users may choose full differential input directly to the ADC's ΣΔ modulator via pins CAPxP and CAPxN. Alternatively, when using the on-chip PGA section, it is also possible to multiplex single-ended inputs on pins VINxP and VINxN or to use these pins for full differential input.

Whichever input topology is chosen (direct or via mux/PGA section), the modulator input pins (CAPxP and CAPxN) require capacitors to act as dynamic charge storage for the switched capacitor input section. Component selection for these capacitors is critical as the input audio signal appears on or across these capacitors. A high quality dielectric is recommened for these capacitors multi-layer ceramic - NPO or metal film - PPS for surface mounted versions and polypropylene for through-hole versions. Indeed, as a general recommendation, high-quality dielectrics should be specified where capacitors are carrying the input audio signal.

Modulator Direct Input

Figure <Analog_Input_Cct_BYP_SE.eps> shows connection of a single-ended source; via an external single-ended to differential converter; to the modulator input of the AD1871. The external amplifier/buffer should have good slewing characteristics to meet the dynamic characteristics of the modulator input which is a switched-capacitor load.

The output of the external amplifier/buffer should be decoupled from the input capacitors via a 250Ω resistor (metal film).

In order to configure the AD1871 for differential input via CAPxP and CAPxN pins , the Mux/PGA section must be disabled by setting the MEL and MER bits in Control Register III to "1".

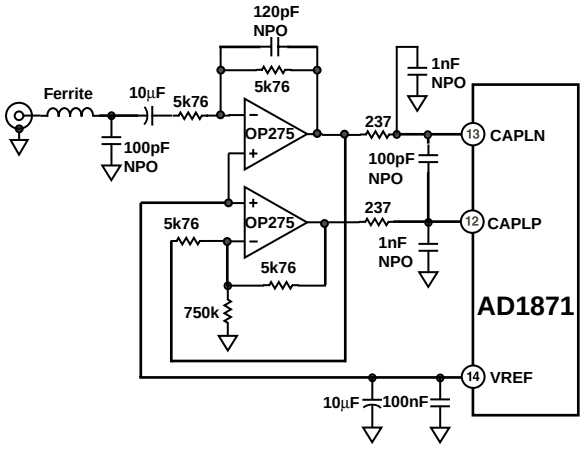


Figure <Analog_Input_Cct_BYP_SE.eps> Direct Connection to Modulator

PGA Input - Single-Ended

Figure <Analog_Input_PGA_Cct_SE.eps> shows connection of a single-ended source to the PGA section of the AD1871. The PGA section is configured for Single-Ended to Differential conversion. The differential outputs are connected internally to the CAPxx pins via 250Ω series resistors.

In order to configure the AD1871 for single-ended input , the control registers must be configured as follows:

Left Channel:
Control Register I = xx0xGGGxxx
  where GGG = Input Gain (see Table <AnalogGainSettings>
Control Register III = 00xx1x0Sxx
  where S = SE Channel Selection

Right Channel:
Control Register I = xx0xxxxGGG
  where GGG = Input Gain (see Table <AnalogGainSettings>
Control Register III = 00xxx1xx0S
  where S = SE Channel Selection

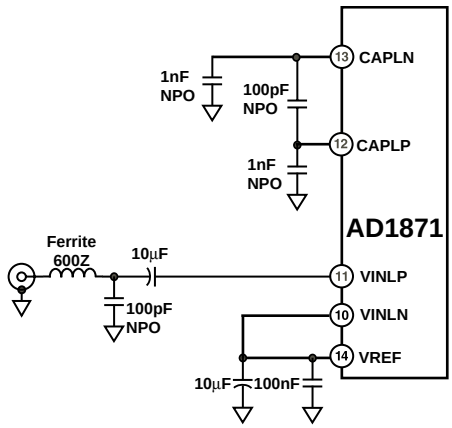


Figure <Analog_Input_PGA_Cct_SE.eps> Single-Ended Input via PGA Section

PGA Input - Differential

Figure <Analog_Input_PGA_Cct_Diff.eps> shows connection of a differential source to the PGA section of the AD1871. The PGA section is configured as a differential buffer. The buffered differential outputs are connected internally to the CAPxx pins via 250Ω series resistors.

In order to configure the AD1871 for differential input via the Mux/PGA , the control registers must be configured as follows:

Left Channel:
Control Register I = xx0xGGGxxx
  where GGG = Input Gain (see Table <AnalogGainSettings>
Control Register III = 00xx0x0xxx

Right Channel:
Control Register I = xx0xxxxGGG
  where GGG = Input Gain (see Table <AnalogGainSettings>
Control Register III = 00xxx0xx0x

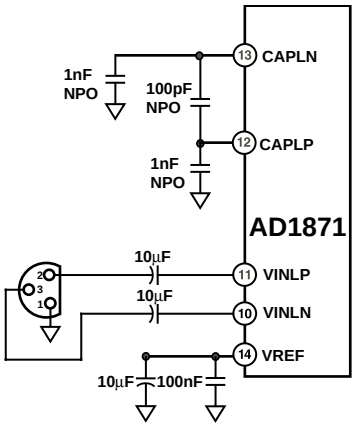


Figure <Analog_Input_PGA_Cct_Diff.eps> Differential Input via PGA Section

LAYOUT CONSIDERATIONS

In order to operate the AD1871 at its specified performance level, careful consideration must be given to the layout of the AD1871 and its ancillary circuits. Since the analog inputs to the AD1871 are differential, the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The analog and digital supplies of the AD1871 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. The digital filters will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filters also remove noise from the analog inputs provided the noise source does not saturate the analog modulator. However, because the resolution of the AD1871's ADC is high, and the noise levels from the AD1871 are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD1871 should be designed so the analog and digital sections are separated and confined to certain sections of the board. The AD1871 pin selection has been configued such that its analog and digital interfaces are connected on opposite ends of the package. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Figure <AD1871EB_Layers_Composite.eps> is a composite view of the solder and component layers of a two-sided PCB layout. The separation between the analog and digital ground planes(on the solder side) and the analog and digital power planes (on the component side) can be seen on the figure.

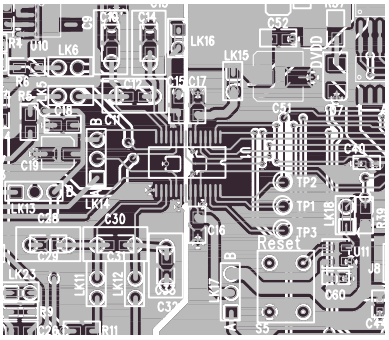


Figure <AD1871EB_Layers_Composite.eps> Ground Layout

NOTE In the above figure, the black area represents the solder side of the layout, while grey represents the component side of the layout. The silkscreen in white is included for clarity

Digital and analog ground planes should be joined in only one place. If this connection is close to the device, it is recommended to use a ferrite bead inductor as shown in Figure <AD1871EB_Solder_SS.eps>. The pads for the ferrite are positioned on the solder-side directly underneath the AD1871 device (U1 in the Figure).

Avoid running digital lines under the device as they may couple noise onto the die. The analog ground plane should be allowed to run under the AD1871 to avoid noise coupling. If it is not possible to use a power supply plane then the power supply lines to the AD1871 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply lines. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the other side.

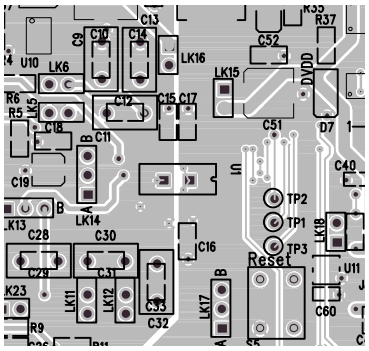


Figure <AD1871EB_Solder_SS.eps> Connecting Analog and Digital Grounds

Good decoupling is important when using high speed devices. All analog and digital supplies should be decoupled to AGND and DGND respectively, with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors. To achieve the best from these decoupling capacitors, they should be placed as close as possible to the device, ideally right up against it., as shown in Figure <AD1871EB_Comp_SS.eps> In systems where a common supply voltage is used to drive both the AVDD and DVDD of the AD1871, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD1871 and AGND and the recommended digital supply decoupling capacitors between the DVDD pin and DGND.

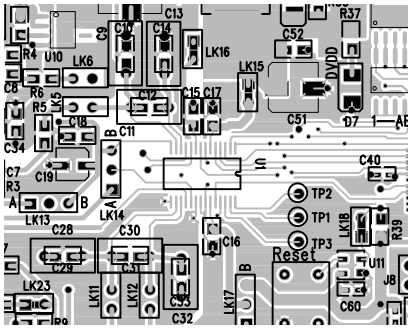


Figure <AD1871EB_Comp_SS.eps> AD1871 Power Supply Decoupling

Another important consideration is the selection of components such as capacitors, resistors and operational amplifiers for the ancillary circuits

Contents

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Shrink Small Outline IC (RS-28)