

# DATA SHEET

## **74LVC157A** Quad 2-input multiplexer

Product specification  
Supersedes data of 2002 Mar 15

2003 Jun 17

## Quad 2-input multiplexer

## 74LVC157A

### FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

### DESCRIPTION

The 74LVC157A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC157A is a quad 2-input multiplexer which select four bits of data from two sources under the control of a common select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input ( $\bar{E}$ ) is active LOW. When  $\bar{E}$  is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all the other input conditions. Moving the data from two groups of registers to four common output buses is a common use of the 74LVC157A. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any 4 of the 16 different functions of two variables with one variable common.

The 74LVC157A is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay nI0, nI1 to nY $\bar{E}$ to nY S to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V $C_L = 50$ pF; $V_{CC} = 3.3$ V $C_L = 50$ pF; $V_{CC} = 3.3$ V	2.6 2.8 2.6	ns ns ns
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2	15	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in Volts;  
 $N$  = total switching outputs;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_I = \text{GND to } V_{CC}$ .

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**FUNCTION TABLE**

See note 1.

INPUT				OUTPUT
$\bar{E}$	S	nI <sub>0</sub>	nI <sub>1</sub>	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

**Note**

1. H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

**ORDERING INFORMATION**

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVC157AD	-40 to +125 °C	16	SO16	plastic	SOT109-1
74LVC157ADB	-40 to +125 °C	16	SSOP16	plastic	SOT338-1
74LVC157APW	-40 to +125 °C	16	TSSOP16	plastic	SOT403-1
74LVC157ABQ	-40 to +125 °C	16	DHVQFN16	plastic	SOT763-1

**PINNING**

PIN	SYMBOL	DESCRIPTION
1	S	common data select input
2	1I0	data input from source 0
3	1I1	data input from source 1
4	1Y	multiplexer output
5	2I0	data input from source 0
6	2I1	data input from source 1
7	2Y	multiplexer output
8	GND	ground (0 V)
9	3Y	multiplexer output
10	3I1	data input from source 1
11	3I0	data input from source 0
12	4Y	multiplexer output
13	4I1	data input from source 1
14	4I0	data input from source 0
15	$\bar{E}$	enable input (active LOW)
16	V <sub>CC</sub>	supply voltage

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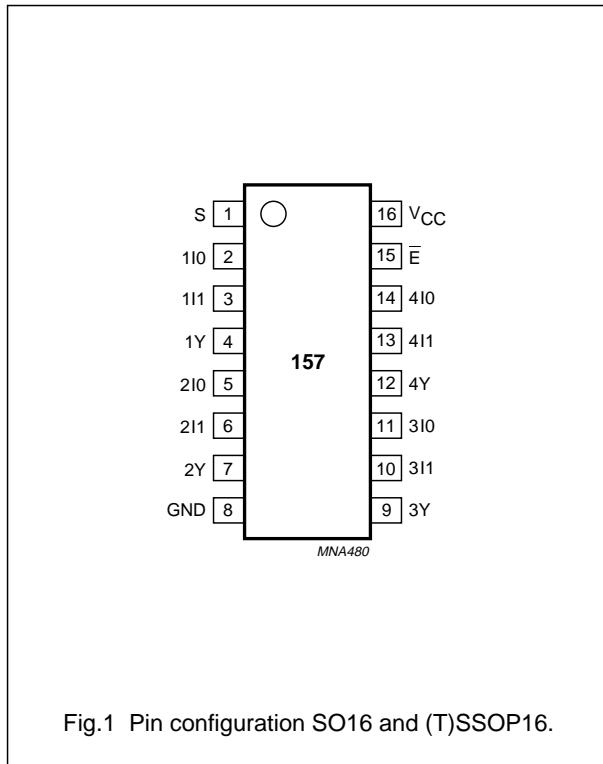
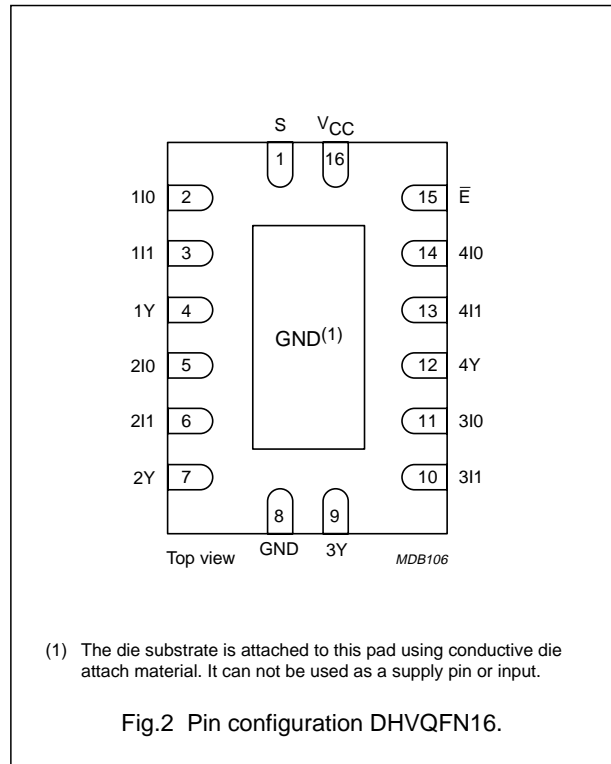


Fig.1 Pin configuration SO16 and (T)SSOP16.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN16.

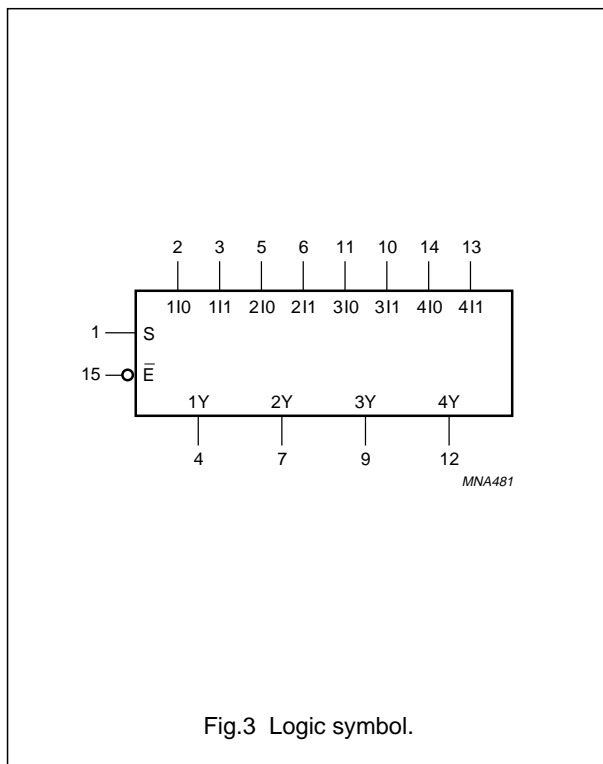


Fig.3 Logic symbol.

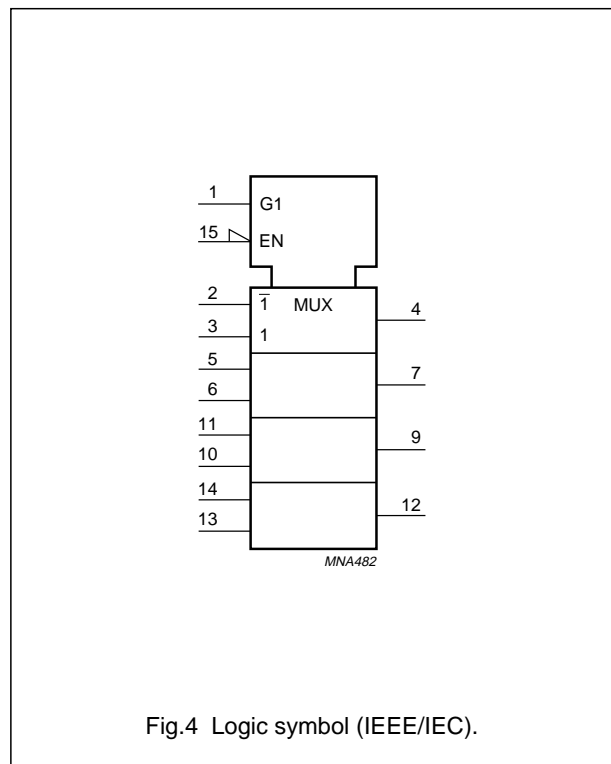
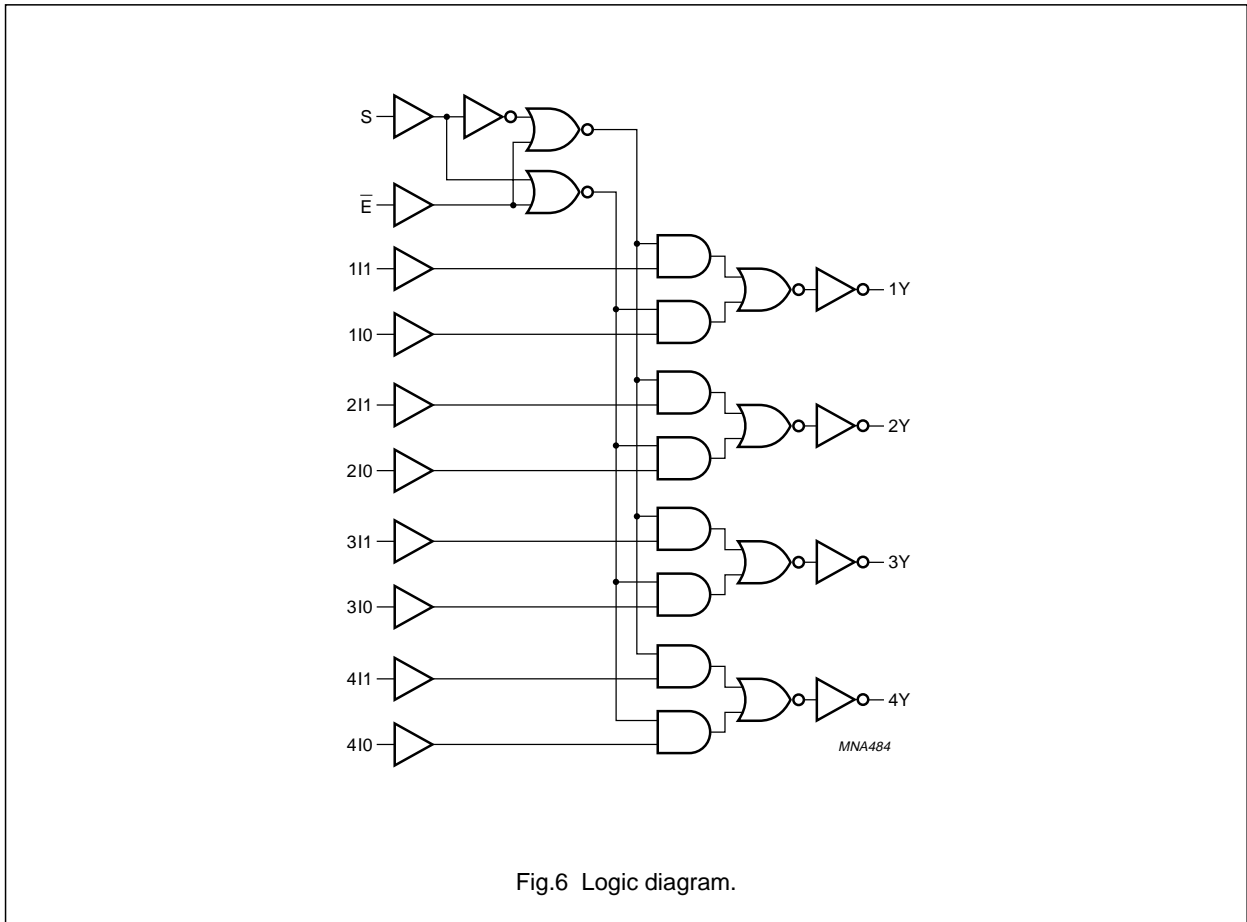
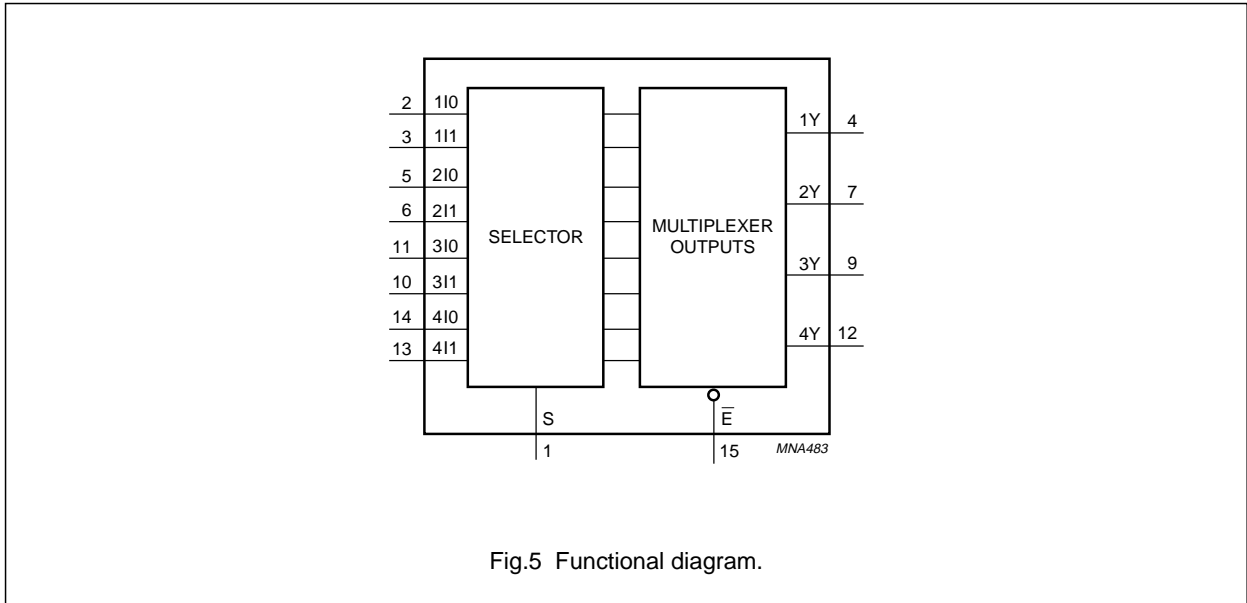


Fig.4 Logic symbol (IEEE/IEC).

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage		0	$V_{CC}$	V
$T_{amb}$	operating ambient temperature		-40	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 1.2$ to $2.7$ V	0	20	ns/V
		$V_{CC} = 2.7$ to $3.6$ V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$	-	-50	mA
$V_I$	input voltage	note 1	-0.5	+6.5	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
$V_O$	output voltage	note 1	-0.5	$V_{CC} + 0.5$	V
$I_O$	output source or sink current	$V_O = 0$ to $V_{CC}$	-	±50	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ to $+125$ °C; note 2	-	500	mW

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO16 packages: above 70 °C the value of  $P_D$  derates linearly with 8 mW/K.  
For (T)SSOP16 packages: above 60 °C the value of  $P_D$  derates linearly with 5.5 mW/K.  
For DHVQFN16 packages: above 60 °C the value of  $P_D$  derates linearly with 4.5 mW/K.

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**DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 µA	2.7 to 3.6	V <sub>CC</sub> - 0.2	–	–	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.5	–	–	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.6	–	–	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 0.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA	2.7 to 3.6	–	–	0.2	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.4	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	–	±0.1	±5	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	0.1	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	5	500	µA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	V <sub>CC</sub> – 0.3	–	–	V
		I <sub>O</sub> = –100 μA		V <sub>CC</sub> – 0.65	–	–	V
		I <sub>O</sub> = –12 mA		V <sub>CC</sub> – 0.75	–	–	V
		I <sub>O</sub> = –18 mA		V <sub>CC</sub> – 1	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	–	–	0.3	V
		I <sub>O</sub> = 100 μA		–	–	0.6	V
		I <sub>O</sub> = 12 mA		–	–	0.8	V
		I <sub>O</sub> = 24 mA		–	–	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	–	–	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	–	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	–	5000	μA

**Note**

1. All typical values are measured at T<sub>amb</sub> = 25 °C.



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**AC CHARACTERISTICS**GND = 0 V;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nI0, nI1 to nY	see Figs 8 and 9	1.2	–	16	–	ns
			2.7	1.5	3.0	5.9	ns
			3.0 to 3.6	1.0	2.6 <sup>(2)</sup>	5.2	ns
	propagation delay $\bar{E}$ to nY	see Figs 7 and 9	1.2	–	17	–	ns
			2.7	1.5	3.4	7.8	ns
			3.0 to 3.6	1.0	2.8 <sup>(2)</sup>	6.8	ns
	propagation delay S to nY	see Figs 8 and 9	1.2	–	16	–	ns
			2.7	1.5	3.0	7.3	ns
			3.0 to 3.6	1.0	2.6 <sup>(2)</sup>	6.3	ns
t <sub>sk(0)</sub>	skew	note 3		–	–	1.0	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nI0, nI1 to nY	see Figs 8 and 9	1.2	–	–	–	ns
			2.7	1.5	–	7.5	ns
			3.0 to 3.6	1.0	–	6.5	ns
	propagation delay $\bar{E}$ to nY	see Figs 7 and 9	1.2	–	–	–	ns
			2.7	1.5	–	10.0	ns
			3.0 to 3.6	1.0	–	8.5	ns
	propagation delay S to nY	see Figs 8 and 9	1.2	–	–	–	ns
			2.7	1.5	–	9.5	ns
			3.0 to 3.6	1.0	–	8.0	ns
t <sub>sk(0)</sub>	skew	note 3		–	–	1.5	ns

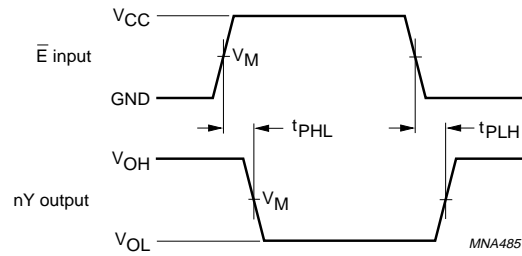
**Notes**

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. This typical value is measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

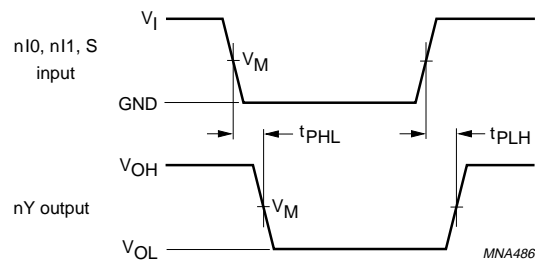
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## AC WAVEFORMS



$V_M = 1.5 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$ ;  
 $V_M = 0.5V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$ ;  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

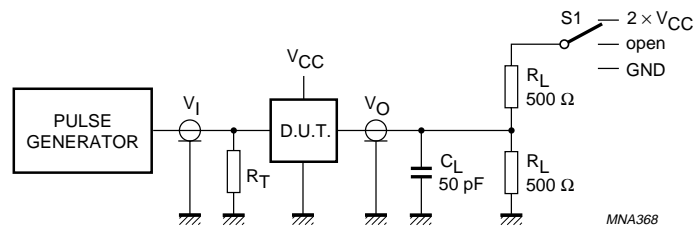
Fig.7 Enable input ( $\bar{E}$ ) to output (nY) propagation delays.

$V_M = 1.5 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$ ;  
 $V_M = 0.5V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$ ;  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

Fig.8 Data inputs (nI0, nI1) and common data select input (S) to output (nY) propagation delays.

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$V_{CC}$	$V_I$	$t_{PLH}/t_{PHL}$
1.2 V	$V_{CC}$	open
2.7 V	2.7 V	open
3.0 to 3.6 V	2.7 V	open

Definitions for test circuits:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.9 Load circuitry for switching times.

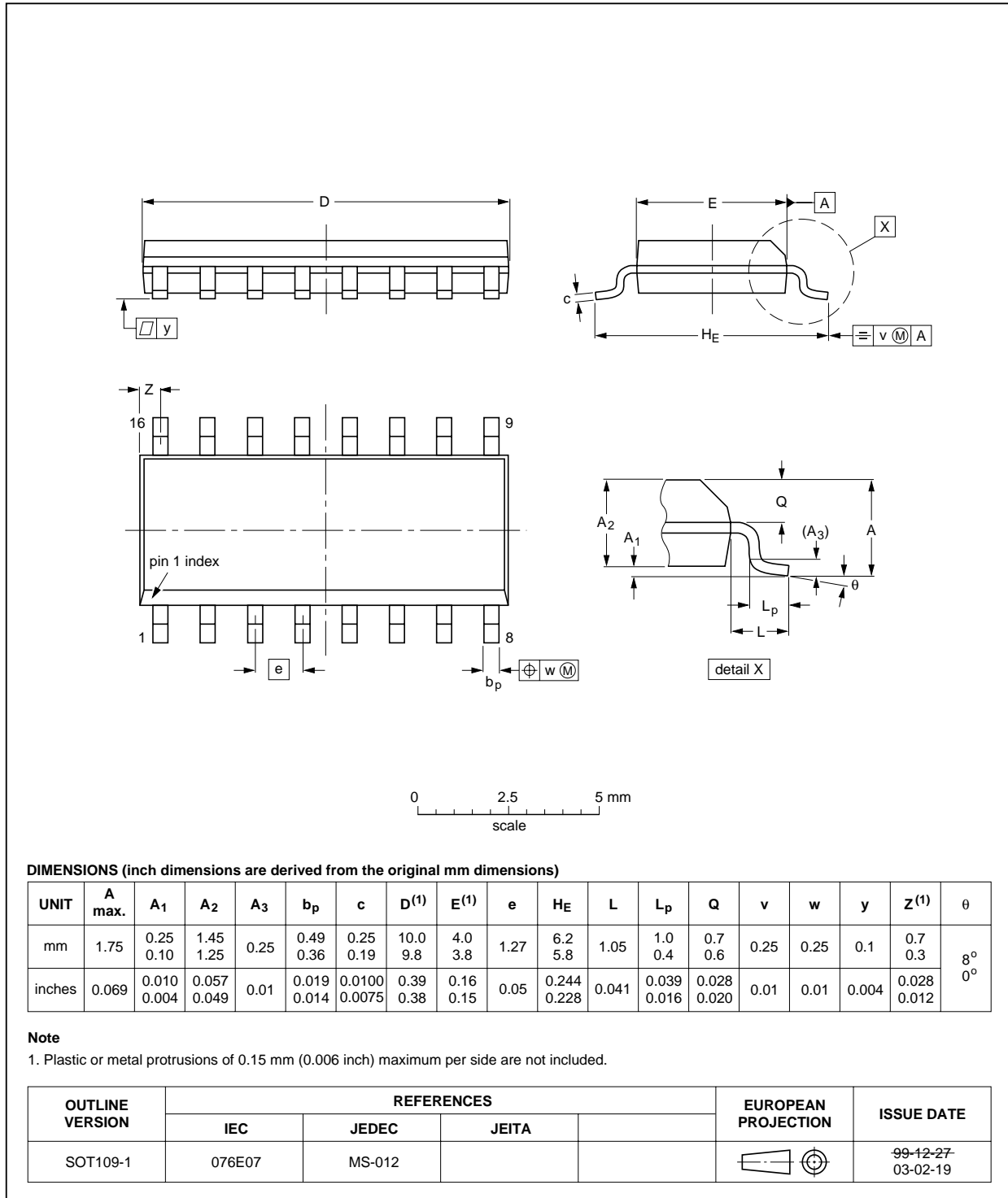
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PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

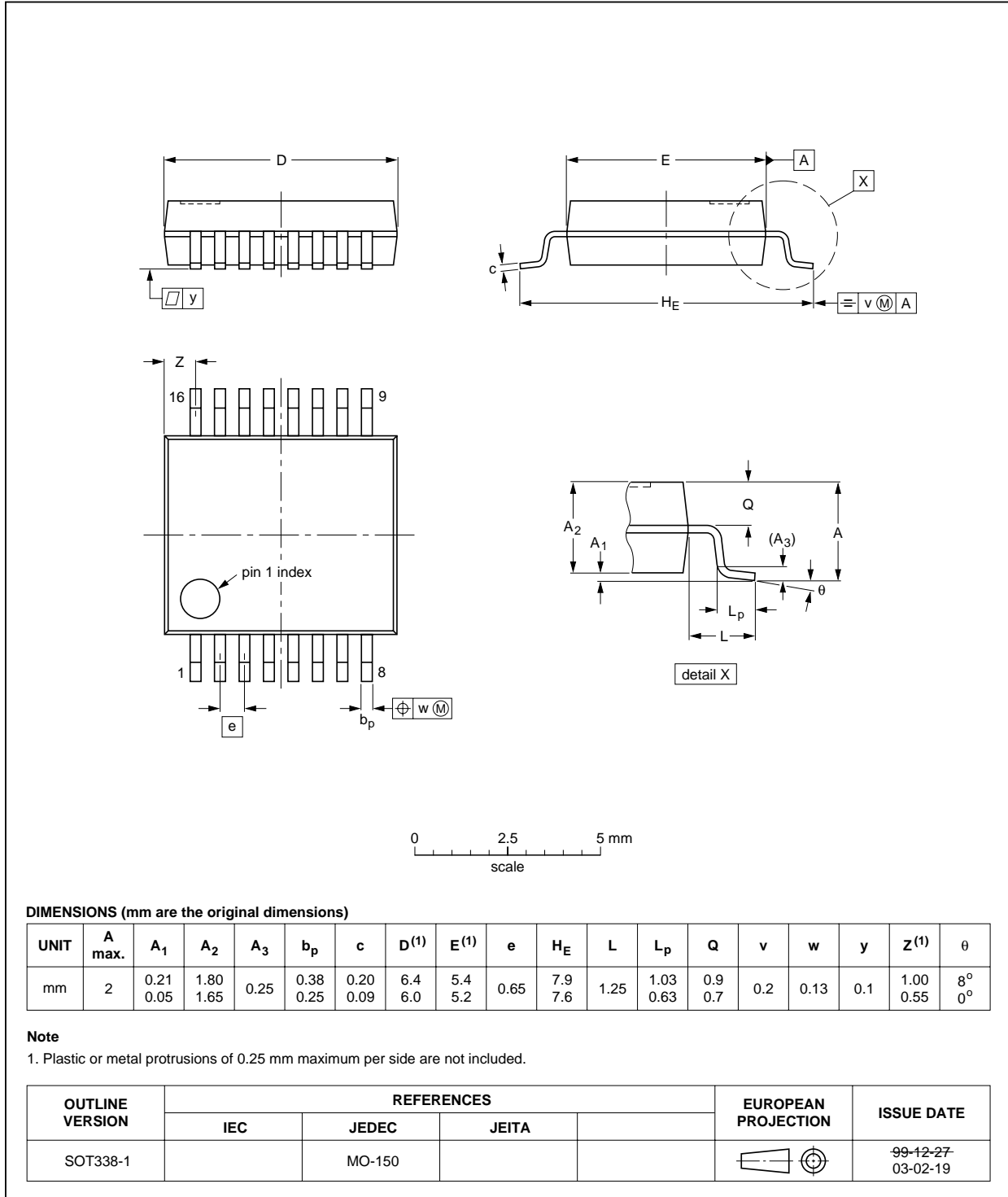


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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

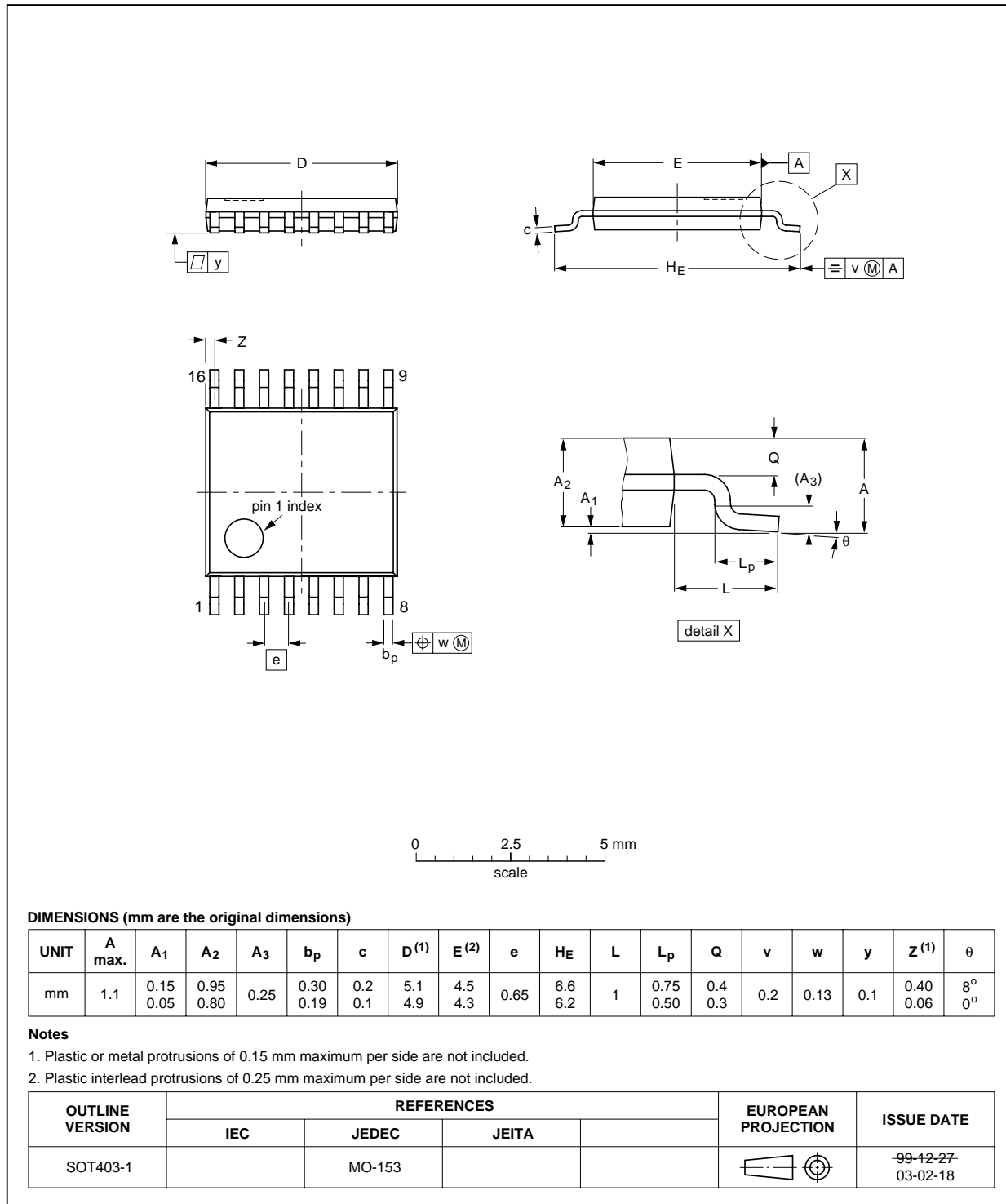


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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

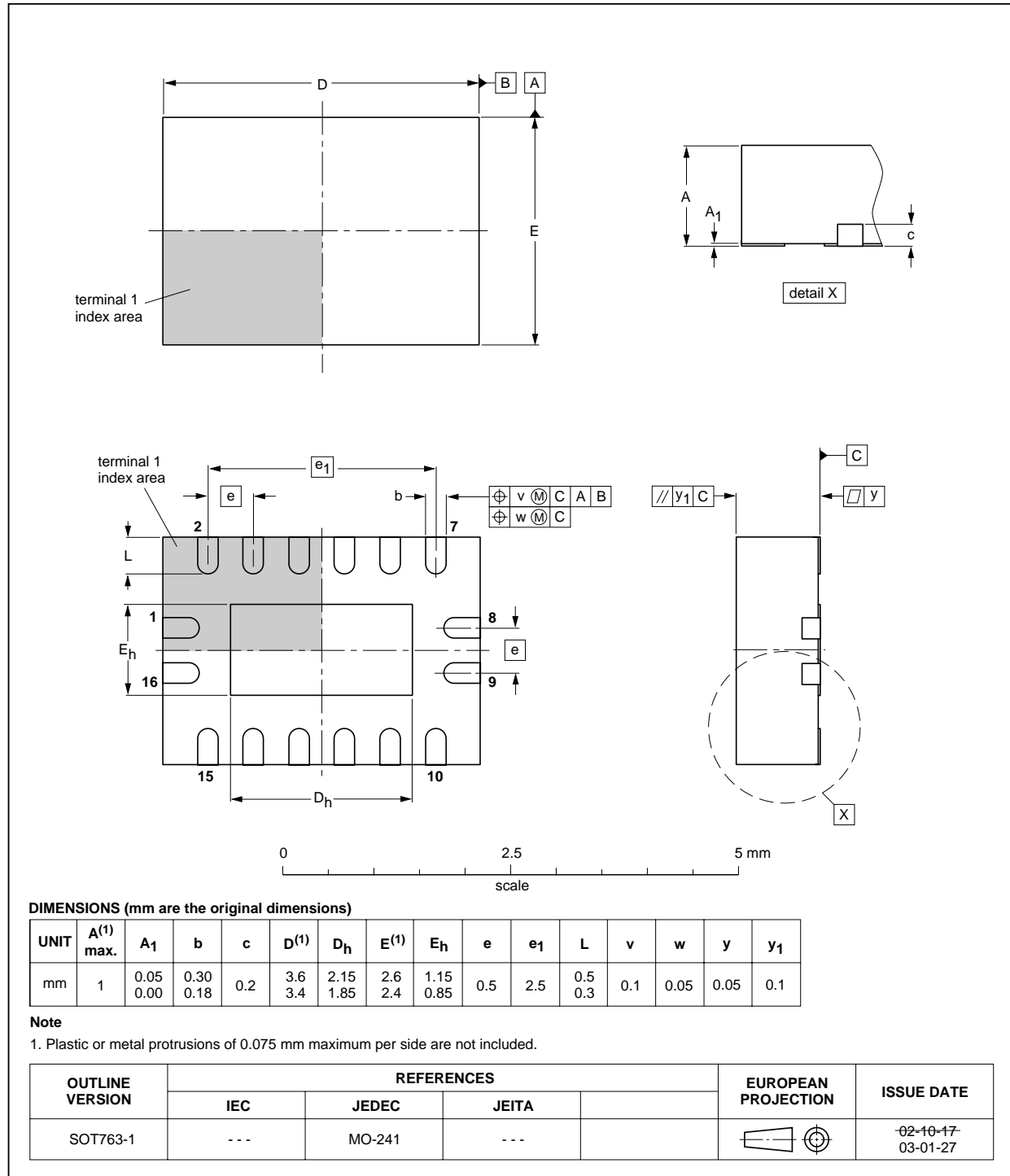


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DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1



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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept:

- below 220 °C for all the BGA packages and packages with a thickness  $\geq 2.5$  mm and packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages
- below 235 °C for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



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**Suitability of surface mount IC packages for wave and reflow soldering methods**

PACKAGE <sup>(1)</sup>	SOLDERING METHOD	
	WAVE	REFLOW <sup>(2)</sup>
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>(3)</sup>	suitable
PLCC <sup>(4)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(4)(5)</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>(6)</sup>	suitable

**Notes**

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

## Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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Quad 2-input multiplexer

74LVC157A

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**NOTES**

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