M50957-XXXSP/FP, M50958-XXXSP/FP
PRELIMINARY (M50958-XXXSP/FP) M50959-XXXSP/FP

Notice: These are not a final specification. Some parametric limits are subject to change.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50957-XXXSP, the M50958-XXXSP and the M50959-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 64-pin shrink plastic molded DIP (flat package type also available). These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences among M50957-XXXSP, M50958-XXXSP and M50959-XXXSP are noted below. The following explanations apply to the M50957-XXXSP. Specification variations for other chips are noted accordingly.

Type name	ROM size
M50957-XXXSP	10240bytes
M50958-XXXSP	12288bytes
M50959-XXXSP	16384bytes

The differences between the M50957-XXXSP and the M50957-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

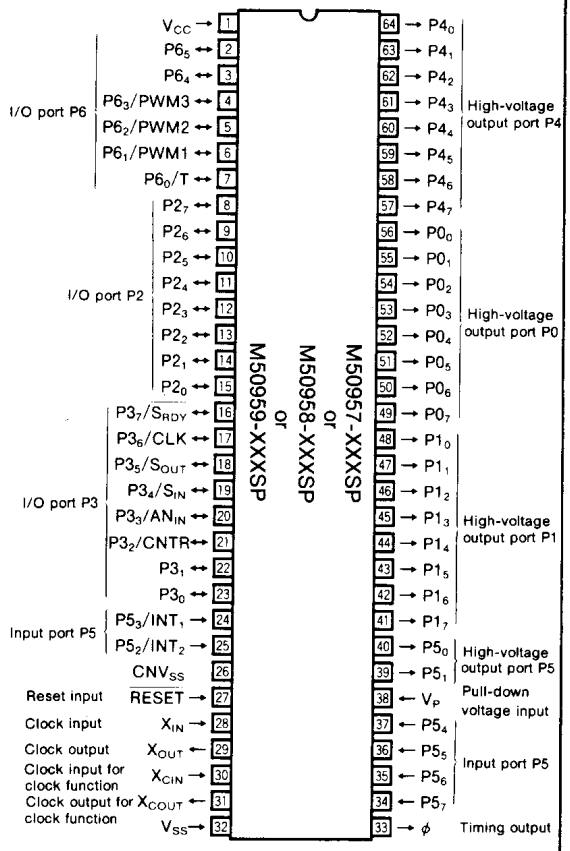
FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 10240 bytes (M50957-XXXSP)
  12288 bytes (M50958-XXXSP)
  16384 bytes (M50959-XXXSP)
  RAM ..... 256 bytes
- Instruction execution time
  ..... 1.9μs (minimum instructions at 4.2MHz frequency)
- Single power supply 4.0~5.5V (at f(X_{IN})=4.2MHz)
  3.0~5.5V (below f(X_{IN})=1.0MHz)
- Power dissipation
  normal operation mode, at 4.2MHz frequency ... 20mW
  low speed operation mode,
  at 32kHz frequency for clock function 0.3mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P2, P3, P6) 22
- Input ports (Port $P5_2$~$P5_7$) 6
- High-voltage output ports
  (Ports P0, P1, P4, $P5_0$, $P5_1$) 26
- Serial I/O (8-bit) 1
- PWM function ..... 14-bit×1
  6-bit×2
- Two clock generator circuits (One is for main clock, the other is for clock function)
- Comparator 1
- Generating function for clock input of EAROM

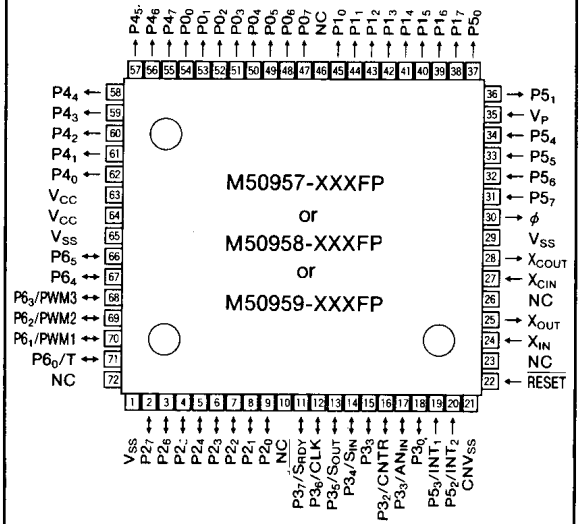
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

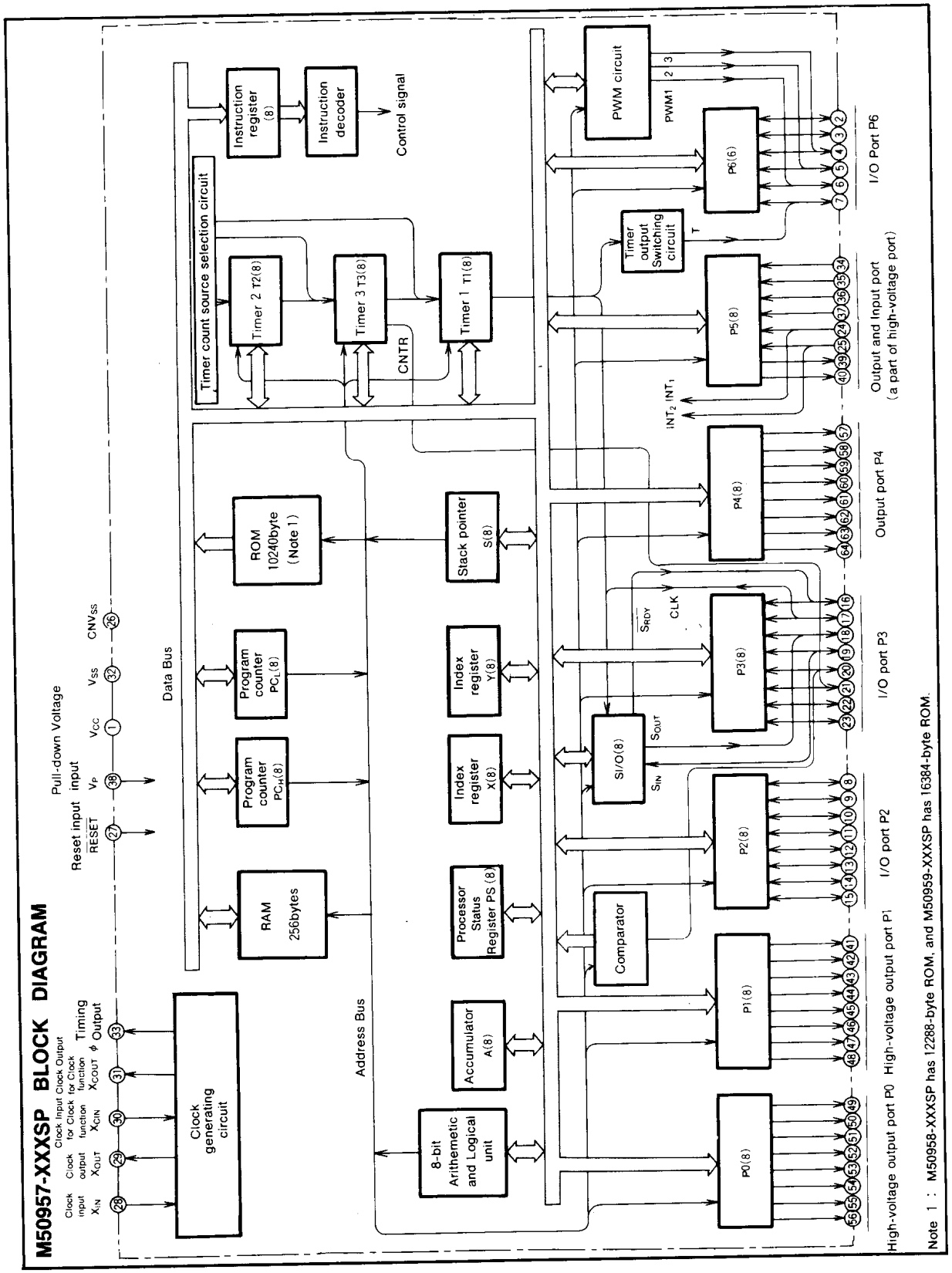


Outline 72P6

NC : No connection

MITSUBISHI ELECTRIC

M50957-XXXSP BLOCK DIAGRAM



Note 1 : M50958-XXXSP has 12288-byte ROM, and M50959-XXXSP has 16384-byte ROM.

FUNCTIONS OF M50957-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1.9μs (minimum instructions, at 4.2MHz frequency)
Clock frequency			4.2MHz
Memory size	ROM		10240bytes (12288bytes for M50958 and16384bytes for M50959)
	RAM		256bytes
Input/output ports	P0, P1, P4	Output	8-bit×3 (high-voltage P-channel open drain; V_{CC}−38V)
	P2, P3	I/O	8-bit×2 (P3 can partially be used as among serial I/O, clock input for timer 3 and normal I/O.)
	$P5_0$, $P5_1$	Output	2-bit×1 (high-voltage P-channel open drain; V_{CC}−38V)
	$P5_2$, $P5_3$	Input	2-bit×1 (can be used as an input for either INT_2 or INT_1.)
	$P5_4$~$P5_7$	Input	4-bit×1
	P6	I/O	6-bit×1 (can be used as T_1 output or PWM output.)
Serial I/O			8-bit×1
Timers			8-bit timer×3 (×2, when used as serial I/O)
Subroutine nesting			96levels (max.)
Interrupt			Two external interrupts, three internal timer interrupts (or timer×2, serial I/O×1)
Clock generating circuit			Two built-in circuits (externally connected ceramic or quartz crystal oscillator)
Supply voltage	at $f(X_{IN})$=4.2MHz		4.0~5.5V
	below $f(X_{IN})$=1.0MHz		3.0~5.5V
Power dissipation	at high-speed operation		20mW (clock frequency X_{IN}=4.2MHz)
	at low-speed operation		0.3mW (clock frequency X_{CIN}=32kHz)
	at stop mode		5μW (when clock is stopped)
Input/Output characteristics	Input/Output voltage		12V (input/output P2, P3, $P5_2$, $P5_3$ except $P3_3$)
			V_{CC}−38V (P0, P1, P4, $P5_0$, $P5_1$)
			−0.3V~V_{CC}+0.3V (input/output P6)
	Output current		10mA (P2, P3 : N-channel open drain)
			−18mA (P0, P1 : high-voltage P-Channel open drain)
			−12mA (P4, $P5_0$, $P5_1$: high-voltage P-Channel open drain)
			0.5~−0.5mA (P6 : CMOS tri-states)
Memory expansion			Possibe
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M50957-XXXSP, M50958-XXXSP, M50959-XXXSP		64-pin shrink plastic molded DIP
	M50957-XXXFP, M50958-XXXFP, M50959-XXXFP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 4.0~5.5V at f(X_{IN})=4.2MHz and 3.0~5.5V below f(X_{IN})=1.0MHz to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1, P4, $P5_0$ and $P5_1$.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	Output port P0	Output	Port P0 is an 8-bit output port. Output structure is high-voltage P-channel open drain. A pull-down transistor is built in between the V_P pin and this port. At reset, this port is set to a "L" level.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P2. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. $P3_3$ works as an analog input for comparator, and $P3_2$ works as a clock input for timer 3.
$P4_0$~$P4_7$	Output port P4	Output	Port P4 is an 8-bit output port and has basically the same functions as port P2.
$P5_0$, $P5_1$	Output port P5	Output	Bit 0 and 1 of port P5 are 2-bit output port and has basically the same functions as port P0.
$P5_2/INT_2$, $P5_3/INT_1$	Input port P5	Input	Bit 2 and 3 of port P5 are 2-bit input port and are in common with interrupt inputs.
$P5_4$~$P5_7$		Input	Bit 4~7 of port P5 are 4-bit input port.
$P6_0$~$P6_7$	I/O port P6	I/O	Port P6 is a 6-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS tri-state output. $P6_0$, $P6_1$, $P6_2$, $P6_3$ can be programmed to function as timer output pin (T), PWM output pins (PWM1, PWM2, and PWM3), respectively.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50957-XXXSP is shown in Figure 1. Addresses $D800_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 10240 bytes.

Addresses $D000_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M50958-XXXSP.

Addresses $C000_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M50959-XXXSP.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $013F_{16}$ are assigned to the built-in RAM and consist of 256 bytes of static RAM. In addition to data storage, this RAM except the area in the page 1 is used for the stack during subroutine calls and interrupts.

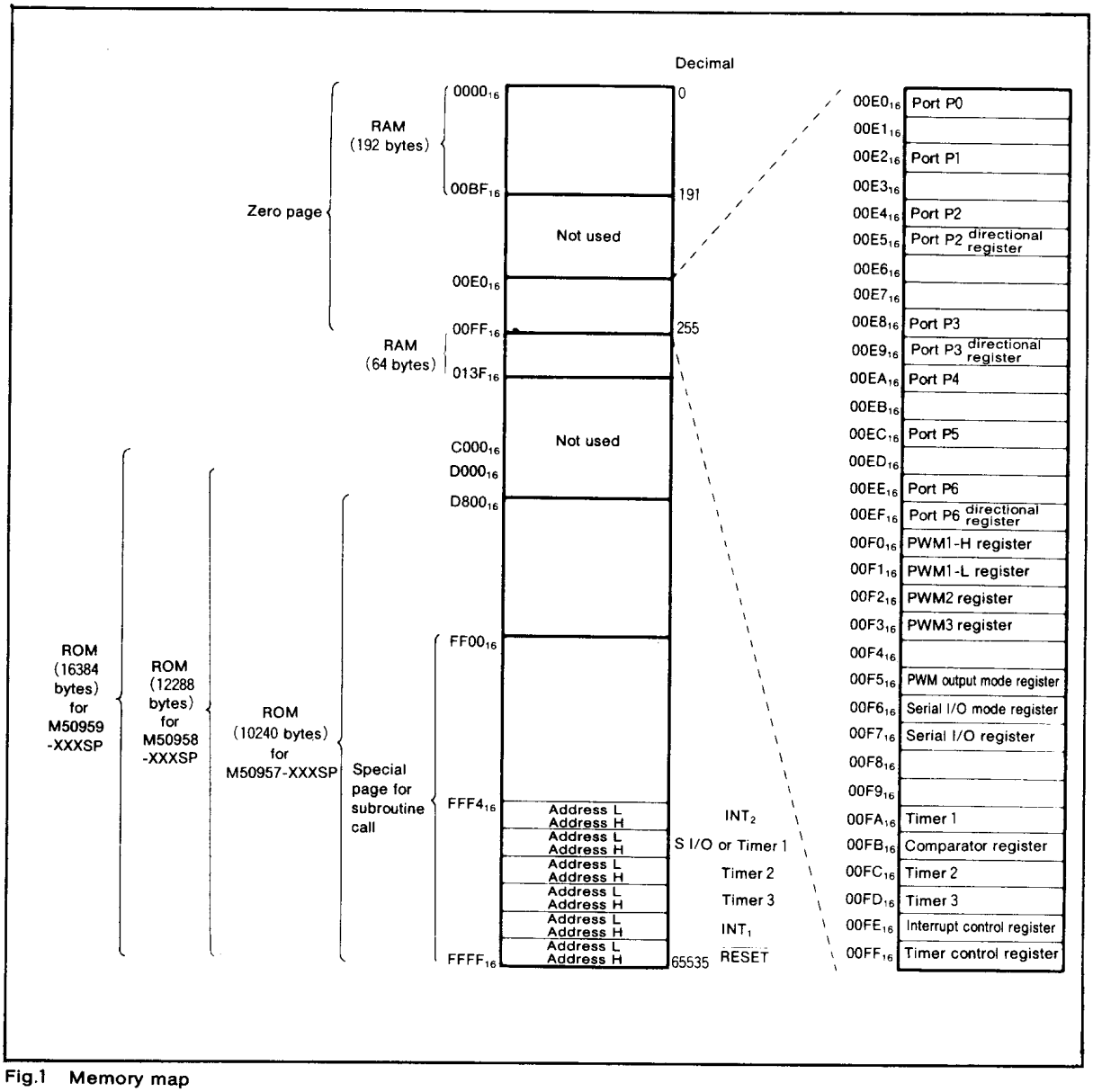


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

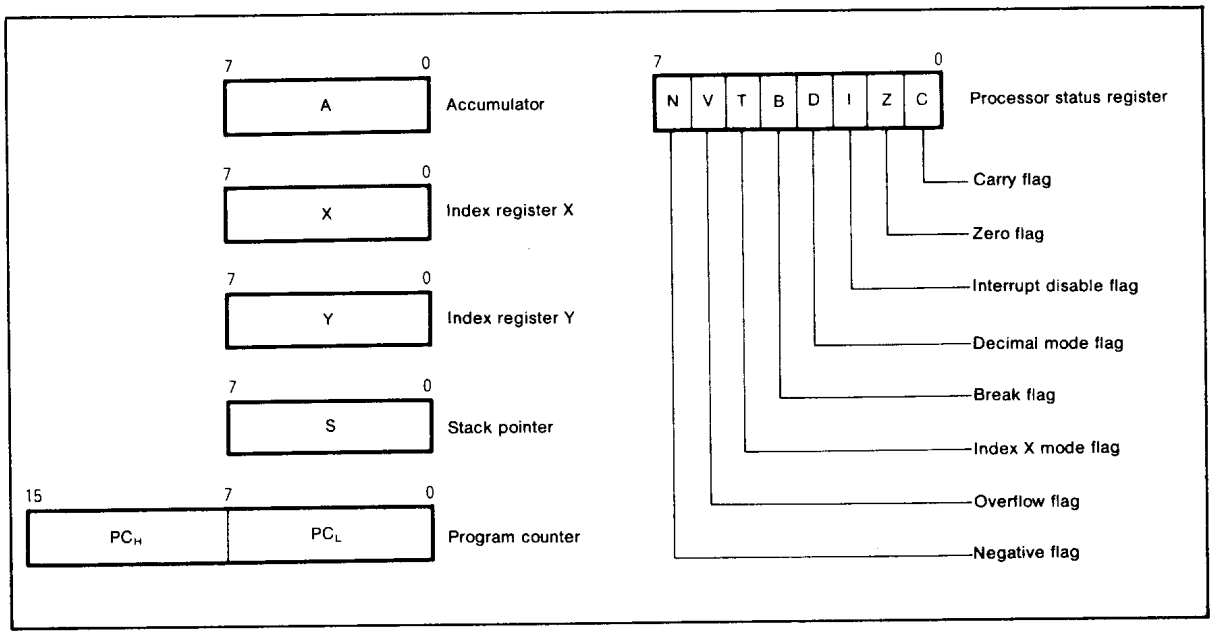


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When using this microcomputer in the single-chip mode, the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal arithmetic can be performed only with the ADC and SBC instructions. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a singed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
INT_1	2	$FFFD_{16}$, $FFFC_{16}$
Timer 3	3	$FFFB_{16}$, $FFFA_{16}$
Timer 2	4	$FFF9_{16}$, $FFF8_{16}$
Timer 1 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
INT_2(BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50957-XXXSP can be interrupted from seven souces; INT_1, timer 3, timer 2, timer 1/serial I/O, or INT_2/BRK instruction.

The value of bit 2 of the serial I/O mode register (address $00F6_{16}$) determine whether the interrupt is from timer 1 or from serial I/O. When bit 2 is "0" the interrupt is from timer 1, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag I is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

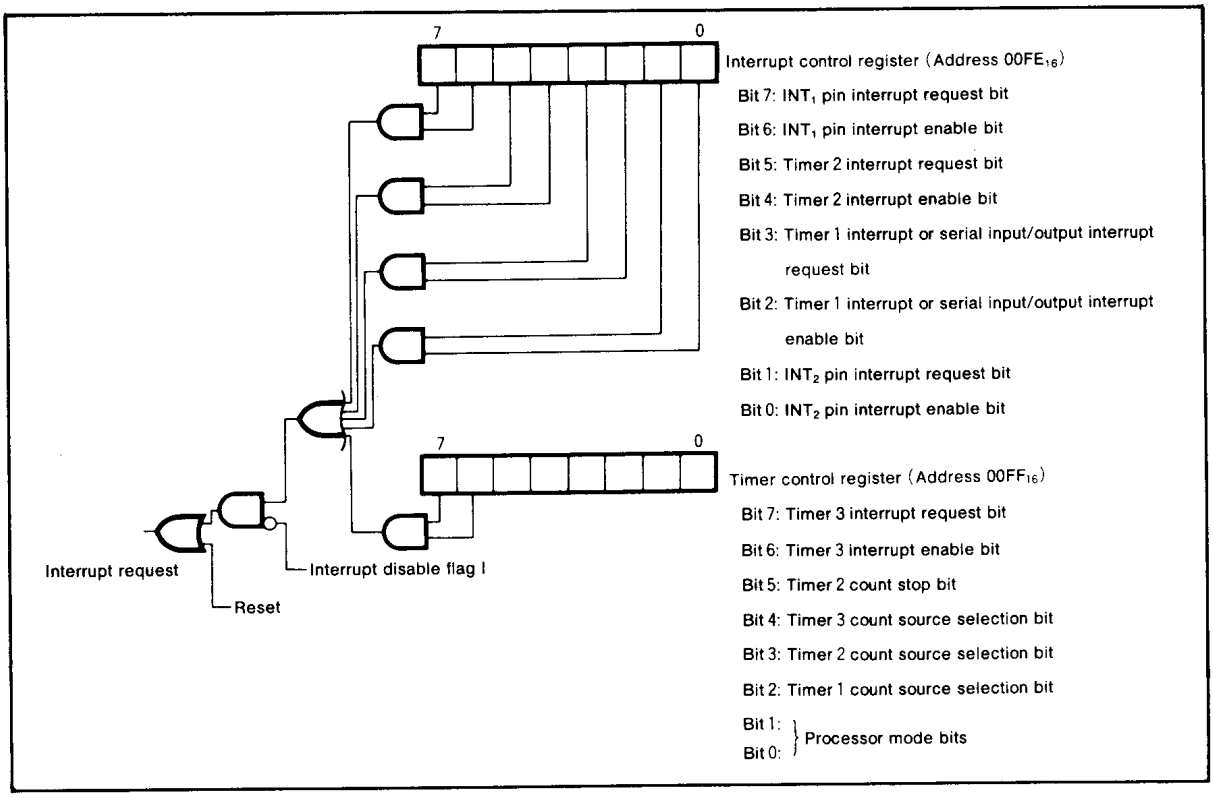


Fig.3 Interrupt control

The interrupt request bits are set when the following conditions occur:

(1) When the level of pins INT_1 and INT_2 change.
(2) When the contents of timer 3, timer 2, timer 1 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but cannot be set by the progream. However, the interrupt enable bit can be set and reset by the program.

The change in level at which the INT pins generate a interrupt varies according to the content of bits 4 and 5 of the PWM output mode register (address $00F5_{16}$). When these bits are "0", the interrupt request is generated when INT changes from high-level to low-level. When these bits are "1", the interrupt request is generated when INT changes from low-level to high-level. Bits 4 (PM_4) and 5 (PM_5) correspond to INT_1 and INT_2 respectively.

Since the BRK instruction and the INT_2 interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if INT_2 generated the interrupt.

TIMER

The M50957-XXXSP has three timers; timer 1, timer 2, and timer 3. Since P3 (in serial I/O mode) and timer 1 use some of the same architecture, they cannot be used at the same time (see serial I/O section). The count source for each timer can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 5.

A block diagram of timer 1 through 3 is shown in Figure 4.

All of the timers are down count timers and have 8-bit latchs. When a timer counter reaches "0", the contents of the reload latch are loaded into the timer at the next clock pulse. The division ratio of the timers is $1/(n+1)$, where n is the contents of the timer latch.

The timer interrupt request bit is set to "1" at the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The starting/stopping of timer 2 can be controlled by bit 5 of the timer control register. If bit 5 (address $00FF_{16}$) is "0", the timer starts counting and when bit 5 is "1", the timer stops. The count source of timer 3 can be controlled by bit 4 of the timer control register. If bit 4 (address $00FF_{16}$) is "1", the timer counts from the $P3_2$/CNTR pin.

When the STP instruction is executed, or after reset, the timer 2 and timer 3 latch are set to FF_{16} and 07_{16}, respectivery.

After a STP instruction is executed, timer 2, timer 3, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if the timer 3 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 2 count stop bit) and bit 4 of the interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

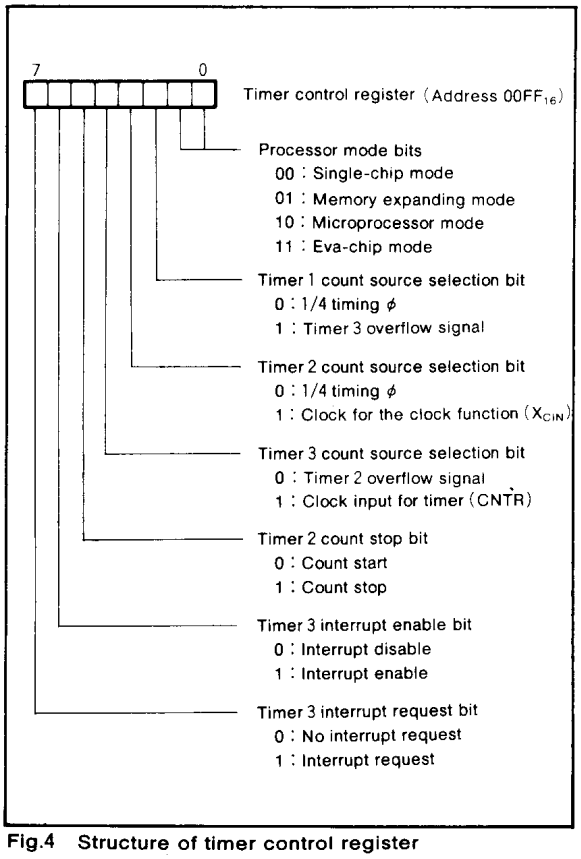


Fig.4 Structure of timer control register

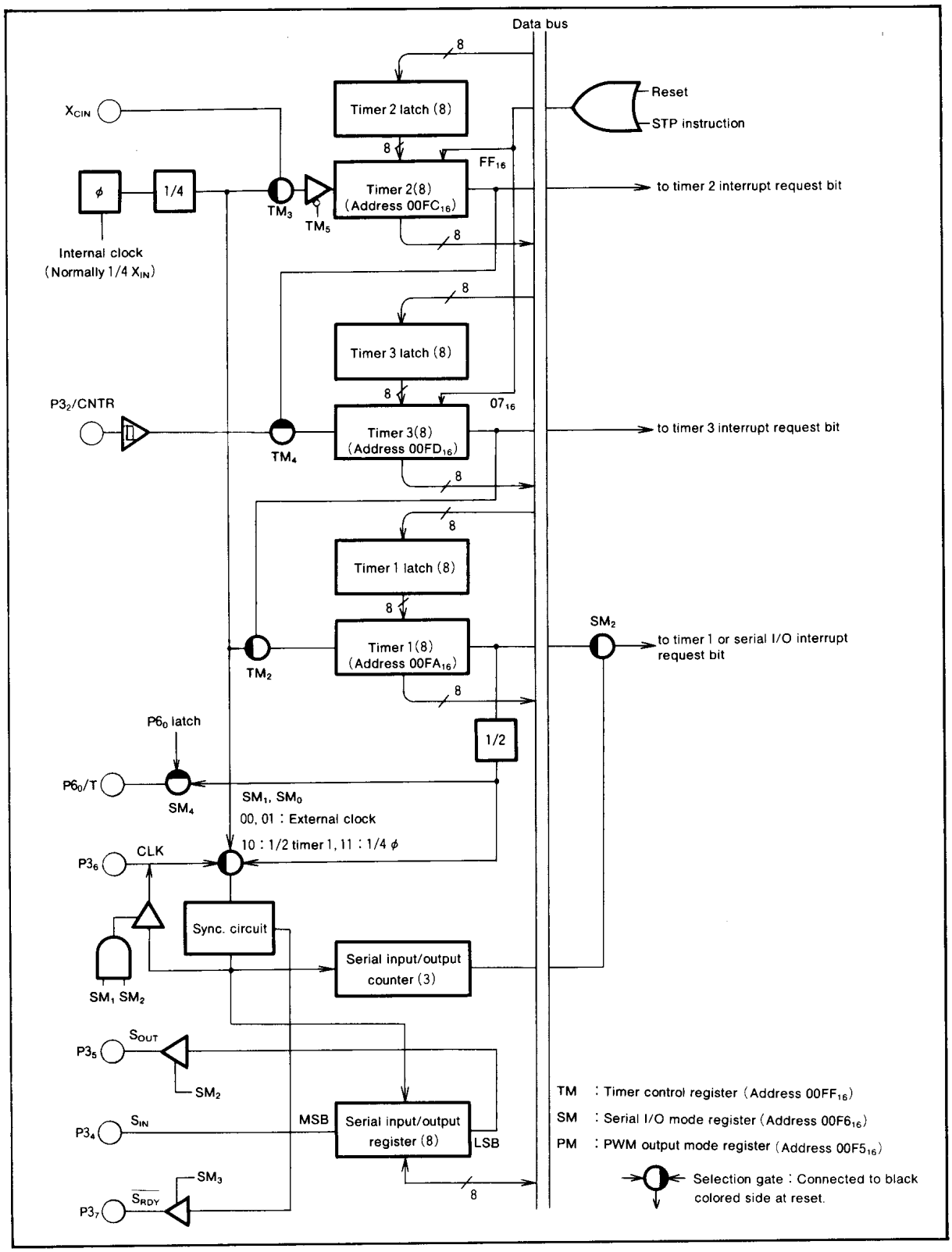


Fig.5 Block diagram of timer 1, timer 2, timer 3

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 6.

In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input /output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is 8-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 1, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], timing ϕ divided by 4, becomes the clock.

Bit 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is a "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 1. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY}}$) or used as normal I/O pin

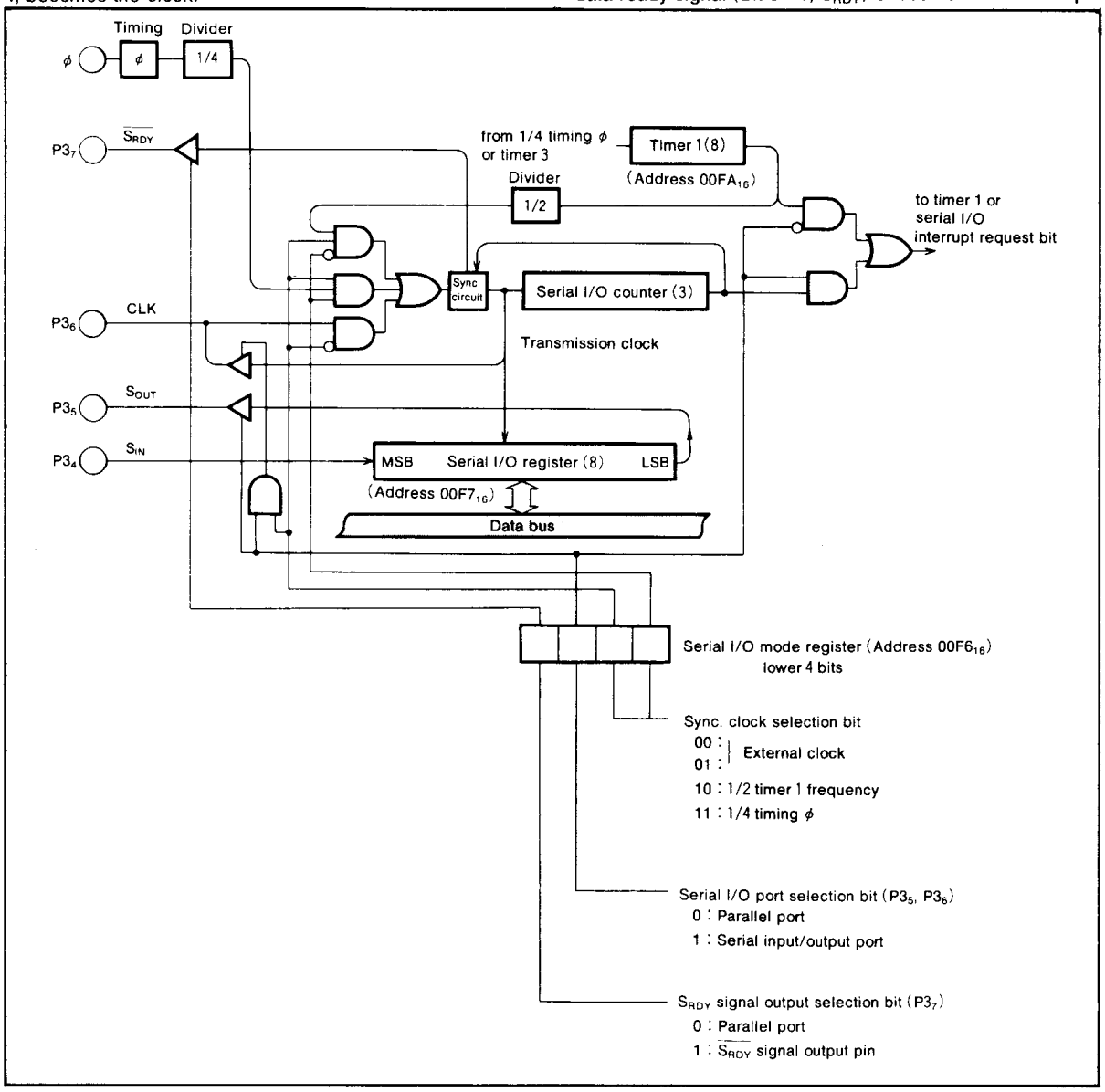


Fig.6 Block diagram of serial I/O

(bit 3=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50957-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 7. An example of communication between two M50957-XXXSPs is shown in Figure 8.

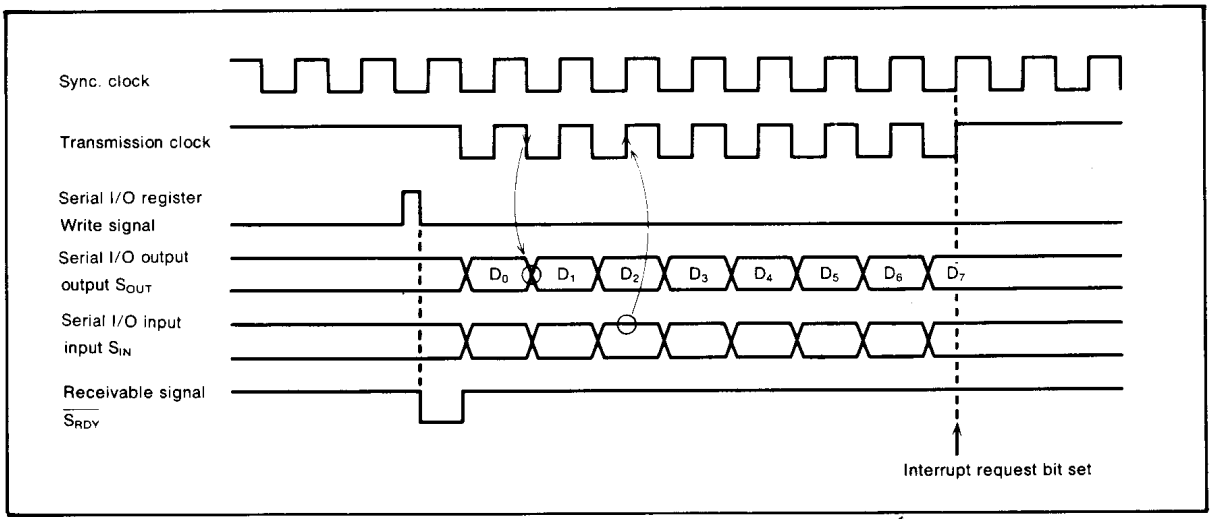


Fig.7 Serial I/O timing

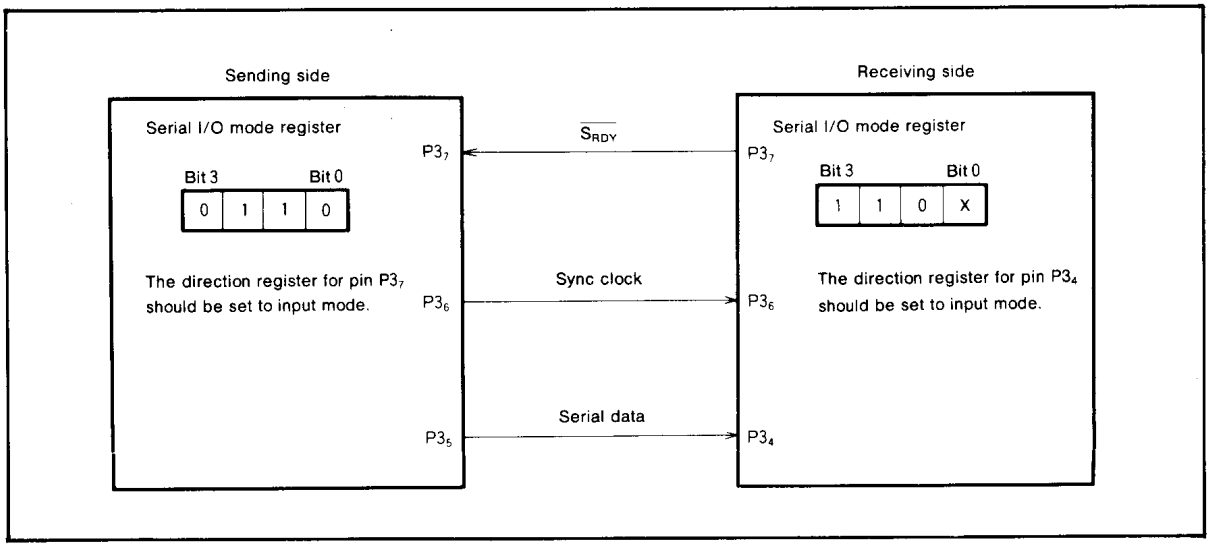


Fig.8 Example of serial I/O connection

PWM OUTPUT CIRCUIT

(1) Introduction

The M50957-XXXSP is equipped with one 14-bit PWM and two 6-bit PWMs. The 14-bit resolution gives PWM1 the minimum resolution bit width of 500ns (for X_{IN} = 4MHz) and a repeat period of 8192μs. PWM2 and PWM3 have a 6-bit resolution with minimum resolution bit width of 16μs and repeat period of 1024μs.

Block diagram of the PWM is shown in Figures 9 and 10.

The PWM timing generator section applies individual control signals to PWM 1~3, using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM1, PWM2 and PWM3 are in common with pins $P6_1$, $P6_2$ and $P6_3$ of port P6 (i.e. for PWM output, PM1~PM3 of the PWM control register and the P6 directional register $D6_1$~$D6_3$ should be set). When PWM1 is used for output, first set the higher 8-bit of the PWM1-H register (address $00F0_{16}$), then the lower 6-bit of the PWM1-L register (address $00F1_{16}$). In case of M50958-XXXSP and M50959-XXXSP, if the low-order 6 bits are the same, this is also possible by changing the H register only. When either PWM2 or PWM3 is used for output, set the 6-bit in the PWM2 (address $00F2_{16}$) or PWM3 (address $00F3_{16}$) register, respectively. Note that the higher 2 bits of these 8-bit registers are ignored when used 6-bit register.

(3) Transferring data from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data at addresses $00F0_{16}$ ~ $00F3_{16}$ is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. When the 6-bit latch is being read, the upper 2 bits of the register becomes undefined. However, bit 7 of the PWM1-L register indicated the completion of the data transfer from the PWM1 register to the PWM1 latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 6-bit PWMs

The timing diagram of the two 6-bit PWMs (PWM2 and PWM3) is shown in Figure 10. One period (T) is composed of 64 (2^6) segments.

There are six different pulse types configured from bits 0~5 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 11(a).

Six different pulses can be output from the PWM. These can be selected by bits 0 through 5. Depending on the content of the 6-bit PWM latch, pulses from 5~0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 11(b). Changes in the contents of the PWM latch allows the selection of 64 lengths of high-level area outputs varying from 0/64 to 63/64. An length of entirely high-level output cannot be output, i.e. 64/64.

(5) 14-bit PWM operation

The timing diagram of the 14-bit PWM1 is shown in Figure 11. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length N times τ is output every short area of t = 256 τ = 128μs as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 12 and 13.)

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ. As a result, the short-area period t (= 128μs, approx. 7.8kHz) becomes an approximately repetitive period.

(6) Output after reset

At reset the output of port P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data (LSB)	Area longer by τ than that of other t_m (m = 0 ~63)
0 0 0 0 0 0	Nothing
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m= 8, 24, 40, 56
0 0 1 0 0 0	m= 4, 12, 20, 28, 36, 42, 50, 58
0 1 0 0 0 0	m= 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m= 1, 3, 5, 7, ····· 57, 59, 61, 63

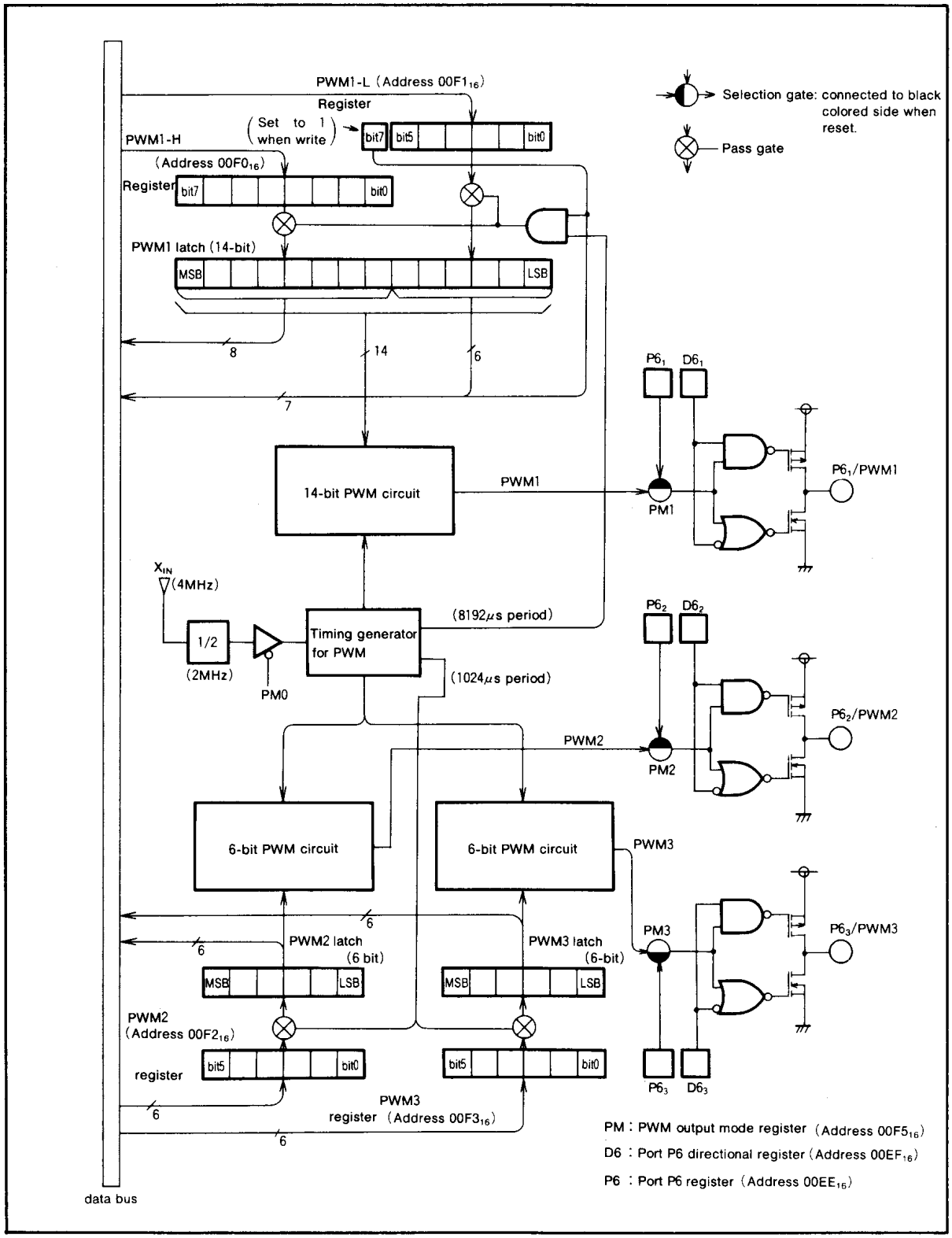


Fig.9 Block diagram of the PWM circuit (M50957-XXXSP)

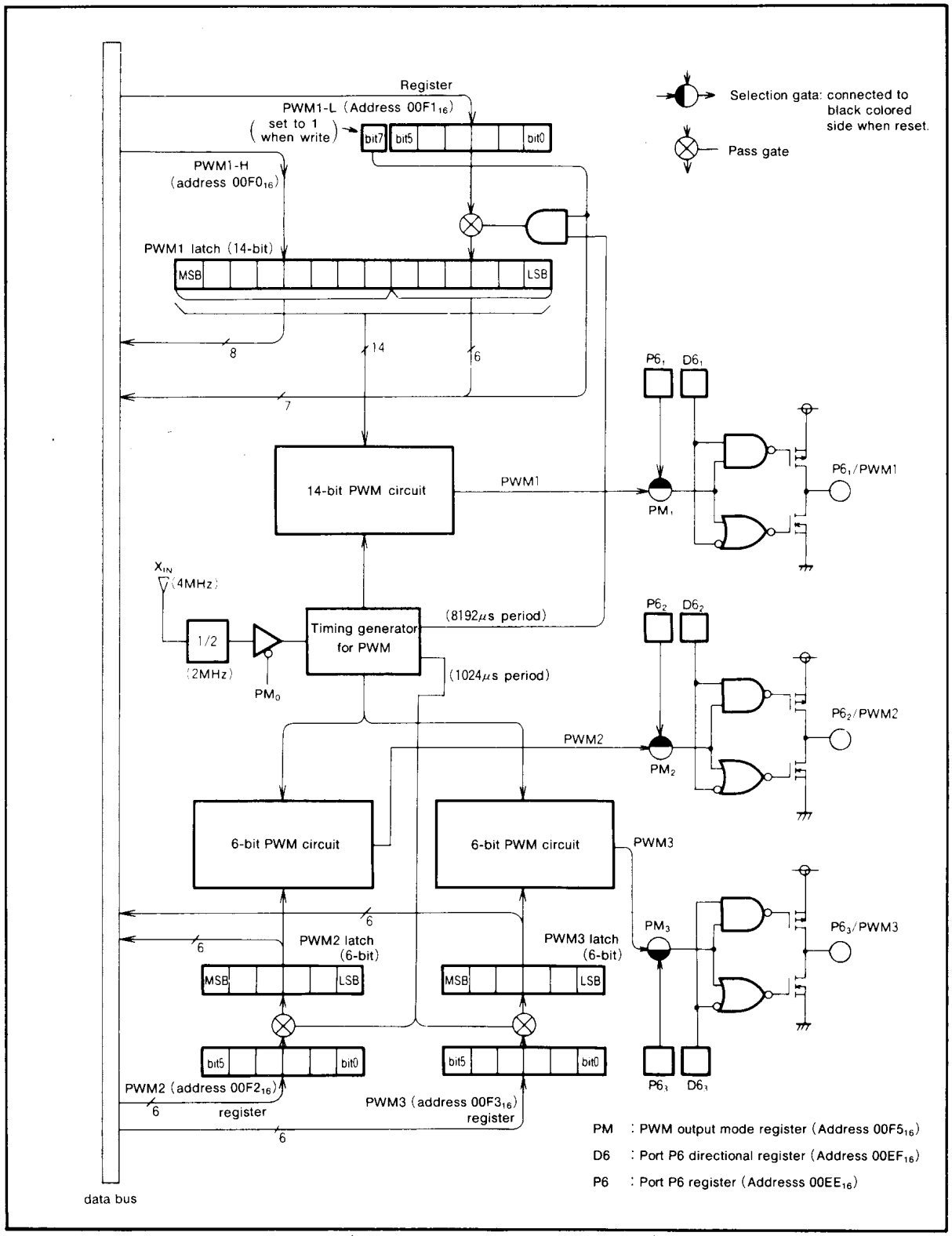


Fig.10 Block diagram of the PWM circuit (M50958-XXXSP and M50959-XXXSP)

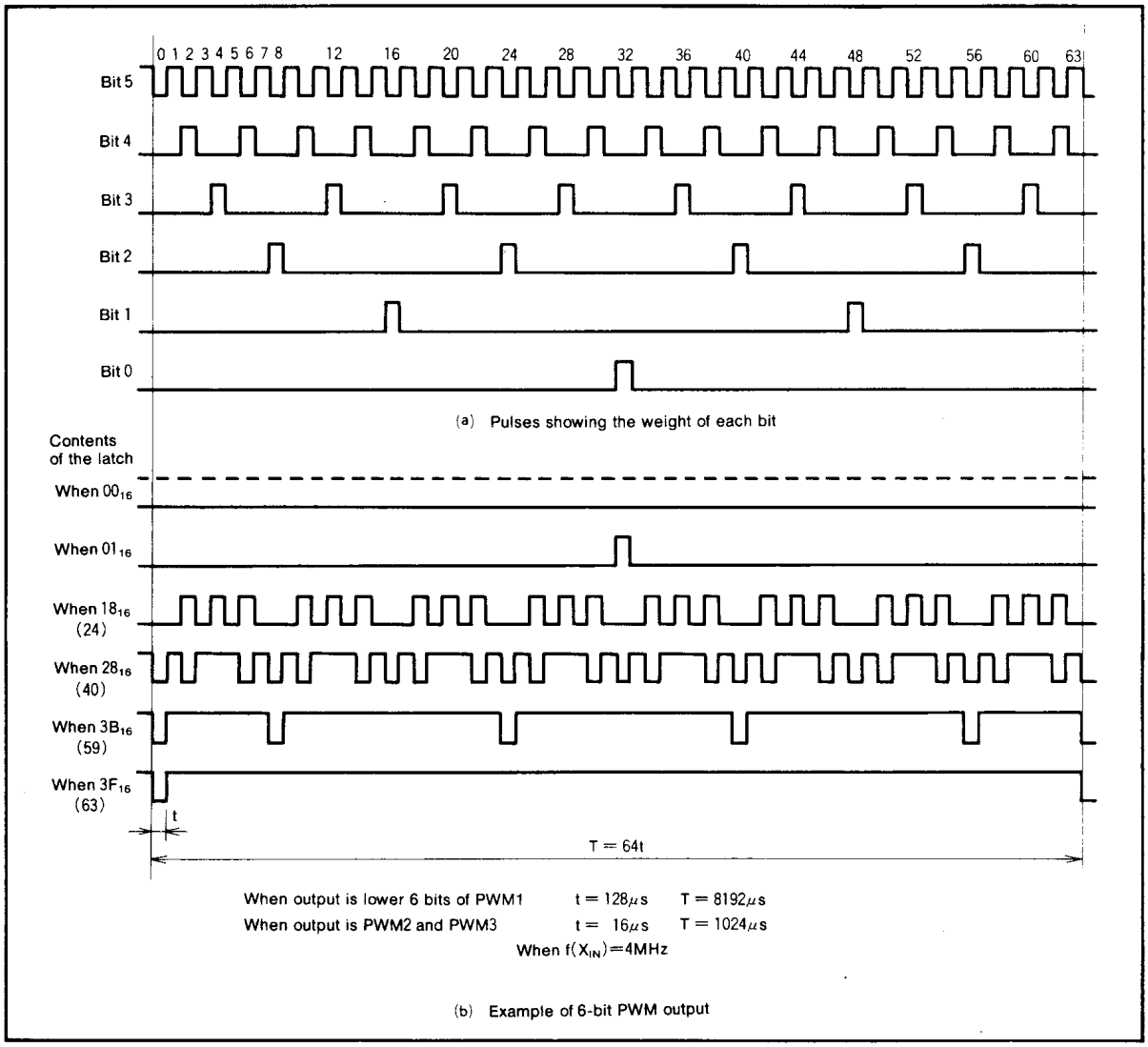


Fig.11 6-bit PWM timing diagram

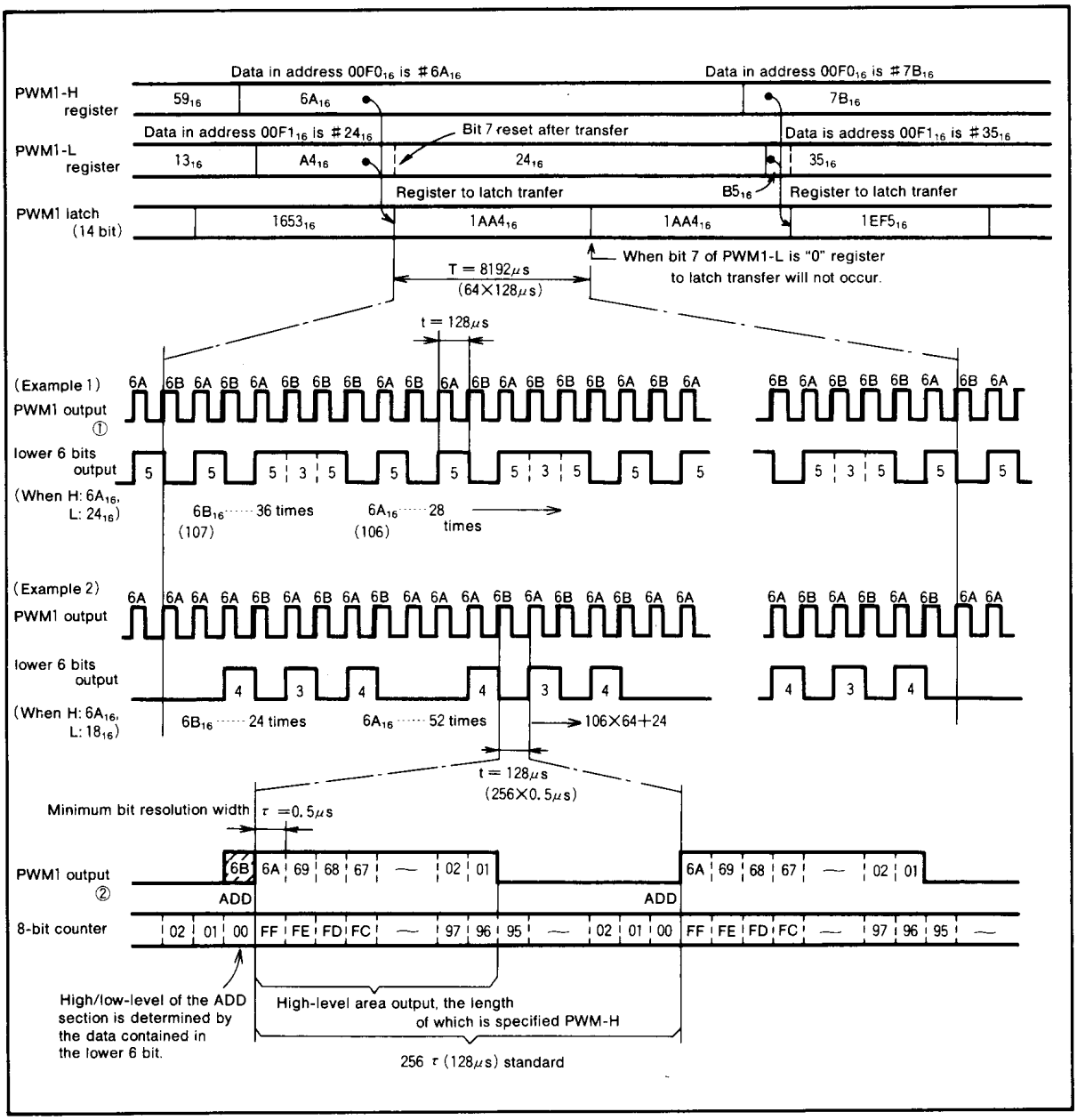


Fig.12 14-bit PWM timing diagram (M50957-XXXSP)

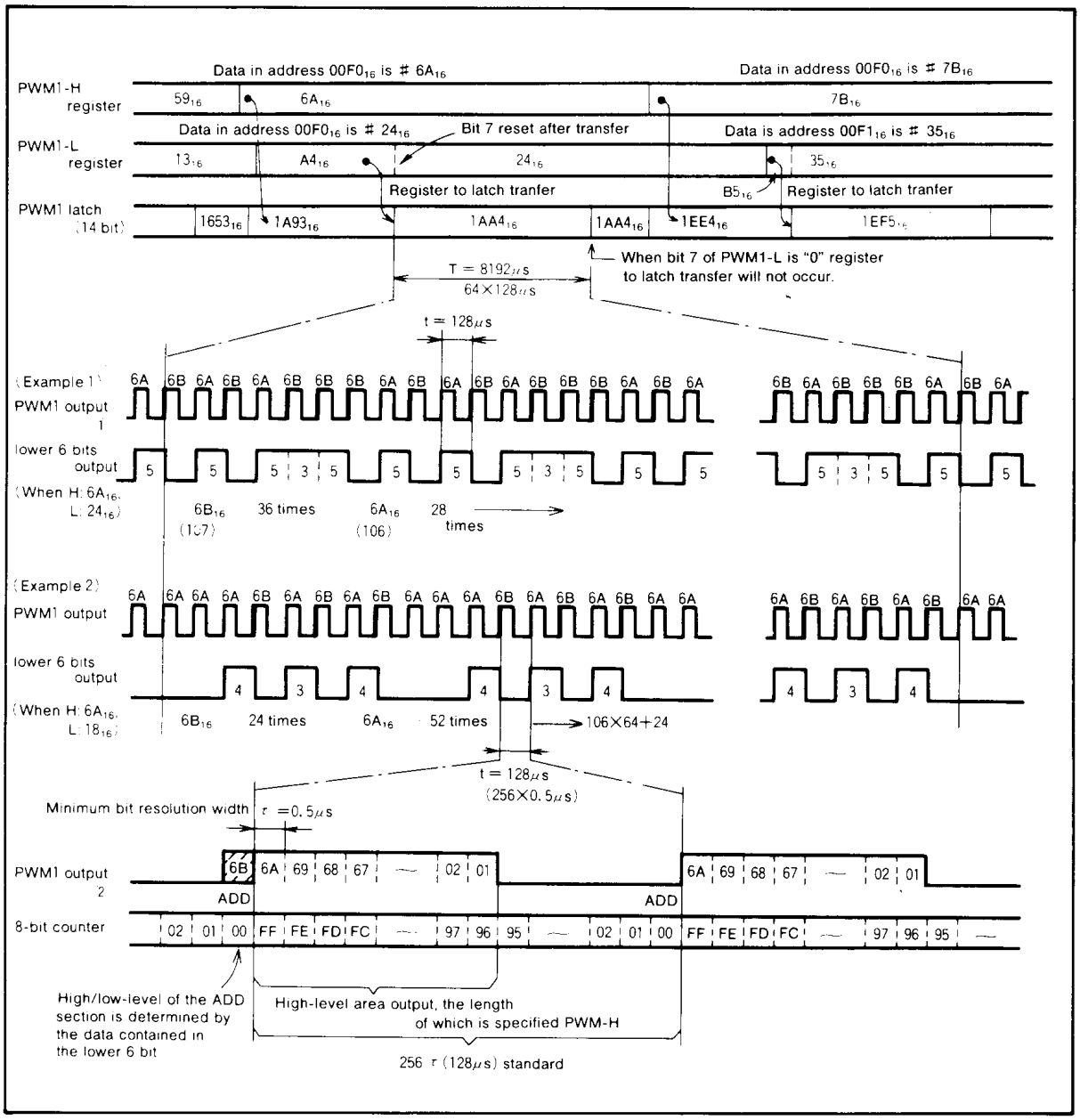


Fig.13 14-bit PWM timing diagram (M50958-XXXSP and M50959-XXXSP)

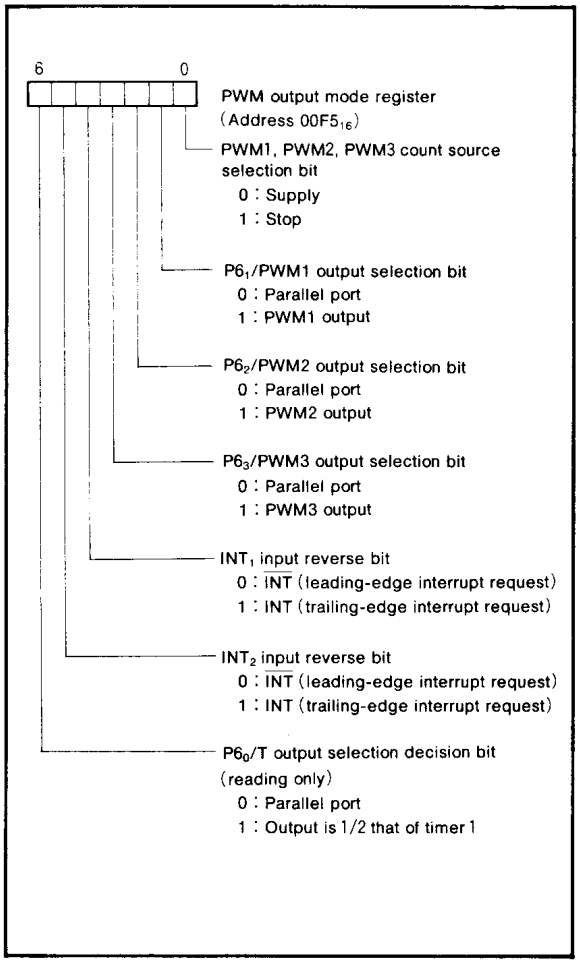


Fig.14 Structure of PWM output mode register

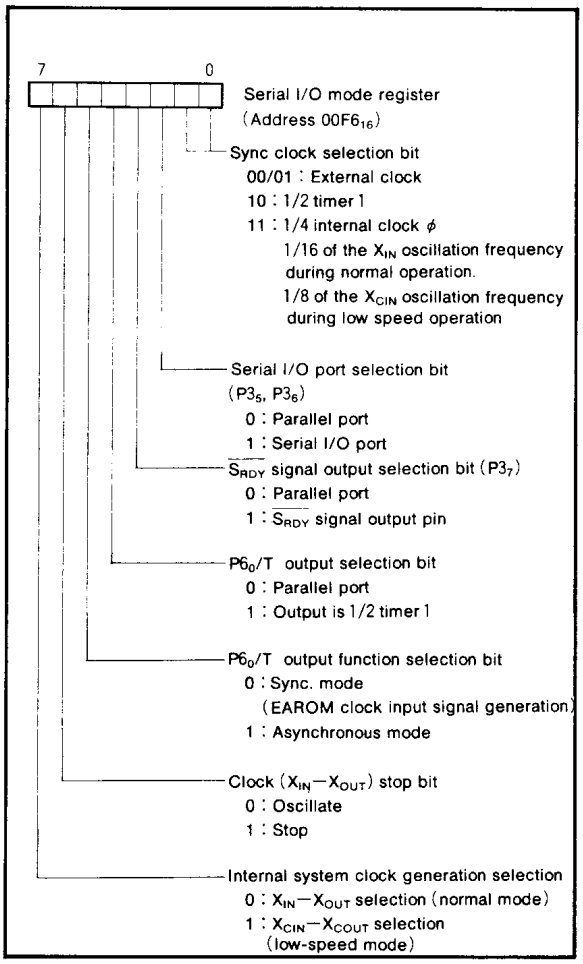


Fig.15 Structure of serial I/O mode register

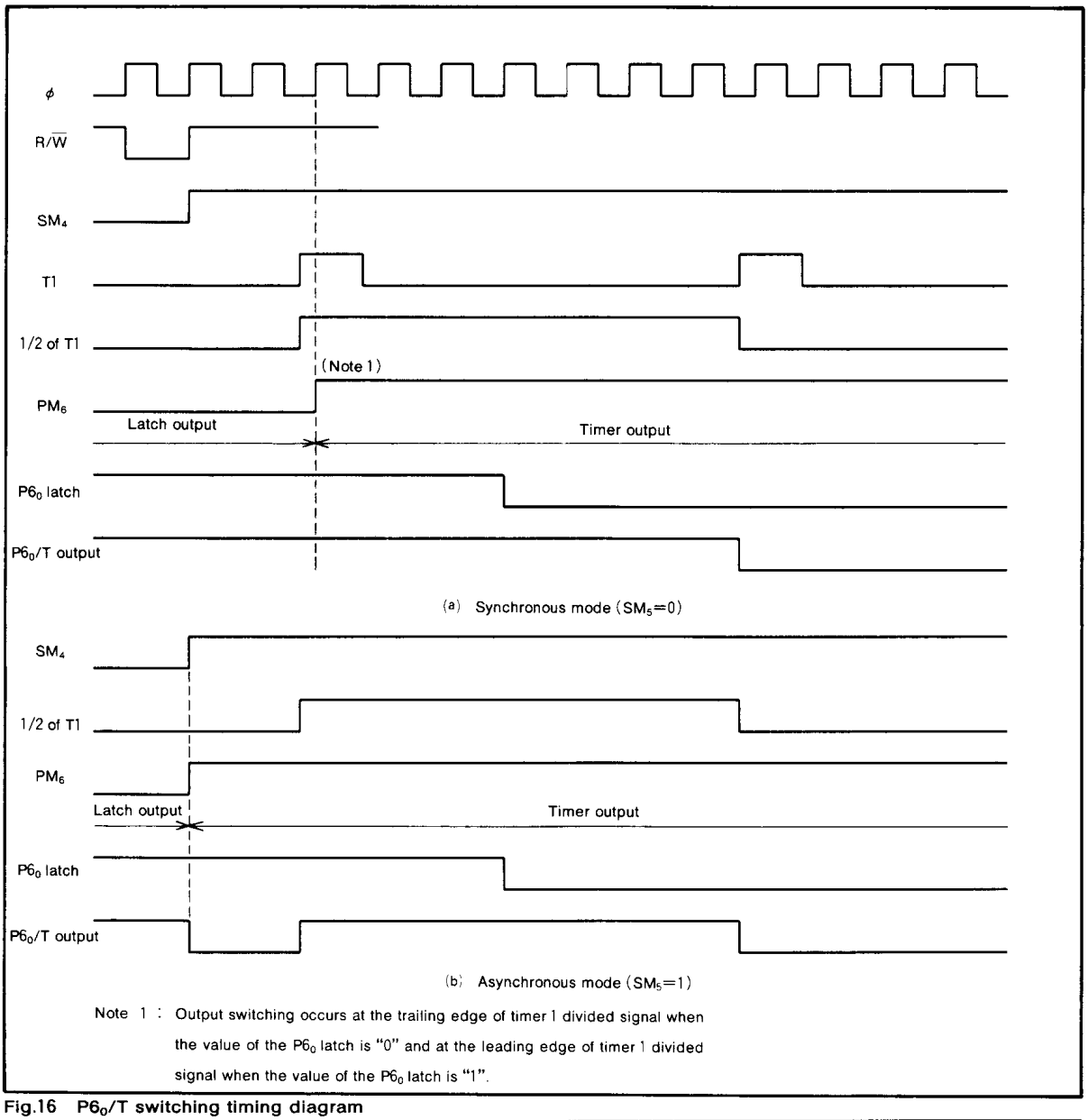
PORT $P6_0$/TIMER 1 OUTPUT

Bit 0 of port P6 outputs 1/2 the frequency of timer 1 when bit 4 of the serial I/O mode register (address $00F6_{16}$) is changed. The output switching can be accomplished with either of two procedures, synchronous mode or asynchronous mode, depending on the setting of bit 5 (SM_5) of the serial I/O mode register.

When SM_5 is set to "0" the synchronous mode is set. In such a case, after SM_4 has been changed, synchronization is set to the 1/2 frequency of timer 1 and switching between the port latch and timer takes place. It is possible to ascertain whether switching actually occurred by reading the value of bit 6 (PM_6) of the PWM output mode register.

From the time that the contents of SM_4 was changed to the point where switching completes, the contents of neither SM_4 nor $P6_0$ may be changed. Use of the synchronous mode prevents the generation of a pulse shorter than the timer output during switching. Figure 16 (a) gives an example of timing in the synchronous mode. Use of the synchronous mode allows generation of an EAROM clock input signal through the use of a simple program.

When SM_5 is set to "1", the asynchronous mode is set. In this case, the output switching occurs directly after SM_4 has been changed. Figure 16 (b) gives an example of timing in the asynchronous mode.



Note 1 : Output switching occurs at the trailing edge of timer 1 divided signal when the value of the $P6_0$ latch is "0" and at the leading edge of timer 1 divided signal when the value of the $P6_0$ latch is "1".

Fig.16 $P6_0$/T switching timing diagram

COMPARATOR CIRCUIT

The comparator circuit is shown in Figure 17. The comparator circuit consists of the switch tree, ladder resistor, comparator, comparator control circuit, comparator register (address $00FB_{16}$), and analog signal input pin ($P3_3/AN_{IN}$). The analog input pin is common with the digital input/output terminal to the data bus.

The 5-bit comparator register can generate $1/16V_{CC}$-step internal analog voltage, based on the settings of bits 0 to 3. Table 3 gives the relation between the descriptions of comparator register bits 0 to 3 and the generated internal analog voltage. The comparator result of the analog input voltage and the internal analog voltage is stored in the comparator register, bit 4.

The data is compared by setting the directional register corresponding to port $P3_3$ to "0" (port $P3_3$ enters the input mode), to allow port $P3_3/AN_{IN}$ to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the comparision register (address $00FB_{16}$), bits 0 to 3. The voltage comparision starts as soon as the writing is completed. 4-cycle (required for comparating) later, the result of comparison is stored in the comparator register, bit 4. Bit 4 is "1" when analog input voltage > internal analog voltage and "0" when analog input voltage < internal analog voltage.

When voltage is compared to by setting bits 0 to 3 of the comparator register "0", bit 4 of the comparator register becomes "1" regardless of the analog input voltage.

Table 3. Relationship between the contents of comparator register and internal voltage

Comparator register				Internal analog voltage
bit 3	bit 2	bit 1	bit 0	
0	0	0	1	$1/16V_{CC}-1/32V_{CC}$
0	0	1	0	$2/16V_{CC}-1/32V_{CC}$
0	0	1	1	$3/16V_{CC}-1/32V_{CC}$
0	1	0	0	$4/16V_{CC}-1/32V_{CC}$
0	1	0	1	$5/16V_{CC}-1/32V_{CC}$
0	1	1	0	$6/16V_{CC}-1/32V_{CC}$
0	1	1	1	$7/16V_{CC}-1/32V_{CC}$
1	0	0	0	$8/16V_{CC}-1/32V_{CC}$
1	0	0	1	$9/16V_{CC}-1/32V_{CC}$
1	0	1	0	$10/16V_{CC}-1/32V_{CC}$
1	0	1	1	$11/16V_{CC}-1/32V_{CC}$
1	1	0	0	$12/16V_{CC}-1/32V_{CC}$
1	1	0	1	$13/16V_{CC}-1/32V_{CC}$
1	1	1	0	$14/16V_{CC}-1/32V_{CC}$
1	1	1	1	$15/16V_{CC}-1/32V_{CC}$

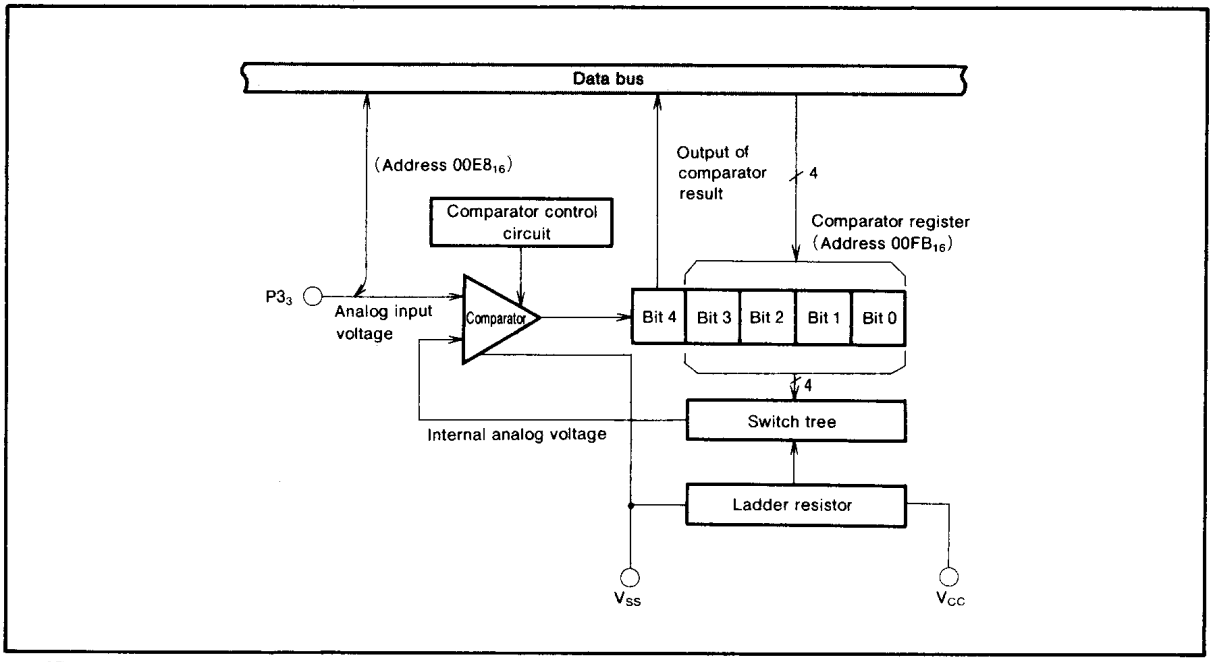


Fig.17 Comparator Circuit

RESET CIRCUIT

The M50957-XXXSP is reset according to the sequence shown in Figure 18. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 2 μs while the power voltage is between 4 and 5.5V and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 19.

An example of the reset circuit is shown in Figure 20. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.0V.

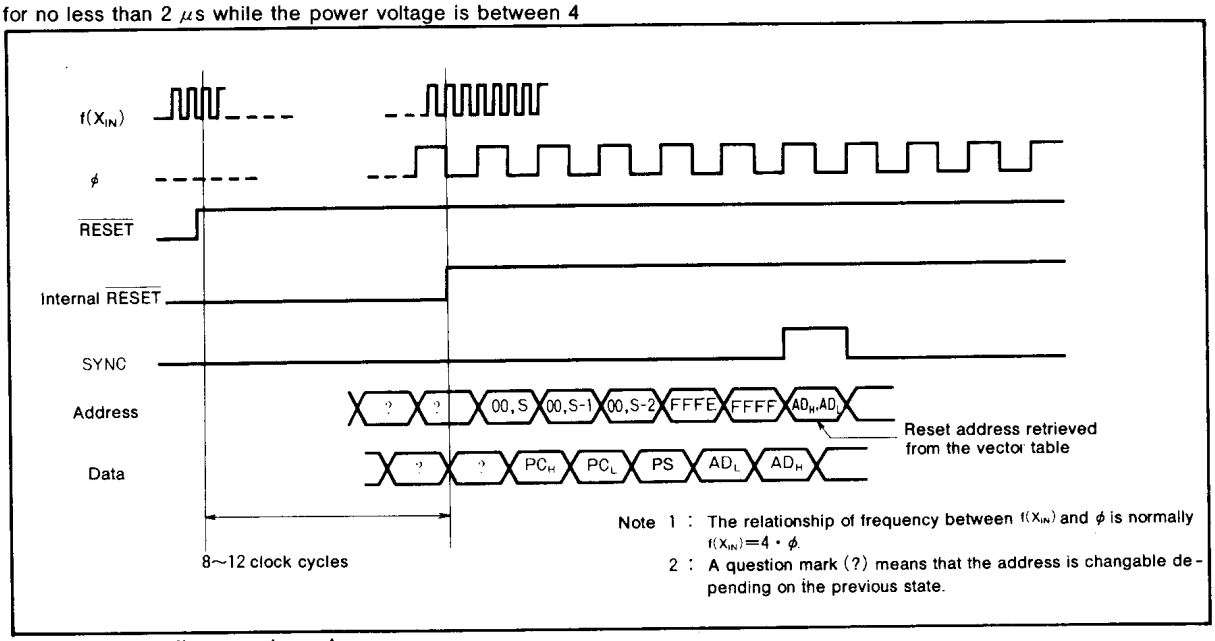


Fig.18 Timing diagram at reset

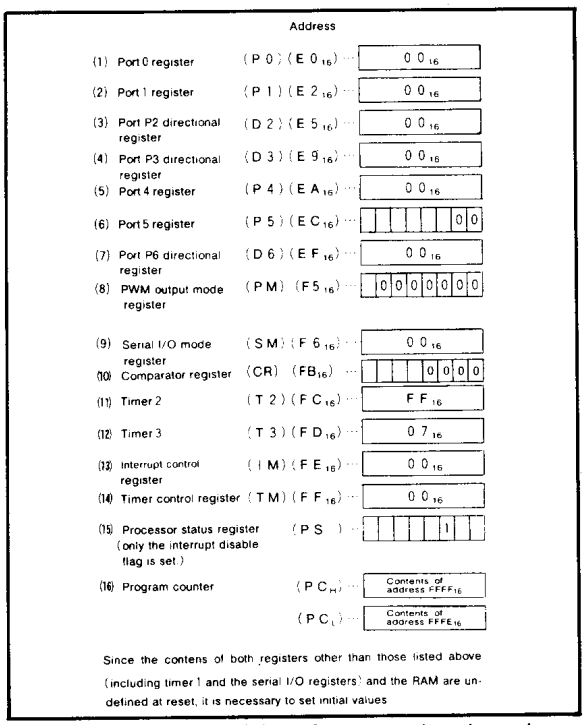


Fig.19 Internal state of the microcomputer at reset

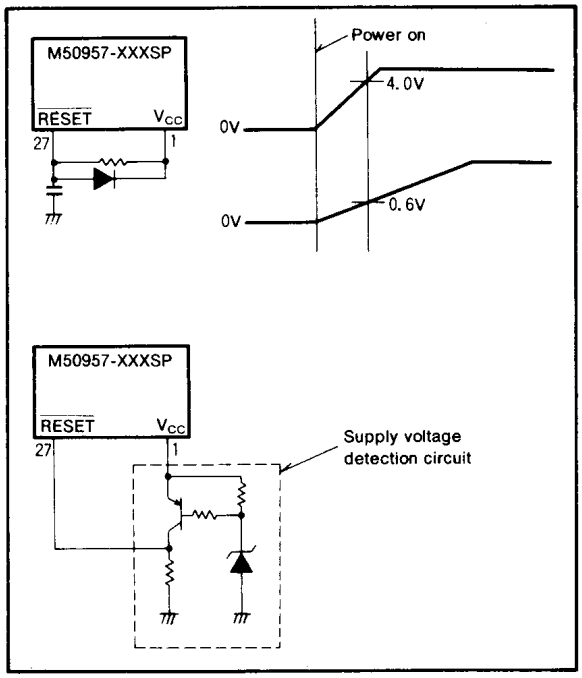


Fig.20 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit output port with high-breakdown voltage P-channel open drain outputs featuring a breakdown voltage of V_{CC}-36V. Each pin contains a pull-down resistor making V_P a negative power source. As shown in the memory map in Figure 1, port P0 is used on the zero page at address $00E0_{16}$ in memory.

Depending on the content of the processor mode bit (bits 0 and 1 of address $00FF_{16}$), four modes can be selected, single-chip mode, memory expanding mode, microprocessor mode, memory expanding mode, microprocessor mode, and eva-chip mode. Modes other than the single-chip mode also have functions as address output pins besides their original functions. For details, refer to the section on the processor mode.

(2) Port P1

Port P1 has the same functions as port P0 in the single-chip mode. In modes other than the single-chip mode, functions vary slightly. For details, see the section on the processor mode.

(3) Port P2

Port P2 is an 8-bit I/O port with N-channel open drain outputs As shown in Figure 1, port P2 is used at address $00E4_{16}$ in the memory.

Port P2 has a data direction register (address $00E5_{16}$ on zero page) and programming can be undertaken for an individual bit to use the port for input or output. The pins where the data direction register is programmed to "1" are for output and those where the register is programmed to "0" are for input.

The data written into the pin programmed as an output pin are written into the port latch and supplied directly to the output pin. When reading the data from a pin programmed as an output pin, it is not the output pin contents which are read but the port latch contents. Consequently, since an LED or other similar part is driven directly, the value output previously can be read correctly even if the low-level output voltage goes high. The pin programmed as an input pin remains floating, so external signals can be read. When data is written, it is written into the port latch only and the pin remains floating.

This port has the same functions as port P0 except for the single-chip mode. For details, see the section on the processor mode.

(4) Port P3

Apart from the fact that part of the pins are also used as serial input/output pins, analog input pin and timer 3 clock input pin, its functions are the same as those of port P2 in the single-chip mode. This port has the same functions as port P0 except in the single-chip mode. For details, see the section on the processor mode.

(5) Port P4

Port P4 has the same functions as port P0 in the single-chip mode. The functions of this port do not change regardless of though the processor mode.

(6) Port P5

Bits 0 and 1 of port P5 have the same functions as port P4.

Bits 2 and 3 are exclusively used as inputs for mutual use as interrupt inputs. These pins feature hysteresis characteristics. These pins can also be used for fetching inputs even when being used as interrupt inputs.

The interrupt request bits (bit 7 and 1 of address $00FE_{16}$ = INT_1 and INT_2, respectively) are set to "1" when the inputs of ports $P5_3$ (INT_1) and $P5_2$ (INT_2) change. Depending on the contents of bits 4 and 5 of the PWM output mode register PM (address $00F5_{16}$), either a raising-edge interrupt or a falling-edge interrupt may be selected as the interrupt source. (Refer to Figure 14.)

Since interrupt input and normal input ports are used together in the M50957-XXXSP, unwanted noise may mistakenly cause interrupts. This problem can be overcome by programming.

When changing either bit 4 (PM_4) or bit 5 (PM_5) of the PWM output mode register, it is necessary for the interrupt request enable bit (either bit 6 or 0 of address $00FE_{16}$) to be set to the interrupt disable condition ("0"). If this is not done, an interrupt will be generated when either PM_4 or PM_5 is changed.

Bits 4 through 7 of port P5 is a 4-bit input port.

(7) Port P6

Port P6 is a 6-bit I/O port having the same functions as Port P2. The output is CMOS three-state. Bit 0 is used in common with the timer output. Bits 1~3 are used in common with PWMs 1~3.

The functions of this port do not change, being the same as in the single-chip mode, even though the processor mode may change.

A block diagram of ports P0 through P6 are shown in Figure 21.

(8) Clock ϕ output pin

The clock frequency, divided by four, is output (X_{IN}). However, in the low-speed mode 1/2 the clock frequency for timer (X_{CIN}) is output.

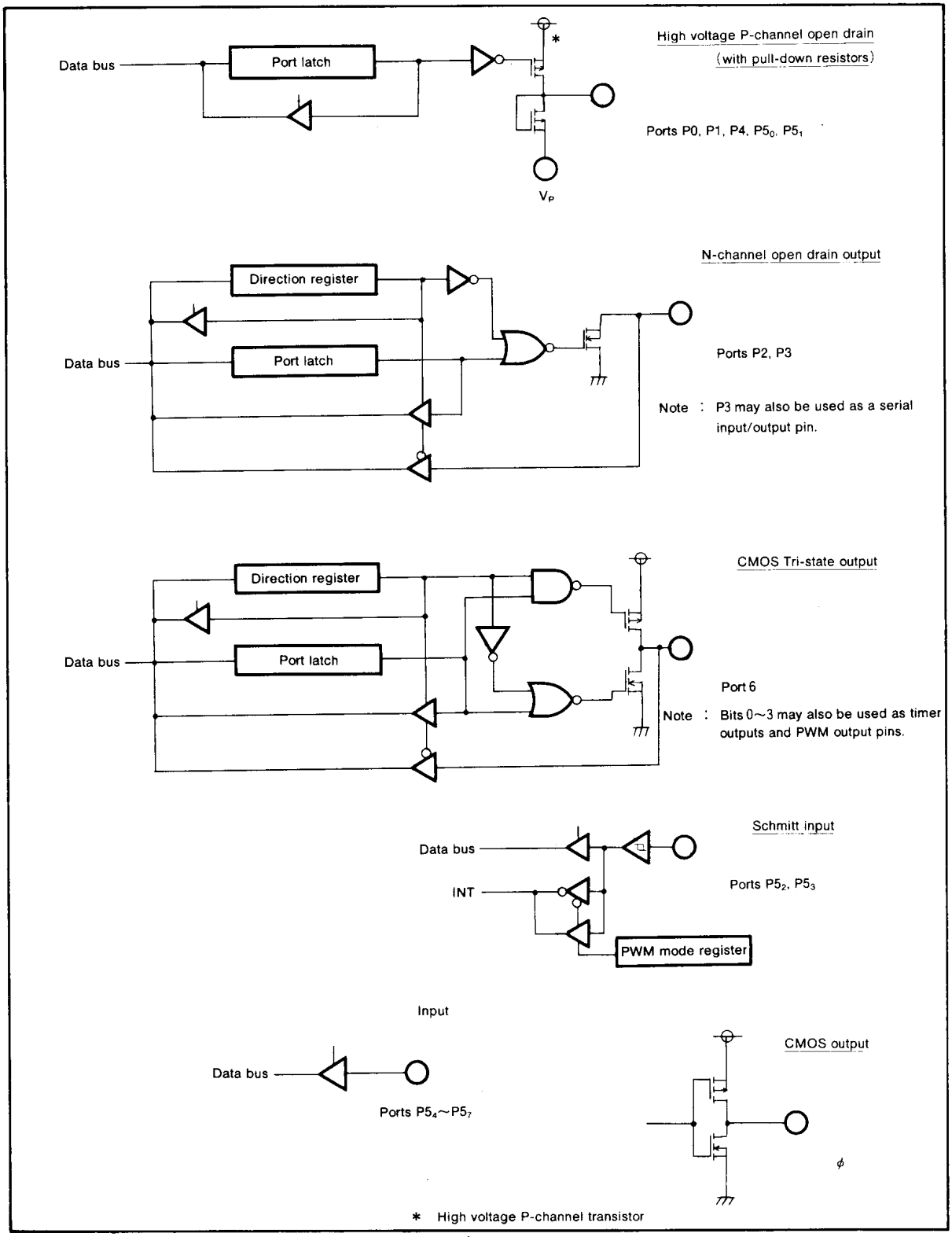


Fig.21 Block diagram of port P0~P6 (single-chip mode) and output format of ϕ

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 23 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 22.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

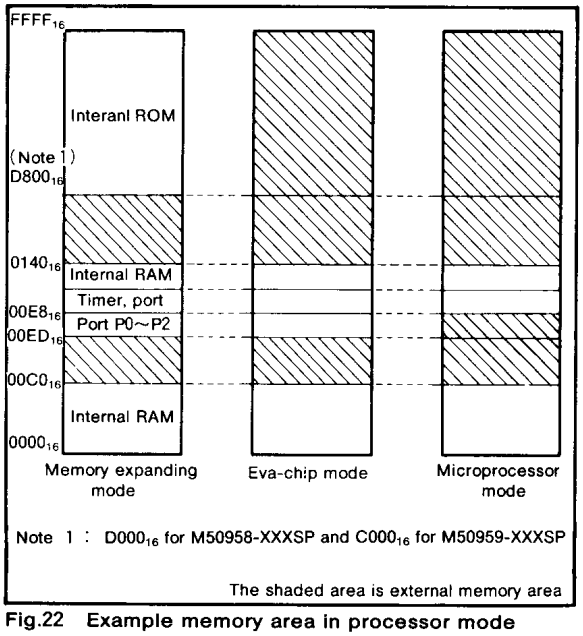


Fig.22 Example memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original output functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original output functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus (D_7～D_0) and loses its normal output functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is required.

This mode has almost the same function as the memory expanding mode except that it needs to attach all program memories to the outside.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

Port \ Mode	Single-chip mode (TM_1=0, TM_0=0)	Memory expanding mode (TM_1=0, TM_0=1)	Eva-chip mode (TM_1=1, TM_0=1)	Microprocessor mode (TM_1=1, TM_0=0)
Port P0	ϕ Ports $P0_7$~$P0_0$ I/O port	ϕ Ports $P0_7$~$P0_0$ Address A_7~A_0 / I/O port	Same as left	ϕ Ports $P0_7$~$P0_0$ Address A_7~A_0
Port P1	ϕ Ports $P1_7$~$P1_0$ I/O port	ϕ Ports $P1_7$~$P1_0$ Address A_{15}~A_8 / I/O port	Same as left	ϕ Ports $P1_7$~$P1_0$ Address A_{15}~A_8
Port P2	ϕ Ports $P2_7$~$P2_0$ I/O port	ϕ Ports $P2_7$~$P2_0$ Output port / Data D_7~D_0	Same as left	ϕ Ports $P2_7$~$P2_0$ Data D_7~D_0
Port P3	ϕ Ports $P3_7$~$P3_0$ I/O port	ϕ Ports $P3_7$~$P3_2$ I/O port Port $P3_1$ SYNC / I/O port Port $P3_0$ R/$\overline{W}$ / I/O port	Same as left	ϕ Ports $P3_7$~$P3_2$ I/O port Port $P3_1$ SYNC Port $P3_0$ R/$\overline{W}$

Fig.23 Processor mode and functions of ports P0~P3

Table 4. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The M50957-XXXSP has two internal clock generating circuits. Figure 26 shows a block diagram of the clock generating circuits. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of serial I/O mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 24 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 25.

The M50957-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 2 and timer 3 are forcibly connected and $\phi/4$ is selected as timer 2 input. When restarting oscillation, FF_{16} is automatically set in timer 2 and 07_{16} in timer 3 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 2 count stop bit must be set to supply ("0"), timer 2 interrupt enable bit and timer 3 interrupt enable bit must be set to disable ("0"), and timer 3 interrupt request bit must be set to no request ("0").

Oscillation is restarted (release the stop mode) when INT_1, INT_2, or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 3 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it recieves an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock (200μA or less at $f(X_{CIN})=32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the $\overline{RESET}$ pin unit the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 27 shows the transition of states for the system clock.

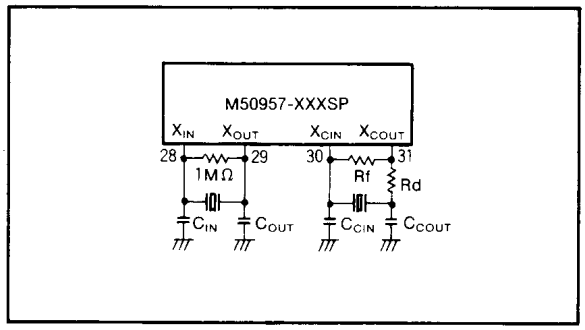


Fig.24 Example ceramic resonator circuit

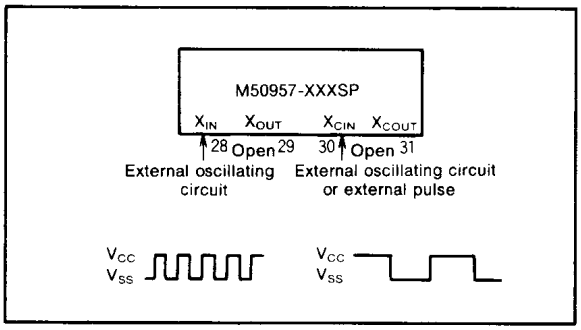


Fig.25 Example clock input circuit

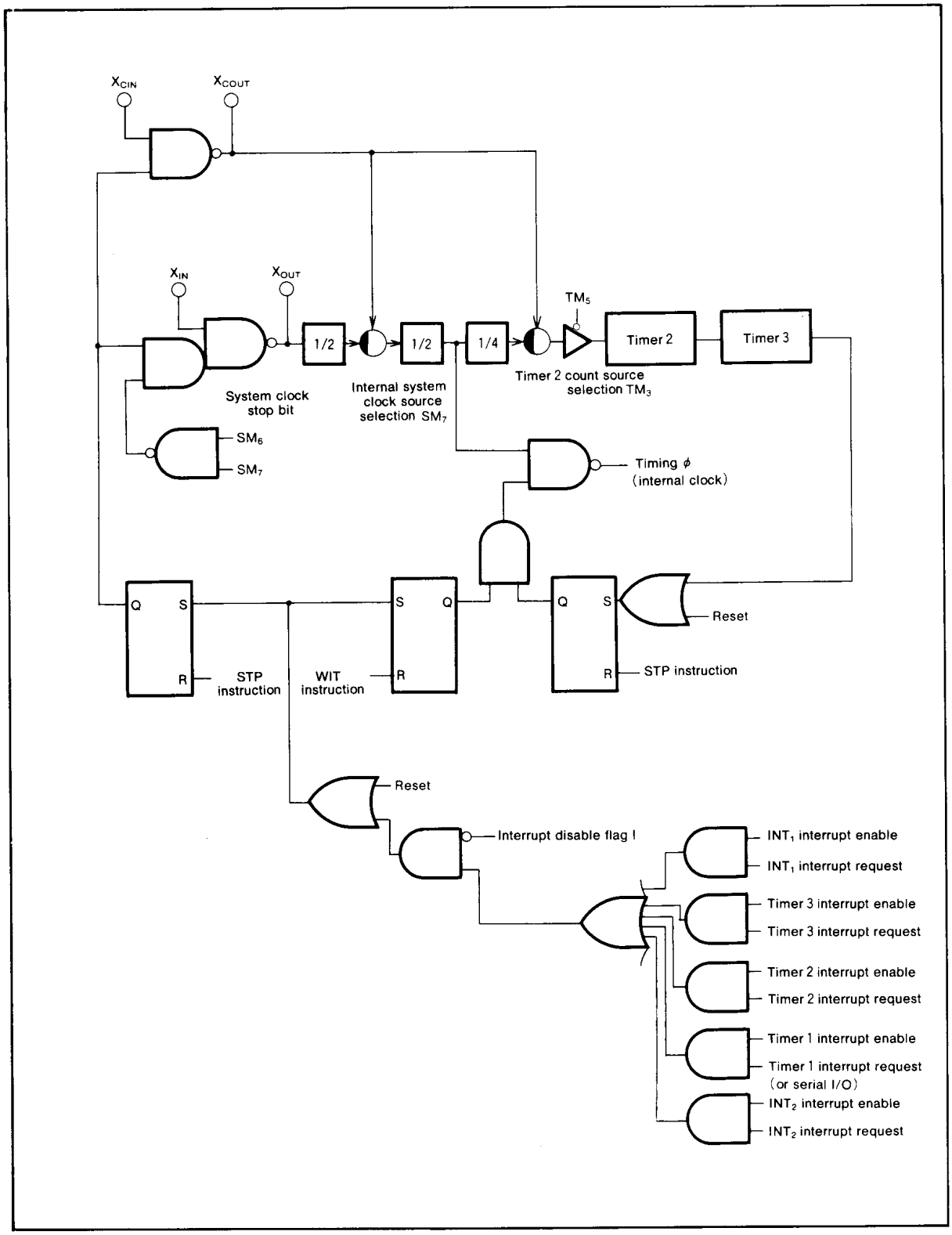
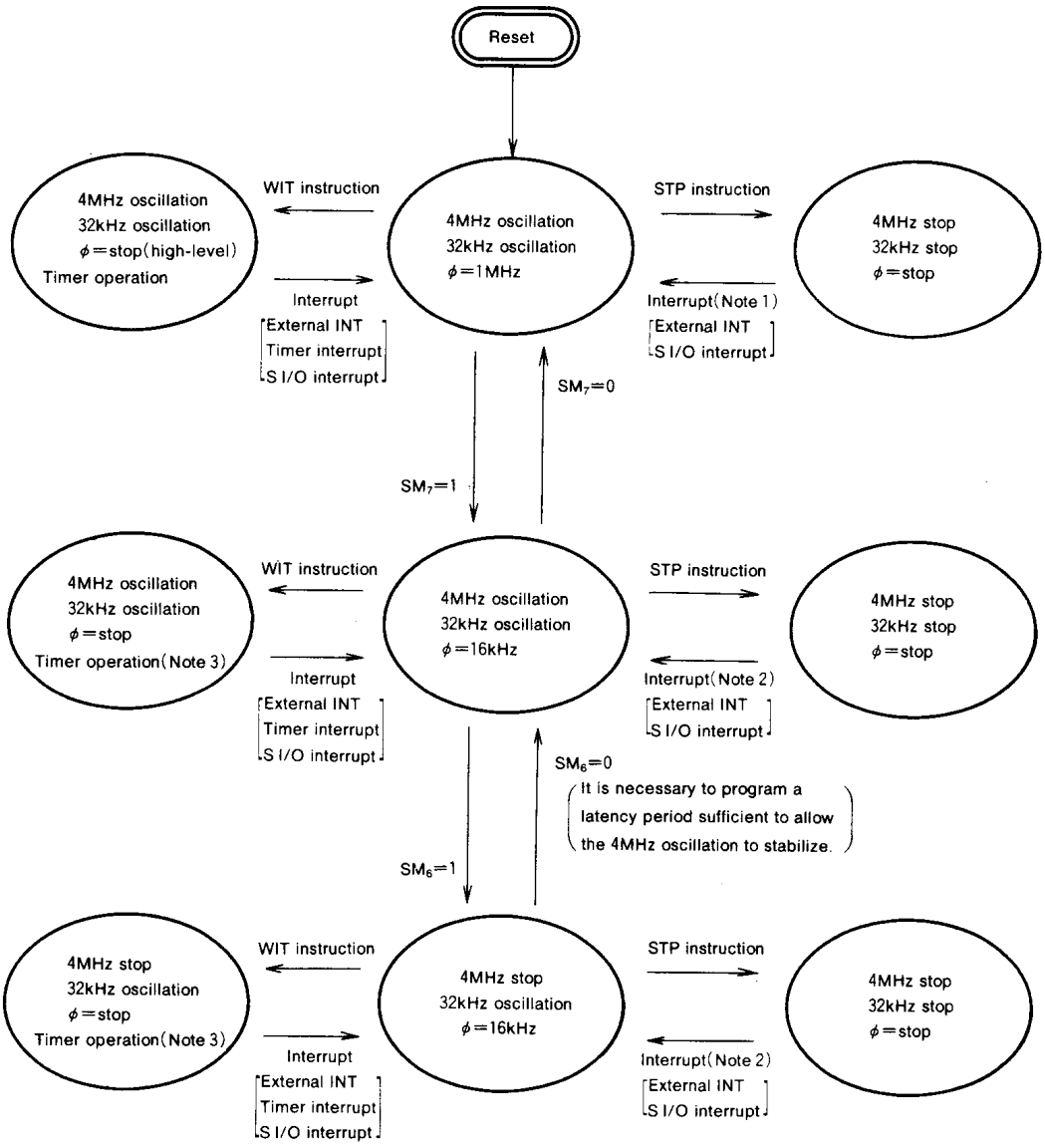


Fig.26 Block diagram of clock generating circuit

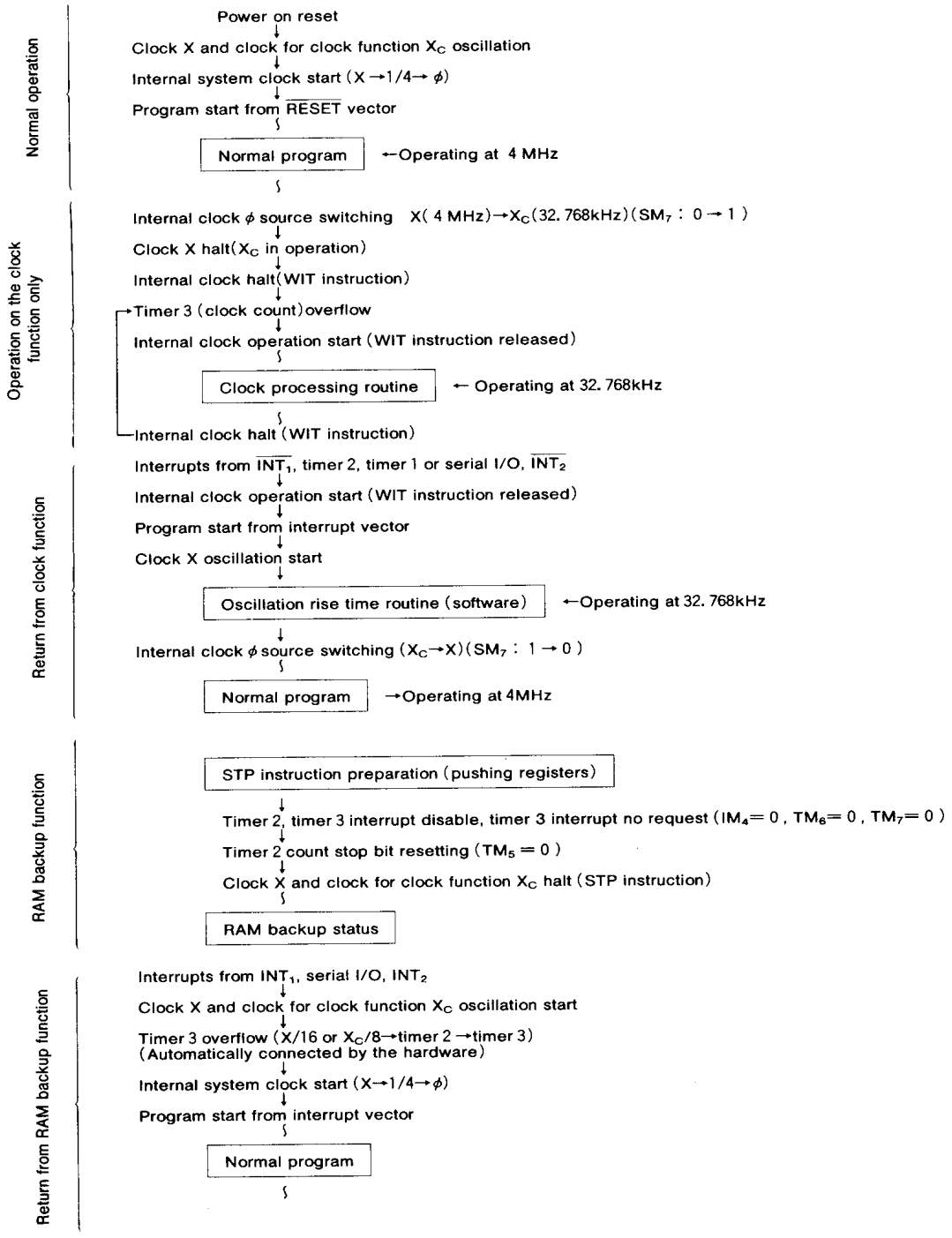


The above example assumes that signals of 4MHz and 32kHz are being applied to pins X_{IN} X_{CIN} respectively. ϕ signifies the internal clock.

Note 1 : Appreximately 8ms of latency time are automatically generated upon release from the STP instruction due to connections of timer 2 and 3.
2 : Approximately 500ms of latency time exists after the release of the STP instruction.
3 : When the internal clock 1/4 frequency is connected as a timer count source the count source becomes 4kHz.

Fig.27 Transition of states for the system clock

<An example of flow for system>



PROGRAM NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When $\phi/4$ or it divided by timer are used as clock for timer, the contents of the timer can be read at voluntary timing.
However, when an other clock (except above clocks) is input to timer, read the contents of timer either while the input of the timer is not changing or after timer count is stopped.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3 sets

Write the following option on the mask confirmation form

(1) ϕ output stop option

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off.	−0.3~7	V
V_P	Pull-down input voltage		V_{CC}−40~V_{CC}+0.3	V
V_I	Input voltage, $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P3_4$~$P3_7$, CNV_{SS}, $P5_2/INT_2$, $P5_3/INT_1$		−0.3~13	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3~7	V
V_I	Input voltage, $P6_0$~$P6_5$, $P3_3$		−0.3~V_{CC}+0.3	V
V_I	Input voltage, $P5_4$~$P5_7$		−0.3~13	V
V_O	Output voltage, $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P3_4$~$P3_7$		−0.3~13	V
V_O	Output voltage, $P6_0$~$P6_5$, X_{OUT}, X_{COUT}, ϕ, $P3_3$		−0.3~V_{CC}+0.3	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$		V_{CC}−40~V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
Topr	Operating temperature		−10~70	℃
Tstg	Storage temperature		−40~125	℃

Note 1 : 600mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Supply voltage	$f(X_{IN})$=4.2MHz	4	5	5.5	V
		$f(X_{IN})$=less than1MHz	3	5	5.5	V
V_P	Pull-down supply voltage		V_{CC}−38		V_{CC}	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNV_{SS}(Note 2), $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$~$P6_5$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P5_4$~$P5_7$		0.4V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNV_{SS}, $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$~$P6_5$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P5_4$~$P5_7$		0		0.12V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$				−120	mA
$I_{OH(sum)}$	"H" sum output current $P6_0$~$P6_5$				−5	mA
$I_{OL(sum)}$	"L" sum output current $P2_0$~$P2_7$, $P3_0$~$P3_7$				50	mA
$I_{OL(sum)}$	"L" sum output current $P6_0$~$P6_5$				5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$~$P0_4$				−40	mA
$I_{OH(peak)}$	"H" peak output current $P0_5$~$P0_7$, $P1_0$~$P1_7$				−30	mA
$I_{OH(peak)}$	"H" peak output current $P4_0$~$P4_7$, $P5_0$, $P5_1$				−30	mA
$I_{OH(peak)}$	"H" peak output current $P6_0$~$P6_5$				−3	mA
$I_{OL(peak)}$	"L" peak output current $P2_0$~$P2_7$, $P3_0$~$P3_7$				15	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$~$P6_5$				3	mA
$I_{OH(avg)}$	"H" average output current $P0_0$~$P0_4$				−18	mA
$I_{OH(avg)}$	"H" average output current $P0_5$~$P0_7$, $P1_0$~$P1_7$				−18	mA
$I_{OH(avg)}$	"H" average output current $P4_0$~$P4_7$, $P5_0$, $P5_1$				−12	mA
$I_{OH(avg)}$	"H" average output current $P6_0$~$P6_5$				−1.5	mA
$I_{OL(avg)}$	"L" average output current $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P6_0$~$P6_5$				10	mA
$I_{OL(avg)}$	"L" average output current $P6_0$~$P6_5$				1.5	mA
$f_{(P3_2/CNTR)}$	Timer 3 counter clock input oscillation frequency (Note 3)	$f(X_{IN})$=4.2MHz			500	kHz
		$f(X_{IN})$=1MHz			100	kHz
$f(X_{IN})$	Clock input oscillating frequency (Note 3, 4, 6)				4.2	MHz
$f(X_{CIN})$	Clock oscillating frequency for clock function				500	kHz

Note 2 : High-level input voltage of up to +12V may be applied to permissible for ports $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P3_4$~$P3_7$, CNV_{SS}, $P5_2$ and $P5_3$.
3 : Oscillation frequency is at 50% duty cycle.
4 : When used in the low-speed mode, the timer clock input frequency should be $f(X_{IN}) < f(X_{IN})/3$.
5 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are in period of 100ms.
6 : When external clock input is used, the timer clock input frequency should be $f(X_{CIN}) \leqq 50kHz$.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, f(X_{IN}) = 4MHz, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P6_0$~$P6_5$		I_{OH}=−0.5mA	V_{CC}−0.4			V
V_{OH}	"H" output voltage ϕ		I_{OH}=−2.5mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$		I_{OH}=−18mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P4_0$~$P4_7$, $P5_0$, $P5_1$		I_{OH}=−12mA	V_{CC}−2			V
V_{OL}	"L" output voltage $P2_0$~$P2_7$, $P3_0$~$P3_7$		I_{OL}=10mA			2	V
V_{OL}	"L" output voltage $P6_0$~$P6_5$		I_{OL}=0.5mA			0.4	V
V_{OL}	"L" output voltage ϕ		I_{OL}=2.5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $P5_2/INT_2$, $P5_3/INT_1$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$		When used as CNTR input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$		When used as CLK input	0.3		1	V
I_{IL}	"L" input current $P2_0$~$P2_7$, $P3_0$~$P3_7$		V_I=0V			−5	μA
I_{IL}	"L" input current $P6_0$~$P6_5$		V_I=0V			−5	μA
I_{IL}	"L" input current $P5_4$~$P5_7$		V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}		V_I=0V			−5	μA
I_{IL}	"L" input current $P5_2/INT_2$, $P5_3/INT_1$		V_I=0V			−5	μA
I_{IH}	"H" input current	$P2_0$~$P2_7$, $P3_0$~$P3_7$	V_I=5V			5	μA
		$P2_0$~$P2_7$, $P3_0$~$P3_2$, $P3_4$~$P3_7$	V_I=12V			12	
I_{IH}	"H" input current $P6_0$~$P6_5$		V_I=5V			5	μA
I_{IH}	"H" input current $P5_4$~$P5_7$		V_I=5V			5	μA
			V_I=12V			12	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}		V_I=5V			5	μA
I_{IH}	"H" input current $P5_2/INT_2$, $P5_3/INT_1$		V_I=5V			5	μA
			V_I=12V			12	
I_{LOAD}	"L" output current	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$	V_P=V_{CC}−36V, V_{OL}=V_{CC}	150	500	900	μA
I_{LEAK}		$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$	V_P=V_{CC}−38V, V_{OL}=V_{CC}−38V			30	μA
V_{RAM}	RAM retention voltage		at clock stop	2		5.5	V
I_{CC}	Supply current		Output pins open (output OFF) V_P=V_{CC}, V_P=V_{SS} Input and I/O pins all at V_{SS} X_{IN}=4MHz (system operation)		4	8	mA
			ditto (at comparator mode)		5	10	
			ditto (at wait mode)		1		
			X_{IN}−X_{OUT} stop X_{CIN}=32kHz (at system operation) all other conditions same as above.		60	200	μA
			ditto (at wait mode)		40		
			Oscillation all stopped. (at STOP mode) T_a=25℃			1	
			T_a=70℃			10	

COMPARATOR CHARACTERISTICS (V_{CC}=5V±10%, V_{CC}=0V, T_a=25℃, f(X_{IN})=4MHz)

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Resolution	—	—	(1/16)V_{CC}	V
Internal analog voltage error	—	—	±(1/16)V_{CC}	V
Analog input voltage	0	—	V_{CC}	V

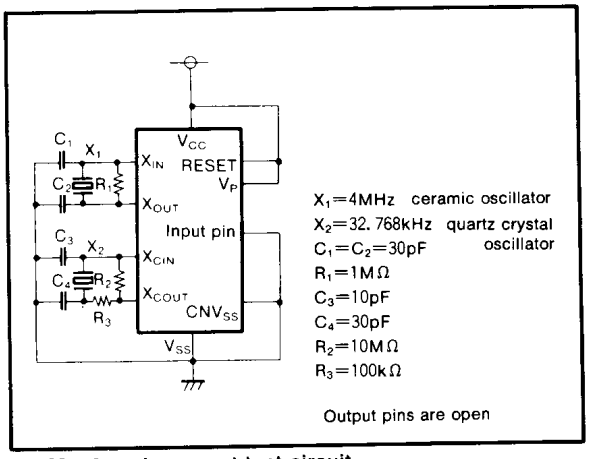


Fig.28 Supply current test circuit

TIMING REQUIREMENTS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, f(X_{IN}) = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P5D-\phi)}$	Port $P5_2/INT_2$, $P5_3/INT_1$ input setup time	270			ns
$t_{su(P5D-\phi)}$	Port $P5_4$~$P5_7$ input setup time	270			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port $P5_2/INT_2$, $P5_3/INT_1$ input hold time	20			ns
$t_{h(\phi-P5D)}$	Port $P5_4$~$P5_7$ input hold time	50			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time	20			ns
$t_{C(X_{IN})}$	External clock input cycle time (X_{IN} input)	235			ns
$t_{W(X_{IN})}$	External clock input pulse width (X_{IN} input)	75			ns
$t_{C(X_{CIN})}$	External clock input cycle time (X_{CIN})	2.0			ms
$t_{W(X_{CIN})}$	External clock input pulse width (X_{CIN})	1.0			ms
t_r	External clock rise time			25	ns
t_f	External clock fall time			25	ns

Memory expanding mode and eva-chip mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, f(X_{IN}) = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Microprocessor mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, f(X_{IN}) = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, f(X_{IN}) = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 30			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 29			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time	Fig. 30			230	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time	Fig. 29			230	ns

Memory expanding mode and eva-chip mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, f(X_{IN}) = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.29 Fig.30			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/\overline{W})}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-R/\overline{W}F)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Microprocessor mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, f(X_{IN}) = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.29 Fig.30			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/\overline{W})}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

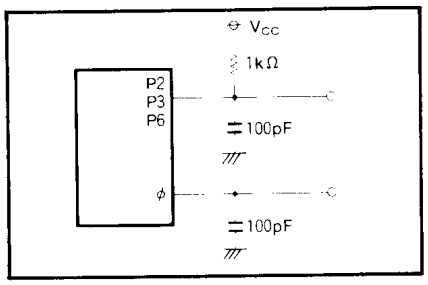


Fig.29 Port P2, P3, P6 test circuit

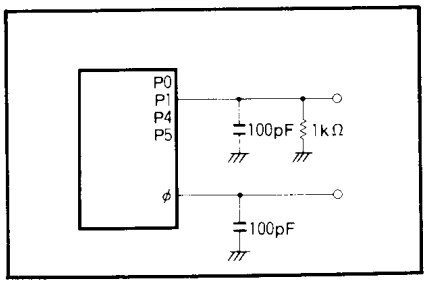
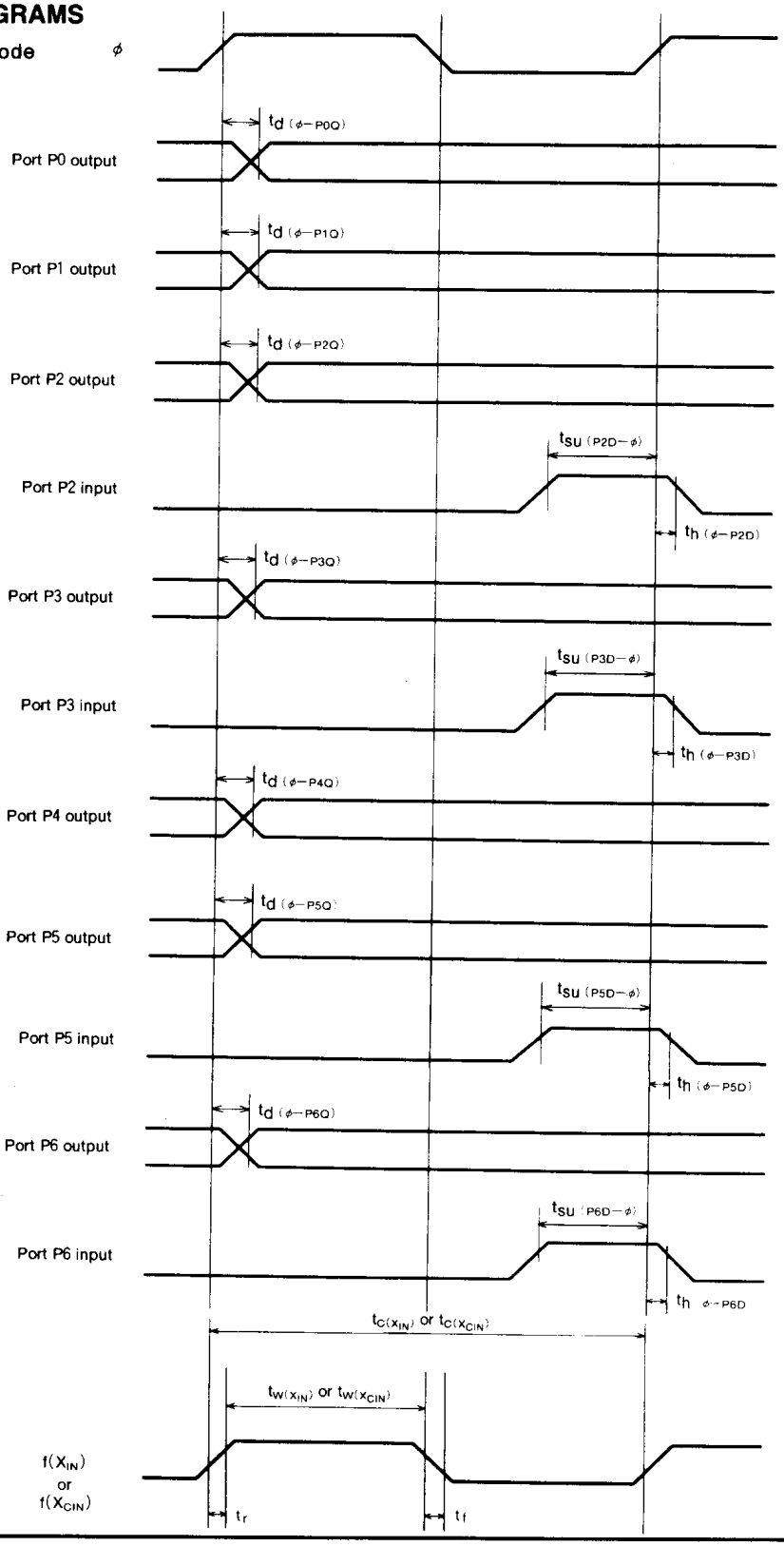


Fig.30 Port P0, P1, P4, P5 test circuit

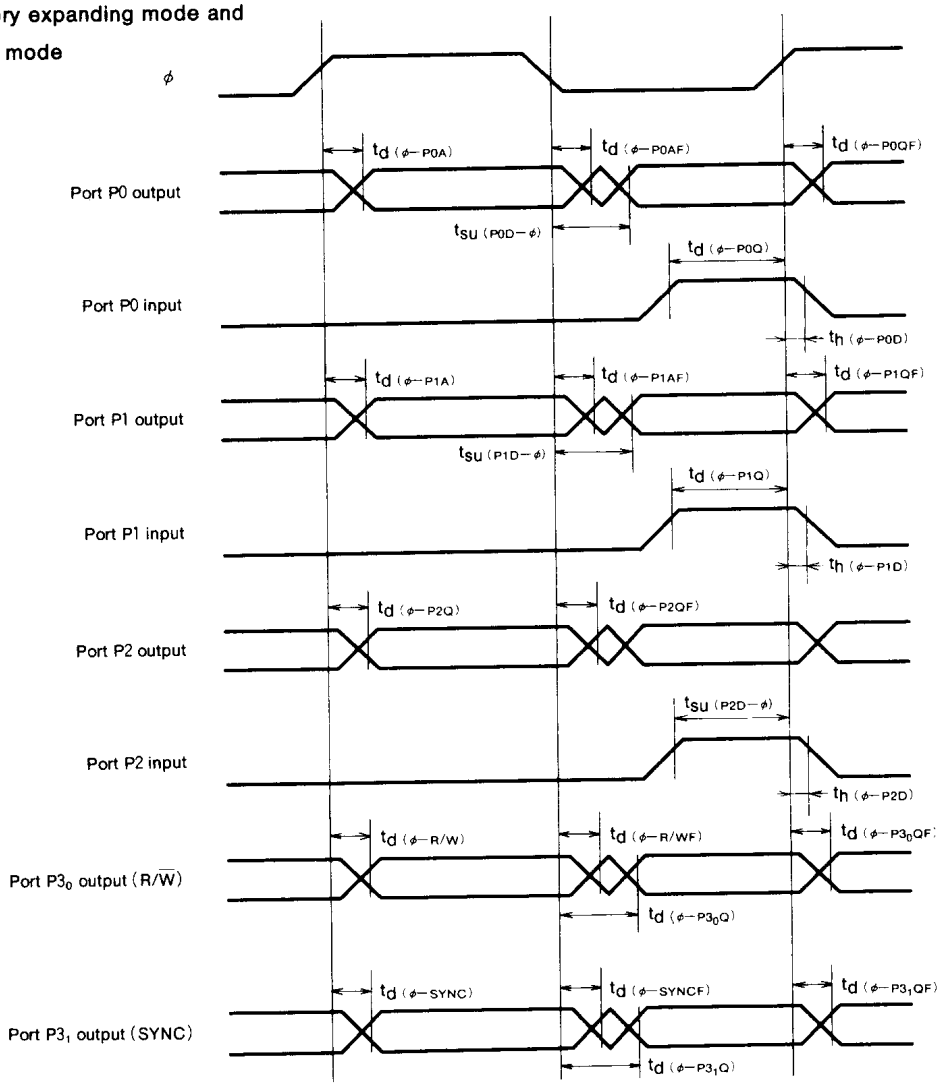
TIMING DIAGRAMS

In single-chip mode



MITSUBISHI ELECTRIC

In memory expanding mode and
Eva-chip mode



In microprocessor mode