

**MITSUBISHI MICROCOMPUTERS**  
**M50930-XXXFP, M50931-XXXFP**  
**M50932-XXXFP**  
**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**DESCRIPTION**

The M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 80-pin plastic molded QFP. These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

These microcomputers are also suitable for applications which require controlling LCDs.

The differences among the M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP are noted below. The following explanations apply to the M50930-XXXFP. Specification variations for other chips are noted accordingly.

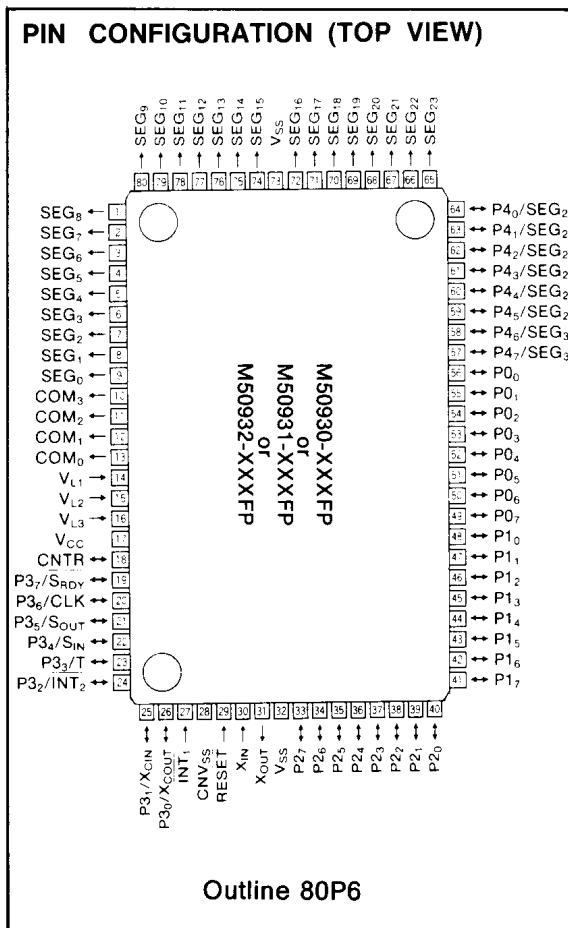
Type name	ROM size	RAM size
M50930-XXXFP	4096 bytes	128 bytes
M50931-XXXFP	4096 bytes	512 bytes
M50932-XXXFP	8192 bytes	512 bytes

M50932-XXXFP only has pull-up transistor option for CNTR pin.

**FEATURES**

- Number of basic instructions..... 69
- Memory size
  - ROM ... 4096 bytes (M50930-XXXFP, M50931-XXXFP)  
8192 bytes (M50932-XXXFP)
  - RAM ..... 128 bytes (M50930-XXXFP)  
512 bytes (M50931-XXXFP, M50932-XXXFP)
- Instruction execution time
  - ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply
  - f(X<sub>IN</sub>)=4MHz ..... 5V±10%
  - f(X<sub>IN</sub>)=1MHz ..... 2.7V ≤ V<sub>CC</sub> ≤ 5.5V(Typ.)
- Power dissipation
  - normal operation mode (at 4MHz frequency)  
..... 15mW(V<sub>CC</sub>=5V, Typ.)
  - low-speed operation mode (at 32kHz frequency for clock function) ..... 225μW (V<sub>CC</sub>=5V, Typ.)
  - stop mode(at 25°C) ..... 5μW (V<sub>CC</sub>=5V, Max.)
- RAM retention voltage (stop mode)
  - ..... 2.0V ≤ V<sub>RAM</sub> ≤ 5.5V
- Subroutine nesting ..... 64 levels (Max.)
- Interrupt..... 8 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- 16-bit timer ..... 1 (Two 8-bit timers make one set)
- Programmable I/O ports
  - (Ports P0, P1, P2, P3)..... 32
- Input ports (Port P4)..... 8
- Serial I/O (8-bit) ..... 1

**PIN CONFIGURATION (TOP VIEW)**



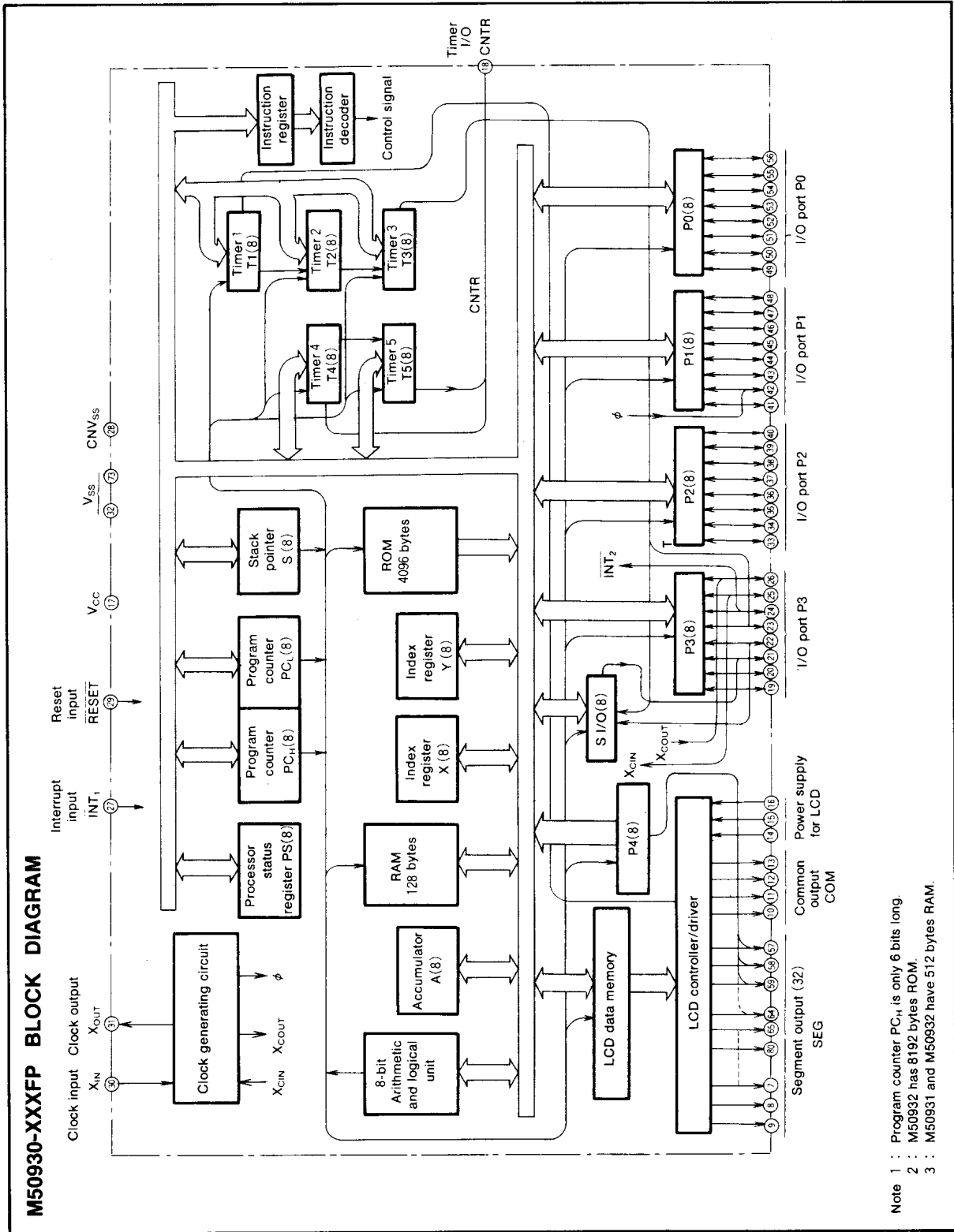
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty) segment output..... 32
- common output ..... 4
- Two clock generator circuits  
(One is for main clock, the other is for clock function)

**APPLICATION**

Office automation equipment  
 VCR, Tuner, Audio-visual equipment  
 Telephone

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**FUNCTIONS OF M50930-XXXFP**

Parameter		Functions
Number of basic instructions		69
Instruction execution time		2 $\mu$ s (minimum instructions, at 4MHz frequency).
Clock frequency		4.3MHz
Memory size	ROM	4096 bytes (8192 bytes for M50932-XXXFP)
	RAM	128 bytes (512 bytes for M50931-XXXFP and M50932-XXXFP)
	RAM for display LCD	16 bytes
Input/Output port	P0, P1, P2, P3	I/O 8-bitX4
	P4	Input 8-bitX1 (Port P4 are in common with SEG)
	SEG	LCD output 32-bitX1
	COM	LCD output 4-bitX1
Serial I/O		8-bitX1
Timers		8-bit timerX3 (2 when serial I/O is used) 16-bit timerX1 (combination of two 8-bit timers)
LCD controller/driver	Bias	1/2, 1/3 bias selectable
	Duty ratio	1/2, 1/3, 1/4 duty selectable
	Common output	4
	Segment output	32 (SEG <sub>24</sub> ~SEG <sub>31</sub> are in common with port P4)
Subroutine nesting		64 (max.)
Interrupt		Two external interrupts, Three timer interrupts (or two timer, one serial I/O)
Clock generating circuit		Two built-in circuits (ceramic or quartz crystal oscillator)
Supply voltage		2.7~5.5V (RAM retention voltage at clock stop is 2~5.5V)
Power dissipation	At high-speed operation V <sub>CC</sub> =5V	15mW (at clock frequency X <sub>IN</sub> =4MHz, typ.)
	At low-speed operation V <sub>CC</sub> =5V	225 $\mu$ W (at clock frequency X <sub>CIN</sub> =32kHz, typ.)
	At STOP mode	5 $\mu$ W (at clock stop, max.)
Input/Output characteristics	Input/Output voltage	5V
	Output current	I <sub>OH</sub> =-2mA (V <sub>OH</sub> =3V)
		I <sub>OL</sub> =10mA (V <sub>OL</sub> =2V)
		Pull-up current : Min. -30 $\mu$ A, max. -140 $\mu$ A, typ -70 $\mu$ A (V <sub>CC</sub> =5V input voltage 0V)
Memory expansion		Possible
Operating temperature range		-10~70°C
Device structure		CMOS silicon gate
Package		80-pin plastic molded QFP

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**PIN DESCRIPTION**

Pin	Name	Input/ Output	Functions
$V_{CC}$ , $V_{SS}$	Supply voltage		Power supply inputs $5V \pm 10\%$ to $V_{CC}$ , and 0V to $V_{SS}$ .
$CNV_{SS}$	$CNV_{SS}$		This is usually connect to $V_{SS}$ .
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than $2\mu s$ (under normal $V_{CC}$ conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
$X_{IN}$	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the $X_{IN}$ and $X_{OUT}$ pins. If an external clock is used, the clock source should be connected the $X_{IN}$ pin and the $X_{OUT}$ pin should be left open.
$X_{OUT}$	Clock output	Output	
$\overline{INT}_1$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0 \sim P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0 \sim P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0 \sim P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0 \sim P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$ , $P3_6$ , $P3_5$ , and $P3_4$ work as $\overline{S_{RDV}}$ , CLK, $S_{OUT}$ , and $S_{IN}$ pins, respectively. Also $P3_3$ , $P3_2$ , $P3_1$ , and $P3_0$ work as timer 3 overflow signal divided by 2 output pin (T), $\overline{INT}_2$ pin, $X_{CIN}$ and $X_{COUT}$ pins, respectively.
$P4_0 \sim P4_7$	Input port P4	I/O	Port P4 is an 8-bit input port and can be used as segment output pins.
$V_{L1} \sim V_{L3}$	Voltage input for LCD	Input	These are voltage input pins for LCD. Supply voltage as $0V \leq V_{L1} \leq V_{L2} \leq V_{L3} \leq V_{CC}$ . $0V \sim V_{L3}$ is supplied to LCD.
$COM_0 \sim$ $COM_3$	Common output	Output	These are LCD common output pins. At 1/2 duty, $COM_2$ and $COM_3$ pins are not used. At 1/3 duty, $COM_3$ is not used.
$SEG_0 \sim$ $SEG_{23}$	Segment output	Output	These are LCD segment output pins.
CNTR	Timer I/O	I/O	This is an output pin for the timer 4 and 5.

# MITSUBISHI MICROCOMPUTERS

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### SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

#### BASIC FUNCTION BLOCKS

#### MEMORY

A memory map for the M50930-XXXFP is shown in Figure 1. Address 3000<sub>16</sub> to 3FFF<sub>16</sub> are assigned for the built-in ROM area which consists of 4096 bytes (Addresses 2000<sub>16</sub> to 3FFF<sub>16</sub> are assigned for the built-in ROM area which consists of 8192 bytes for M50932-XXXFP). Addresses 3F00<sub>16</sub> to 3FFF<sub>16</sub> are a special address area (special page). By using the special page addressing mode of JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses 3FF4<sub>16</sub> to 3FFF<sub>16</sub> are vector addresses used for the reset and interrupts (See interrupts chapter).

Addresses 0000<sub>16</sub> to 00FF<sub>16</sub> are the zero page address area. By using zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the zero page. Addresses 0000<sub>16</sub> to 007F<sub>16</sub> are assigned for the built-in RAM which consists of 128 bytes (Addresses 0000<sub>16</sub> to 007F<sub>16</sub> and 0100<sub>16</sub> to 027F<sub>16</sub> are assigned for the built-in RAM which consists of 512 bytes for M50931-XXXFP and M50932-XXXFP). This RAM is used as the stack during subroutine calls and interrupts, in addition to data storage.

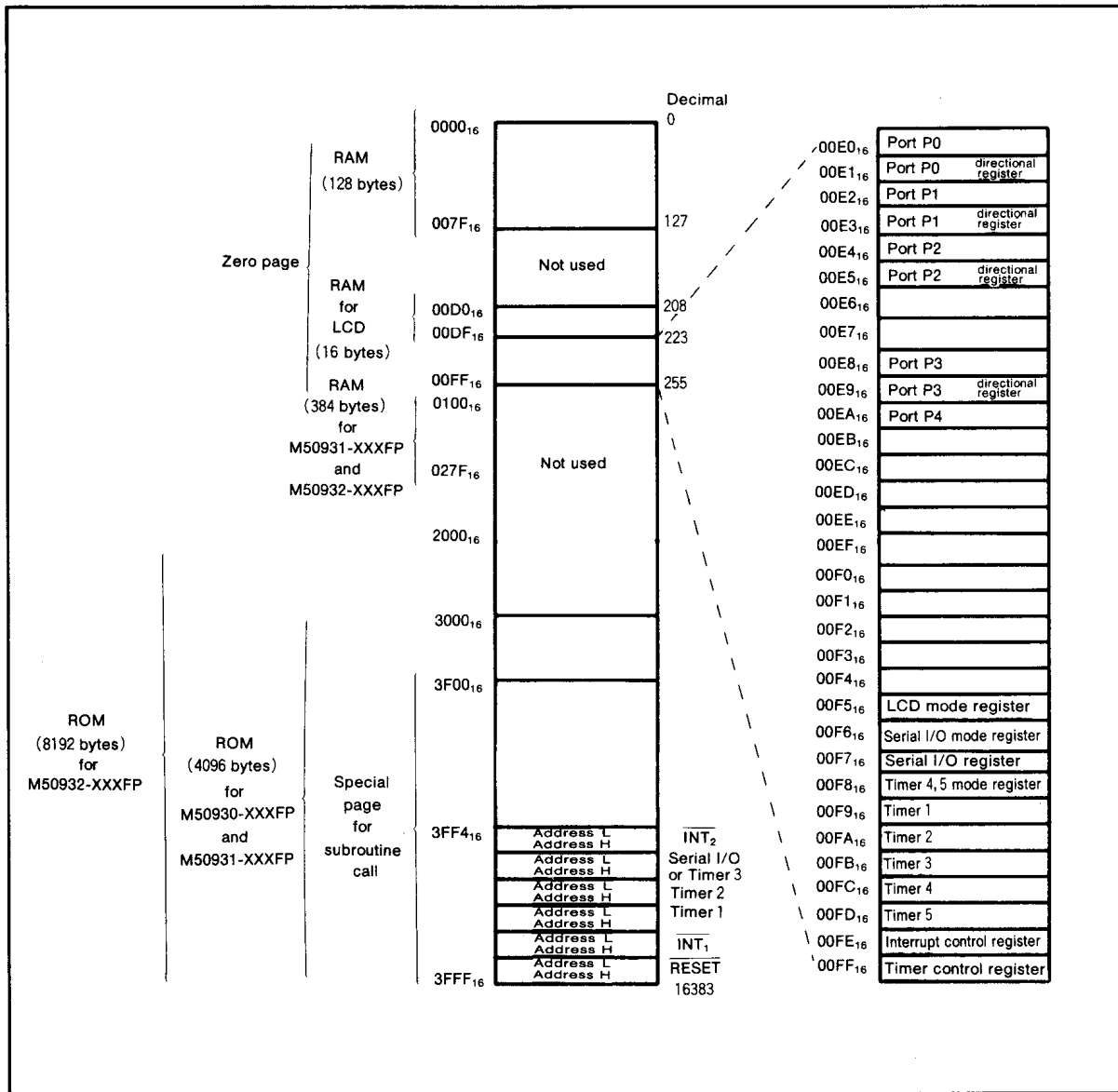


Fig.1 Memory map

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**CENTRAL PROCESSING UNIT (CPU)**

The CPU consists of 6 registers and is shown in Figure 2.

**ACCUMULATOR (A)**

The 8-bit accumulator (A) is the main register of the micro-computer. Data operations such as data transfer, input/output, etc., is executed mainly through the accumulator.

**INDEX REGISTER X (X)**

The index register X is an 8-bit register. In the index register X addressing mode, the value of the OPERAND added to the contents of the index register X specifies the real address. When the T flag in the processors status register is set to "1", the index register X itself becomes the address for the second OPERAND.

**INDEX REGISTER Y (Y)**

The index register Y is an 8-bit register. In the index register Y addressing mode, the value of the OPERAND added to the contents of the index register Y specifies the real address.

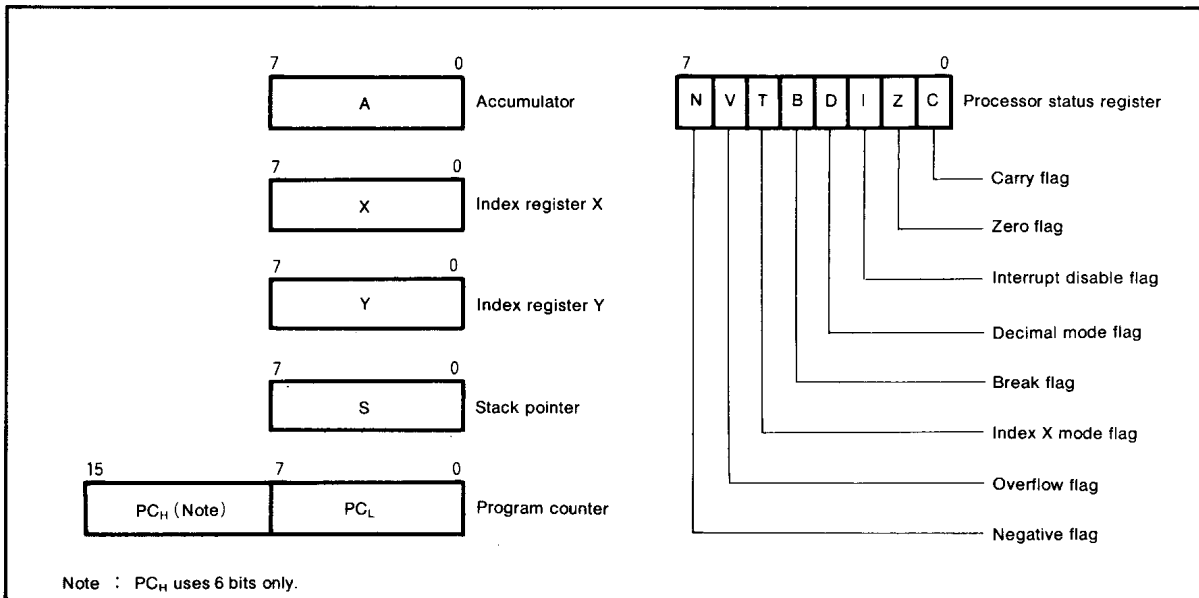


Fig.2 Register structure

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### **STACK POINTER (S)**

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter is pushed into the stack first, the stack pointer is decremented, and then the lower 8 bits of the program counter is pushed into the stack. Next the contents of the processor status register is pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is popped off the stack in reverse order from above.

The accumulator is never pushed into the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pop Accumulator instruction (PLA). It is executed in the reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and popped to and from the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the Program Counter is pushed into the stack. Therefore, any registers that should not be destroyed should be pushed into the stack manually. To return from a subroutine call, the RTS instruction is used.

### **PROGRAM COUNTER (PC)**

The 16-bit program counter consists of two 8-bit registers PC<sub>H</sub> and PC<sub>L</sub>. The program counter is used to indicate the address of the next instruction to be executed.

PC<sub>H</sub> is only 6 bits long.

### **PROCESSOR STATUS REGISTER (PS)**

The 8-bit PS is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flags (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

#### **1. Carry flag (C)**

The carry flag contains the carry or borrow generated by the Arithmetic Logic Unit (ALU) immediately after an operation. It is also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

#### **2. Zero flag (Z)**

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "0". If the result is not zero, the zero flag will be set to "1".

#### **3. Interrupt disable flag (I)**

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt is accepted, this flag is automatically set to "1" to prevent from other interrupts until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

#### **4. Decimal mode flag (D)**

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

#### **5. Break flag (B)**

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the B flag will be "1", otherwise, it will be "0".

#### **6. Index X mode flag (T)**

When the T flag is "1", operations between memories are executed directly, without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the T flag, respectively.

#### **7. Overflow flag (V)**

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or -128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the V flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

#### **8. Negative flag (N)**

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the N flag. There are no instructions for directly setting or resetting the N flag.

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**INTERRUPT**

The M50930-XXXFP can be interrupted from eight sources;  $\overline{INT}_1$ , Timer 1, Timer 2, Timer 3 or Serial I/O,  $\overline{INT}_2$  or Key on wake up, and BRK instruction.

The value of bit 2 of the serial I/O register (address 00F6<sub>16</sub>) determines whether the interrupt is from timer 3 or from serial I/O. When the bit 2 is "1" the interrupt is from serial I/O, and when bit 2 is "0" the interrupt is from timer 3. Also, when bit 2 is "1", parts of Port 3 are used for serial I/O. Bit 7 of the serial I/O register determines if an interrupt is from  $\overline{INT}_2$  or from "Key on wake up". When bit 7 is "0", the interrupt is from  $\overline{INT}_2$ . When bit 7 is "1" the interrupt is from "key on wake up". "key on wake up" can only be used at power down by the STP or WIT instruction. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, as discussed in the stack pointer section, and the interrupt disable flag (1) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The Reset interrupt is the highest priority interrupt and can never be inhibited. Except for the Reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0". The interrupt request bits are set when the following conditions occur:

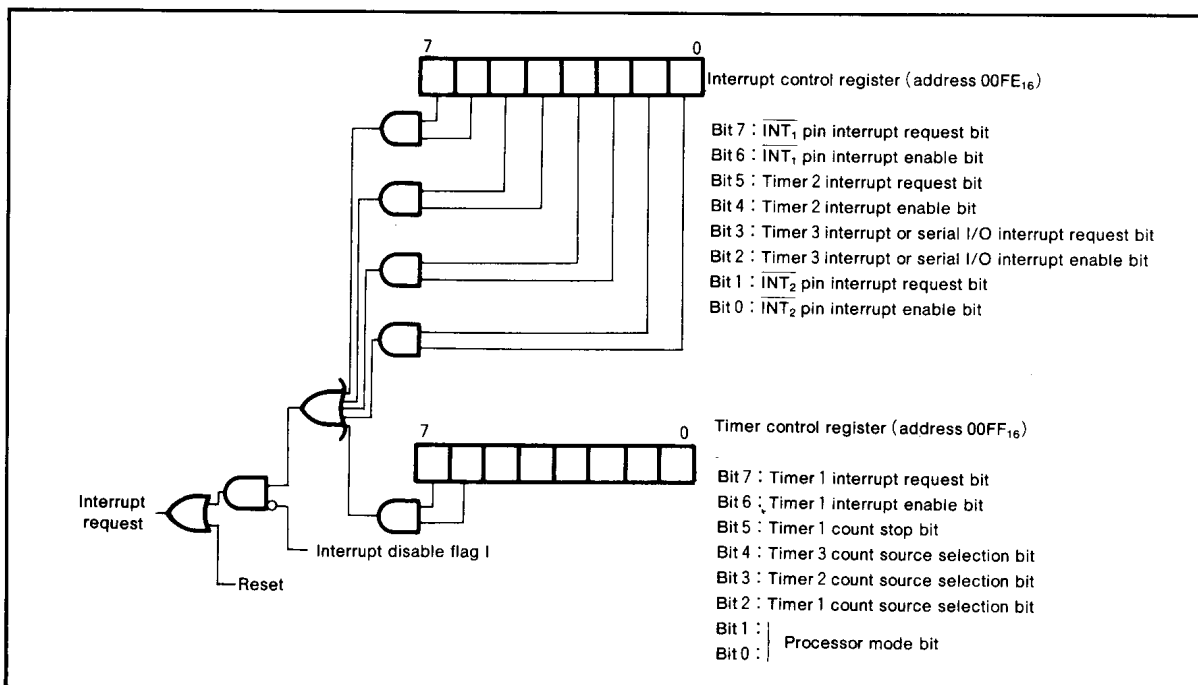
- (1) When the  $\overline{INT}_1$  or  $\overline{INT}_2$  pins go from "H" to "L"
- (2) When the levels any pin of P2 goes "L" (at power down mode)
- (3) When the contents of timer 1, timer 2, timer 3 or the counter of serial I/O go to "0"

These request bits can be reset by a program but can not be set.

Since the BRK instruction interrupt and the  $\overline{INT}_2$  interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if  $\overline{INT}_2$  generated the interrupt.

**Table 1. Interrupt vector address and priority.**

interrupt	Priority	Vector address
RESET	1	3FFF <sub>16</sub> , 3FFE <sub>16</sub>
$\overline{INT}_1$	2	3FFD <sub>16</sub> , 3FFC <sub>16</sub>
Timer 1	3	3FFB <sub>16</sub> , 3FFA <sub>16</sub>
Timer 2	4	3FF9 <sub>16</sub> , 3FF8 <sub>16</sub>
Timer 3 or serial I/O	5	3FF7 <sub>16</sub> , 3FF6 <sub>16</sub>
$\overline{INT}_2$ or key on wake up (BRK)	6	3FF5 <sub>16</sub> , 3FF4 <sub>16</sub>



**Fig. 3 Interrupt control**



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**TIMER**

The M50930-XXXFP has five timers; timer 1, timer 2, timer 3, timer 4 and timer 5. Timer 3 cannot be used when serial I/O is used (see serial I/O section). The count source for each timer can be selected by using bit 2, 3 and 4 of the timer control register (address 00FF<sub>16</sub>), as shown in Figure 4.

A block diagram of timer 1 through 5 is shown in Figure 6. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timers is  $1/(n+1)$ , where n is the contents of timer latch.

The timer interrupt request bit is set at the next count pulse after the timer reaches "0". The interrupt and timer control registers are located at addresses 00FE<sub>16</sub> and 00FF<sub>16</sub>, respectively (see Interrupt section). The starting and stopping of timer 1 is controlled by bit 5 of the timer control register. If bit 5 (address 00FF<sub>16</sub>) is "0", the timer starts counting. When bit 5 is "1", the timer stops.

After a STP instruction is executed, timer 2, timer 1, and the clock ( $\phi$  divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if timer 2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 1, count stop bit), bit 6 of the timer control register (timer 1 interrupt enable bit), and bit 4 of interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

**TIMER 4 AND TIMER 5 MODES**

(1) Timer Mode (00).

The internal clock divided by 4 is counted. When the timer counts to "0", the interrupt request bit is set to "1", the contents of the timer latch is reloaded, and the counting starts again.

(2) Pulse Output Mode (01).

The output level of the CNTR pin inverts each time the timer contents to zero.

(3) Event Counter Mode (10).

The same function is executed as that of mode "00", except that the counting source is input from the CNTR pin. The count decremented each time the CNTR input goes from "L" to "H".

(4) Pulse Width Measurement Mode (11).

This mode is used to measure the pulse width of a signal (between "L"s) input into the CNTR pin. The counting is done using the oscillation frequency divided by 4, and only while the CNTR pin is at a low level. When the contents of the counter reaches zero, the timer 5 overflow flag is set to "1", the timer is reloaded from the reload latch, and counting starts again. The overflow flag can be reset by writing a "0" to bit 7 of address 00F8<sub>16</sub>. The structure of timer 4, 5 mode register is shown in Figure 5.

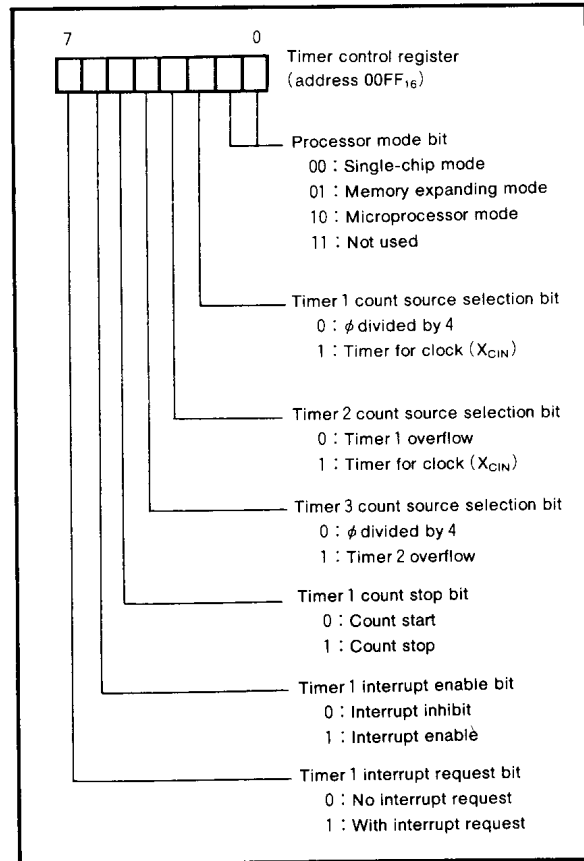


Fig.4 Structure of timer control register

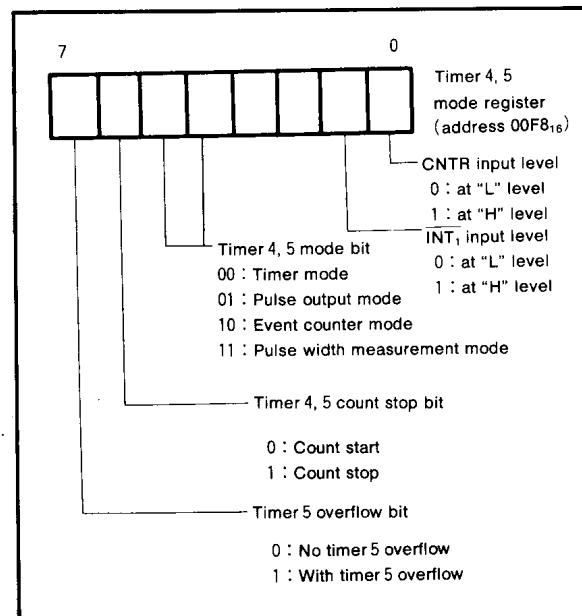


Fig.5 Structure of timer 4, 5 mode register

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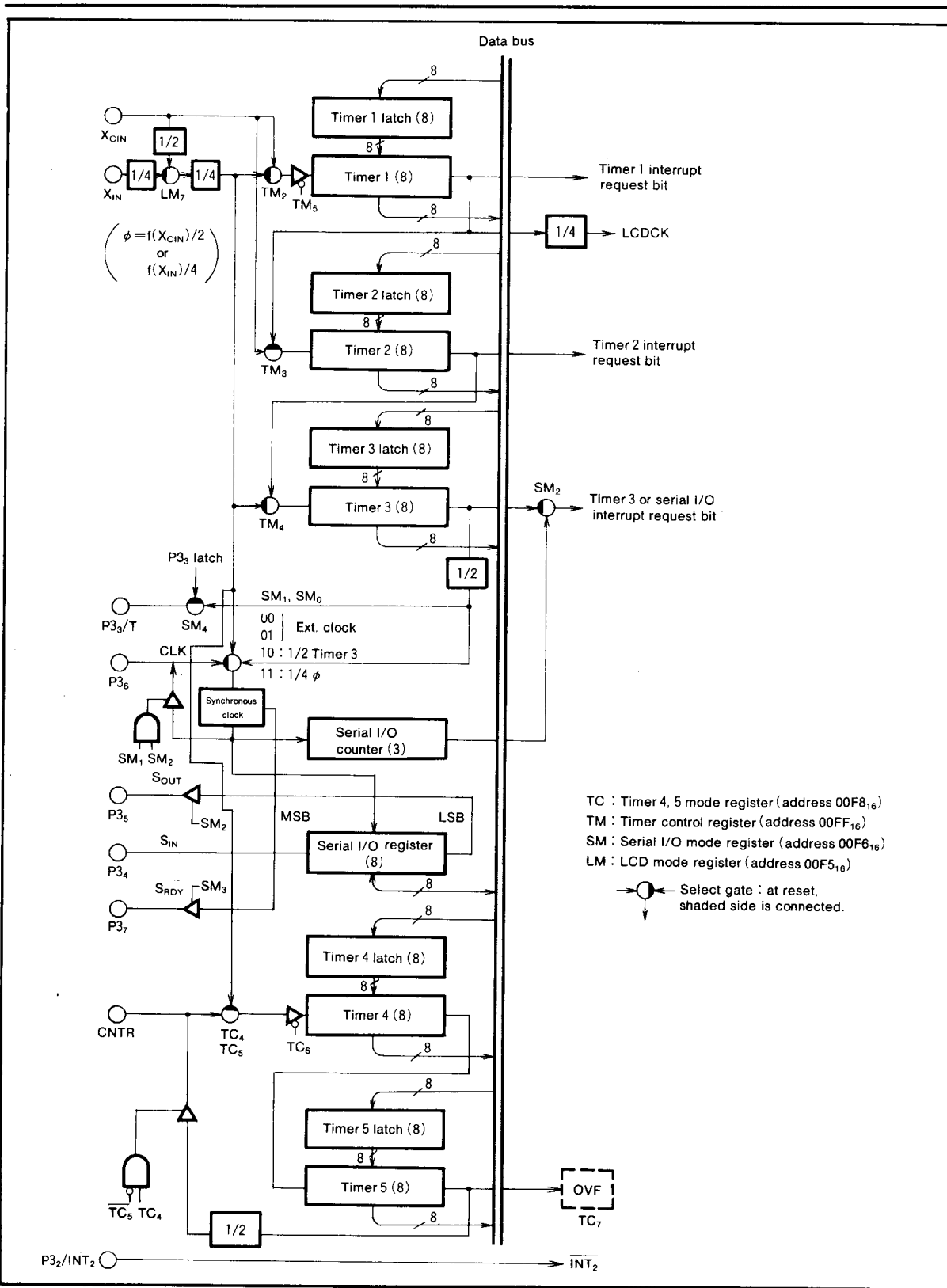


Fig.6 Block diagram of timers 1 through 5

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**PORT P3<sub>3</sub>/TIMER 3 OUTPUT**

The signal that timer 3 is divided by 2 is output from P3<sub>3</sub> (T), at the contents of bit 4 of the serial I/O mode register (address 00F6<sub>16</sub>) is "1".

**WATCHDOG TIMER FUNCTION**

Timer 4 and 5 can be used as a watchdog timer by connecting the CNTR pin and the RESET pin as shown in Figure 7, and by setting bit 4 and 5 of address 00F8<sub>16</sub> to 01. At this time the output of the 1/2 divider counter (connected to timer 5) is initialized to "1" when data is written to timer 5. After a delay of 2.5 to 3.0 $\mu$ s (at  $f(X_{IN})=4$ MHz) after the reset is input, bits 4, 5, and 6 of the timer 4,5 mode register are initialized to 0. The initialization program to set the watchdog timer mode should have the following sequence:

- (1) Set the pulse output mode after writing a value to timer 4 and 5 registers.
- (2) If the program is running correctly, the CNTR pin should never go low due to data being continuously written to timer 5. If the program sequence is interrupted, timer 5 will overflow and the CNTR pin will output a "L" and retain this value until the Reset is executed.
- (3) 2.5 to 3.5 $\mu$ s (at  $f(X_{IN})=4$ MHz) after a reset, the CNTR pin will be in high impedance state.

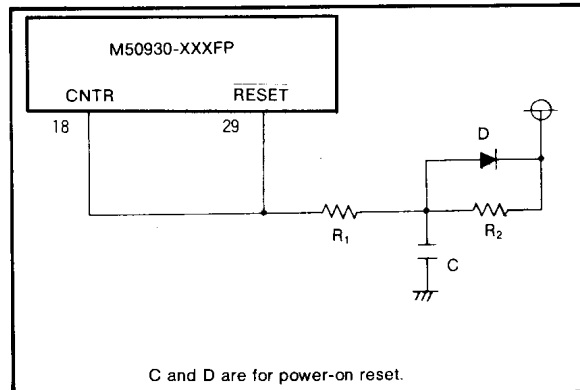


Fig.7 Reset circuit with the watchdog timer

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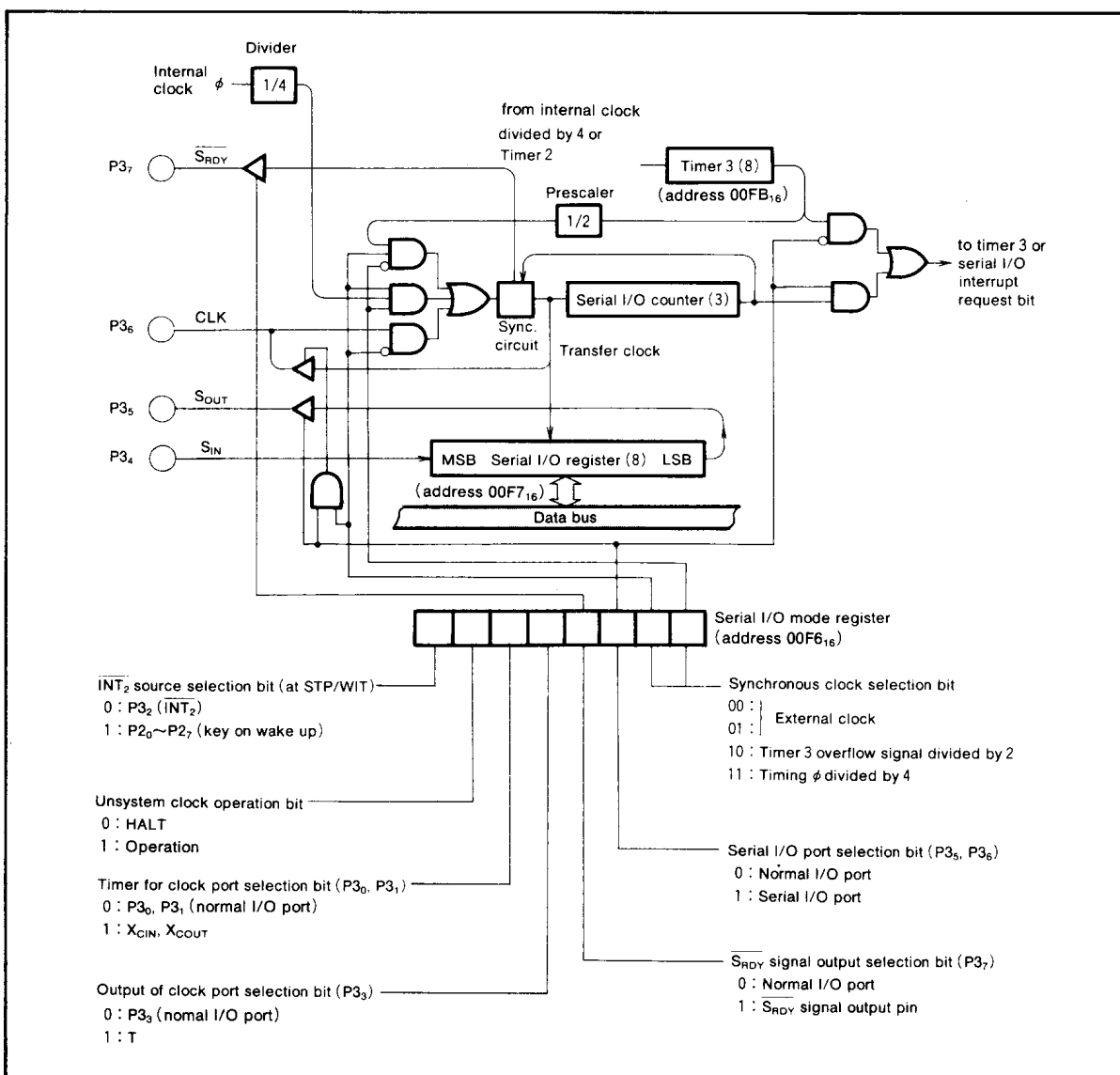
**SERIAL I/O**

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode the receive ready signal ( $\overline{S_{RDY}}$ ), synchronous input/output clock (CLK), and the serial I/O ( $S_{OUT}$ ,  $S_{IN}$ ) pins are used as P3<sub>7</sub>, P3<sub>6</sub>, P3<sub>5</sub>, and P3<sub>4</sub>, respectively. The serial I/O mode register (address 00F6<sub>16</sub>) is an 8-bit register. Bit 0 and 1 of this register is used to select a synchronous clock source. When these bits are (00) or (01), an external clock from P3<sub>6</sub> is selected. When these bits are (10), the overflow signal divided by two from timer 3 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are

(11), the internal clock  $\phi$  divided by 4 (ie. 4 $\mu$ s at 4MHz) becomes the clock.

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", P3<sub>6</sub> becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from P3<sub>6</sub>. If the external synchronous clock is selected, the clock is input to P3<sub>6</sub>. And P3<sub>5</sub> will be a serial output and P3<sub>4</sub> will be a serial input. To use P3<sub>4</sub> as a serial input, set the directional register bit which corresponds to P3<sub>4</sub>, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0"



**Fig.8** Block diagram of serial I/O

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P3<sub>6</sub> will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 3. Bit 3 determines if P3<sub>7</sub> is used as an output pin for the receive data ready signal (bit 3="1",  $\overline{S_{RDY}}$ ) or used as a normal I/O pin (bit 3="0").

The function of serial I/O differs depending on the clock source: external clock or internal clock.

**Internal clock**—The  $\overline{S_{RDY}}$  signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the  $\overline{S_{RDY}}$  signal becomes low signaling that the M50930-XXXFP is ready to receive the external serial data. The  $\overline{S_{RDY}}$  signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to P3<sub>5</sub>. During the rising edge of this clock, data can be input from P3<sub>4</sub> and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. Af-

ter the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

**External Clock**—If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9, and connection between two M50930-XXXFPs are shown in Figure 10. When using an external clock for transfer, the external clock must be held at "H" level when the serial I/O counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

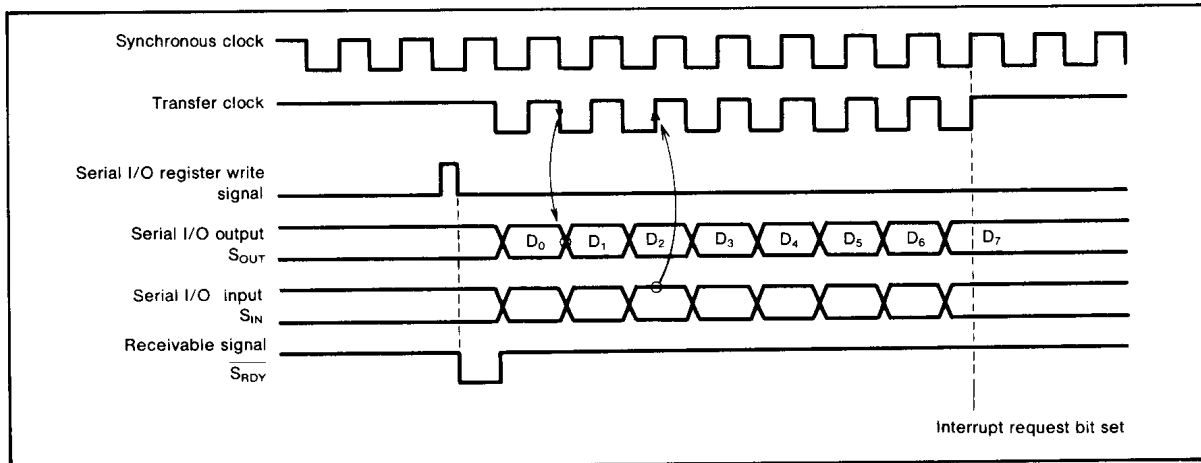


Fig.9 Serial I/O timing

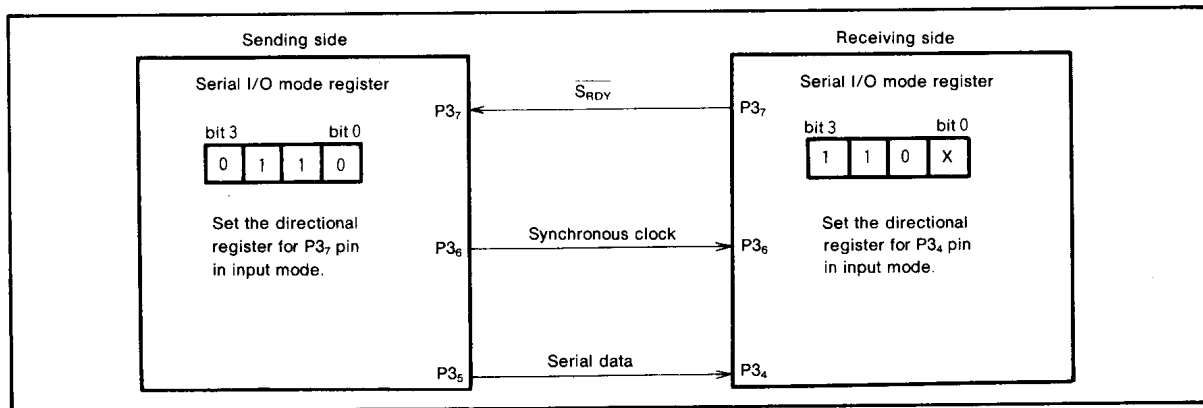


Fig.10 Example of serial I/O connection

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**LCD CONTROLLER/DRIVER**

The M50930-XXXFP has internal LCD controllers and drivers. A Block diagram of LCD circuit is shown in Figure 13. The terminals for LCD consist of 4 common-pin and 32 segments pin. SEG<sub>24</sub> ~ SEG<sub>31</sub> are in common with input P4. These pins are selected by bit 4 of the LCD mode register (LM<sub>4</sub>, address 00F5<sub>16</sub>). Two biases (1/2 and 1/3) can also be selected. When bit 2 of the LCD mode register is "1", 1/2 bias is selected. When bit 2 is "0", 1/3 bias is selected. A 1/2, 1/3, or 1/4 duty cycle can also be selected. When bits 0 and 1 of the LCD mode register (LM<sub>0</sub>, LM<sub>1</sub>) is n, the duty ratio is 1/(n+1).

Address 00D0<sub>16</sub> ~ 00DF<sub>16</sub> is the designated RAM for the LCD display. When 1s' are written to these addresses, the corresponding segments of the LCD display panel are turned on. A map of the LCD display RAM is shown in Figure 12.

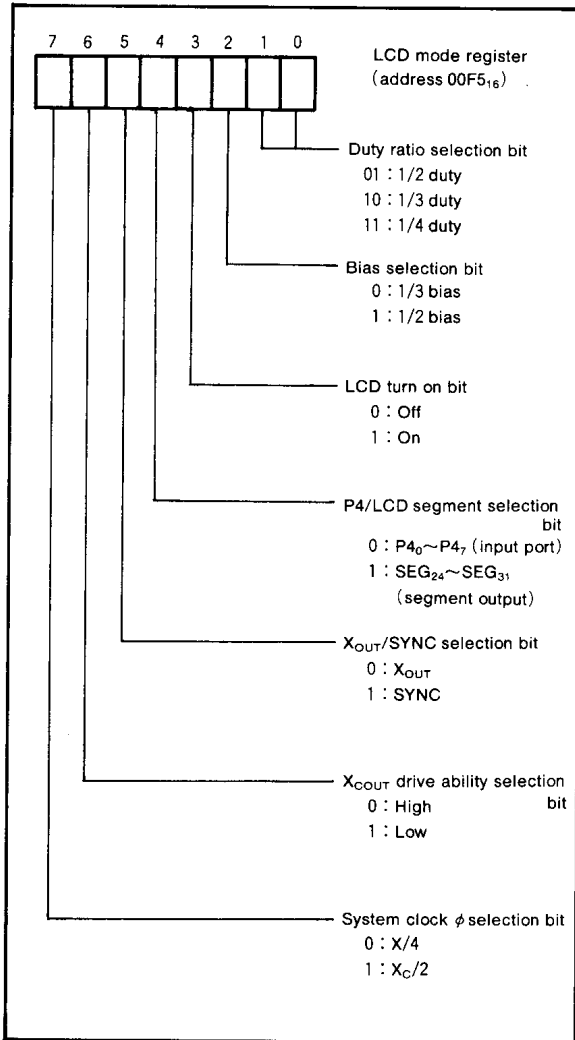


Fig.11 Structure of LCD mode register

The ON/OFF function for the LCD controller is controlled by bit 3 of the LCD mode register (LM<sub>3</sub>). When this bit is "1" all the segments of the LCD are turned on. When this bit is "0" all the segments are turned off.

When a 1/2 bias is used, V<sub>L1</sub> and V<sub>L2</sub> should be shorted together. An example circuit for each bias is shown in Figure 14. Also Figure 15 shows an example of 1/2 bias, 1/4 duty drive waveforms and resulting voltage differential between SEG<sub>n</sub> and COM<sub>n</sub> and Figure 16 shows examples of drive waveforms for each bias and duty.

The LCDCK timing frequency (LCD driver timing) is generated internally and the frame frequency can be determined with the following equation:

$$f(\text{LCDCK}) = \frac{\text{(frequency of timer 1 count source)}}{\text{(timer 1 setting+1)} \times 4}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{n} ; \text{ at } 1/n \text{ duty}$$

Bit Address	7	6	5	4	3	2	1	0
D0	1	1	1	1	0	0	0	0
D1	3	3	3	3	2	2	2	2
D2	5	5	5	5	4	4	4	4
D3	7	7	7	7	6	6	6	6
D4	9	9	9	9	8	8	8	8
D5	11	11	11	11	10	10	10	10
D6	13	13	13	13	12	12	12	12
D7	15	15	15	15	14	14	14	14
D8	17	17	17	17	16	16	16	16
D9	19	19	19	19	18	18	18	18
DA	21	21	21	21	20	20	20	20
DB	23	23	23	23	22	22	22	22
DC	25	25	25	25	24	24	24	24
DD	27	27	27	27	26	26	26	26
DE	29	29	29	29	28	28	28	28
DF	31	31	31	31	30	30	30	30
	COM <sub>3</sub>	COM <sub>2</sub>	COM <sub>1</sub>	COM <sub>0</sub>	COM <sub>3</sub>	COM <sub>2</sub>	COM <sub>1</sub>	COM <sub>0</sub>

\* Number in data memory area indicates corresponding segment.

Fig. 12 Map of RAM for LCD segment

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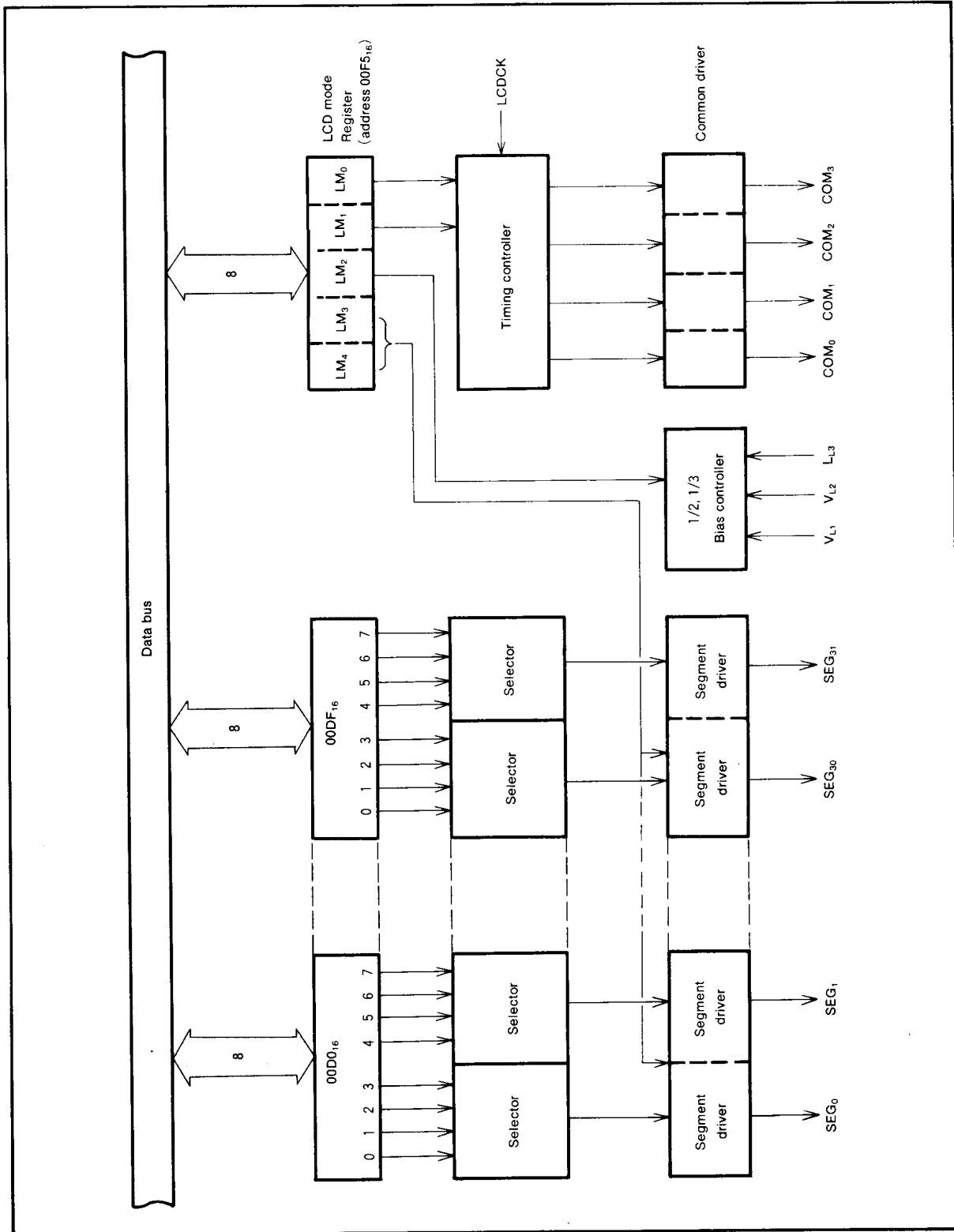


Fig.13 Block diagram of LCD control circuit

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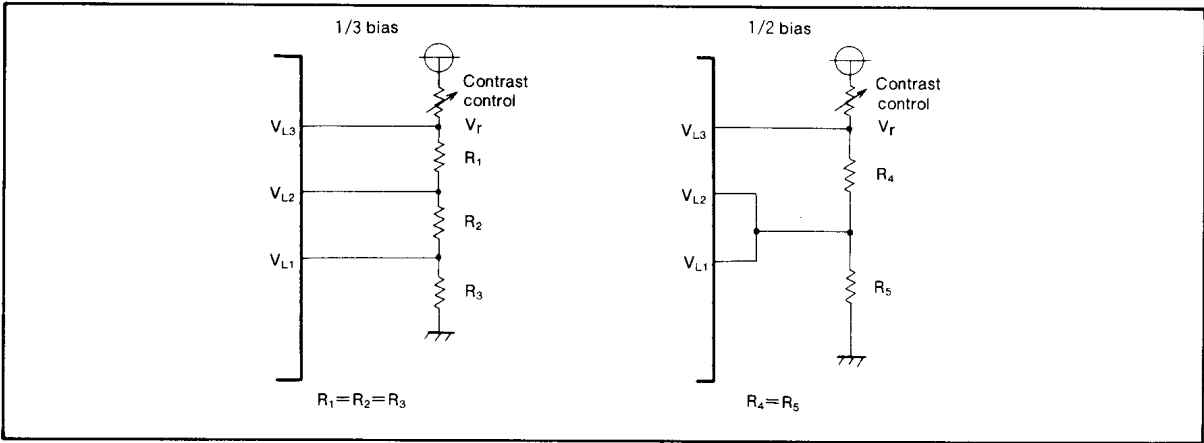


Fig.14 Example of circuit at 1/3 bias, 1/2 bias

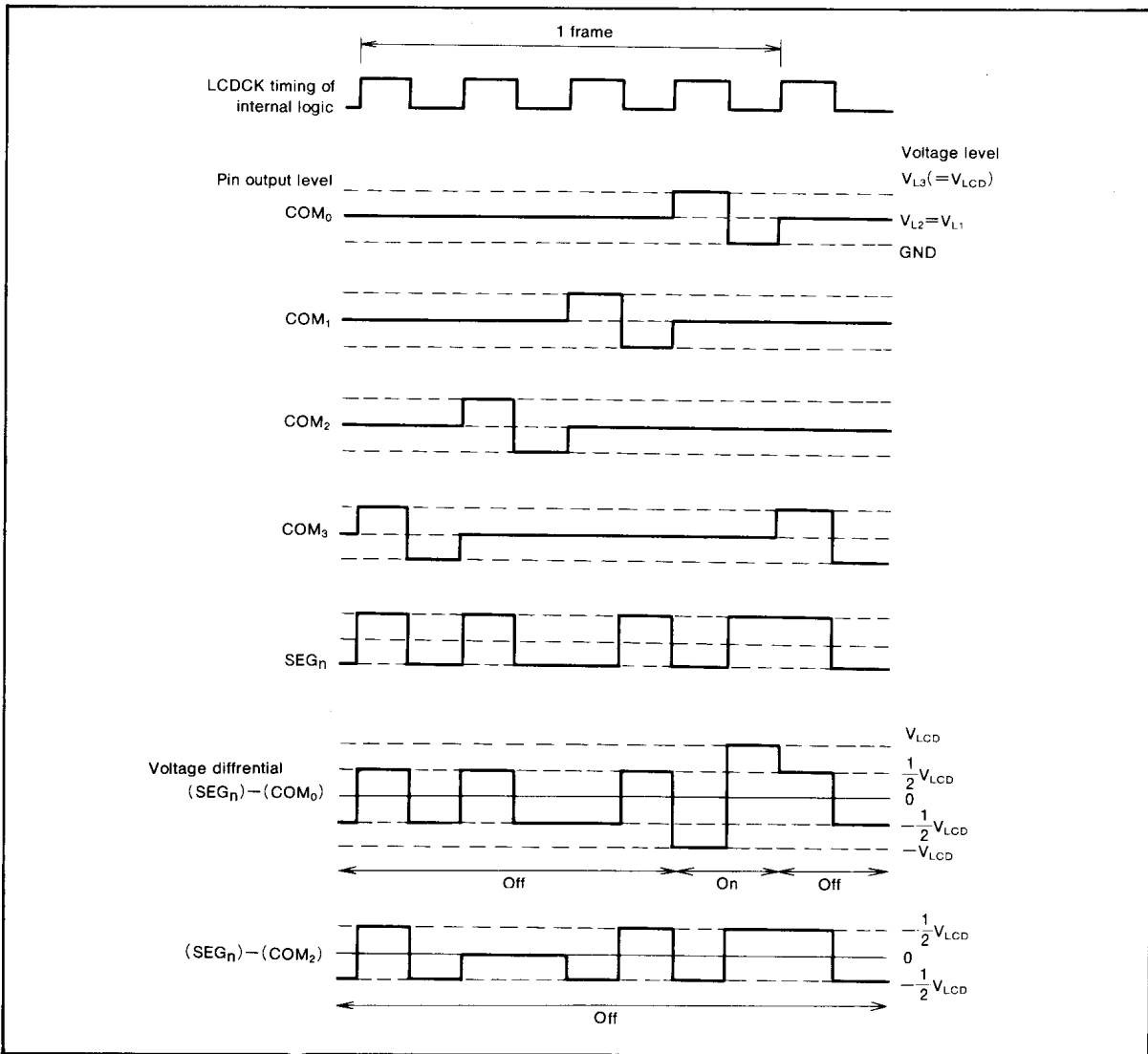


Fig.15 Example of 1/2 bias, 1/4 duty waveforms and resulting voltage differential between  $SEG_n$  and  $COM_n$ .



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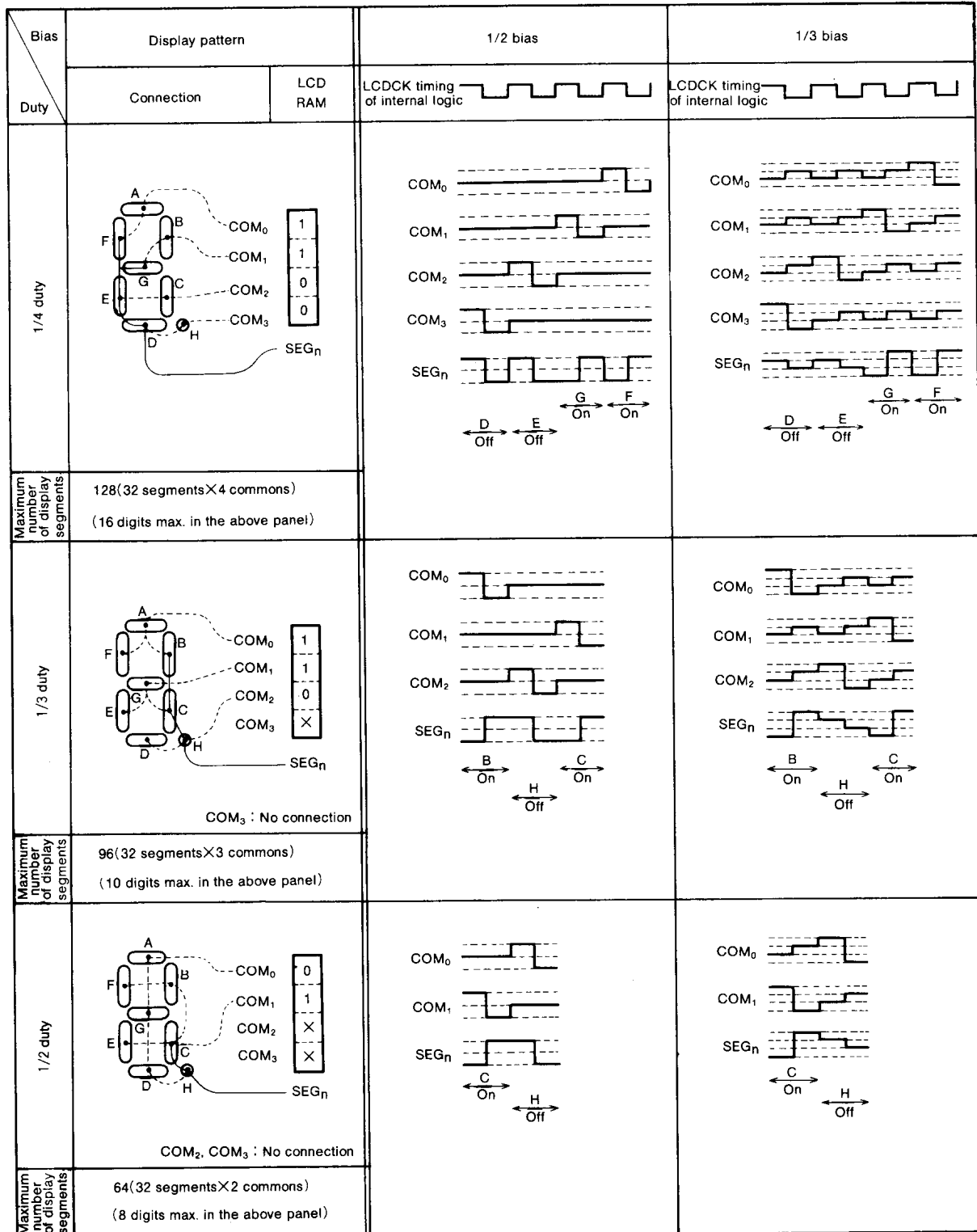


Fig.16 Example of drive waveforms for each bias and duty

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**KEY ON WAKE UP**

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P2 has a "L" level applied, after bit 7 of the serial I/O mode register ( $SM_7$ ) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. As shown in Figure 17, a key matrix can be connected to port P2 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the  $\overline{INT}_2$  interrupt. When  $SM_7$  is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and  $\overline{INT}_2$  are invalid.

In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and  $SM_7$  is "1", all of port P2 must be input "H".

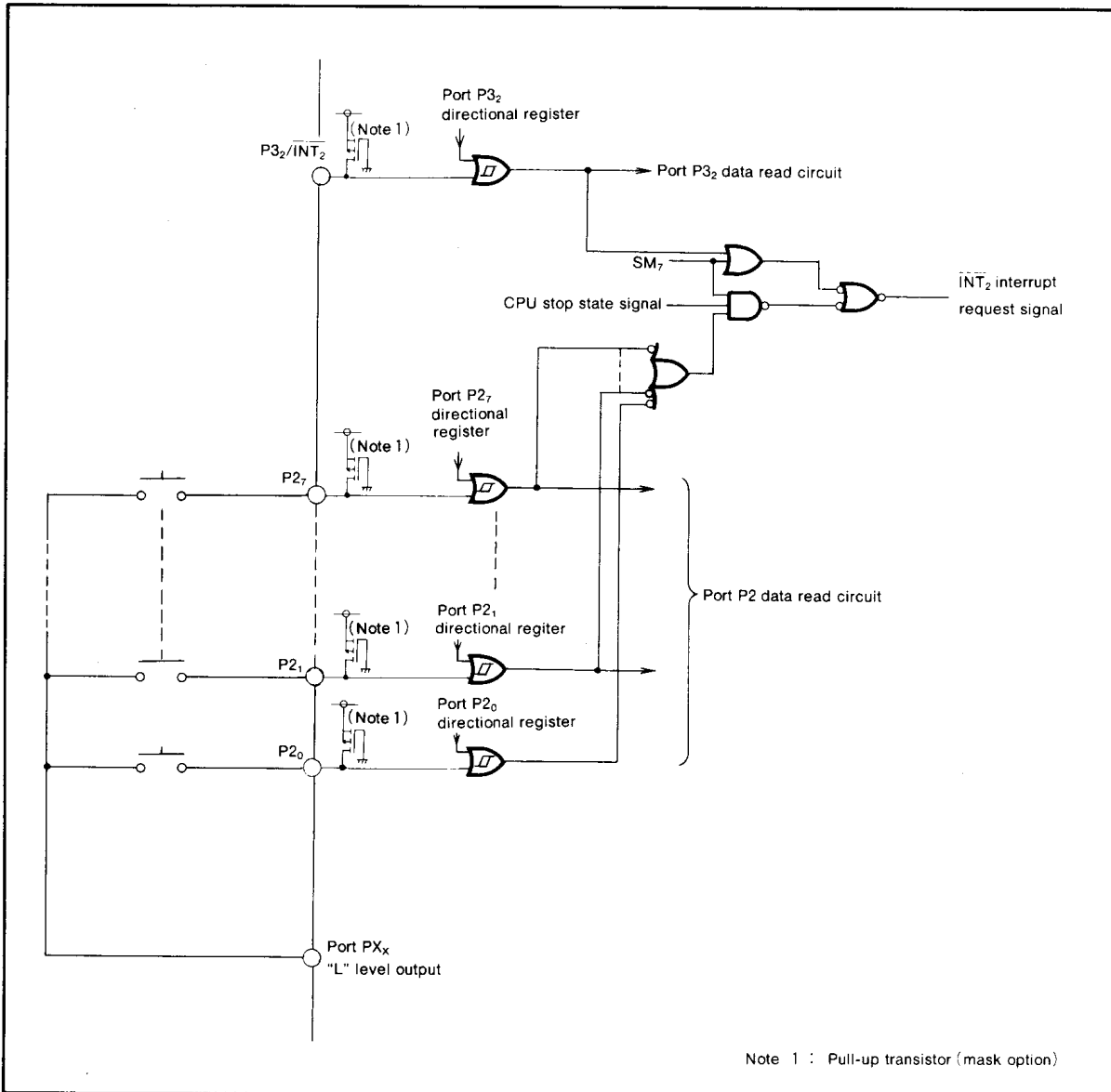


Fig.17 Block diagram of port P2 and P3<sub>2</sub>, and example of wired at used key on wake up

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**RESET CIRCUIT**

The M50930-XXXXP is reset according to the sequence shown in Figure 20. It starts the program from the address formed by using the content of address 3FFF<sub>16</sub> as the high order address and the content of the address 3FFE<sub>16</sub> as the low order address, when the RESET pin is held at "L" level for at least 8 rising edges from X<sub>IN</sub> while the power voltage

is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 18.

An example of the reset circuit is shown in Figure 19. When the power on reset is used, the RESET pin must be held "L" until the oscillation of X<sub>IN</sub>-X<sub>OUT</sub> becomes stable.

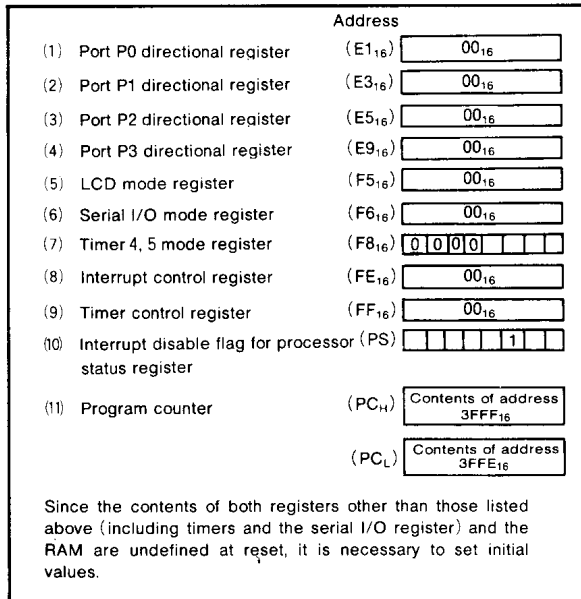


Fig.18 Internal state of microcomputer at reset

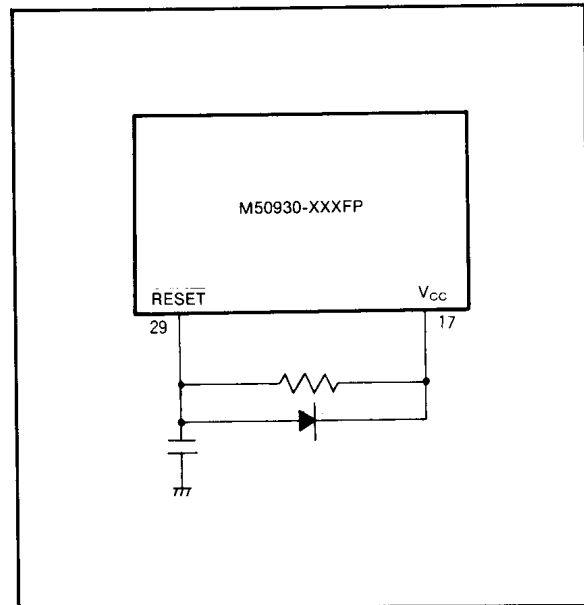


Fig.19 Example of reset circuit

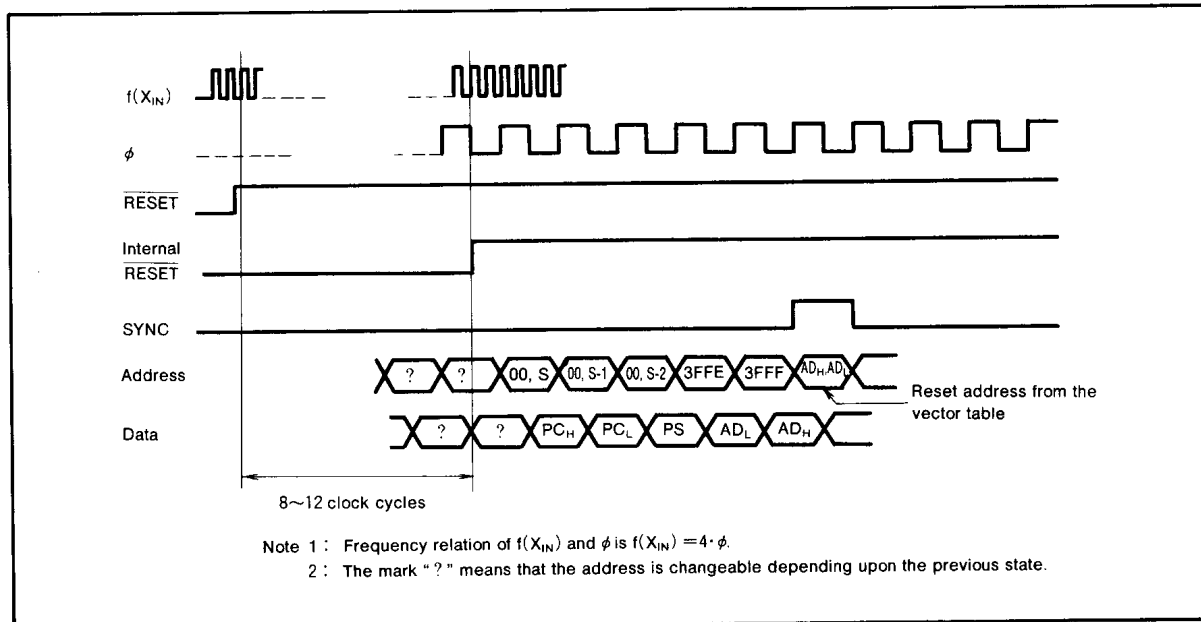


Fig.20 Timing diagram at reset

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### I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 1, P0 can be accessed as memory through zero page address 00E0<sub>16</sub>. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address 00E1<sub>16</sub>) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

Depending on the status of the processor status bits (bit 0 and bit 1 of address 00FF<sub>16</sub>), three different modes can be selected; single-chip mode, memory expanding mode and microprocessor mode. For more details, refer to the timing diagram shown in Figure 24.

(2) Port P1

In the single chip mode, Port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's. For more details, see the processor mode information. Following the execution of STP or WIT instruction, P2 can be used to generate the "wake up mode". This mode is used to bring the microcomputer back in its normal operating mode after being in the power-down mode.

(4) Port P3

Port P3 has the same functions as P0 except that part of P3 is common with the serial I/O lines (ie. output of timer 3, input/output of timer clock, and interrupt input).

(5) Segment Output (SEG<sub>0</sub>~SEG<sub>23</sub>)

These ports drive and control the LCD segments.

(6) Port P4

Port P4 is an 8-bit input port which can be used as a LCD segment output port.

(7) Common output (COM<sub>0</sub>~COM<sub>3</sub>)

These port provides output drive and control for the LCD common lines.

(8) Power Supply for LCD. (V<sub>L1</sub>~V<sub>L3</sub>)

Supplies power to the LCD terminals.

(9)  $\overline{\text{INT}}_1$

The  $\overline{\text{INT}}_1$  pin is an interrupt input pin. The  $\overline{\text{INT}}_1$  interrupt request bit (bit 7 of address 00FE<sub>16</sub>) is set to "1" when the input level of this pin changes from "H" to "L". This input level is read into bit 1 of the timer 4 and 5 mode register (address 00F8<sub>16</sub>).

(10)  $\overline{\text{INT}}_2$  ( $\overline{\text{INT}}_2/\text{P3}_2$ )

The  $\overline{\text{INT}}_2$  pin is an interrupt input pin common with P3<sub>2</sub>. When P3<sub>2</sub>'s directional register is set for input ("0"), this pin can be used as an interrupt input. The  $\overline{\text{INT}}_2$  interrupt request bit (bit 1 of address 00FE<sub>16</sub>) is automatically set to "1" when the input level of this pin changes from "H" to "L".

(11) CNTR

The CNTR pin is an I/O pin of timers 4 and 5. The input level is read into bit 0 of the timer 4 and 5's mode register (address 00F8<sub>16</sub>).

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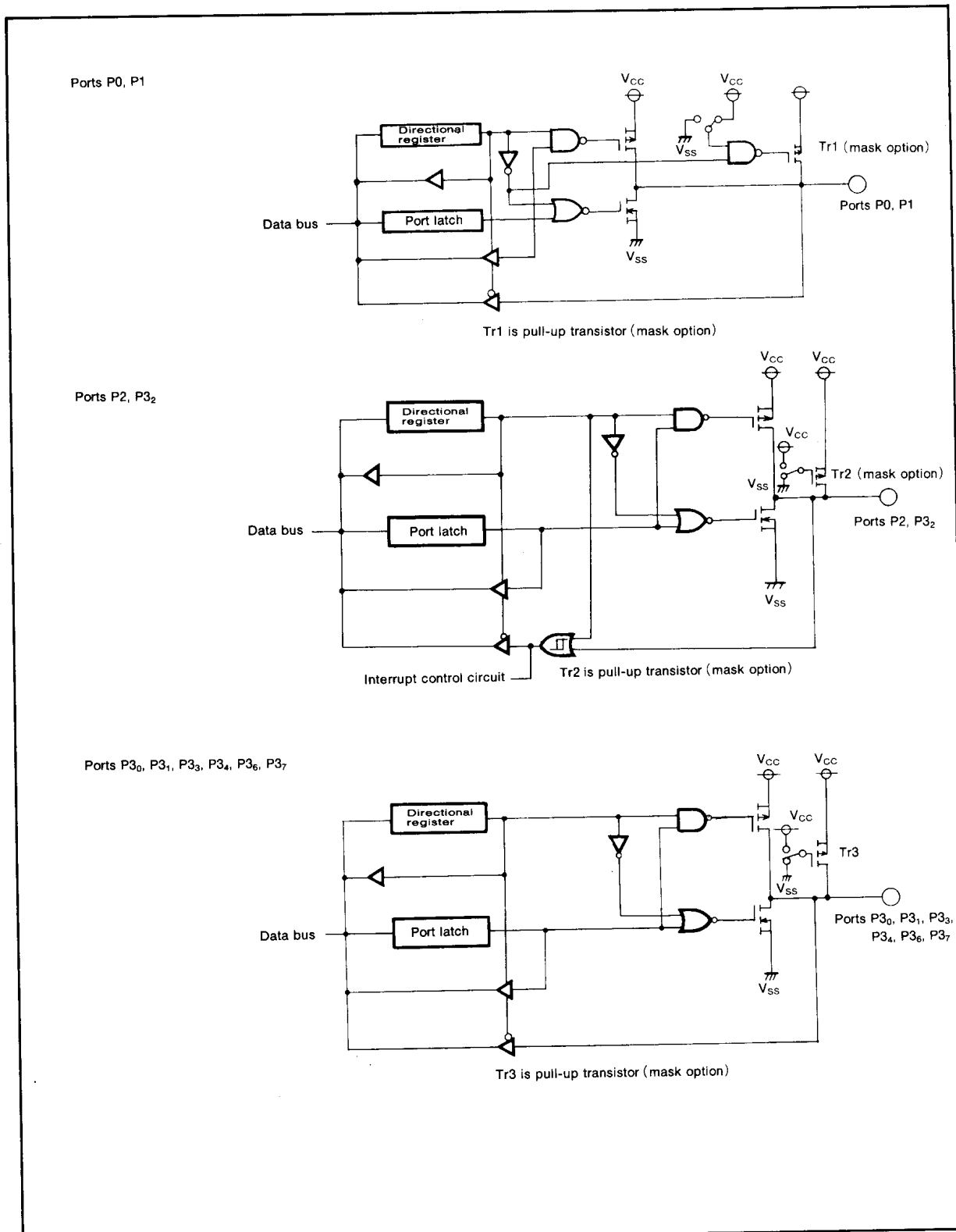


Fig.21 Block diagram of ports P0~P3

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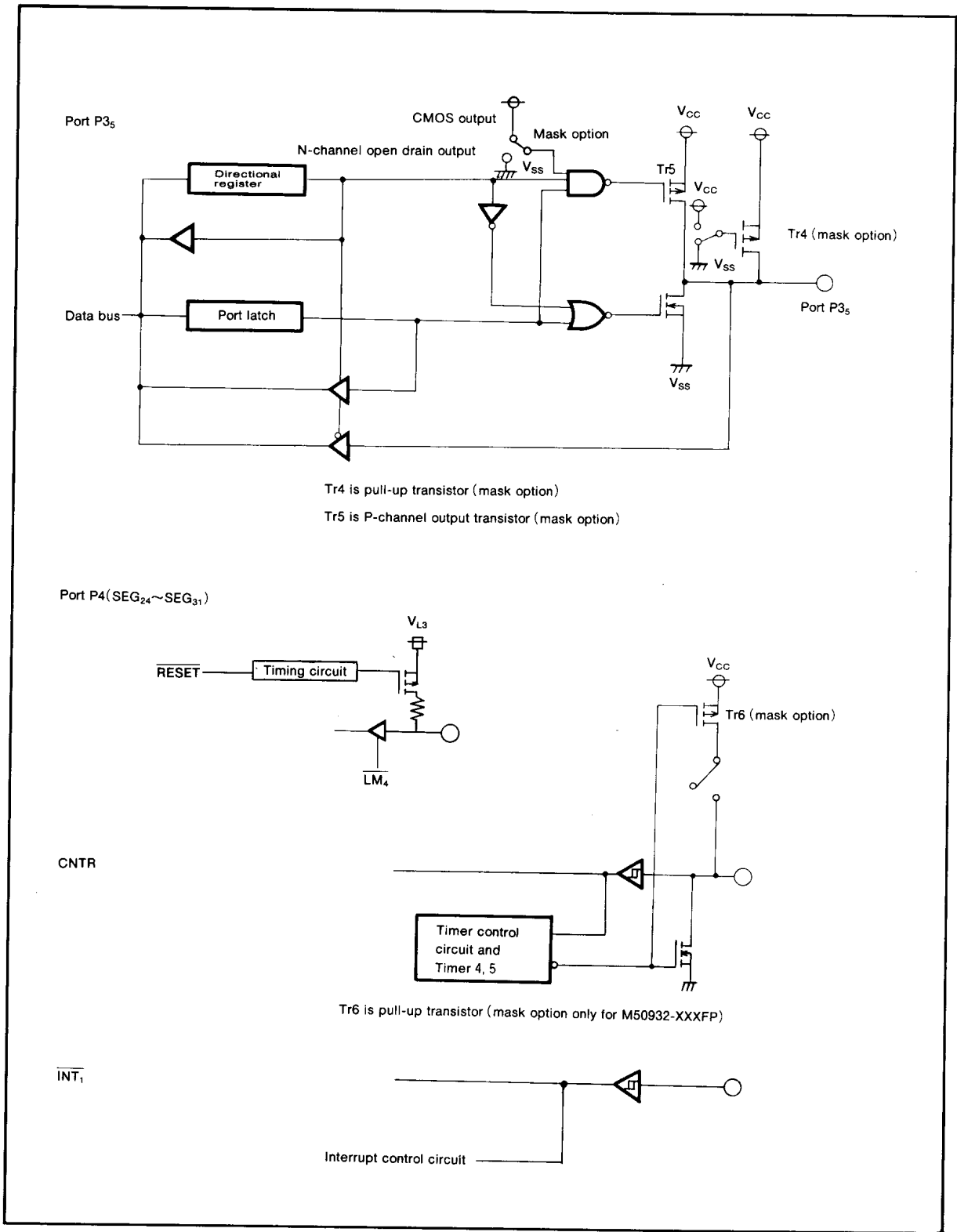


Fig.22 Block diagram of ports P3, P4, CNTR, and INT<sub>1</sub>

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**PROCESSOR MODE**

By changing the contents of the processor mode bit (bit 0 and 1 of address  $00FF_{16}$ ), three different operation modes can be selected; single-chip mode, memory expanding mode and microprocessor mode. In the memory expanding mode and microprocessor mode, ports P0~P2 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports. The function of the  $X_{OUT}$  pin can also be changed. For more details see Figure 24.

The memory map of the single-chip mode is illustrated in Figure 1, and the other modes are shown in Figure 23. By connecting the  $CNV_{SS}$  to  $V_{SS}$ , all three modes can be selected through software by changing the processor mode register. Connecting  $CNV_{SS}$  to  $V_{CC}$  automatically forces the microcomputer into microprocessor mode. The three different modes are explained as follows:

- (1) Single-chip mode [00]  
 The microcomputer will automatically be in the single-chip mode when started from reset, if  $CNV_{SS}$  is connected to  $V_{SS}$ . Ports P0~P2 will work as original I/O ports.
- (2) Memory expanding mode [01]  
 The microcomputer will be changed to the memory expanding mode if  $CNV_{SS}$  is connected to  $V_{SS}$  and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient. Ports P0 and P1 are used as address output with the original I/O function lost. Port P2 is used as  $D_7 \sim D_0$  data I/O with the original I/O function lost. Port P1<sub>7</sub> and P1<sub>6</sub> works as  $R/\bar{W}$  and  $\phi$ .
- (3) Microprocessor mode [10].  
 After connecting  $CNV_{SS}$  to  $V_{CC}$  and initiating a reset, the microcomputer will automatically default to this mode. This mode is the same as the memory expanding mode except that the internal ROM is disable and external ROM is needed. The relationship between the input level of the  $CNV_{SS}$  and the processor mode is shown in Table 2.

The SYNC signal is output from the  $X_{OUT}$  pin in every mode except the single-chip mode, when 10V is supplied to the  $\overline{RESET}$  pin or when bit 5 of the LCD mode register is set to "1". The SYNC signal becomes a synchronous signal that goes to "H" level while the Op code is being fetched. When the SYNC output signal is selected, the original function of the  $X_{OUT}$  pin is lost. In addition, if  $LM_7=1$  and  $SM_6=0$ , the SYNC signal is not output from the  $X_{OUT}$  pin.

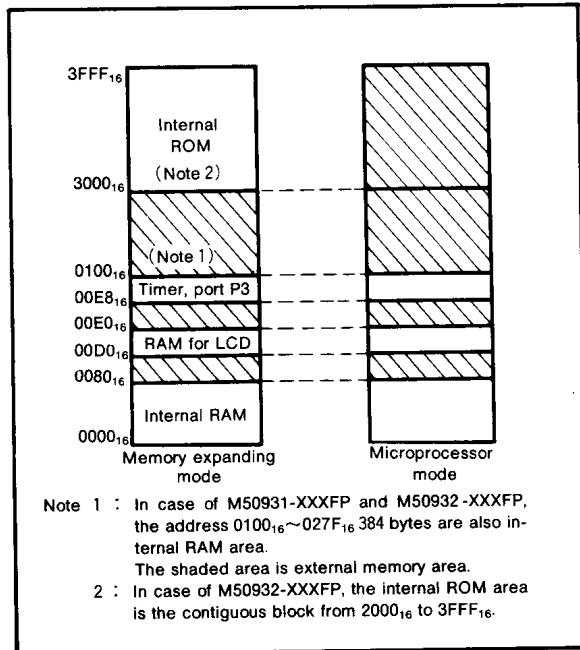


Fig.23 External memory area in processor mode

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	TM <sub>1</sub>	0	0	1
	TM <sub>0</sub>	0	1	0
Mode				
Port		Single-chip mode	Memory expanding mode	Microprocessor mode
Port P0			Same as left	
Port P1 lower 6 Bits			Same as left	
Port P2			Same as left	
Port P1 higher 2 bits			Same as left	
X <sub>OUT</sub>			Same as left	

**Fig.24 Processor mode and functions of ports P0~P2 and X<sub>OUT</sub>**

Note 1 : In order to use X<sub>OUT</sub> pin as SYNC output, put  $\overline{\text{RESET}}$  to 10V or set bit 5 of the address 00F5<sub>16</sub> to "1".  
 When LM<sub>7</sub>=1 and SM<sub>6</sub>=0, X<sub>OUT</sub> does not output SYNC.

**Table 2. Relationship between CNV<sub>SS</sub> pin input level and processor mode**

CNV <sub>SS</sub>	Mode	Explanation
V <sub>SS</sub>	<ul style="list-style-type: none"> <li>• Single-chip mode</li> <li>• Memory expanding mode</li> <li>• Microprocessor mode</li> </ul>	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V <sub>CC</sub>	<ul style="list-style-type: none"> <li>• Microprocessor mode</li> </ul>	The microprocessor mode is set by the reset.



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**CLOCK GENERATING CIRCUIT**

The M50930-XXXFP has two internal clock generating circuit. Figure 27 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin  $X_{IN}$  divided by four is used as the internal clock (timing output)  $\phi$ . Bit 7 of LCD mode register can be used to switch the internal clock  $\phi$  to 1/2 the frequency applied to the clock input pin  $X_{CIN}$ .

Figure 25 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input form the  $X_{IN}(X_{CIN})$  pin and leave the  $X_{OUT}(X_{COUT})$  pin open. A circuit example is shown in Figure 26.

The M50930-XXXFP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both  $X_{IN}$  clock and  $X_{CIN}$  clock) stops with the internal clock  $\phi$  held at "H" level. In this case timer 1 and timer 2 are forcibly connected and  $\phi/4$  is selected as timer 1 input. Before executing the STP instruction, appropriate values must be set in timer 1 and timer 2 to enable the oscillator to stabilize when restarting oscillation. Before executing the STP instruction, the timer 1 count stop bit must be set to supply ("0"), timer 1 interrupt enable bit and timer 2 interrupt enable bit must be set to disable ("0"), and timer 2 interrupt request bit must be set to no request ("0").

Oscillation is restarted (release the stop mode) when  $INT_1$ ,  $INT_2$ , or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock  $\phi$  is held "H" until timer 2 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the  $\overline{RESET}$  pin until the oscillation stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock  $\phi$  stops at "H" level, but the oscillator does not stop.  $\phi$  is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the  $X_{IN}$  clock is stopped and the internal clock  $\phi$  is generated from the  $X_{CIN}$  clock ( $45\mu A$  Typ. at  $f(X_{CIN})=32kHz$ ).  $X_{IN}$  clock oscillation is stopped when the bit 6 of LCD mode register (address  $00F6_{16}$ ) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the  $\overline{RESET}$  pin until the oscillation stabilizes when resetting while the  $X_{IN}$  clock is stopped. Figure 28 shows the transition of states for the system clock.

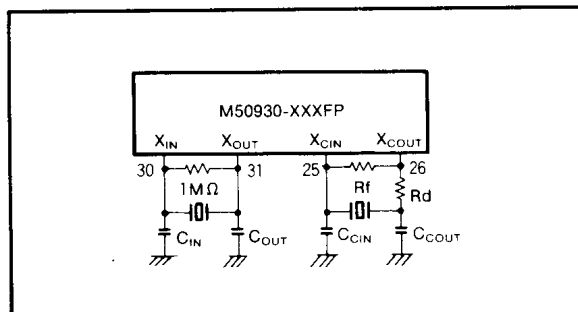


Fig.25 External ceramic resonator circuit

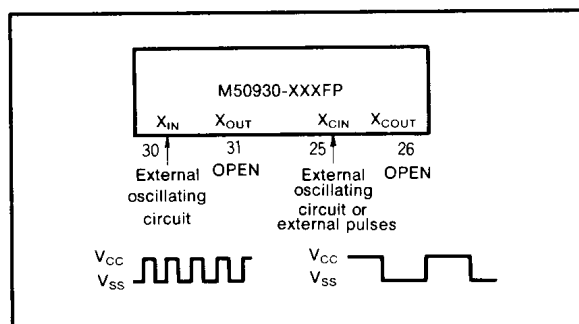


Fig.26 External clock input circuit



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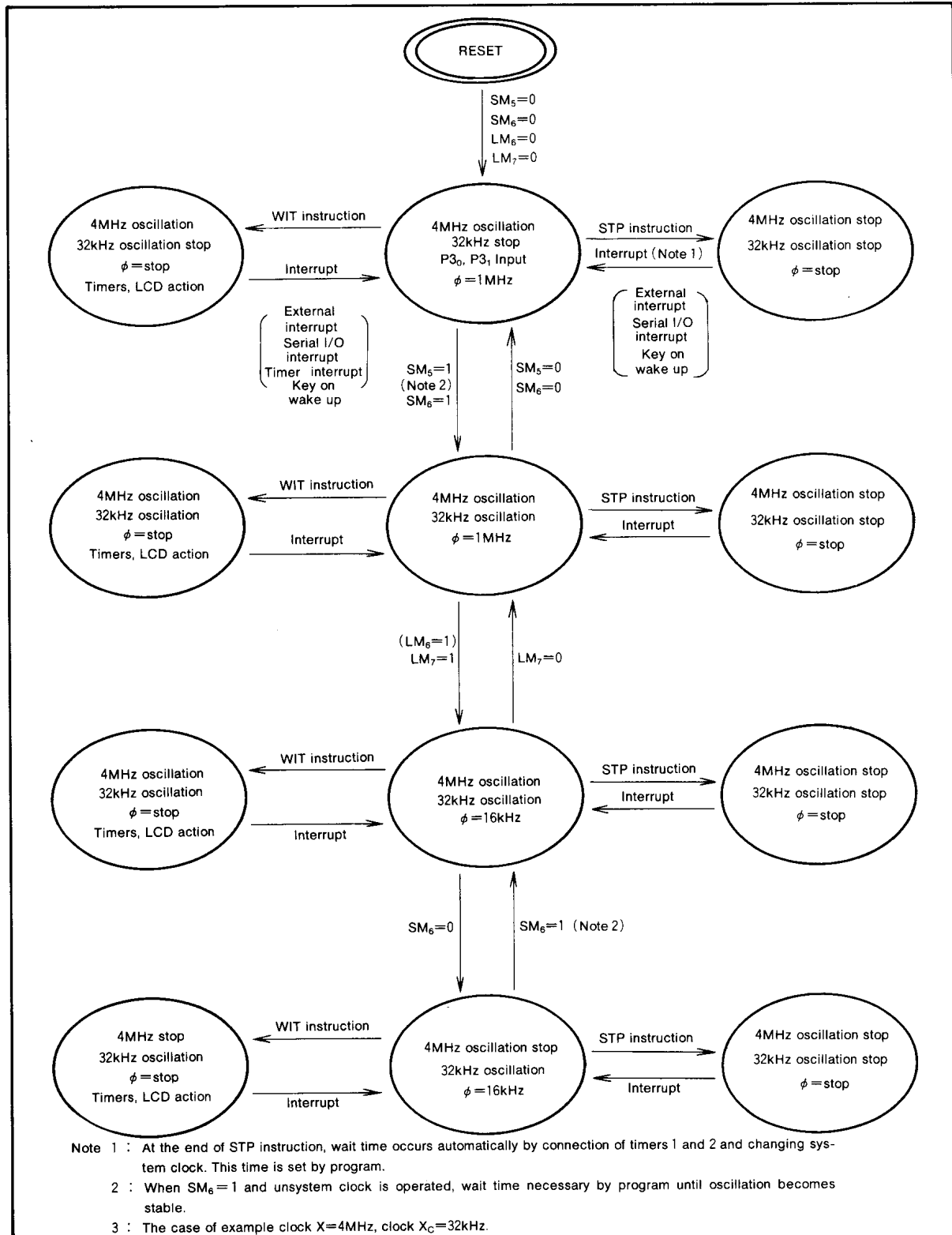
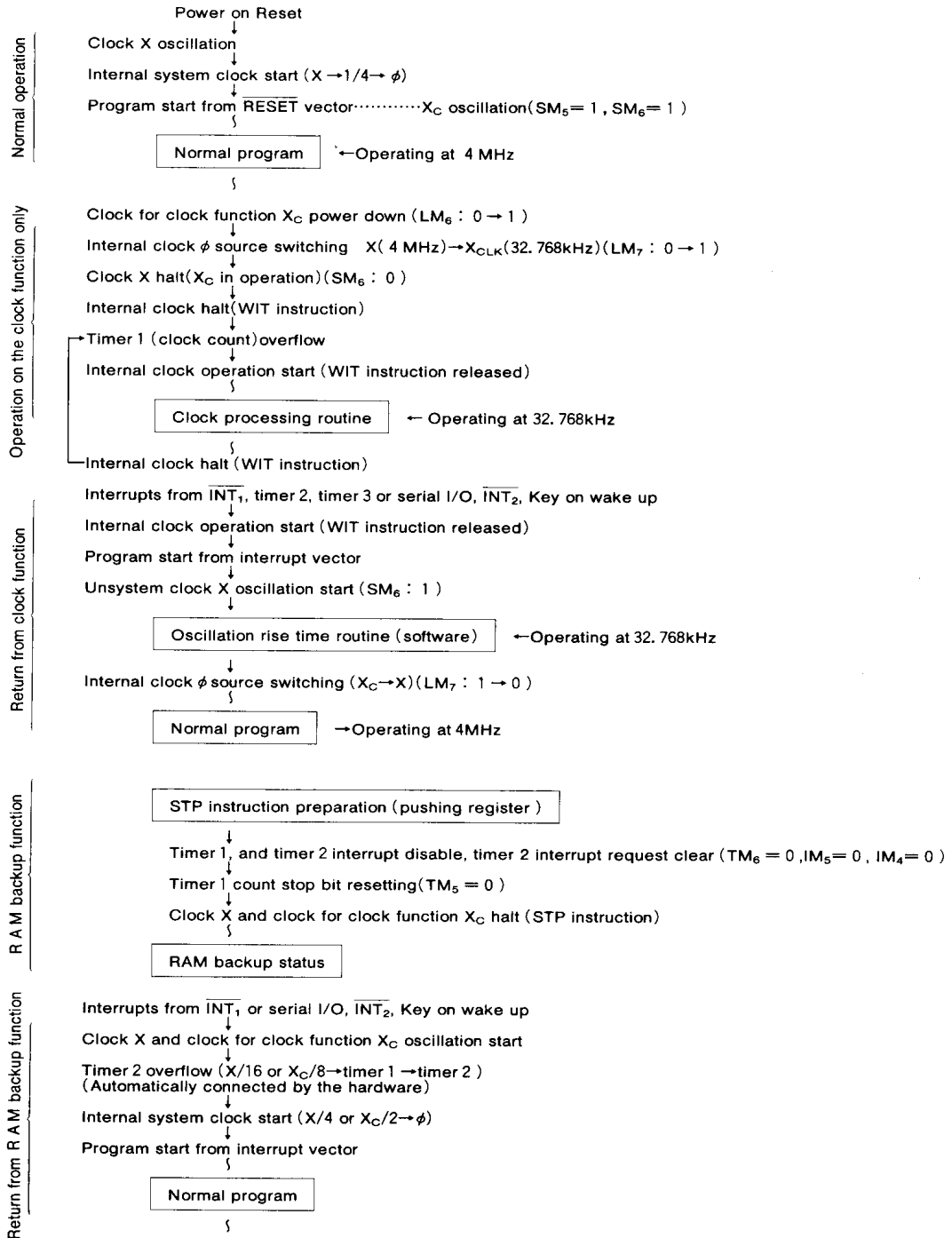


Fig.28 Transition of states for the system clock

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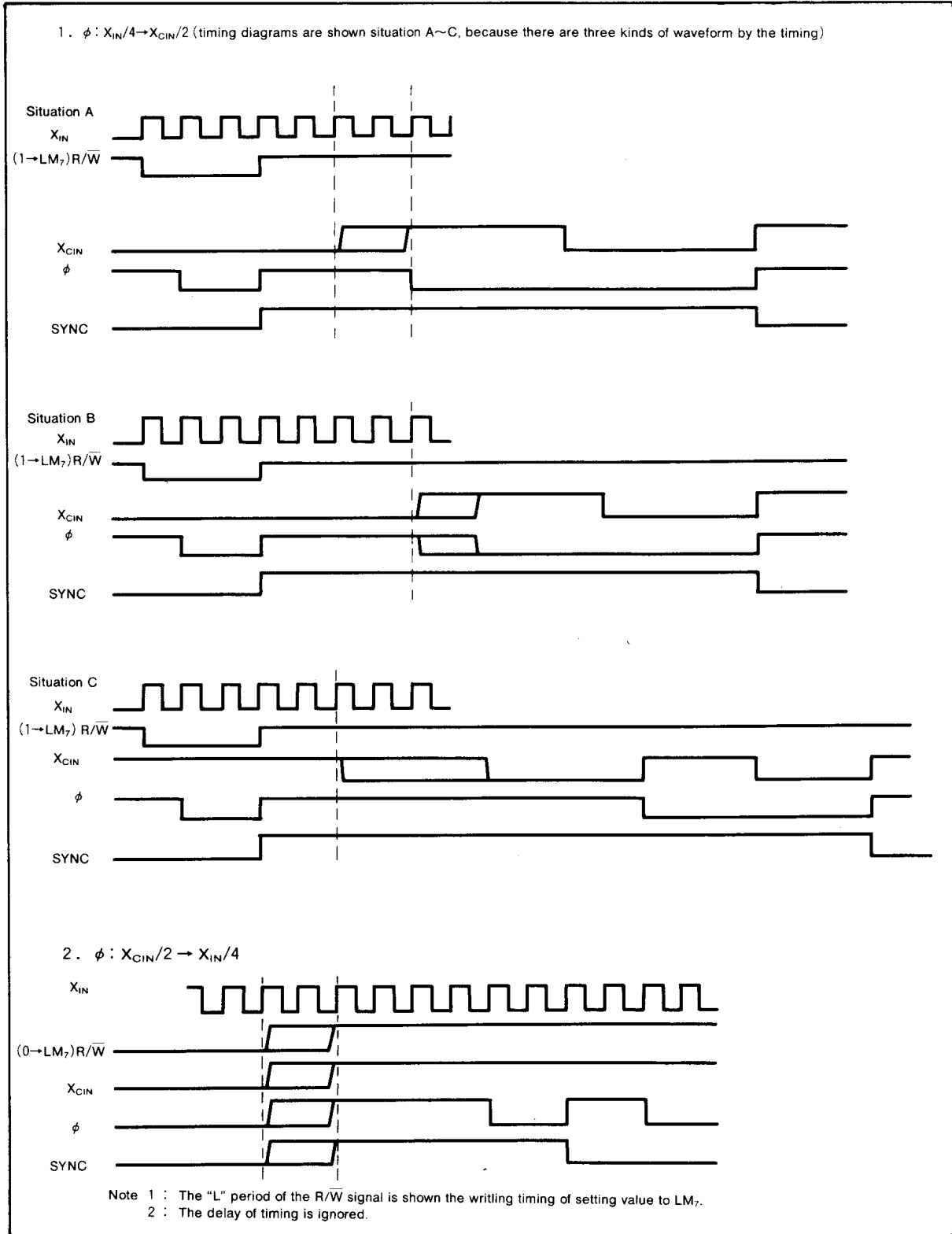
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<An example of flow for system>



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**Fig.29** Timing diagram of the changing system clock

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**PROGRAMMING NOTES**

- (1) The frequency ratio of the timer is  $1/(n+1)$ .
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) When the timer 4 and the timer 5 are used at event counter mode, read the contents of these timers either while the input of the these timers are not changing or after timer 4, 5 count stop bit (bit 6 of address 00F8<sub>16</sub>) is set to "1".  
Also, when the timer 1, timer 2, or timer 3 is input the clock except  $\phi/4$  or it divided by timer, control the same as above.
- (4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC,CLC, or CLD instructions are executed.
- (5) A NOP instruction must be used after the execution of a PLP instruction.
- (6) When LCD turn-on bit (bit 3 of address 00F5<sub>16</sub>) of the LCD mode register is "1", don't stop the timers or count source for timers.
- (7) The serial I/O counter must be initialized (write to 00F7<sub>16</sub>) after switching the transfer clock source.
- (8) When using an external clock as the transfer clock source, the serial I/O counter must be initialized while the external clock is at "H" level.
- (9) The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.
- (10) When using pins P3<sub>0</sub> and P3<sub>1</sub> as clock I/O pins, the pull-up option must not be used.
- (11) Notes on controlling the clock generation circuit
  - ① When system clock is changed  $X_{IN}/4$  to  $X_{CIN}/2$ , set LM<sub>7</sub> to "1" after oscillation is stable by the software in side of clock X<sub>C</sub>.
  - ② When system clock is changed  $X_{CIN}/2$  to  $X_{IN}/4$ , set LM<sub>7</sub> to "0" after oscillation is stable by the software in side of clock X.
  - ③ When SM<sub>5</sub> is "0" or when LM<sub>7</sub> is "0" and SM<sub>6</sub> is "0", LM<sub>6</sub> is automatically set to "0" by the hardware.
  - ④ When system clock selection bit (bit 7 of address 00F5<sub>16</sub>) of the LCD mode register is "1", don't set SM<sub>5</sub> to "0".
  - ⑤ In single-chip mode, the X<sub>OUT</sub> pin uses as X<sub>OUT</sub> output except setting value of LM<sub>5</sub>.
  - ⑥ The other than single-chip mode and the input voltage for RESET pin is 10V, X<sub>OUT</sub> pin uses as SYNC output except setting value of LM<sub>5</sub>.

Just for reference, timing diagram of the changing system clock are shown in Figure 29.

**DATA REQUIRED FOR MASK ORDERING**

Please send the following data for mask orders.

- (1) mask ROM confirmation form
- (2) mark specification form
- (3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P3<sub>5</sub>/S<sub>OUT</sub> output format
- CNTR pin pull-up transistor (M50932-XXXFP only)

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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage		-0.3~7	V
$V_i$	Supply voltage for LCD $V_{L1}\sim V_{L3}$		-0.3~ $V_{CC}+0.3$	V
$V_i$	Input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7, P4_0\sim P4_7, X_{IN}$		-0.3~ $V_{CC}+0.3$	V
$V_i$	Input voltage $INT_1, CNV_{SS}$		-0.3~7	V
$V_i$	Input voltage $RESET, CNTR$	Output transistor are "off"	-0.3~13	V
$V_o$	Output voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7, COM_0\sim COM_3, SEG_0\sim SEG_{31},$ $X_{OUT}$		-0.3~ $V_{CC}+0.3$	V
$V_o$	Output voltage $CNTR$		-0.3~7	V
$P_d$	Power dissipation	$T_a = 25^\circ C$	300	mW
$T_{opr}$	Operating temperature		-10~70	$^\circ C$
$T_{stg}$	Storage temperature		-40~125	$^\circ C$

**RECOMMENDED OPERATING CONDITIONS** ( $V_{CC}=2.7\sim 5.5V, V_{SS}=0V, T_a=-10\sim 70^\circ C$ , unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$V_{CC}$	Supply voltage (Note 1)	$f(X_{IN})=4.3MHz$ $f(X_{IN})=1.1MHz$	4.5 2.7		5.5 5.5	V
$V_{SS}$	Supply voltage			0		V
$V_{IH}$	"H" input voltage $P0_0\sim P0_7, P1_0\sim P1_7,$ $P3_0, P3_1$ (Note 2), $P3_3\sim P3_7$ (Note 3), $P4_0\sim P4_7,$ $RESET, X_{IN}, CNV_{SS}$		$0.7V_{CC}$		$V_{CC}$	V
$V_{IH}$	"H" input voltage $P2_0\sim P2_7, P3_2, P3_6$ (Note 4), $INT_1, CNTR$		$0.74V_{CC}$		$V_{CC}$	V
$V_{IL}$	"L" input voltage $P0_0\sim P0_7, P1_0\sim P1_7,$ $P3_0, P3_1$ (Note 2), $P3_3\sim P3_7$ (Note 3), $P4_0\sim P4_7,$ $CNV_{SS}$		0		$0.3V_{CC}$	V
$V_{IL}$	"L" input voltage $P2_0\sim P2_7, P3_2, P3_6$ (Note 4), $INT_1, CNTR$		0		$0.26V_{CC}$	V
$V_{IL}$	"L" input voltage $RESET$		0		$0.12V_{CC}$	V
$V_{IL}$	"L" input voltage $X_{IN}$		0		$0.16V_{CC}$	V
$I_{OH}$	"H" output current $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7$ (Note 5), $X_{OUT}$				-2	mA
$I_{OL(peak)}$	"L" peak output current $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7,$ $P3_0\sim P3_7, CNTR, X_{OUT}$ (Note 6)				10	mA
$I_{OL(avg)}$	"L" average output current $P0_0\sim P0_7, P1_0\sim P1_7,$ $P2_0\sim P2_7, P3_0\sim P3_7,$ $CNTR, X_{OUT}$ (Note 7)				5	mA
$f(X_{IN})$	Clock oscillating frequency (Note 8)	$V_{CC}=4.5\sim 5.5V$ $V_{CC}=2.7\sim 5.5V$	64 64		4300 1100	kHz
$f(X_{CIN})$	Clock oscillating frequency for clock function (Note 8)		32		50	kHz

- Note 1 : When only maintaining the RAM data, minimum value of  $V_{CC}$  is 2V.  
 2 : When using port  $P3_1$  as  $X_{CIN}$ ,  $0.85V_{CC} \leq V_{IH} \leq V_{CC}$ ,  $0 \leq V_{IL} \leq 0.15V_{CC}$  for port  $P3_1$ .  
 3 : In this case of using port  $P3_6$  as normal input.  
 4 : In this case of using port  $P3_6$  as CLK input.  
 Especially when the input oscillation frequency is more than 50kHz, recommend the following :  
 $0.8V_{CC} \leq V_{IH} \leq V_{CC}$ ,  $0 \leq V_{IL} \leq 0.2V_{CC}$   
 5 : The total of  $I_{OH}$  of port  $P0, P1, P2, P3$  and  $X_{OUT}$  should be 35mA max.  
 6 : The total of  $I_{OL(peak)}$  of port  $P0, P1, P2, P3$  should be 55mA max, and the total of  $I_{OL(peak)}$  of port  $P3, CNTR$ , and  $X_{OUT}$  should be 45mA max.  
 7 :  $I_{OL(avg)}$  is the average current in 100ms.  
 8 : When changing the contents of the most significant bit at address 00F5<sub>16</sub>,  $f(X_{IN})$  needs the following range :  $f(X_{IN}) > 3f(X_{CIN})$ .

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**ELECTRICAL CHARACTERISTICS** ( $V_{SS}=0V$ ,  $T_a=-10\sim 70^\circ C$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit		
			Min.	Typ.	Max.			
$V_{OH}$	"H" output voltage $P_0\sim P_7$ , $P_{10}\sim P_{17}$ , $P_{20}\sim P_{27}$ , $P_{30}\sim P_{37}$ (Note 9)(Note10)	$V_{CC}=5V$ , $I_{OH}=-2mA$	3			V		
		$V_{CC}=3V$ , $I_{OH}=-0.7mA$	2					
$V_{OH}$	"H" output voltage $X_{OUT}$	$V_{CC}=5V$ , $I_{OH}=-1.5mA$ $V_{CC}=3V$ , $I_{OH}=-0.3mA$	3 2			V		
$V_{OL}$	"L" output voltage $P_0\sim P_7$ , $P_{10}\sim P_{17}$ , $P_{20}\sim P_{27}$ , $P_{30}\sim P_{37}$ (Note10), CNTR	$V_{CC}=5V$ , $I_{OL}=10mA$			2	V		
		$V_{CC}=3V$ , $I_{OL}=3mA$			1			
$V_{OL}$	"L" output voltage $X_{OUT}$	$V_{CC}=5V$ , $I_{OL}=1.5mA$			2	V		
		$V_{CC}=3V$ , $I_{OL}=0.3mA$			1			
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$ , CNTR	$V_{CC}=5V$	0.25		1	V		
		$V_{CC}=3V$	0.15		0.7			
$V_{T+}-V_{T-}$	Hysteresis $P_{36}$	When used as CLK input	$V_{CC}=5V$ $V_{CC}=3V$		0.5 0.4	V		
		When used as $X_{CIN}$ input	$V_{CC}=5V$ $V_{CC}=3V$		0.7 0.5			
$V_{T+}-V_{T-}$	Hysteresis $P_{31}$	$V_{CC}=5V$			0.5	V		
		$V_{CC}=3V$			0.4			
$V_{T+}-V_{T-}$	Hysteresis $P_{20}\sim P_{27}$ , $P_{32}$	$V_{CC}=5V$			0.5	V		
		$V_{CC}=3V$			0.4			
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	$V_{CC}=5V$			0.5	V		
		$V_{CC}=3V$			0.35			
$V_{T+}-V_{T-}$	Hysteresis $X_{IN}$	$V_{CC}=5V$			0.5	V		
		$V_{CC}=3V$			0.35			
$I_{IL}$	"L" input current $P_4\sim P_7$ (except reset state), $[P_0\sim P_7, P_{10}\sim P_{17}, P_{20}\sim P_{27}, P_{30}\sim P_{37},$ CNTR (Note 12)] without pull-up Tr. CNTR (Note 11), $\overline{INT_1}$ , $\overline{RESET}$ , $X_{IN}$	$V_{CC}=5V$ $V_i=0V$			-5	$\mu A$		
		$V_{CC}=3V$ $V_i=0V$			-4			
		$V_{CC}=5V$ , $V_i=0V$ $V_{CC}=3V$ , $V_i=0V$	-30 -6	-70 -25	-140 -45			
$I_{IL}$	"L" input current $[P_0\sim P_7, P_{10}\sim P_{17}, P_{20}\sim P_{27}, P_{30}\sim P_{37},$ CNTR (Note 12)] with pull-up Tr.	$V_{CC}=5V$ , $V_i=0V$	-30		-140	$\mu A$		
		$V_{CC}=3V$ , $V_i=0V$	-6		-45			
$I_{IL}$	"L" input current $P_4\sim P_7$ (at reset state)	$V_{CC}=5V$ , $V_{L3}=5V$ , $V_i=0V$ $V_{CC}=3V$ , $V_{L3}=3V$ , $V_i=0V$	-30 -6		-140 -45	$\mu A$		
$I_{IH}$	"H" input current $P_4\sim P_7$ (except reset state), $P_0\sim P_7$ , $P_{10}\sim P_{17}$ , $P_{20}\sim P_{27}$ , $P_{30}\sim P_{37}$ , CNTR, $\overline{INT_1}$ , $\overline{RESET}$ , $X_{IN}$	$V_{CC}=5V$ $V_i=5V$			5	$\mu A$		
		$V_{CC}=3V$ $V_i=3V$			4			
		$V_{CC}=5V$ , $V_{L3}=5V$ , $V_i=5V$ $V_{CC}=3V$ , $V_{L3}=3V$ , $V_i=3V$			5 4			
$R_{COM}$	Output impedance $COM_0\sim COM_3$	$V_{L1}=V_{CC}/3$ $V_{L2}=2V_{L1}$ $V_{L3}=V_{CC}$	$V_{CC}=5V$ $V_{CC}=3V$	30 70	200 500	2000 4000	$\Omega$	
		Other COM, SEG pins are open.	$V_{CC}=5V$ $V_{CC}=3V$		2 3			
$R_S$	Output impedance $SEG_0\sim SEG_{31}$							
$I_{CC}$	Supply current (at operation)	Output pin are opened. $\overline{RESET}$ , $P_0\sim P_7$ , $P_{10}\sim P_{17}$ , $P_{20}\sim P_{27}$ , and $P_{30}\sim P_{37}$ are connected to $V_{CC}$ . Except the above pins are connected to $V_{SS}$ . However, $X_{IN}$ and $X_{CIN}$ are input signal according to the conditions.	$f(X_{IN})=4MHz$ , $V_{CC}=5V$ $f(X_{IN})=1MHz$ , $V_{CC}=3V$		3 0.4	6	mA	
			$T_a=25^\circ C$ $X_{IN}=0V$ $f(X_{CIN})=32.8kHz$ at low power mode ( $LM_6=1$ )	$V_{CC}=5V$ $V_{CC}=3V$		45 18		
			$f(X_{IN})=4MHz$ , $V_{CC}=5V$ $f(X_{IN})=1MHz$ , $V_{CC}=3V$			1 0.2		mA
			$T_a=25^\circ C$ $X_{IN}=0V$ $f(X_{CIN})=32.8kHz$ at low power mode ( $LM_6=1$ )	$V_{CC}=5V$ $V_{CC}=3V$		20 4	60 12	
$I_{CC}$	Supply current		$f(X_{IN})=0$ $f(X_{CIN})=0$ $V_{CC}=5V$	$T_a=25^\circ C$ $T_a=70^\circ C$	0.1	1 10	$\mu A$	
			$f(X_{IN})=0$ , $f(X_{CIN})=0$					
$V_{RAM}$	RAM retention voltage	$f(X_{IN})=0$ , $f(X_{CIN})=0$	2		5.5	V		

Note 9 : Except when the output type of  $P_{35}$  is N-channel open drain (mask option).  
10 : If  $P_{30}$  is used as  $X_{COUT}$ , capability of load driving is lower than the above.  
11 : For M50930-XXXFP and M50931-XXXFP  
12 : For M50932-XXXFP



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**TIMING REQUIREMENTS**

**Memory expanding mode and microprocessor mode** ( $V_{CC}=5V\pm 10\%$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ )

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU} (P2D-\phi)$	Port P2 input setup time		270			ns
$t_{SU} (P3D-\phi)$	Port P3 input setup time		270			ns
$t_{SU} (P4D-\phi)$	Port P4 input setup time		270			ns
$t_{WI}$	$\overline{INT}_1, \overline{INT}_2$ external clock input pulse width		1			$\mu S$
		$V_{CC}=2.7V$	4			
$t_{WR}$	RESET external clock input pulse width (Note 13)		2			$\mu S$
		$V_{CC}=2.7V$	8			
$t_h (\phi-P2D)$	Port P2 input hold time		20			ns
$t_h (\phi-P3D)$	Port P3 input hold time		20			ns
$t_h (\phi-P4D)$	Port P4 input hold time		20			ns
$t_C$	External clock input cycle time ( $X_{IN}$ pin)		250			ns
$t_W$	External clock input pulse width ( $X_{IN}$ pin)		75			ns
$t_r$	External clock rising edge time ( $X_{IN}$ pin)				25	ns
$t_f$	External clock falling edge time ( $X_{IN}$ pin)				25	ns
$t_{CC}$	External clock input cycle time ( $P3_1/X_{CIN}$ pin, $X_{CIN}$ )		20			$\mu S$
$t_{WC}$	External clock input pulse width ( $P3_1/X_{CIN}$ pin, $X_{CIN}$ )		5			$\mu S$
$t_{rC}$	External clock rising edge time ( $P3_1/X_{CIN}$ pin, $X_{CIN}$ )				6.2	$\mu S$
$t_{fC}$	External clock falling edge time ( $P3_1/X_{CIN}$ pin, $X_{CIN}$ )				6.2	$\mu S$

Note 13 : Hold RESET to "L" level while eight or more rise pulses are input from  $X_{IN}$ .

**SWITCHING CHARACTERISTICS**

**Memory expanding mode and microprocessor mode** ( $V_{CC}=5V\pm 10\%$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ )

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_d (\phi-P0A)$	Port P0 address output delay time	Fig. 30			250	ns
$t_d (\phi-P1A)$	Port P1 address output delay time				250	ns
$t_d (\phi-P2Q)$	Port P2 data output delay time				330	ns
$t_d (\phi-P2QF)$	Port P2 data output delay time				300	ns
$t_d (\phi-R/W)$	R/W signal output delay time				$t_{cyc}/4 + 200$	ns
$t_d (\phi-R/WF)$	R/W signal output delay time				250	ns
$t_d (\phi-SYNC)$	SYNC signal output delay time				250	ns
$t_d (\phi-P3Q)$	Port P3 data output delay time				250	ns

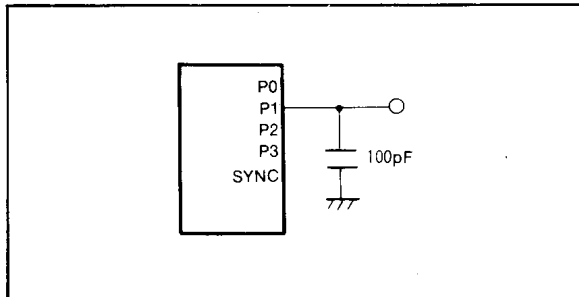


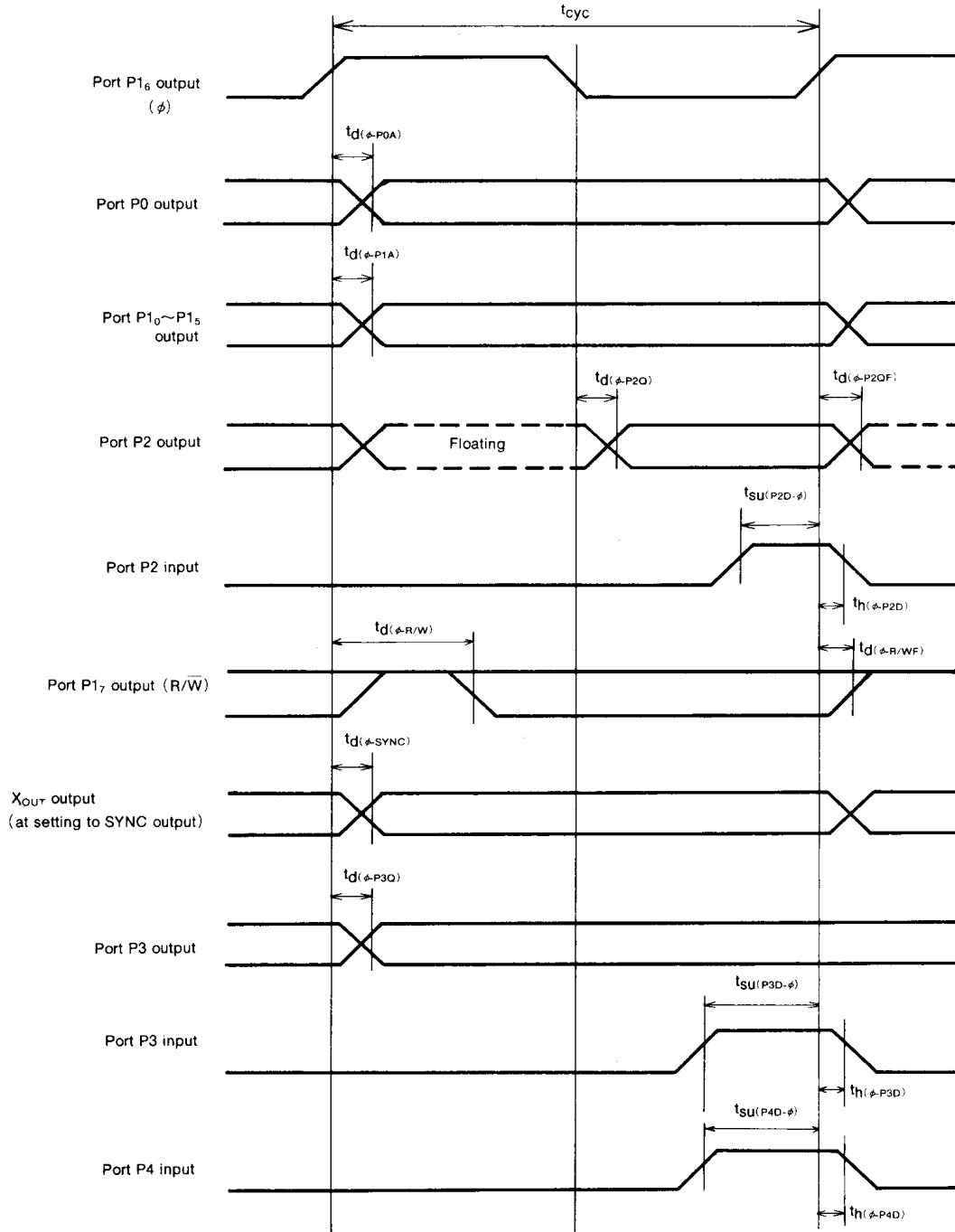
Fig.30 Port P0, P1, P2, P3, SYNC ( $X_{OUT}$ ) test circuit

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**TIMING DIAGRAMS**

In memory expanding mode and microprocessor mode



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