

# MITSUBISHI MICROCOMPUTERS

## M50743-PGYS

PIGGYBACK for M50743-XXXSP

### DESCRIPTION

The M50743-PGYS is an EPROM mounted-type micro-computer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputer M50743-XXXSP. The M50743-PGYS, being housed in a piggyback-type 64-pin shrink DIP, is compatible with the M50743-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2764K or the M5L27128K EPROM may be used.

The M50743-PGYS simplifies the development of programs for the M50743-XXXSP and is excellent for making prototypes.

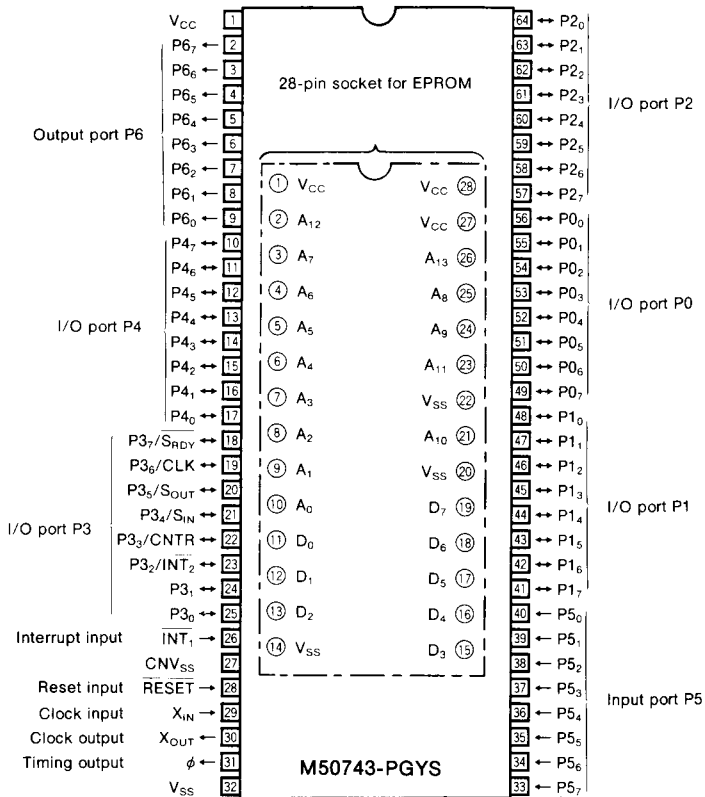
### DISTINCTIVE FEATURES

- Differences with the M50743-XXXSP are:
  - (1) ROMless, EPROM is attached externally
  - (2) Suitable EPROM is the M5L2764K or the M5L27128K.

### APPLICATION

Development of programs for VCR, tuners, and audio equipment.

### PIN CONFIGURATION (TOP VIEW)



The symbol "○" indicates sockets for EPROM.

**PIN DESCRIPTION**

Pin	Name	Input/ Output	Functions
V <sub>CC</sub> V <sub>SS</sub>	Supply voltage		Power supply inputs 5V±5% to V <sub>CC</sub> , and 0V to V <sub>SS</sub> .
CNV <sub>SS</sub>	CNV <sub>SS</sub>		This is usually connected to V <sub>SS</sub> .
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V <sub>CC</sub> conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X <sub>IN</sub>	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X <sub>IN</sub> and X <sub>OUT</sub> pins. If an external clock is used, the clock source should be connected the X <sub>IN</sub> pin and the X <sub>OUT</sub> pin should be left open.
X <sub>OUT</sub>	Clock output	Output	
φ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an output pin for the timer X.
INT <sub>1</sub>	Interrupt input	Input	This is the highest order interrupt input pin.
P0 <sub>0</sub> ~P0 <sub>7</sub>	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
P1 <sub>0</sub> ~P1 <sub>7</sub>	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
P2 <sub>0</sub> ~P2 <sub>7</sub>	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
P3 <sub>0</sub> ~P3 <sub>7</sub>	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, P3 <sub>7</sub> , P3 <sub>6</sub> , P3 <sub>5</sub> , and P3 <sub>4</sub> work as S <sub>RDY</sub> , CLK, S <sub>OUT</sub> , and S <sub>IN</sub> pins, respectively. Also P3 <sub>3</sub> and P3 <sub>2</sub> work as CNTR pin and the lowest order order interrupt input pin (INT <sub>2</sub> ), respectively.
P4 <sub>0</sub> ~P4 <sub>7</sub>	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0.
P5 <sub>0</sub> ~P5 <sub>7</sub>	Input port P5	Input	Port P5 is an 8-bit input port.
P6 <sub>0</sub> ~P6 <sub>7</sub>	Output port P6	Output	Port P6 is an 8-bit output port. The output structure is CMOS output.
A <sub>0</sub> ~A <sub>13</sub>	Output port A	Output	Port A outputs to the address of the EPROM mounted on top of the package.
D <sub>0</sub> ~D <sub>7</sub>	Input port D	Input	Port D inputs from the address of the EPROM mounted on top of the package.

**EXPLANATION OF FUNCTION BLOCK OPERATION**

The differences between the M50743-PGYS and the M50743-XXXSP are explained below. As all other points are the same, only the differences are explained.

**MEMORY**

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is  $E000_{16}$  to  $FFFF_{16}$ , having 8k bytes. Other than this, the M50743-PGYS has the same functions as the M50743-XXXSP has.

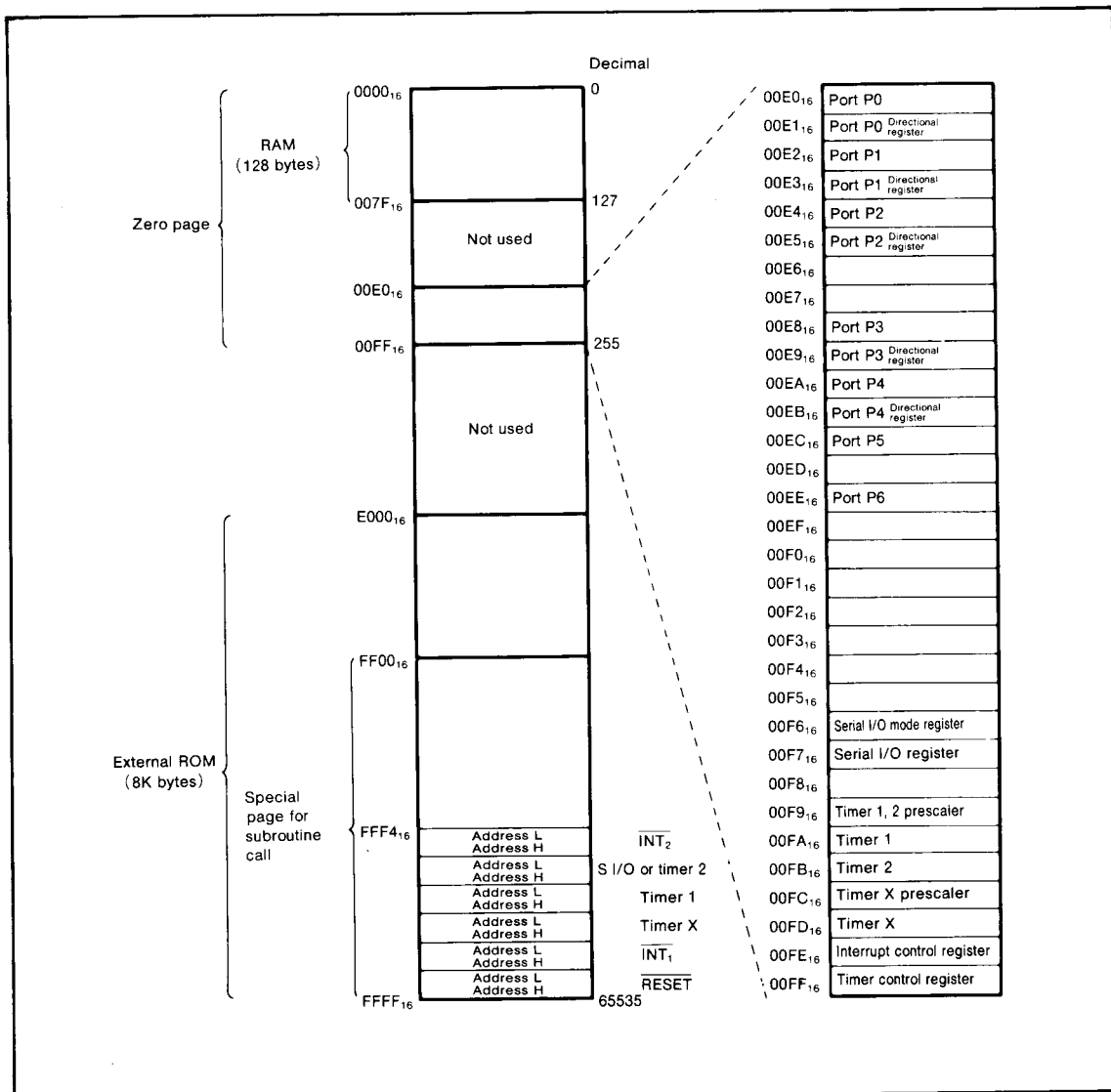


Fig.1 Memory map

**PROCESSOR MODE**

External memory area differs from the M50743-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50743-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50743-XXXSP.

**PRECAUTION FOR USE**

When developing programs with the M50743-PGYS, carefully consider the ROM capacity of the M50743-XXXSP. In the case of the M50743-XXXSP, use the ROM area from F000<sub>16</sub> to FFFF<sub>16</sub>. (In the case of the M5L2764K and the M5L27128K use the areas from 1000<sub>16</sub> to 1FFF<sub>16</sub> and from 3000<sub>16</sub> to 3FFF<sub>16</sub>, respectively.)

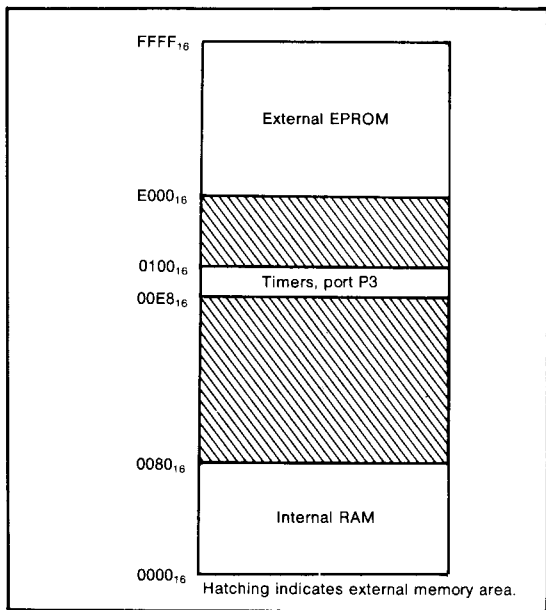


Fig.2 Memory map in memory expanding mode

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.3~7	V
V <sub>i</sub>	Input voltage, RESET, X <sub>IN</sub> , INT <sub>1</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , D <sub>0</sub> ~D <sub>7</sub>		-0.3~7	V
V <sub>i</sub>	Input voltage, P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> P3 <sub>0</sub> ~P3 <sub>7</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub>	With respect to V <sub>SS</sub> With the output transistor isolated.	-0.3~V <sub>CC</sub> +0.3	V
V <sub>i</sub>	Input voltage, CNV <sub>SS</sub>		-0.3~13	V
V <sub>o</sub>	Output voltage, P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>7</sub> P4 <sub>0</sub> ~P4 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , X <sub>OUT</sub> , φ, A <sub>0</sub> ~A <sub>13</sub>		-0.3~V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25°C	1000	mW
T <sub>opr</sub>	Operating temperature		-10~70	°C
T <sub>stg</sub>	Storage temperature		-40~125	°C

**RECOMMENDED OPERATING CONDITIONS** ( $V_{CC}=5V\pm 5\%$ ,  $T_a = -10\sim 70^\circ C$  unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{SS}$	Supply voltage		0		V
$V_{IH}$	"H" input voltage, P <sub>0</sub> ~P <sub>07</sub> , P <sub>10</sub> ~P <sub>17</sub> , P <sub>20</sub> ~P <sub>27</sub> P <sub>30</sub> ~P <sub>37</sub> , P <sub>40</sub> ~P <sub>47</sub> , P <sub>50</sub> ~P <sub>57</sub> INT <sub>1</sub> , RESET, X <sub>IN</sub> , CNV <sub>SS</sub>	0.8V <sub>CC</sub>		V <sub>CC</sub>	V
$V_{IH}$	"H" input voltage, D <sub>0</sub> ~D <sub>7</sub>	0.45V <sub>CC</sub>		V <sub>CC</sub>	V
$V_{IL}$	"L" input voltage, P <sub>0</sub> ~P <sub>07</sub> , P <sub>10</sub> ~P <sub>17</sub> , P <sub>20</sub> ~P <sub>27</sub> P <sub>30</sub> ~P <sub>37</sub> , P <sub>40</sub> ~P <sub>47</sub> , P <sub>50</sub> ~P <sub>57</sub> INT <sub>1</sub> , CNV <sub>SS</sub>	0		0.2V <sub>CC</sub>	V
$V_{IL}$	"L" input voltage, RESET	0		0.12V <sub>CC</sub>	V
$V_{IL}$	"L" input voltage, X <sub>IN</sub>	0		0.16V <sub>CC</sub>	V
$V_{IL}$	"L" input voltage, D <sub>0</sub> ~D <sub>7</sub>	0		0.15V <sub>CC</sub>	V
$I_{OL(peak)}$	"L" peak output current P <sub>0</sub> ~P <sub>07</sub> , P <sub>10</sub> ~P <sub>17</sub> P <sub>20</sub> ~P <sub>27</sub> , P <sub>30</sub> ~P <sub>37</sub> P <sub>40</sub> ~P <sub>47</sub> , P <sub>60</sub> ~P <sub>67</sub>			10	mA
$I_{OL(avg)}$	"L" average output current P <sub>0</sub> ~P <sub>07</sub> , P <sub>10</sub> ~P <sub>17</sub> P <sub>20</sub> ~P <sub>27</sub> , P <sub>30</sub> ~P <sub>37</sub> P <sub>40</sub> ~P <sub>47</sub> , P <sub>60</sub> ~P <sub>67</sub> (Note 1)			5	mA
$I_{OH(peak)}$	"H" peak output current P <sub>0</sub> ~P <sub>07</sub> , P <sub>10</sub> ~P <sub>17</sub> P <sub>20</sub> ~P <sub>27</sub> , P <sub>30</sub> ~P <sub>37</sub> P <sub>40</sub> ~P <sub>47</sub> , P <sub>60</sub> ~P <sub>67</sub>			-10	mA
$I_{OH(avg)}$	"H" average output current P <sub>0</sub> ~P <sub>07</sub> , P <sub>10</sub> ~P <sub>17</sub> P <sub>20</sub> ~P <sub>27</sub> , P <sub>30</sub> ~P <sub>37</sub> P <sub>40</sub> ~P <sub>47</sub> , P <sub>60</sub> ~P <sub>67</sub> (Note 1)			-5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			8	MHz

Note 1 : The average output currents  $I_{OL(avg)}$  and  $I_{OH(avg)}$  are the average value of a period of 100ms.

2 : Do not allow the combined current of the following ports to exceed stated values.

$I_{OL(peak)}$  of P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub>, P<sub>3</sub>, P<sub>4</sub> and P<sub>6</sub> not to exceed 80mA.  $I_{OH(peak)}$  of P<sub>2</sub> not to exceed 50mA.

$I_{OH(peak)}$  of P<sub>0</sub> and P<sub>1</sub> not to exceed 30mA.  $I_{OH(peak)}$  of P<sub>3</sub>, P<sub>4</sub> and P<sub>6</sub> not to exceed 30mA.

**ELECTRICAL CHARACTERISTICS** ( $T_a = 25^\circ C$ ,  $V_{CC} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{(X_{IN})} = 8MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$V_{OH}$	"H" output voltage, P <sub>0</sub> ~P <sub>07</sub> , P <sub>10</sub> ~P <sub>17</sub> , P <sub>20</sub> ~P <sub>27</sub> P <sub>30</sub> ~P <sub>37</sub> , P <sub>40</sub> ~P <sub>47</sub> , P <sub>60</sub> ~P <sub>67</sub>	$I_{OH} = -10mA$	3			V
$V_{OH}$	"H" output voltage, $\phi$ , A <sub>0</sub> ~A <sub>13</sub>	$I_{OH} = -2.5mA$	3			V
$V_{OL}$	"L" output voltage, P <sub>0</sub> ~P <sub>07</sub> , P <sub>10</sub> ~P <sub>17</sub> , P <sub>20</sub> ~P <sub>27</sub> P <sub>30</sub> ~P <sub>37</sub> , P <sub>40</sub> ~P <sub>47</sub> , P <sub>60</sub> ~P <sub>67</sub>	$I_{OL} = 10mA$			2	V
$V_{OL}$	"L" output voltage, $\phi$ , A <sub>0</sub> ~A <sub>13</sub>	$I_{OL} = 5mA$			2	V
$V_{T+} - V_{T-}$	Hysteresis, P <sub>36</sub>	When used as CLK input	0.3		1	V
$V_{T+} - V_{T-}$	Hysteresis, INT <sub>1</sub>		0.3		1	V
$V_{T+} - V_{T-}$	Hysteresis, P <sub>32</sub>	When used as INT <sub>2</sub> input	0.3		1	V
$V_{T+} - V_{T-}$	Hysteresis, P <sub>33</sub>	When used as CNTR input	0.3		1	V
$V_{T+} - V_{T-}$	Hysteresis, RESET			0.5	0.7	V
$V_{T+} - V_{T-}$	Hysteresis, X <sub>IN</sub>		0.1		0.5	V
$I_{IL}$	"L" input current P <sub>0</sub> ~P <sub>07</sub> , P <sub>10</sub> ~P <sub>17</sub> , P <sub>20</sub> ~P <sub>27</sub> P <sub>30</sub> ~P <sub>37</sub> , P <sub>40</sub> ~P <sub>47</sub> , P <sub>50</sub> ~P <sub>57</sub> P <sub>60</sub> ~P <sub>67</sub> , INT <sub>1</sub> , RESET, X <sub>IN</sub> D <sub>0</sub> ~D <sub>7</sub>	$V_I = 0V$			-5	$\mu A$
$I_{IH}$	"H" input current P <sub>0</sub> ~P <sub>07</sub> , P <sub>10</sub> ~P <sub>17</sub> , P <sub>20</sub> ~P <sub>27</sub> P <sub>30</sub> ~P <sub>37</sub> , P <sub>40</sub> ~P <sub>47</sub> , P <sub>50</sub> ~P <sub>57</sub> P <sub>60</sub> ~P <sub>67</sub> , INT <sub>1</sub> , RESET, X <sub>IN</sub> D <sub>0</sub> ~D <sub>7</sub>	$V_I = 5V$			5	$\mu A$
$I_{CC}$	Supply current	Output pins opened, input and input/output pins at $V_{SS}$ and a square wave input at X <sub>IN</sub> .		6	12	mA