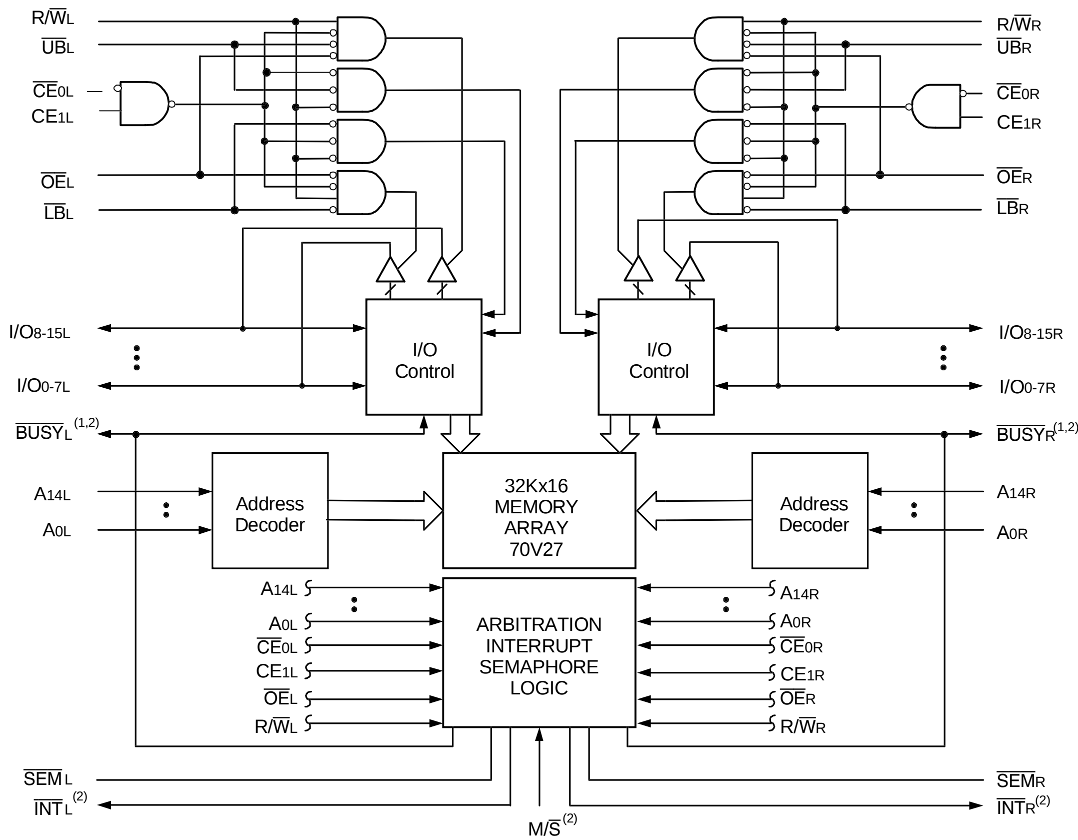
HIGH-SPEED 3.3V 32K x 16 DUAL-PORT STATIC RAM

IDT70V27S/L

Features:

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed access
  - *Industrial: 35ns (max.)*
  - *Commercial: 15/20/25/35/55ns (max.)*
- Low-power operation
  - *IDT70V27S*
    Active: 500mW (typ.)
    Standby: 3.3mW (typ.)
  - *IDT70V27L*
    Active: 500mW (typ.)
    Standby: 660µW (typ.)
- Separate upper-byte and lower-byte control for bus matching capability
- Dual chip enables allow for depth expansion without external logic
- IDT70V27 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/S = V_{IH} for BUSY output flag on Master,
  M/S = V_{IL} for BUSY input on Slave
- Busy and Interrupt Flags
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- LVTTL-compatible, single 3.3V (±0.3V) power supply
- Available in 100-pin Thin Quad Flatpack (TQFP), 108-pin Ceramic Pin Grid Array (PGA), and 144-pin Fine Pitch BGA (fpBGA)
- Industrial temperature range (-40°C to +85°C) is available for selected speeds

Functional Block Diagram



3603 drw 01

NOTES:
1) BUSY is an input as a Slave (M/S=V_{IL}) and an output as a Master (M/S=V_{IH}).
2) BUSY and INT are non-tri-state totem-pole outputs (push-pull).

JANUARY 2001

DSC 3603/7

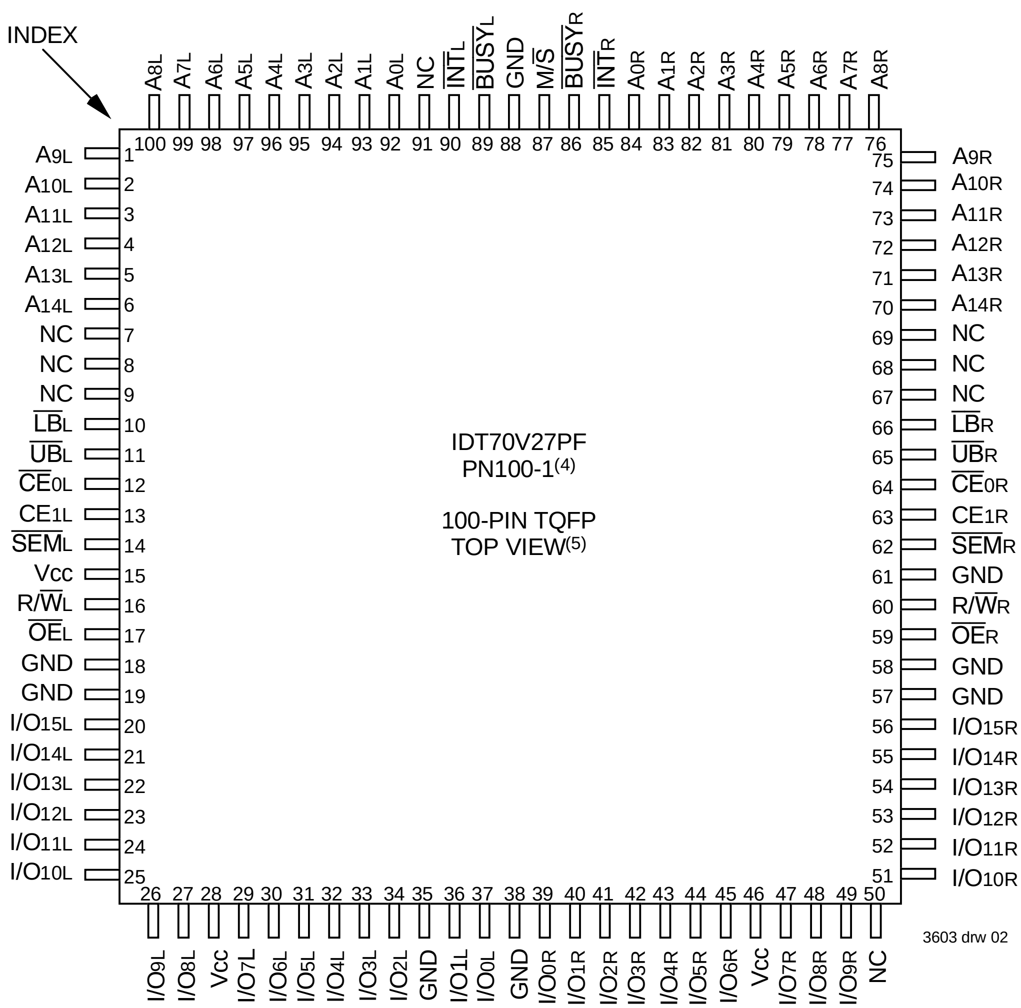
Description:

The IDT70V27 is a high-speed 32K x 16 Dual-Port Static RAM, designed to be used as a stand-alone 512K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit and wider word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

The device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by the chip enables ($\overline{CE}_0$ and CE_1) permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 500mW of power. The IDT70V27 is packaged in a 100-pin Thin Quad Flatpack (TQFP), a 108-pin ceramic Pin Grid Array (PGA), and a 144-pin Fine Pitch BGA (fp BGA).

Pin Configurations(1,2,3)



NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations[1,2,3] (con't.)

A1 NC	A2 NC	A3 A_{8L}	A4 A_{5L}	A5 A_{1L}	A6 $\overline{INT}_L$	A7 GND	A8 $\overline{BUSY}_R$	A9 A_{1R}	A10 A_{5R}	A11 NC	A12 NC	A13 NC
B1 NC	B2 NC	B3 NC	B4 A_{6L}	B5 A_{2L}	B6 NC	B7 $M/\overline{S}$	B8 $\overline{INT}_R$	B9 A_{2R}	B10 A_{6R}	B11 NC	B12 NC	B13 NC
C1 A_{10L}	C2 A_{9L}	C3 NC	C4 A_{7L}	C5 A_{3L}	C6 NC	C7 NC	C8 NC	C9 A_{3R}	C10 A_{7R}	C11 A_{9R}	C12 A_{10R}	C13 A_{11R}
D1 A_{14L}	D2 A_{13L}	D3 A_{12L}	D4 A_{11L}	D5 A_{4L}	D6 A_{0L}	D7 $\overline{BUSY}_L$	D8 A_{0R}	D9 A_{4R}	D10 A_{8R}	D11 A_{12R}	D12 A_{13R}	D13 A_{14R}
E1 $\overline{LB}_L$	E2 NC	E3 NC	E4 NC						E10 NC	E11 NC	E12 NC	E13 $\overline{LB}_R$
F1 $\overline{SEM}_L$	F2 CE_{1L}	F3 $\overline{CE}_{0L}$	F4 $\overline{UB}_L$			IDT70V27BF BF144-1[4]			F10 $\overline{UB}_R$	F11 $\overline{CE}_{0R}$	F12 CE_{1R}	F13 $\overline{SEM}_R$
G1 V_{CC}	G2 V_{CC}	G3 V_{CC}	G4 NC			144-Pin fpBGA Top View[5]			G10 NC	G11 NC	G12 GND	G13 GND
H1 NC	H2 $R/\overline{W}_L$	H3 $\overline{OE}_L$	H4 NC						H10 NC	H11 $\overline{OE}_R$	H12 $R/\overline{W}_R$	H13 GND
J1 GND	J2 I/O_{15L}	J3 I/O_{14L}	J4 I/O_{13L}						J10 I/O_{13R}	J11 I/O_{14R}	J12 I/O_{15R}	J13 GND
K1 I/O_{12L}	K2 NC	K3 NC	K4 NC	K5 I/O_{6L}	K6 I/O_{3L}	K7 I/O_{0R}	K8 I/O_{3R}	K9 I/O_{6R}	K10 I/O_{11R}	K11 NC	K12 NC	K13 I/O_{12R}
L1 I/O_{11L}	L2 I/O_{10L}	L3 NC	L4 NC	L5 I/O_{5L}	L6 I/O_{2L}	L7 GND	L8 V_{CC}	L9 I/O_{5R}	L10 NC	L11 NC	L12 NC	L13 I/O_{10R}
M1 I/O_{9L}	M2 NC	M3 NC	M4 V_{CC}	M5 I/O_{4L}	M6 GND	M7 I/O_{0L}	M8 I/O_{2R}	M9 I/O_{4R}	M10 I/O_{7R}	M11 I/O_{8R}	M12 NC	M13 I/O_{9R}
N1 NC	N2 NC	N3 I/O_{8L}	N4 I/O_{7L}	N5 NC	N6 I/O_{1L}	N7 V_{CC}	N8 I/O_{1R}	N9 NC	N10 V_{CC}	N11 NC	N12 NC	N13 NC

3603 drw 02a

NOTES:
1. All V_{CC} pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 12mm x 12mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations(1,2,3) (con't.)

	A	B	C	D	E	F	G	H	J	K	L	M
12	81 A10R	80 A11R	77 A14R	74 NC	72 UBR	69 SEMR	68 GND	65 GND	63 NC	60 I/O13R	57 I/O10R	54 NC
11	84 A7R	83 A8R	78 A13R	76 NC	73 LBR	70 CE1R	67 R/WR	64 GND	61 I/O14R	59 I/O12R	56 I/O9R	53 NC
10	87 A4R	86 A5R	82 A9R	79 A12R	75 NC	71 CE0R	66 OER	62 I/O15R	58 I/O11R	55 NC	51 I/O8R	50 I/O7R
09	90 A1R	88 A3R	85 A6R							52 NC	49 Vcc	47 I/O5R
08	92 INTR	91 A0R	89 A2R							48 I/O6R	46 I/O4R	45 I/O3R
07	95 GND	94 M/S	93 BUSYR				IDT70V27G G108-1(4)			44 I/O2R	43 I/O1R	42 I/O0R
06	96 BUSYL	97 INTL	98 NC				108-PIN PGA TOP VIEW(5)			39 I/O1L	40 I/O0L	41 GND
05	99 A0L	100 A1L	102 A3L							35 I/O4L	37 I/O2L	38 GND
04	101 A2L	103 A4L	106 A7L							31 Vcc	34 I/O5L	36 I/O3L
03	104 A5L	105 A6L	1 A10L	4 A13L	8 NC	12 CE1L	17 GND	21 I/O14L	25 I/O10L	28 NC	32 I/O7L	33 I/O6L
02	107 A8L	2 A11L	5 A14L	7 NC	10 UBL	13 SEML	16 OEL	19 GND	22 I/O13L	24 I/O11L	29 NC	30 I/O8L
01	108 A9L	3 A12L	6 NC	9 LBL	11 CE0L	14 Vcc	15 R/WL	18 NC	20 I/O15L	23 I/O12L	26 I/O9L	27 NC

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3603 drw 0

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 1.21in x 1.21in x .16in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
CE0L, CE1L	CE0R, CE1R	Chip Enable
R/WL	R/WR	Read/Write Enable
OEL	OER	Output Enable
A0L - A14L	A0R - A14R	Address
I/O0L - I/O15L	I/O0R - I/O15R	Data Input/Output
SEML	SEMR	Semaphore Enable
UBL	UBR	Upper Byte Select
LBL	LBR	Lower Byte Select
INTL	INTR	Interrupt Flag
BUSYL	BUSYR	Busy Flag
M/S		Master or Slave Select
Vcc		Power
GND		Ground

3603 tbl 01

Truth Table I – Chip Enable(1,2,3)

$\overline{CE}$	$\overline{CE}_0$	CE_1	Mode
L	V_{IL}	V_{IH}	Port Selected (TTL Active)
	$\leq$ 0.2V	$\geq V_{CC}$ -0.2V	Port Selected (CMOS Active)
H	V_{IH}	X	Port Deselected (TTL Inactive)
	X	V_{IL}	Port Deselected (TTL Inactive)
	$\geq V_{CC}$ -0.2V	X	Port Deselected (CMOS Inactive)
	X	$\leq$0.2V	Port Deselected (CMOS Inactive)

3603 tbl 02

NOTES:
1. Chip Enable references are shown above with the actual $\overline{CE}_0$ and CE_1 levels, $\overline{CE}$ is a reference only.
2. Port "A" and "B" references are located where $\overline{CE}$ is used.
3. "H" = V_{IH} and "L" = V_{IL}

Truth Table II – Non-Contention Read/Write Control

Inputs(1)						Outputs		Mode
$\overline{CE}$(2)	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_{8-15}	I/O_{0-7}	
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	$DATA_{IN}$	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	H	L	L	H	H	$DATA_{OUT}$	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

3603 tbl 03

NOTES:
1. A_{0L} — $A_{14L} \neq A_{0R}$ — A_{14R}.
2. Refer to Chip Enable Truth Table.

Truth Table III – Semaphore Read/Write Control

Inputs(1)						Outputs		Mode
$\overline{CE}$(2)	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_{8-15}	I/O_{0-7}	
H	H	L	X	X	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag
X	H	L	H	H	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag
H	↑	X	X	X	L	$DATA_{IN}$	$DATA_{IN}$	Write I/O_0 into Semaphore Flag
X	↑	X	H	H	L	$DATA_{IN}$	$DATA_{IN}$	Write I/O_0 into Semaphore Flag
L	X	X	L	X	L	——	——	Not Allowed
L	X	X	X	L	L	——	——	Not Allowed

3603 tbl 04

NOTES:
1. There are eight semaphore flags written to I/O_0 and read from all the I/Os (I/O_0-I/O_{15}). These eight semaphore flags are addressed by A_0-A_2.
2. Refer to Chip Enable Truth Table.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

3603 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 0.3V.

Capacitance(1)
(T_A = +25°C, f = 1.0mhz)TQFP ONLY

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

3603 tbl 08

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage(1,2)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

3603 tbl 06

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Recommended DC Operating Conditions(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{CC}+0.3V(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

3603 tbl 07

NOTES:
1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.3V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	70V27S		70V27L		Unit
			Min.	Max.	Min.	Max.	
$\lvert I_{LI}\rvert$	Input Leakage Current(1)	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

3603 tbl 09

NOTE:
1. At Vcc ≤ 2.0V, input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,6,7] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V27X15 Com'l Only		70V27X20 Com'l Only		70V27X25 Com'l Only		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L	S L	170 170	260 225	165 165	255 220	145 145	245 210	mA
			IND'L	S L	— —	— —	— —	— —	145 145	280 245	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L	S L	44 44	70 60	39 39	60 50	27 27	50 40	mA
			IND'L	S L	— —	— —	— —	— —	27 27	60 50	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S L	115 115	160 145	105 105	155 140	90 90	150 135	mA
			IND'L	S L	— —	— —	— —	— —	90 90	170 150	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ $\geq$ V_{CC} - 0.2V V_{IN} $\geq$ V_{CC} - 0.2V or V_{IN} $\leq$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ $\geq$ V_{CC} - 0.2V	COM'L	S L	1.0 0.2	6 3	1.0 0.2	6 3	1.0 0.2	6 3	mA
			IND'L	S L	— —	— —	— —	— —	1.0 0.2	10 6	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"}$ $\leq$ 0.2V and $\overline{CE}_{"B"}$ $\geq$ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ $\geq$ V_{CC} - 0.2V V_{IN} $\geq$ V_{CC} - 0.2V or V_{IN} $\leq$ 0.2V Active Port Outputs Disabled f = f_{MAX}[3]	COM'L	S L	115 115	155 140	105 105	150 135	90 90	145 130	mA
			IND'L	S L	— —	— —	— —	— —	90 90	170 145	

3603 tbl 10a

NOTES:
1. 'X' in part numbers indicates power rating (S or L).
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. I_{CCDC} = 90mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
6. Refer to Chip Enable Truth Table.
7. Industrial temperature: for other speeds, packages and powers contact your sales office.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1,6,7) (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V27X35 Com'l & Ind Typ.(2)	70V27X35 Com'l & Ind Max.	70V27X55 Com'l Only Typ.(2)	70V27X55 Com'l Only Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled $\overline{SEM}$ = V_{IH} f = f_{MAX}(3)	COM'L	S L	135 135	235 190	125 125	225 180	mA
			IND'L	S L	135 135	270 235	125 125	260 225	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}(3)	COM'L	S L	22 22	45 35	15 15	40 30	mA
			IND'L	S L	22 22	55 45	15 15	50 40	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}(5) Active Port Outputs Disabled, f=f_{MAX}(3) $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S L	85 85	140 125	75 75	140 125	mA
			IND'L	S L	85 85	160 140	75 75	160 140	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0(4) $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	COM'L	S L	1.0 0.2	6 3	1.0 0.2	6 3	mA
			IND'L	S L	1.0 0.2	10 6	1.0 0.2	10 6	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V(5) $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Disabled f = f_{MAX}(3)	COM'L	S L	85 85	135 120	75 75	135 120	mA
			IND'L	S L	85 85	160 135	75 75	160 135	

3603 tbl 10b

NOTES:
1. 'X' in part numbers indicates power rating (S or L).
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. I_{CCDC} = 90mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
6. Refer to Chip Enable Truth Table.
7. Industrial temperature: for other speeds, packages and powers contact your sales office.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

3603 tbl 11

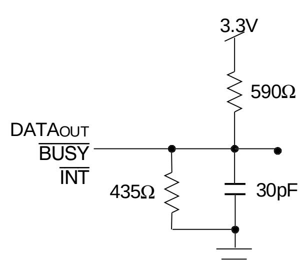
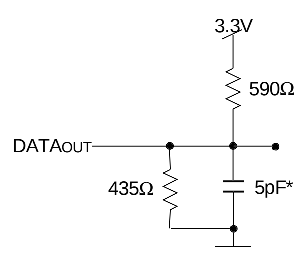


Figure 1. AC Output Test Load



3603 drw 04

Figure 2. Output Test Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(4, 6)

Symbol	Parameter	70V27X15 Com'l Only		70V27X20 Com'l Only		70V27X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACE}	Chip Enable Access Time(3)	—	15	—	20	—	25	ns
t_{ABE}	Byte Enable Access Time(3)	—	15	—	20	—	25	ns
t_{AOE}	Output Enable Access Time	—	10	—	12	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,2)	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	12	—	12	—	15	ns
t_{PU}	Chip Enable to Power Up Time(2,5)	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2,5)	—	15	—	20	—	25	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	15	—	ns
t_{SAA}	Semaphore Address Access Time	—	15	—	20	—	35	ns

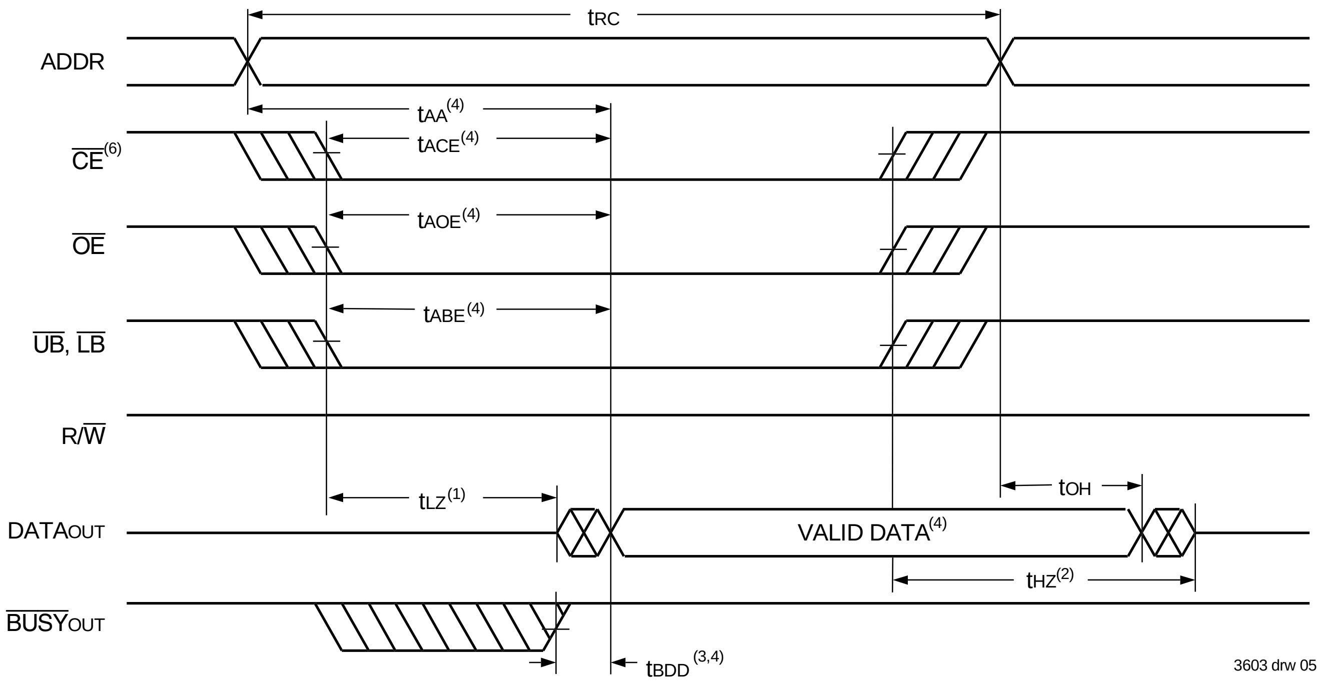
3603 tbl 12a

Symbol	Parameter	70V27X35 Com'l & Ind		70V27X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	35	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time(3)	—	35	—	55	ns
t_{ABE}	Byte Enable Access Time(3)	—	35	—	55	ns
t_{AOE}	Output Enable Access Time	—	20	—	30	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,2)	3	—	3	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	20	—	25	ns
t_{PU}	Chip Enable to Power Up Time(2,5)	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2,5)	—	45	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	ns
t_{SAA}	Semaphore Address Access Time	—	45	—	65	ns

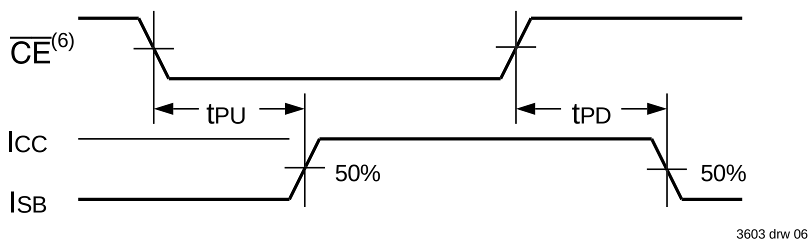
3603 tbl 12b

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$= V_{IH} and $\overline{SEM}$ = V_{IL}.
4. 'X' in part numbers indicates power rating (S or L).
5. Refer to Chip Enable Truth Table.
6. Industrial temperature: for other speeds, packages and powers contact your sales office.

Waveform of Read Cycles(5)



Timing of Power-Up Power-Down



NOTES:

1. Timing depends on which signal is asserted last: CE, OE, LB, or UB.
2. Timing depends on which signal is de-asserted first: CE, OE, LB, or UB.
3. t_{BDD} delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{AOE}, t_{ACE}, t_{AA} or t_{BDD}.
5. SEM = V_{IH}.
6. Refer to Chip Enable Truth Table.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage(5,6)

Symbol	Parameter	70V27X15 Com'l Only		70V27X20 Com'l Only		70V27X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	20	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	15	—	15	—	ns
t_{HZ}	Output High-Z Time (1,2)	—	10	—	10	—	15	ns
t_{DH}	Data Hold Time (4)	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z (1,2)	—	10	—	10	—	15	ns
t_{OW}	Output Active from End-of-Write (1,2,4)	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

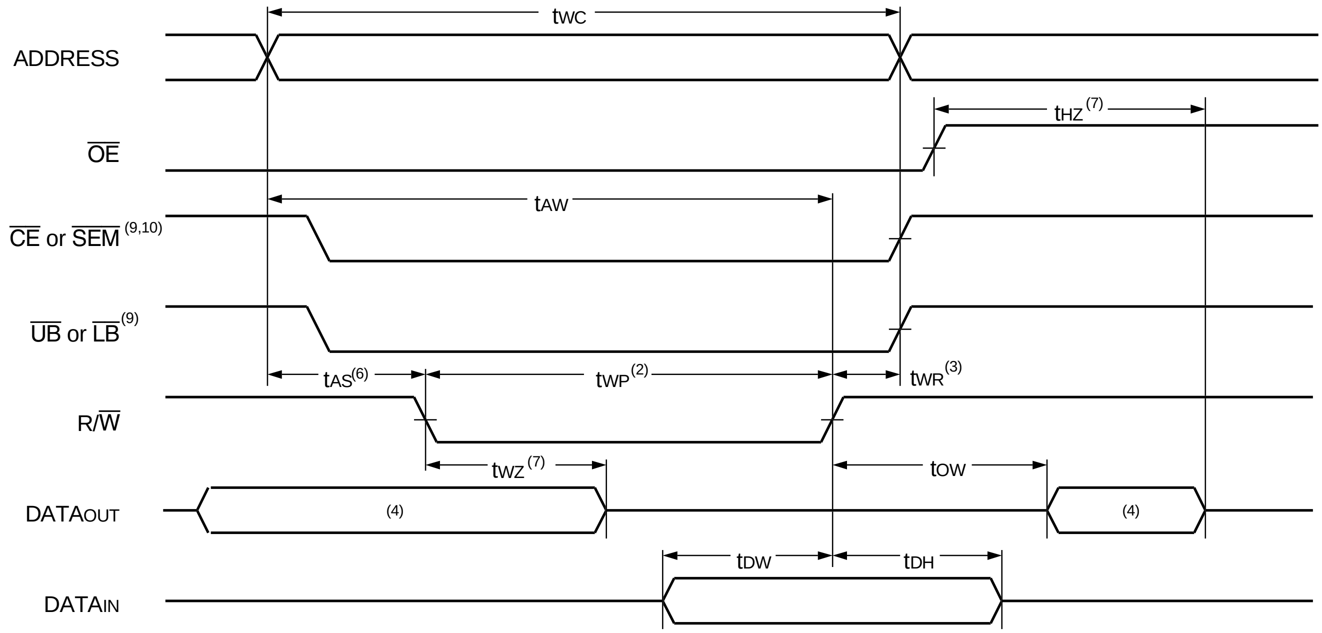
3603 tbl 13a

Symbol	Parameter	70V27X35 Com'l & Ind		70V27X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	30	—	45	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	45	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	20	—	30	—	ns
t_{HZ}	Output High-Z Time (1,2)	—	20	—	25	ns
t_{DH}	Data Hold Time (4)	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z (1,2)	—	20	—	25	ns
t_{OW}	Output Active from End-of-Write (1,2,4)	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

3603 tbl 13b

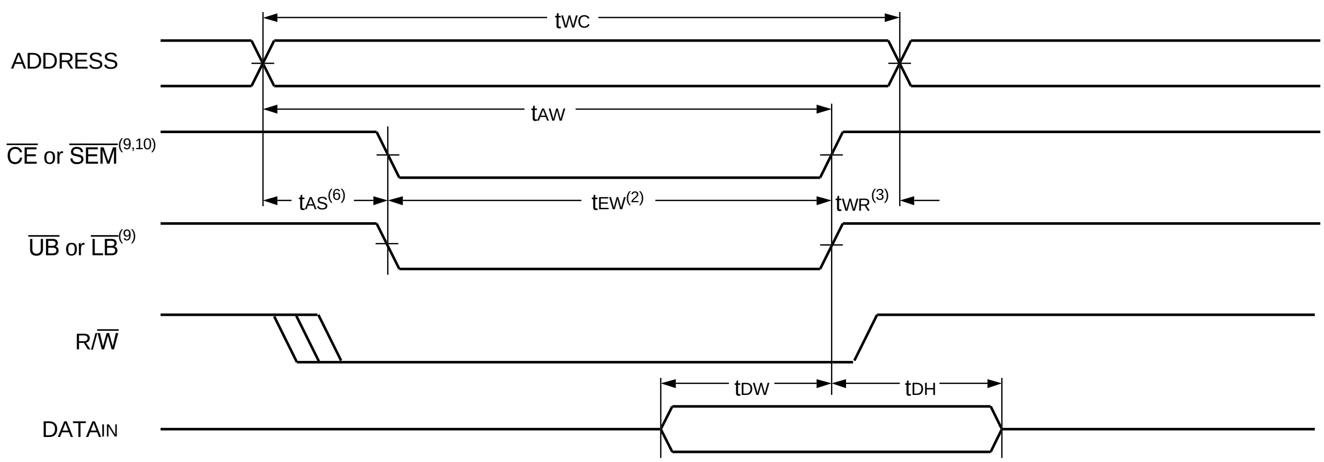
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM $\overline{CE}$= V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time. Refer to Chip Enable Truth Table.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. 'X' in part numbers indicates power rating (S or L).
6. Industrial temperature: for other speeds, packages and powers contact your sales office.

Timing Waveform of Write Cycle No. 1, R/W Controlled Timing(1,5,8)



3603 drw 07

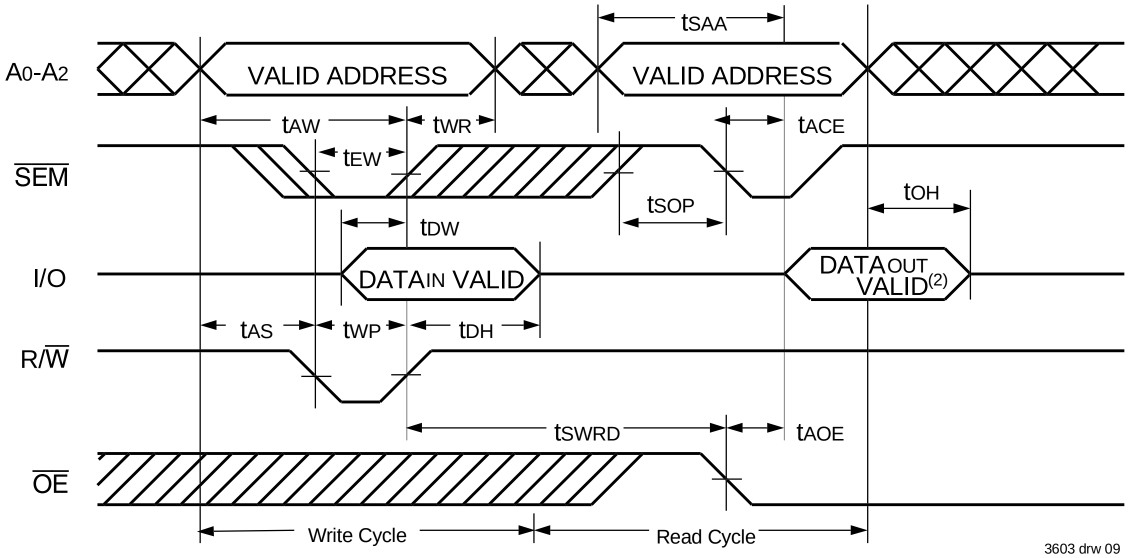
Timing Waveform of Write Cycle No. 2, CE, UB, LB Controlled Timing(1,5)



3603 drw 08

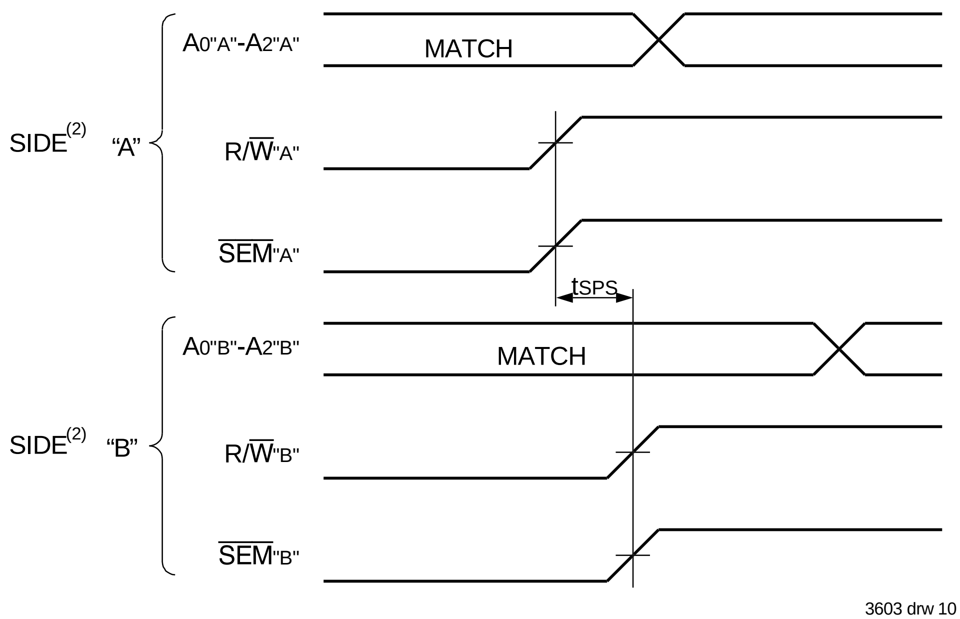
NOTES:
1. R/W or CE or UB and LB must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a LOW CE and a LOW R/W for memory array writing cycle.
3. t_{WR} is measured from the earlier of CE or R/W (or SEM or R/W) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the CE or SEM LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, CE or R/W.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If OE is LOW during R/W controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If OE is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. To access RAM, CE = V_{IL} and SEM = V_{IH}. To access semaphore, CE = V_{IH} and SEM = V_{IL}. t_{EW} must be met for either condition.
10. Refer to Chip Enable Truth Table.

Timing Waveform of Semaphore Read after Write Timing, Either Side(1)



NOTES:
1. CE = V_{IH} or UB and LB = V_{IH} for the duration of the above timing (both write and read cycle), refer to Chip Enable Truth Table.
2. "DATAOUT VALID" represents all I/O's (I/O_0-I/O_{15}) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention(1,3,4)



NOTES:
1. D_{OR} = D_{OL} = V_{IL}, CE_R = CE_L = V_{IH}, or both UB & LB = V_{IH} (refer to Chip Enable Truth Table).
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/W"A" or SEM"A" going HIGH to R/W"B" or SEM"B" going HIGH.
4. If t_{SPS} is not satisfied, there is no guarantee which side will be granted the semaphore flag.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(6,7)

Symbol	Parameter	70V27X15 Com'l Only		70V27X20 Com'l Only		70V27X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$=VIH)								
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	15	—	20	—	25	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	15	—	20	—	25	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable Low	—	15	—	20	—	25	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable High	—	15	—	20	—	25	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	17	—	35	—	35	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	20	—	ns
BUSY TIMING (M/$\overline{S}$=VIL)								
t_{WB}	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	20	—	ns
PORT-TO-PORT DELAY TIMING								
t_{WDD}	Write Pulse to Data Delay(1)	—	30	—	45	—	55	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	25	—	30	—	50	ns

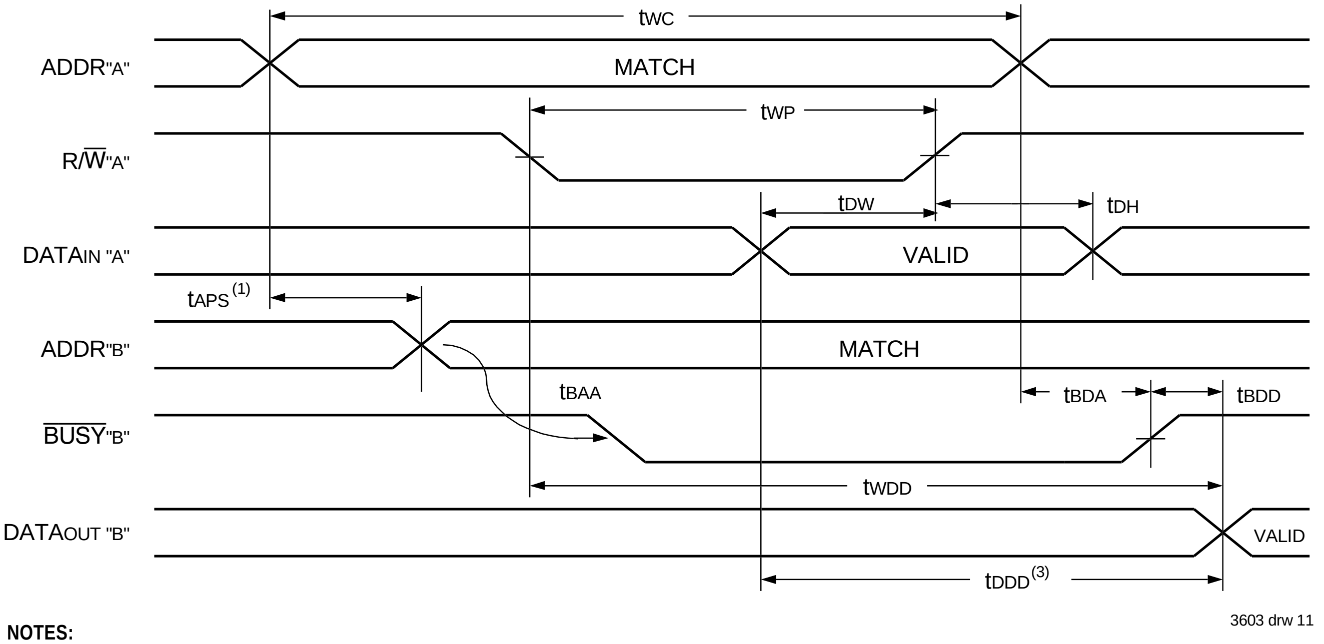
3603 tbl 14a

Symbol	Parameter	70V27X35 Com'l & Ind		70V27X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$=VIH)						
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	35	—	45	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	35	—	45	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable Low	—	35	—	45	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable High	—	35	—	45	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	40	—	50	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	25	—	25	—	ns
BUSY TIMING (M/$\overline{S}$=VIL)						
t_{WB}	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING						
t_{WDD}	Write Pulse to Data Delay(1)	—	65	—	85	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	60	—	80	ns

3603 tbl 14b

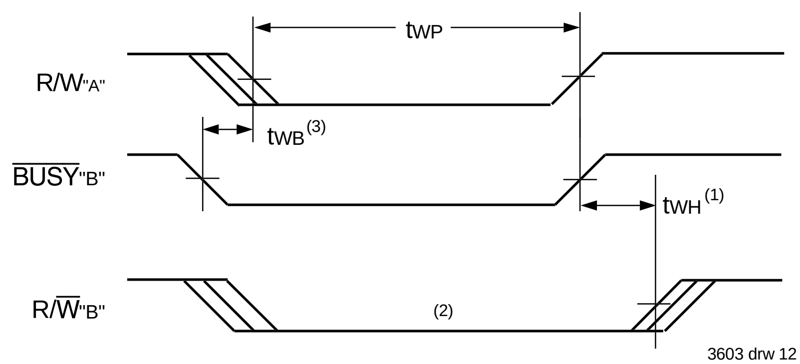
NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual), or $t_{DDD} - t_{DW}$ (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. 'X' in part numbers indicates power rating (S or L).
7. Industrial temperature: for other speeds, packages and powers contact your sales office.

Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$(2,5) (M/$\overline{S}$ = VIH)(4)



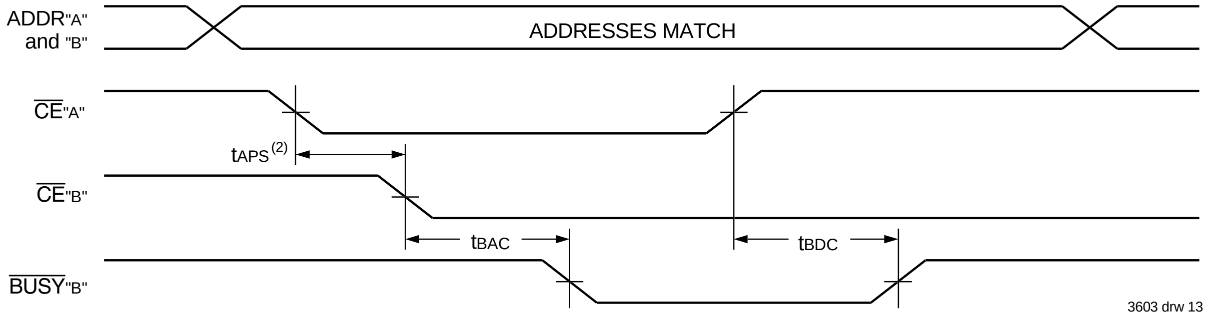
NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}$L = $\overline{CE}$R = VIL (refer to Chip Enable Truth Table).
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$ = VIL (SLAVE), then $\overline{BUSY}$ is an input. Then for this example $\overline{BUSY}$ "A"= VIH and $\overline{BUSY}$ "B"= input is shown above.
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

Timing Waveform Write with $\overline{BUSY}$ (M/$\overline{S}$ = VIL)

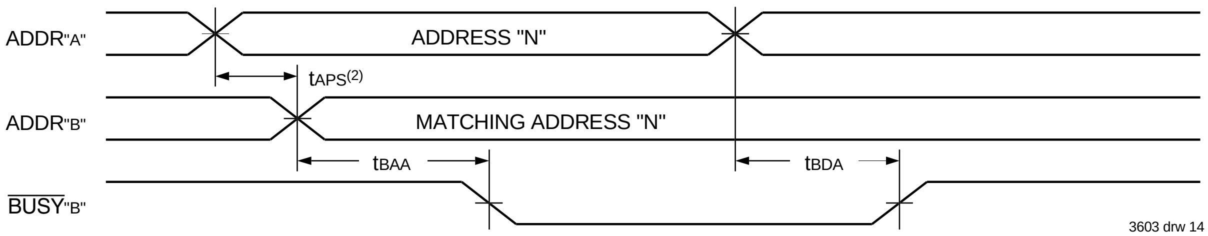


NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes HIGH.
3. tWB is only for the "Slave" version.

Waveform of $\overline{BUSY}$ Arbitration Controlled by $\overline{CE}$ Timing (M/$\overline{S}$ = VIH)(1,3)



Waveform of $\overline{BUSY}$ Arbitration Cycle Controlled by Address Match Timing (M/$\overline{S}$ = VIH)(1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.
3. Refer to Chip Enable Truth Table.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1,2)

Symbol	Parameter	70V27X15 Com'l Only		70V27X20 Com'l Only		70V27X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	20	—	25	ns
tINR	Interrupt Reset Time	—	25	—	20	—	35	ns

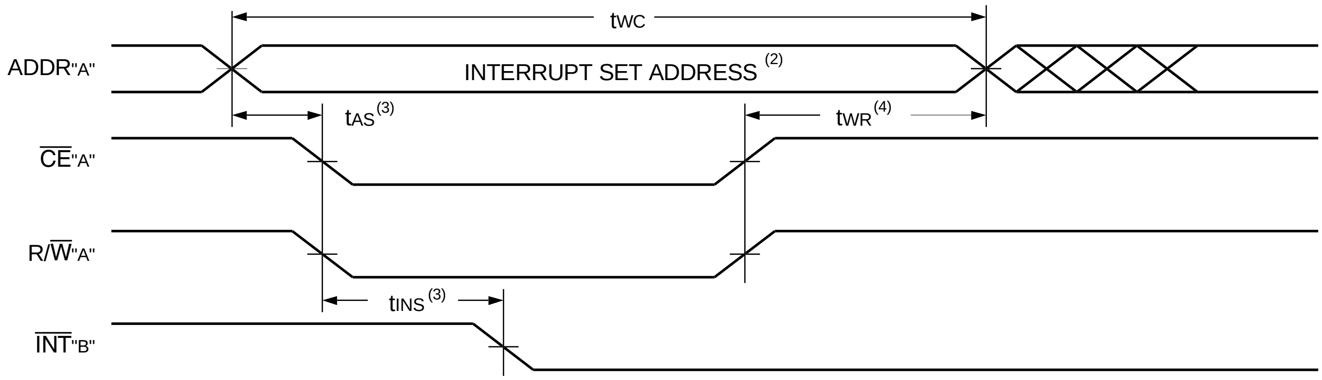
3603 tbl 15a

Symbol	Parameter	70V27X35 Com'l &Ind		70V27X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	30	—	40	ns
tINR	Interrupt Reset Time	—	35	—	45	ns

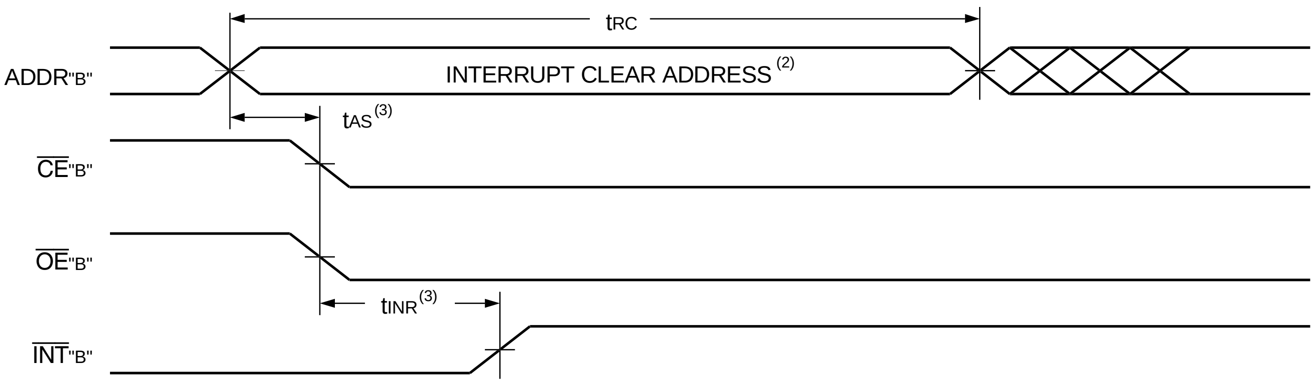
3603 tbl 15b

NOTES:
1. 'X' in part numbers indicates power rating (S or L).
2. Industrial temperature: for other speeds, packages and powers contact your sales office.

Waveform of Interrupt Timing(1,5)



3603 drw 15



3603 drw 16

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. See Interrupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.
5. Refer to Chip Enable Truth Table.

Truth Table IV — Interrupt Flag(1,4)

Left Port					Right Port					Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{14L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{14R}-A_{0R}	$\overline{INT}_R$	
L	L	X	7FFF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FFF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FFE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

3603 tbl 16

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = V_{IH}.
2. If $\overline{BUSY}_L$ = V_{IL}, then no change.
3. If $\overline{BUSY}_R$ = V_{IL}, then no change.
4. Refer to Chip Enable Truth Table.

Truth Table V — Address BUSY Arbitration[4]

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{14L} A_{0R}-A_{14R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

3603 tbl 17

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT70V27 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.
4. Refer to Chip Enable Truth Table.

Truth Table VI — Example of Semaphore Procurement Sequence[1,2]

Functions	D0 - D15 Left	D0 - D15 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

3603 tbl 18

NOTES:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V27.
2. There are eight semaphore flags written to via I/O_0 and read from all the I/O's (I/O_0-I/O_{15}). These eight semaphores are addressed by A_0 - A_2.

Functional Description

The IDT70V27 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V27 has an automatic power down feature controlled by $\overline{CE}_0$ and CE_1. The $\overline{CE}_0$ and CE_1 control the on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FFE (HEX), where a write is defined as $\overline{CE}_R = R/\overline{W}_R = V_{IL}$ per the Truth Table IV. The left port clears the interrupt through access of address location 7FFE when $\overline{CE}_L = \overline{OE}_L = V_{IL}$, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FFF. The message (16 bits) at 7FFE or 7FFF is user-defined since it is an addressable SRAM location. If the interrupt func-tion is not used, address locations 7FFE and 7FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table IV for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a BUSY indication, the write signal is gated internally to prevent the write from proceeding.

The use of BUSY logic is not required or desirable for all applications. In some cases it may be useful to logically OR the BUSY outputs together and use any BUSY indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of BUSY logic is not desirable, the BUSY logic can be disabled by placing the part in slave mode with the M/S pin. Once in slave mode the BUSY pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the BUSY pins HIGH. If desired, unintended write operations can be prevented to a port by tying the BUSY pin for that port LOW.

The BUSY outputs on the IDT 70V27 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the BUSY indication for the resulting array requires the use of an external AND gate.

Width Expansion with BUSY Logic Master/Slave Arrays

When expanding an IDT70V27 RAM array in width while using BUSY logic, one master part is used to decide which side of the RAM array will receive a BUSY indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT70V27 RAM the BUSY pin is an output if the part is used as a master (M/S pin = V_{IH}), and the BUSY pin is an input if the part is used as a slave (M/S pin = V_{IL}) as shown in Figure 3.

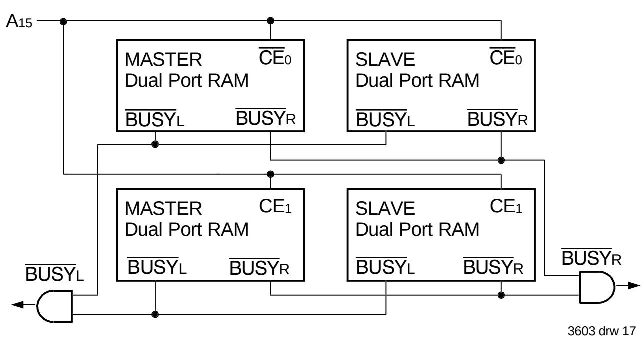


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V27 RAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating BUSY on one side of the array and another master indicating BUSY on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The BUSY arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a BUSY flag to be output from the master before the actual write pulse can be initiated with either the R/W signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Semaphores

The IDT70V27 is a fast Dual-Port 32K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by CE the Dual-Port RAM enable, and SEM, the semaphore enable. The CE and SEM pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table II where CE and SEM are both HIGH.

Systems which can best use the IDT70V27 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V27's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V27 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V27 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0 – A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table VI). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table VI). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during the subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed

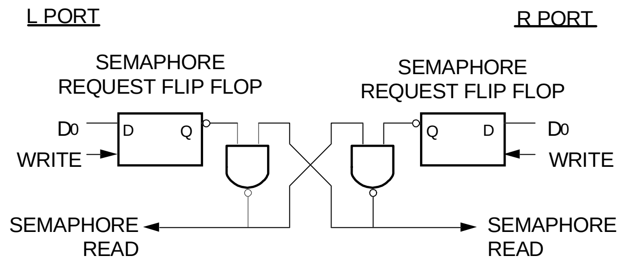


Figure 4. IDT70V27 Semaphore Logic

into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Ordering Information

IDT XXXXX A 999 A A

Device Type — Power — Speed — Package — Process/Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
I(1)	Industrial (-40°C to +85°C)

Package

BF	144-pin fpBGA (BF144-1)
PF	100-pin TQFP (PN100-1)
G	108-pin PGA (G108-1)

Speed (Speed in nanoseconds)

15	Commercial
20	Commercial
25	Commercial
35	Commercial & Industrial
55	Commercial

Power

S	Standard Power
L	Low Power

Device Type

70V27	512K (32K x 16) 3.3V Dual-Port RAM

3603 drw 19

NOTE:
1. Industrial temperature range is available on selected TQFP packages in low power.
For other speeds, packages and powers contact your sales office.

Preliminary Datasheet:

"PRELIMINARY' datasheets contain descriptions for products that are in early release.

Datasheet Document History

12/3/98:	Initiated Document History	
	Converted to new format	
	Typographical and cosmetic changes	
	Added fpBGA information	
	Added 15ns and 20ns speed grades	
	Updated DC Electrical Characteristics	
	Added additional notes to pin configurations	
4/2/99:	Page 5	Fixed typo in Table III
8/1/99:	Page 3	Changed package body height from 1.1mm to 1.4mm
8/30/99:	Page 1	Changed 660mW to 660µW
4/25/00:	Replaced IDT logo	
	Page 2 Made pin correction	
	Changed ±200mV to 0mV in notes	
1/12/01:	Page 1	Fixed page numbering; copywright
	Page 6	Increated storage temperature parameter
		Clarified T_A Parameter
	Page 7 and8 DC Electrical parameters–changed wording from "open" to "disabled"	
	Removed Preliminary status	

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