

## Features

- Six High-side and Six Low-side Drivers
- Outputs Freely Configurable as Switch, Half Bridge or H-bridge
- Capable to Switch All Kinds of Loads Such as DC Motors, Bulbs, Resistors, Capacitors and Inductors
- 0.6A Continuous Current Per Switch
- Low-side:  $R_{DSon} < 1.5\Omega$  Versus Total Temperature Range
- High-side:  $R_{DSon} < 2.0\Omega$  Versus Total Temperature Range
- Very Low Quiescent Current  $I_S < 20 \mu A$  in Standby Mode
- Outputs Short-circuit Protected
- Overtemperature Prewarning and Protection
- Under- and Overvoltage Protection
- Various Diagnosis Functions Such as Shorted Output, Open Load, Overtemperature and Power Supply Fail
- Serial Data Interface
- Daisy Chaining Possible
- SO28 Power Package



## 1. Description

The U6815BM is a fully protected driver interface designed in 0.8- $\mu m$  BCDMOS technology. It is used to control up to 12 different loads by a microcontroller in automotive and industrial applications.

Each of the 6 high-side and 6 low-side drivers is capable to drive currents up to 600 mA. The drivers are freely configurable and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors and inductors can be combined. The IC design especially supports the applications of H-bridges to drive DC motors.

Protection is guaranteed in terms of short-circuit conditions, overtemperature, under- and overvoltage. Various diagnostic functions and a very low quiescent current in standby mode enable a wide range of applications. Automotive qualification referring to conducted interferences, EMC protection and 2-kV ESD protection gives added value and enhanced quality for the strict automotive requirements.

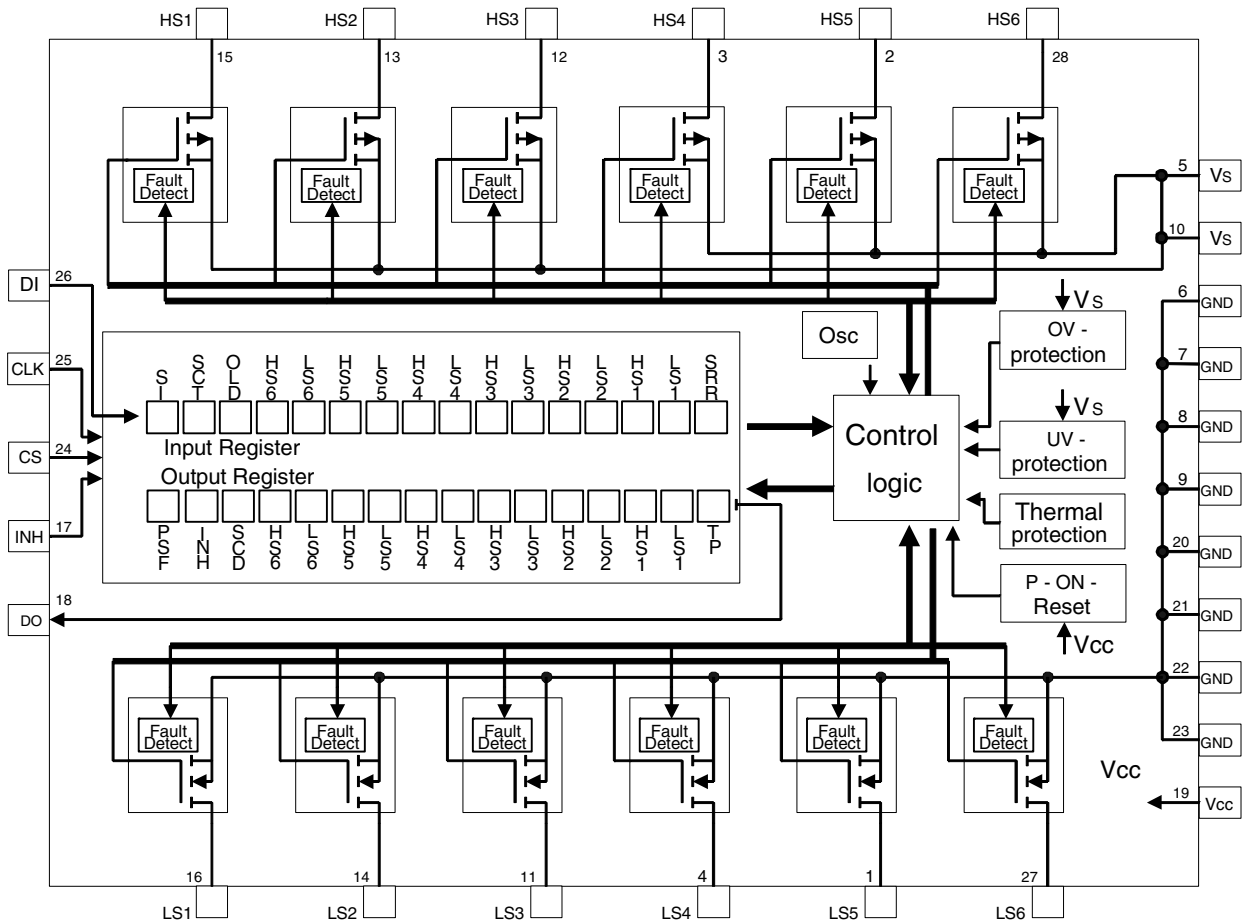


## Dual Hex DMOS Output Driver with Serial Input Control

### U6815BM

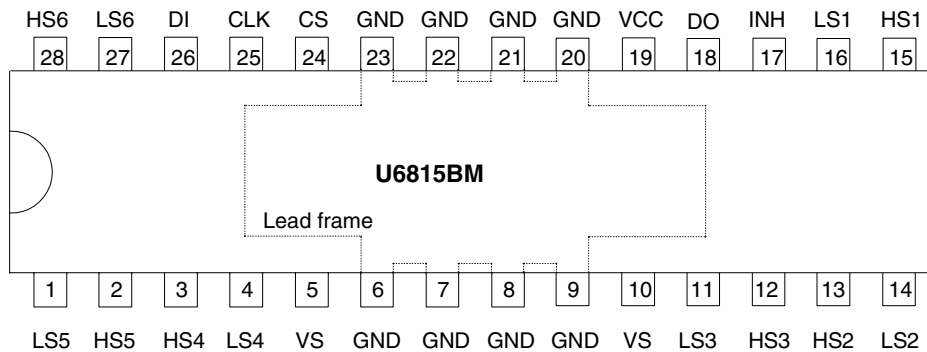


Figure 1-1. Block Diagram



## 2. Pin Configuration

**Figure 2-1.** Pinning SO28



**Table 2-1.** Pin Description

Pin	Symbol	Function
1	LS5	Low-side driver output 5, power-MOS open drain with internal reverse diode, overvoltage protection by active zenering, short-circuit protection, diagnosis for short and open load
2	HS5	High-side driver output 5, power-MOS open drain with internal reverse diode, overvoltage protection by active zenering, short-circuit protection, diagnosis for short and open load
3	HS4	High-side driver output 4 (see pin 2)
4	LS4	Low-side driver output 4 (see pin 1)
5	VS	Power supply output stages HS4, HS5, HS6, internal supply; external connection to pin 10 necessary
6, 7, 8, 9	GND	Ground, reference potential, internal connection to pin 20 to 23, cooling tab
10	VS	Power supply output stages HS1, HS2 and HS3
11	LS3	Low-side driver output 3 (see pin 1)
12	HS3	High-side driver output 3 (see pin 2)
13	HS2	High-side driver output 2 (see pin 2)
14	LS2	Low-side driver output 2 (see pin 1)
15	HS1	High-side driver output 1 (see pin 2)
16	LS1	Low-side driver output 1 (see pin 1)
17	INH	Inhibit input, 5-V logic input with internal pull down, low = standby, high = normal operating
18	DO	Serial data output, 5-V CMOS logic level tristate output for output (status) register data, sends 16-bit status information to the microcontroller (LSB is transferred first). Output will remain tristated unless device is selected by CS = low, therefore, several ICs can operate on one data output line only.
19	VCC	Logic supply voltage (5V)
20, 21, 22, 23	GND	Ground (see pins 6 to 9)
24	CS	Chip select input, 5-V CMOS logic level input with internal pull up, low = serial communication is enabled, high = disabled
25	CLK	Serial clock input, 5-V CMOS logic level input with internal pull down, controls serial data input interface and internal shift register ( $f_{max} = 2 \text{ MHz}$ )
26	DI	Serial data input, 5-V CMOS logic level input with internal pull down, receives serial data from the control device, DI expects a 16-bit control word with LSB being transferred first
27	LS6	Low-side driver output 6 (see pin 1)
28	HS6	High-side driver output 6 (see pin 2)

### 3. Functional Description

#### 3.1 Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and are accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, Pin DO is in tristate condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Figure 3-1. Data Transfer

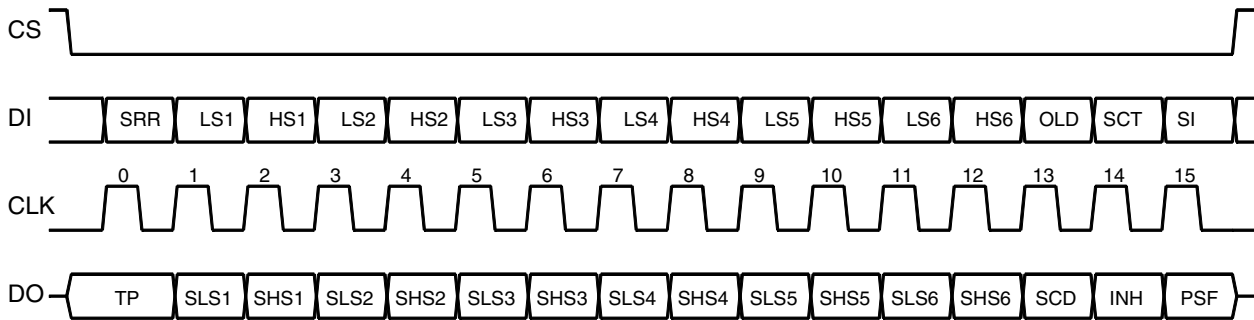


Table 3-1. Input Data Protocol

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF, SCD and overtemperature shutdown in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	LS4	See LS1
8	HS4	See HS1
9	LS5	See LS1
10	HS5	See HS1
11	LS6	See LS1
12	HS6	See HS1
13	OLD	Open load detection (low = on)
14	SCT	Programmable time delay for short circuit and overvoltage shutdown (short circuit shutdown delay high/low = 100 ms/12.5 ms, overvoltage shutdown delay high/low = 15 ms/3.5 ms)
15	SI	Software inhibit; low = standby, high = normal operation (data transfer is not affected by standby function because the digital part is still powered)

After power-on reset, the input register has the following status:

Bit 15 (SI)	Bit 14 (SCT)	Bit 13 (OLD)	Bit 12 (HS6)	Bit 11 (LS6)	Bit 10 (HS5)	Bit 9 (LS5)	Bit 8 (HS4)	Bit 7 (LS4)	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L

**Table 3-2.** Output Data Protocol

Bit	Output (Status) Register	Function
0	TP	Temperature prewarning: high = warning (overtemperature shut down) <sup>(1)</sup>
1	Status LS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off)
2	Status HS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off)
3	Status LS2	Description see LS1
4	Status HS2	Description see HS1
5	Status LS3	Description see LS1
6	Status HS3	Description see HS1
7	Status LS4	Description see LS1
8	Status HS4	Description see HS1
9	Status LS5	Description see LS1
10	Status HS5	Description see HS1
11	Status LS6	Description see LS1
12	Status HS6	Description see HS1
13	SCD	Short circuit detected: set high, when at least one output is switched off by a short circuit condition
14	INH	Inhibit: this bit is controlled by software (bit SI in input register) and hardware inhibit (pin 17). High = standby, low = normal operation
15	PSF	Power supply fail: over- or undervoltage at pin VS detected

Note: 1. Bit 0 to 15 = high: overtemperature shutdown

## 4. Power Supply Fail

In case of over-/undervoltage at pin VS, an internal timer is started. When the overvoltage delay time ( $t_{dOV}$ ) programmed by the SCT Bit, or the undervoltage delay time ( $t_{dUV}$ ) is reached, the power supply fail bit (PSF) in the output register is set and all outputs are disabled. When normal voltage is present again, the outputs are enabled immediately. The PSF bit remains high until it is reset by the SRR bit in the input register.

## 5. Open-load Detection

If the open-load detection bit (OLD) is set to low, a pull-up current for each high-side switch and a pull-down current for each low-side switch is turned on (open-load detection current  $I_{HS1-6}$ ,  $I_{LS1-6}$ ). If  $V_{VS} - V_{HS1-6}$  or  $V_{LS1-6}$  is lower than the open-load detection threshold (open-load condition) the corresponding bit of the output in the output register is set to high. Switching on an output stage with OLD bit set to low disables the open-load function for this output.

## 6. Overtemperature Protection

If the junction temperature exceeds the thermal prewarning threshold,  $T_{jPW\ set}$ , the temperature prewarning bit (TP) in the output register is set. When temperature falls below the thermal prewarning threshold  $T_{jPW\ reset}$ , the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word: with CS = high to low, the state of TP appears at Pin DO. After the microcontroller has read this information, CS is set high and the data transfer is interrupted without affecting the state of input and output registers.

If the junction temperature exceeds the thermal shutdown threshold  $T_{j\ switch\ off}$ , the outputs are disabled and all bits in the output register are set high. The outputs can be enabled again when the temperature falls below the thermal shutdown threshold,  $T_{j\ switch\ on}$ , and when a high has been written to the SRR bit in the input register. Thermal prewarning and shutdown threshold have hysteresis.

## 7. Short-circuit Protection

The output currents are limited by a current regulator. Current limitation takes place when the over-current limitation and shutdown threshold ( $I_{HS1-6}$ ,  $I_{LS1-6}$ ) are reached. Simultaneously, an internal timer is started. The shorted output is disabled when during a permanent short the delay time ( $t_{dSd}$ ) programmed by the Short-Circuit Timer (SCT) bit is reached. Additionally, the Short-Circuit Detection (SCD) bit is set. If the temperature prewarning bit TP in the output register is set during a short, the shorted output is disabled immediately and SCD bit is set. By writing a high to the SRR bit in the input register, the SCD bit is reset and the disabled outputs are enabled.

### 7.1 Inhibit

There are two ways to inhibit the U6815BM:

1. Set bit SI in the input register to zero
2. Switch Pin 17 (INH) to 0V

In both cases, all output stages are turned off but the serial interface stays active. The output stages can be activated again by bit SI = 1 or by pin 17 (INH) switched back to 5V.

## 8. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All values refer to GND pins.

Parameters	Pins	Symbol	Value	Unit
Supply voltage	5, 10	$V_{VS}$	-0.3 to +40	V
Supply voltage, $t < 0.5s$ ; $I_S > -2A$	5, 10	$V_{VS}$	-1	V
Supply voltage difference	$ V_{S\_Pin5} - V_{S\_Pin10} $	$\Delta V_{VS}$	150	mV
Supply current	5, 10	$I_{VS}$	1.4	A
Supply current, $t < 200$ ms	5, 10	$I_{VS}$	2.6	A
Logic supply voltage	19	$V_{VCC}$	-0.3 to +7	V
Input voltage	17	$V_{INH}$	-0.3 to +17	V
Logic input voltage	24 to 26	$V_{DI}, V_{CLK}, V_{CS}$	-0.3 to $V_{VCC} + 0.3$	V
Logic output voltage	18	$V_{DO}$	-0.3 to $V_{VCC} + 0.3$	V
Input current	17, 24 to 26	$I_{INH}, I_{DI}, I_{CLK}, I_{CS}$	-10 to +10	mA
Output current	18	$I_{DO}$	-10 to +10	mA
Output current	1 to 4, 11 to 16	$I_{LS1} \text{ to } I_{LS6}$	Internally limited (see output specification)	mA
	27, 28	$I_{HS1} \text{ to } I_{HS6}$		mA
Reverse conducting current ( $t_{pulse} = 150 \mu s$ )	2, 3, 12, 13, 15, 28 towards 5, 10	$I_{HS1} \text{ to } I_{HS6}$	17	A
Junction temperature range		$T_j$	-40 to +150	°C
Storage temperature range		$T_{stg}$	-55 to +150	°C

## 9. Thermal Resistance

All values refer to GND pins

Parameters	Symbol	Value	Unit
Junction - pin, measured to GND, Pins 6 to 9 and 20 to 23	$R_{thJP}$	25	K/W
Junction ambient	$R_{thJA}$	65	K/W

## 10. Operating Range

All values refer to GND pins

Parameters	Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	5, 10	$V_{VS}$	$V_{UV}^{(1)}$		40 <sup>(2)</sup>	V
Logic supply voltage	19	$V_{VCC}$	4.5	5	5.5	V
Logic input voltage	17, 24 to 26	$V_{INH}, V_{DI}, V_{CLK}, V_{CS}$	-0.3		$V_{VCC}$	V
Serial interface clock frequency	25	$f_{CLK}$			2	MHz
Junction temperature		$T_j$	-40		+150	°C

- Notes: 1. Threshold for undervoltage detection  
 2. Output disabled for  $V_{VS} > V_{OV}$  (threshold for overvoltage detection)

## 11. Noise and Surge Immunity

Parameters	Test Conditions	Value
Conducted interferences	ISO 7637-1	level 4 <sup>(1)</sup>
Interference suppression	VDE 0879 Part 2	level 5
ESD (human body model)	MIL-STD-883D Method 3015.7	2 kV
ESD (machine model)	EOS/ESD - S 5.2	150V

Note: 1. Test pulse 5:  $V_{Smax} = 40V$

## 12. Electrical Characteristics

$7.5V < V_{VS} < 40V$ ;  $4.5V < V_{VCC} < 5.5V$ ; INH = High;  $-40^{\circ}C < T_j < 150^{\circ}C$ ; unless otherwise specified, all values refer to GND pins.

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
<b>Current Consumption</b>						
Quiescent current ( $V_S$ )	$V_{VS} < 16V$ , INH or bit SI = low Pins 5, 10	$I_{VS}$			40	$\mu A$
Quiescent current ( $V_{CC}$ )	$4.5V < V_{VCC} < 5.5V$ , INH or bit SI = low, pin 19	$I_{VCC}$			20	$\mu A$
Supply current ( $V_S$ ) normal operating	$V_{VS} < 16V$ , pins 5, 10 all output stages off	$I_{VS}$		0.8	1.2	mA
	All output stages on, no load	$I_{VS}$			10	mA
Supply current ( $V_{CC}$ )	$4.5V < V_{VCC} < 5.5V$ , normal operating, pin 19	$I_{VCC}$			150	$\mu A$
<b>Internal Oscillator Frequency</b>						
Frequency (time-base for delay timers)		$f_{OSC}$	19		45	kHz
<b>Over- and Undervoltage Detection, Power-on Reset</b>						
Power-on reset threshold	Pin 19	$V_{VCC}$	3.4	3.9	4.4	V
Power-on reset delay time	After switching on $V_{VCC}$	$t_{dPor}$	30	95	160	$\mu s$
Undervoltage detection threshold	Pins 5, 10	$V_{UV}$	5.5		7.0	V
Undervoltage detection hysteresis	Pins 5, 10	$\Delta V_{UV}$		0.4		V
Undervoltage detection delay		$t_{dUV}$	7		21	ms
Overvoltage detection threshold	Pins 5, 10	$V_{OV}$	18		22.5	V
Overvoltage detection hysteresis	Pins 5, 10	$\Delta V_{OV}$		1		V
Overvoltage detection delay	Input register, Bit 14 (SCT) = high	$t_{dOV}$	7		21	ms
Overvoltage detection delay	Input register, Bit 14 (SCT) = low	$t_{dOV}$	1.75		5.25	ms
<b>Thermal Prewarning and Shutdown</b>						
Thermal prewarning, set		$T_{jPWset}$	125	145	165	$^{\circ}C$
Thermal prewarning, reset		$T_{jPWreset}$	105	125	145	$^{\circ}C$
Thermal prewarning hysteresis		$\Delta T_{jPW}$		20		K
Thermal shutdown, off		$T_{j\ switch\ off}$	150	170	190	$^{\circ}C$
Thermal shutdown, on		$T_{j\ switch\ on}$	130	150	170	$^{\circ}C$
Thermal shutdown hysteresis		$\Delta T_{j\ switch\ off}$		20		K

Notes: 1. Only valid for version U6815BM-N.

2. Delay time between rising edge of CS after data transmission and switch-on output stages to 90% of final level.



**12. Electrical Characteristics (Continued)**

7.5V < V<sub>VS</sub> < 40V; 4.5V < V<sub>VCC</sub> < 5.5V; INH = High; -40°C < T<sub>j</sub> < 150°C; unless otherwise specified, all values refer to GND pins.

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
Ratio thermal shutdown, off/thermal prewarning, set		$\frac{T_{j\text{ switch off}}}{T_{j\text{PW set}}}$	1.05	1.17		
Ratio thermal shutdown, on/thermal prewarning, reset		$\frac{T_{j\text{ switch on}}}{T_{j\text{PW reset}}}$	1.05	1.2		
<b>Output Specification (LS1 to LS6, HS1 to HS6), 7.5V &lt; V<sub>VS</sub> &lt; V<sub>OV</sub></b>						
On resistance, low	I <sub>Out</sub> = 600 mA, Pins 1, 4, 11, 14, 16 and 27	R <sub>DS On L</sub>			1.5	Ω
On resistance, high	I <sub>Out</sub> = -600 mA, Pins 2, 3, 12, 13, 15 and 28	R <sub>DS On H</sub>			2.0	Ω
Output clamping voltage	I <sub>LS1-6</sub> = 50 mA, Pins 1, 4, 11, 14, 16, 27	V <sub>LS1-6</sub>	40		60	V
Output leakage current	V <sub>LS1-6</sub> = 40V, all output stages off, Pins 1, 4, 11, 14, 16 and 27	I <sub>LS1-6</sub>			10	μA
	V <sub>HS1-6</sub> = 0V, all output stages off, Pins 2, 3, 12, 13, 15 and 28	I <sub>HS1-6</sub>	-10			μA
Inductive shutdown energy <sup>(1)</sup>	Pins 1-4, 11-16, 27 and 28	W <sub>outx</sub>			15	mJ
Output voltage edge steepness	Pins 1-4, 11-16, 27 and 28	$\frac{dV_{LS1-6}/dt}{dV_{HS1-6}/dt}$	50	200	400	mV/μs
Overcurrent limitation and shutdown threshold	Pins 1, 4, 11, 14, 16 and 27	I <sub>LS1-6</sub>	650	950	1250	mA
	Pins 2, 3, 12, 13, 15 and 28	I <sub>HS1-6</sub>	-1250	-950	-650	mA
Overcurrent shutdown delay time	Input register, bit 14 (SCT) = high	t <sub>dSd</sub>	70	100	140	ms
	Input register, bit 14 (SCT) = low	t <sub>dSd</sub>	8.75		17.5	ms
Open load detection current	Input register, bit 13 (OLD) = low, output off, pins 1, 4, 11, 14, 16, 27	I <sub>LS1-6</sub>	60		200	μA
	Input register, bit 13 (OLD) = low, output off, pins 2, 3, 12, 13, 15, 28	I <sub>HS1-6</sub>	-150		-30	μA
Open load detection current ratio		$\frac{I_{LS1-6}}{I_{HS1-6}}$	1.2			
Open load detection threshold	Input register, bit 13 (OLD) = low, output off, pins 1, 4, 11, 14, 16, 27	V <sub>LS1-6</sub>	0.6		4	V
	Input register, bit 13 (OLD) = low, output off, pins 2, 3, 12, 13, 15, 28	$\frac{V_{VS}}{V_{HS1-6}}$	0.6		4	V
Output switch on delay <sup>(2)</sup>	R <sub>Load</sub> = 1 kΩ	t <sub>don</sub>			0.5	ms
	R <sub>Load</sub> = 1 kΩ	t <sub>doff</sub>			1	ms
<b>Inhibit Input</b>						
Input voltage low level threshold	Pin 17	V <sub>IL</sub>	0.3 × V <sub>VCC</sub>			V
Input voltage high level threshold	Pin 17	V <sub>IH</sub>			0.7 × V <sub>VCC</sub>	V
Hysteresis of input voltage	Pin 17	ΔV <sub>I</sub>	100		700	mV
Pull-down current	V <sub>INH</sub> = V <sub>VCC</sub> , pin 17	I <sub>PD</sub>	10		80	μA

Notes: 1. Only valid for version U6815BM-N.

2. Delay time between rising edge of CS after data transmission and switch-on output stages to 90% of final level.



## 12. Electrical Characteristics (Continued)

7.5V < V<sub>VS</sub> < 40V; 4.5V < V<sub>VCC</sub> < 5.5V; INH = High; -40°C < T<sub>j</sub> < 150°C; unless otherwise specified, all values refer to GND pins.

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
<b>Serial Interface - Logic Inputs (DI, CLK, CS)</b>						
Input voltage low level threshold	Pins 24 to 26	V <sub>IL</sub>	0.3 × V <sub>VCC</sub>			V
Input voltage high level threshold	Pins 24 to 26	V <sub>IH</sub>			0.7 × V <sub>VCC</sub>	V
Hysteresis of input voltage	Pins 24 to 26	ΔV <sub>I</sub>	50		500	mV
Pull-down current, Pins DI and CLK	V <sub>DI</sub> , V <sub>CLK</sub> = V <sub>VCC</sub> , pins 25, 26	I <sub>PDSI</sub>	2		50	μA
Pull-up current Pin CS	V <sub>CS</sub> = 0V, pin 24	I <sub>PUSI</sub>	-50		-2	μA
<b>Serial Interface - Logic Output (DO)</b>						
Output voltage low level	I <sub>OL</sub> = 3 mA, pin 18	V <sub>DOl</sub>			0.5	V
Output voltage high level	I <sub>OL</sub> = -2 mA, pin 18	V <sub>DOH</sub>	V <sub>VCC</sub> - 1V			V
Leakage current (tristate)	V <sub>CS</sub> = V <sub>VCC</sub> , 0V < V <sub>DO</sub> < V <sub>VCC</sub> , pin 18	I <sub>DO</sub>	-10		10	mA

Notes: 1. Only valid for version U6815BM-N.

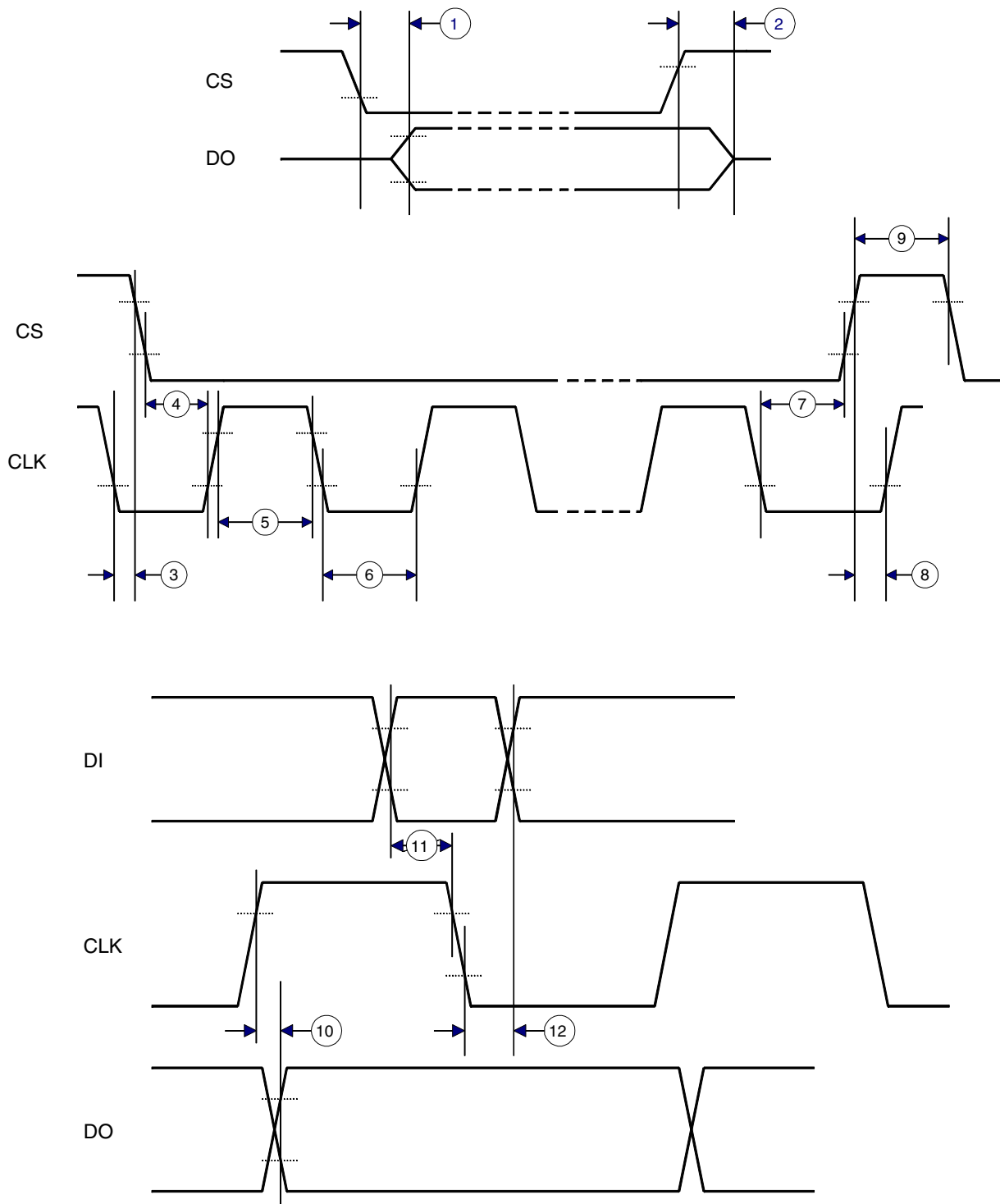
2. Delay time between rising edge of CS after data transmission and switch-on output stages to 90% of final level.

## 13. Serial Interface – Timing

Parameters	Test Conditions	Timing Chart No. <sup>(1)</sup>	Symbol	Min.	Typ.	Max.	Unit
DO enable after CS falling edge	C <sub>DO</sub> = 100 pF	1	t <sub>ENDO</sub>			200	ns
DO disable after CS rising edge	C <sub>DO</sub> = 100 pF	2	t <sub>DISDO</sub>			200	ns
DO fall time	C <sub>DO</sub> = 100 pF	-	t <sub>DOF</sub>			100	ns
DO rise time	C <sub>DO</sub> = 100 pF	-	t <sub>DOr</sub>			100	ns
DO valid time	C <sub>DO</sub> = 100 pF	10	t <sub>DOVal</sub>			200	ns
CS setup time		4	t <sub>CSsethl</sub>	225			ns
CS setup time	V <sub>DO</sub> < 0.2 × V <sub>VCC</sub>	8	t <sub>CSsetlh</sub>	225			ns
CS high time	Input register, Bit 14 (SCT) = high	9	t <sub>CSh</sub>	140			ns
	Input register, Bit 14 (SCT) = low	9	t <sub>CSh</sub>	17.5			ns
CLK high time		5	t <sub>CLKh</sub>	225			ns
CLK low time		6	t <sub>CLKl</sub>	225			ns
CLK period time		-	t <sub>CLKp</sub>	500			ns
CLK setup time		7	t <sub>CLKsethl</sub>	225			ns
CLK setup time		3	t <sub>CLKsetlh</sub>	225			ns
DI setup time		11	t <sub>Dlset</sub>	40			ns
DI hold time		12	t <sub>DlHold</sub>	40			ns

Note: 1. see [Figure 13-1 on page 11](#)

Figure 13-1. Serial Interface Timing Diagram with Chart Numbers

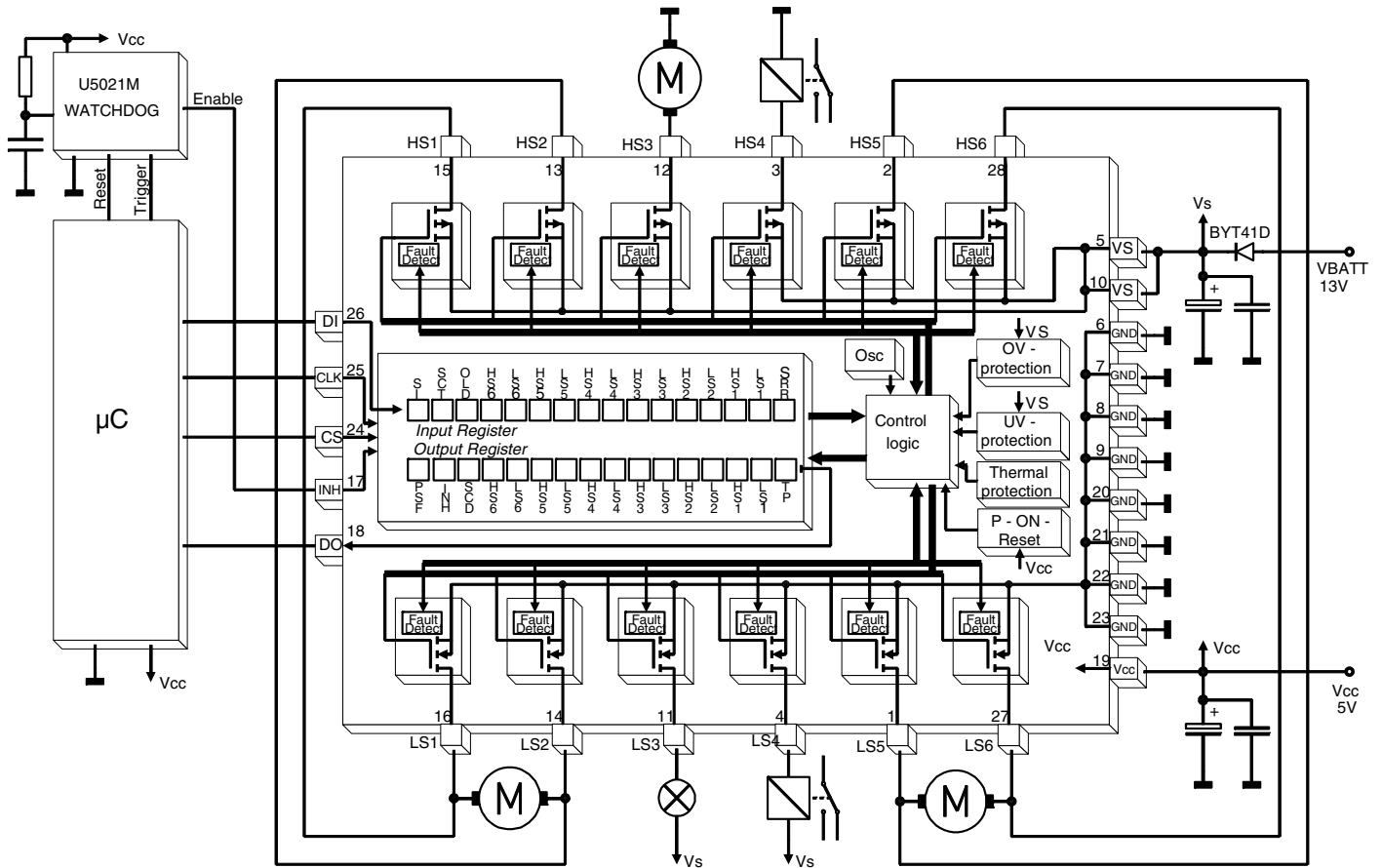


Inputs DI, CLK, CS: High level =  $0.7 \times V_{CC}$ , Low level =  $0.3 \times V_{CC}$

Output DO: High level =  $0.8 \times V_{CC}$ , Low level =  $0.2 \times V_{CC}$

For chart numbers, see Table "Serial Interface – Timing" on page 10.

**Figure 13-2.** Application Circuit



## 14. Application Notes

It is strongly recommended to connect the blocking capacitors at  $V_{CC}$  and  $V_S$  as close as possible to the power supply and GND pins.

Recommended value for capacitors at  $V_S$ :

Electrolytic capacitor  $C > 22 \mu\text{F}$  in parallel with a ceramic capacitor  $C = 100 \text{ nF}$ . Value for electrolytic capacitor depends on external loads, conducted interferences and reverse conducting current  $I_{HSx}$  (see table Absolute Maximum Ratings).

Recommended value for capacitors at  $V_{CC}$ :

Electrolytic capacitor  $C > 10 \mu\text{F}$  in parallel with a ceramic capacitor  $C = 100 \text{ nF}$ . To reduce thermal resistance, it is recommended to place cooling areas on the PCB as close as possible to the GND pins.

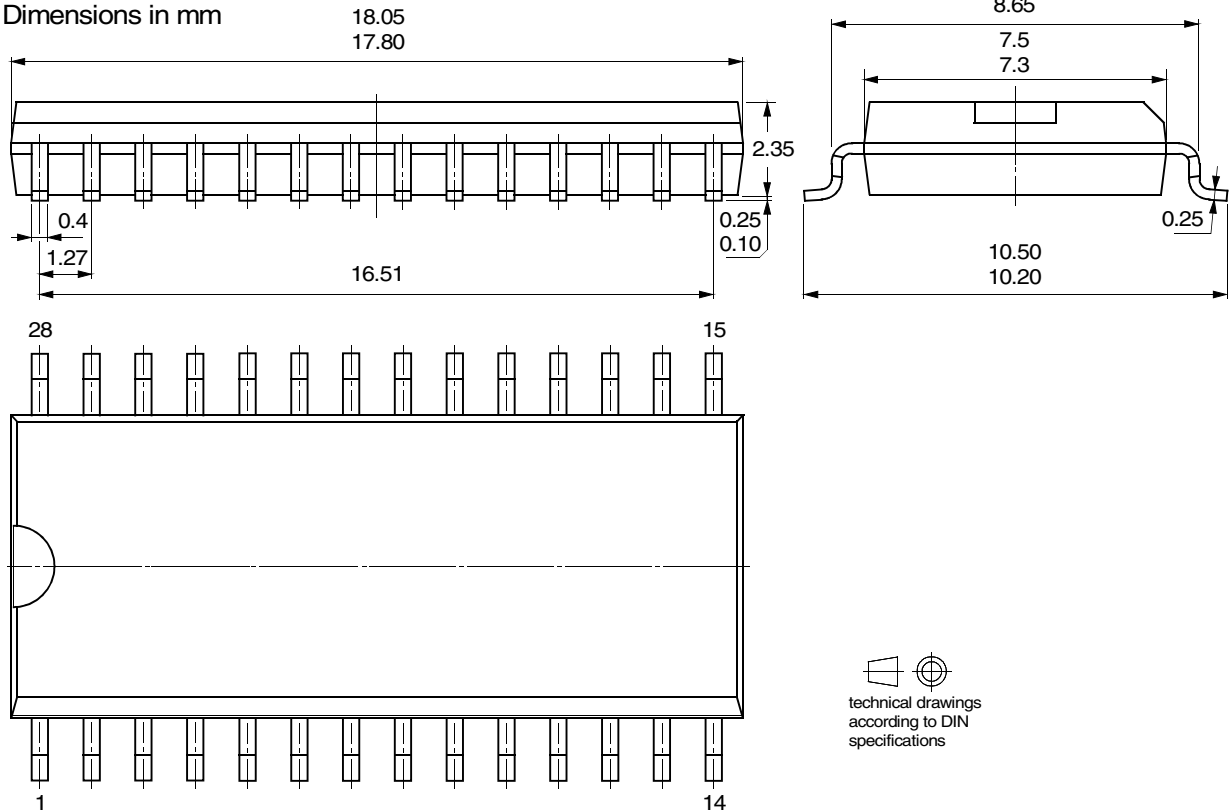
**15. Ordering Information**

Extended Type Number	Package	Remarks
U6815BM-NFLY	SO28	Tubed, Pb-free
U6815BM-NFLG3Y	SO28	Taped and reeled, Pb-free

**16. Package Information**

**Package SO28**

Dimensions in mm



 technical drawings according to DIN specifications

**17. Revision History**

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4545C-BCD-09/05	<ul style="list-style-type: none"> <li>Put datasheet in a new template</li> <li>Pb-free logo on page 1 added</li> <li>New heading rows on Table "Absolute Maximum Ratings" on page 7 added</li> <li>Table "Ordering Information" on page 13 changed</li> </ul>



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