

DATA SHEET

TDA1541A Stereo high performance 16-bit DAC

Product specification
File under Integrated Circuits, IC01

February 1991

Stereo high performance 16-bit DAC

TDA1541A

FEATURES

- High sound quality
- High performance: low noise and distortion, wide dynamic range
- 4 × or 8 × oversampling possible
- Selectable two-channel input format
- TTL compatible inputs.

GENERAL DESCRIPTION

The TDA1541A is a stereo 16-bit digital-to-analog converter (DAC). The ingenious design of the electronic circuit guarantees a high performance and superior sound quality. The TDA1541A is therefore extremely suitable for use in top-end hi-fi digital audio equipment such as high quality Compact Disc players or digital amplifiers.

ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|-------------------------|---------|--------------|----------|--------|
| | PINS | PIN POSITION | MATERIAL | CODE |
| TDA1541A ⁽¹⁾ | 28 | DIL | plastic | SOT117 |

Note

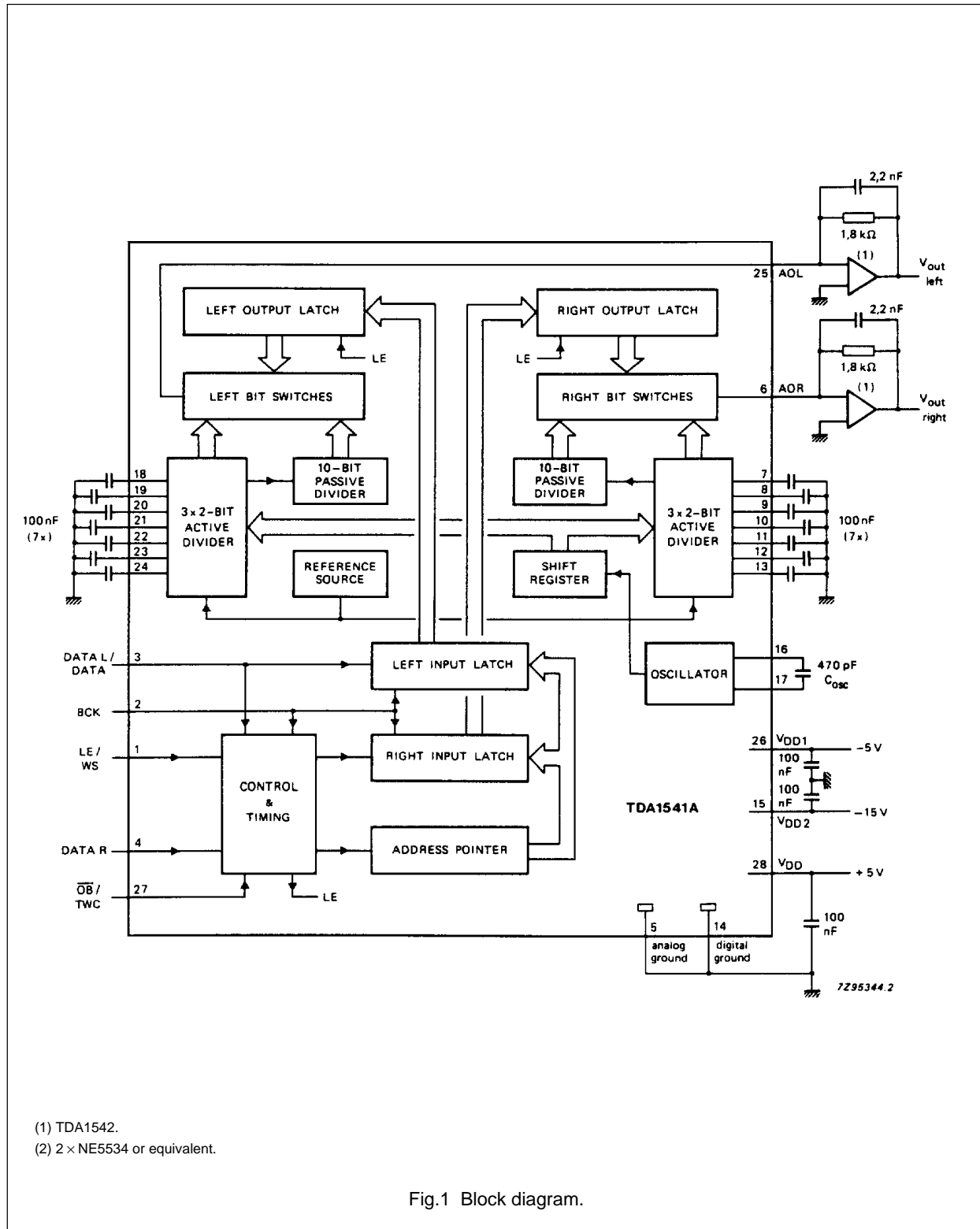
1. SOT117; SOT117-1; 1996 August 09.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-------------------|---|-------------------------------------|------|-------------------------|--------|-----------------|
| V _{DD} | supply voltage; pin 28 | | 4.5 | 5.0 | 5.5 | V |
| -V _{DD1} | supply voltage; pin 26 | | 4.5 | 5.0 | 5.5 | V |
| -V _{DD2} | supply voltage; pin 15 | | 14.0 | 15.0 | 16.0 | V |
| I _{DD} | supply current; pin 28 | | – | 27 | 40 | mA |
| -I _{DD1} | supply current; pin 26 | | – | 37 | 50 | mA |
| -I _{DD2} | supply current; pin 15 | | – | 25 | 35 | mA |
| THD | total harmonic distortion | including noise at 0 dB | – | –95 | –90 | dB |
| | | | – | 0.0018 | 0.0032 | % |
| THD | total harmonic distortion | including noise at –60 dB | – | –42 | – | dB |
| | | | – | 0.79 | – | % |
| NL | non-linearity | at T _{amb} = –20 to +85 °C | – | 0.5 | 1.0 | LSB |
| t _{CS} | current settling time to ± 1LSB | | – | 0.5 | – | µs |
| BR | input bit rate at data input; (pin 3 and 4) | | – | – | 6.4 | Mbits/s |
| f _{BCK} | clock frequency at clock input | | – | – | 6.4 | MHz |
| TC _{FS} | full scale temperature coefficient | at analog (AOL;AOR) | – | ±200 × 10 ⁻⁶ | – | K ⁻¹ |
| T _{amb} | operating ambient temperature range | | –40 | – | +85 | °C |
| P _{tot} | total power dissipation | | – | 700 | – | mW |

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PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|----------|---|
| LE/WS ⁽¹⁾ | 1 | latch enable input/ word select input |
| BCK ⁽¹⁾ | 2 | bit clock input |
| DATA L /DATA /DATA ⁽¹⁾ | 3 | data left channel input/ data input (selected format) |
| DATA R ⁽¹⁾ | 4 | data right channel input |
| GND(A) | 5 | analog ground |
| AOR | 6 | right channel output |
| DECOU | 7 to 13 | decoupling |
| GND (D) | 14 | digital ground |
| V _{DD2} | 15 | -15 V supply voltage |
| COSC | 16,17 | oscillator |
| DECOU | 18 to 24 | decoupling |
| AOL | 25 | left channel output |
| V _{DD1} | 26 | -5 V supply voltage |
| $\overline{\text{OB}}/\text{TWC}^{(1)}$ | 27 | mode select input |
| V _{DD} | 28 | +5 V supply voltage |

Note

- See Table 1 data selection input.

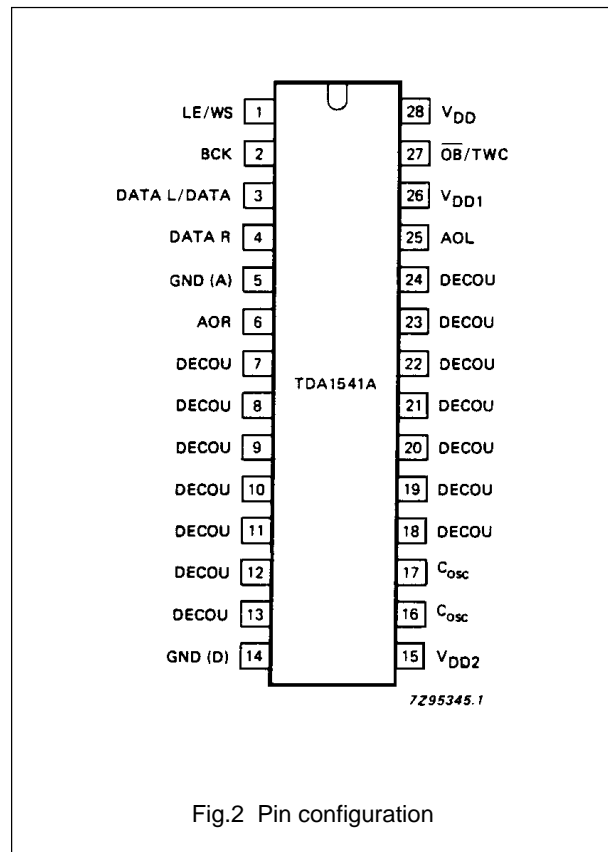


Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode up to 16-bit word length. The most significant bit (MSB) must always be first. The flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast setting facilitates application in $8 \times$ oversampling systems (44.1 kHz to 352.8 kHz or 48 kHz to 384 kHz) with the associated simple analog filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With the input $\overline{\text{OB}}/\text{TWC}$ connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. The converted samples appear at the output, at the first positive going transition of the bit clock signal after a negative going transition of the word select signal.

With $\overline{\text{OB}}/\text{TWC}$ connected to V_{DD} the mode is the same but the data format must be in the two's complement.

When input $\overline{\text{OB}}/\text{TWC}$ input is connected to V_{DD1} the two channels of data (L/R) are input simultaneously via DATA L and DATA R, accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary. The converted samples appear at the output at the positive going transition of the latch enable signal.

The format of the data input signals is shown in Fig.5 and 6.

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True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

| $\overline{\text{OB/TWC}}$ | MODE | PIN 1 | PIN 2 | PIN 3 | PIN 4 |
|----------------------------|--------------|-------|-------|----------|----------|
| -5 V | simultaneous | LE | BCK | DATA L | DATA R |
| 0 V | time MUX OB | WS | BCK | DATA OB | not used |
| +5 V | time MUX TWC | WS | BCK | DATA TWC | not used |

Where:

| | |
|----------|---|
| LE | = latch enable |
| WS | = word select, LOW = left channel; HIGH = right channel |
| BCK | = bit clock |
| DATA L | = data left |
| DATA R | = data right |
| DATA OB | = data offset binary |
| DATA TWC | = data two's complement |
| MUX OB | = multiplexed offset binary |
| MUX TWC | = multiplexed two's complement = I ² S- format |

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-------------------|-------------------------------------|------------|-------|-------|------|
| V _{DD} | supply voltage; pin 28 | | 0 | 7 | V |
| -V _{DD1} | supply voltage; pin 26 | | 0 | 7 | V |
| -V _{DD2} | supply voltage; pin 15 | | 0 | 17 | V |
| T _{stg} | storage temperature range | | -55 | +150 | °C |
| T _{amb} | operating ambient temperature range | | -40 | +85 | °C |
| V _{es} | electrostatic handling* | | -1000 | +1000 | V |

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

| SYMBOL | PARAMETER | TYP. | UNIT |
|---------------------|--------------------------|------|------|
| R _{th j-a} | from junction to ambient | 30 | K/W |

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CHARACTERISTICS

$V_{DD} = 5\text{ V}$; $-V_{DD1} = 5\text{ V}$; $-V_{DD2} = 15\text{ V}$; $T_{amb} = +25\text{ }^{\circ}\text{C}$; measured in the circuit of Fig.1; unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|---|------|--------------------------|------|-----------------|
| Supply | | | | | | |
| V_{DD} | supply voltage; pin 28 | | 4.5 | 5.0 | 5.5 | V |
| $-V_{DD1}$ | supply voltage; pin 26 | | 4.5 | 5.0 | 5.5 | V |
| $-V_{DD2}$ | supply voltage; pin 15 | | 14.0 | 15.0 | 16.0 | V |
| $V_{GND(A)}$ $-V_{GND(D)}$ | voltage difference between analog and digital ground | | -0.3 | 0 | +0.3 | V |
| I_{DD} | supply current; pin 28 | | - | 27 | 40 | mA |
| $-I_{DD1}$ | supply current; pin 26 | | - | 37 | 50 | mA |
| $-I_{DD2}$ | supply current; pin 15 | | - | 25 | 35 | mA |
| Inputs | | | | | | |
| $-I_{IL}$ | input current pins (1, 2, 3 and 4) digital inputs LOW | $V_I = 0.8\text{ V}$ | - | - | 0.4 | mA |
| I_{IH} | digital inputs HIGH | $V_I = 2.0\text{ V}$ | - | - | 20 | μA |
| $ I_{OB/TWC} $ | Digital input currents (pin 27) | | | | | |
| | +5 V | | - | - | 1 | μA |
| | 0 V | | - | - | 20 | μA |
| | -5 V | | - | - | 40 | μA |
| f_{BCK} | input frequency/bit rate clock input pin 2 | | - | - | 6.4 | MHz |
| BR | bit rate data input pin 3 and 4 | | - | - | 6.4 | Mbits/s |
| f_{WS} | word select input pin 2 | | - | - | 200 | kHz |
| f_{LE} | latch enable input 1 | | - | - | 200 | kHz |
| C_I | input capacitance of digital inputs | | - | 12 | - | pF |
| Analog outputs (AOL;AOR; see note 1) | | | | | | |
| Res | resolution | | - | 16 | - | bits |
| I_{FS} | full scale current | | 3.4 | 4.0 | 4.6 | mA |
| $ I_{ZS} $ | zero scale current | | - | 25 | 50 | nA |
| T_{CFS} | full scale temperature coefficient | $T_{amb} = -20\text{ to }+85\text{ }^{\circ}\text{C}$ | - | $\pm 200 \times 10^{-6}$ | - | K^{-1} |
| Analog outputs (V_{ref}) | | | | | | |
| E_L | integral linearity error | $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 0.5 | 1.0 | LSB |
| E_L | integral linearity error | $T_{amb} = -20\text{ to }+85\text{ }^{\circ}\text{C}$ | - | - | 1.0 | LSB |
| E_{dL} | differential linearity error | $T_{amb} = 20\text{ }^{\circ}\text{C}$, note 2 | - | 0.5 | 1.0 | LSB |
| E_{dL} | differential linearity error | $T_{amb} = -20\text{ to }+85\text{ }^{\circ}\text{C}$ | - | - | 1.0 | LSB |
| THD | total harmonic distortion | at 0 dB; note 3 | -100 | - | - | dB |
| | | | - | 0.0010 | - | % |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------------------|---|---|------|--------|--------|---------|
| THD | total harmonic distortion | including noise at 0 dB; note 3, Fig. 3, 4 | – | –95 | –90 | dB |
| | | | – | 0.0018 | 0.0032 | % |
| THD | total harmonic distortion | including noise at –60 dB; note 3, Fig. 3, 4 | – | –42 | – | dB |
| | | | – | 0.79 | – | % |
| t_{cs} | settling time ± 1 LSB | | – | 0.5 | – | μ s |
| α | channel separation | | 90 | 98 | – | dB |
| $ d_{IO} $ | unbalance between outputs | note 4 | – | < 0.1 | 0.3 | dB |
| $ t_d $ | time delay between outputs | | – | – | 0.2 | μ s |
| SSVR | supply voltage ripple rejection | $V_{DD} = +5$ V; note 4 | – | –76 | – | dB |
| SSVR | supply voltage ripple rejection | $V_{DD1} = -5$ V; note 4 | – | –84 | – | dB |
| SSVR | supply voltage ripple rejection | $V_{DD2} = -15$ V; note 4 | – | –58 | – | dB |
| S/N | signal-to-noise ratio | at bipolar zero | – | 110 | – | dB |
| S/N | signal-to-noise ratio | at full scale | 98 | 104 | – | dB |
| Timing (Fig. 5 and 6) | | | | | | |
| t_r | rise time | | – | – | 32 | ns |
| t_f | fall time | | – | – | 32 | ns |
| t_{CY} | bit clock cycle time | | 156 | – | – | ns |
| t_{HB} | bit clock HIGH time | | 46 | – | – | ns |
| t_{LB} | bit clock LOW time | | 46 | – | – | ns |
| t_{FBRL} | bit clock fall time to latch enable rise time | | 0 | – | – | ns |
| t_{RBFL} | bit clock rise time to latch enable fall time | | 0 | – | – | ns |
| $t_{SU;DAT}$ | data set-up time | | 32 | – | – | ns |
| $t_{HD;DAT}$ | data hold time to bit clock | | 0 | – | – | ns |
| $t_{HD;WS}$ | word select hold time | | 0 | – | – | ns |
| $t_{SU;WS}$ | word select set-up time | | 32 | – | – | ns |

Notes to the characteristics

- To ensure no performance losses, permitted output voltage compliance is ± 25 mV maximum.
- Selections have been made with respect to the maximum differential linearity error (E_{dL}):

TDA1541A/N2 bit 1-16 $E_{dL} < 1$ LSB

TDA1541A/N2/R1 bit 1-16 $E_{dL} < 2$ LSB

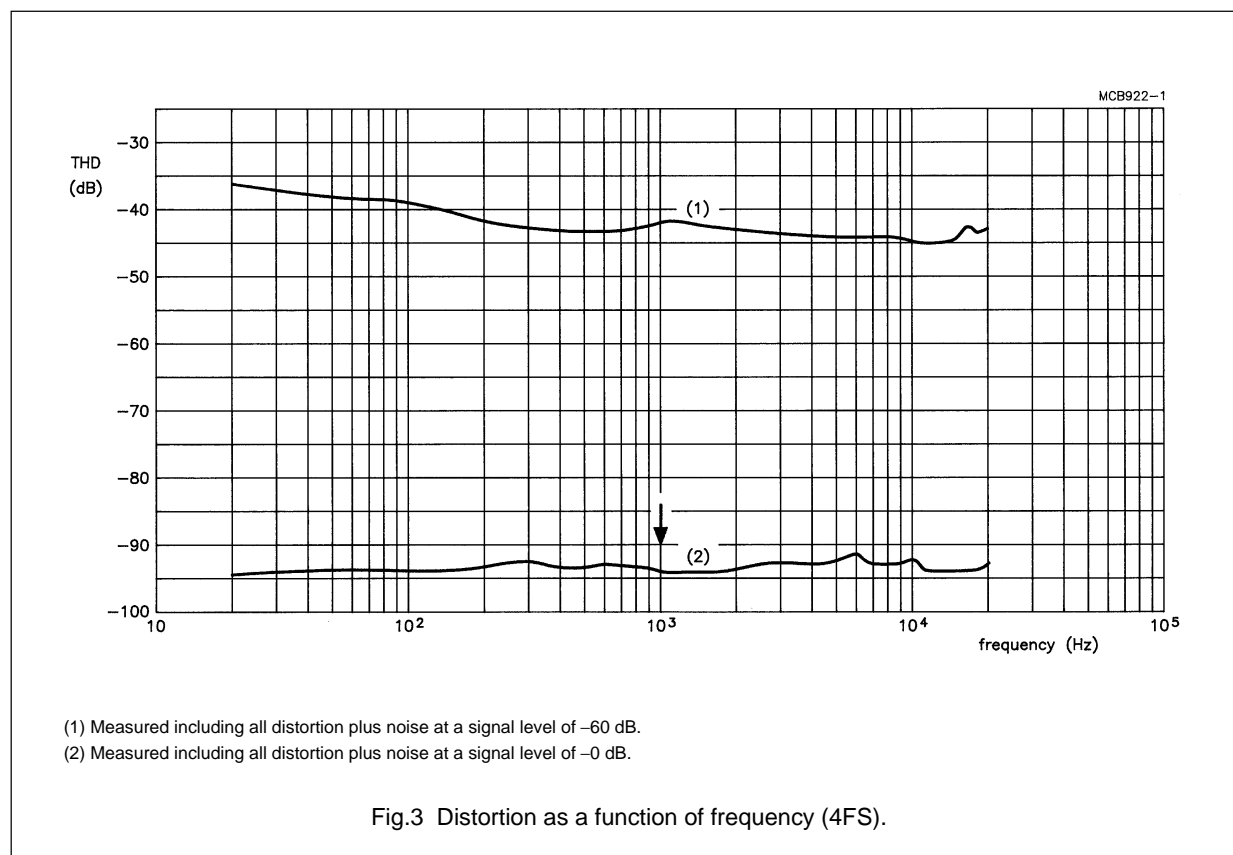
TDA1541A/N2/S1 bit 1-7 $E_{dL} < 0.5$ LSB
 bit 8-15 $E_{dL} < 1$ LSB
 bit 16 $E_{dL} < 0.75$ LSB

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The S1 version has been specially selected to achieve extremely good performance even for small signals.

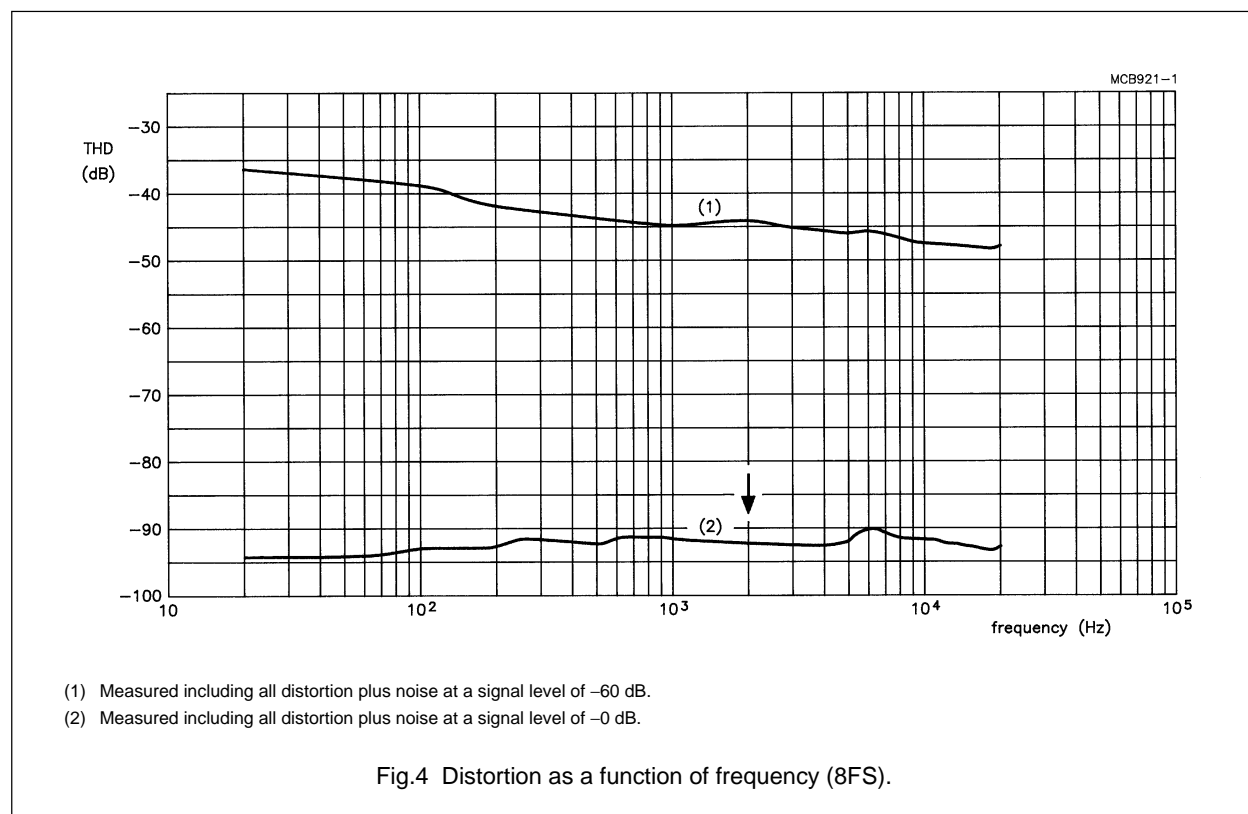
3. Measured using a 1 kHz sinewave generated at a sampling rate of 176.4 kHz.
4. $V_{\text{ripple}} = 100 \text{ mV}$ and $f_{\text{ripple}} = 100 \text{ Hz}$.

**Notes to Fig.3**

- The sample frequency 4FS: 176.4 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.

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**Notes to Fig.4**

- The sample frequency 8FS: 352.8 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.

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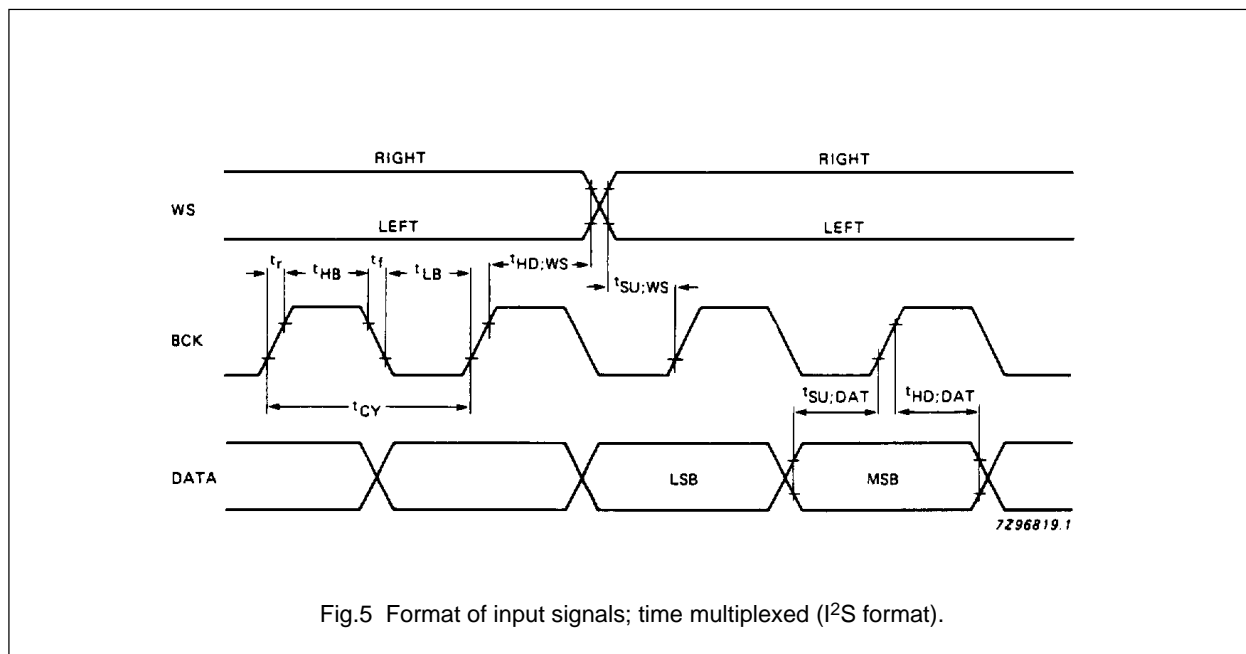


Fig.5 Format of input signals; time multiplexed (I2S format).

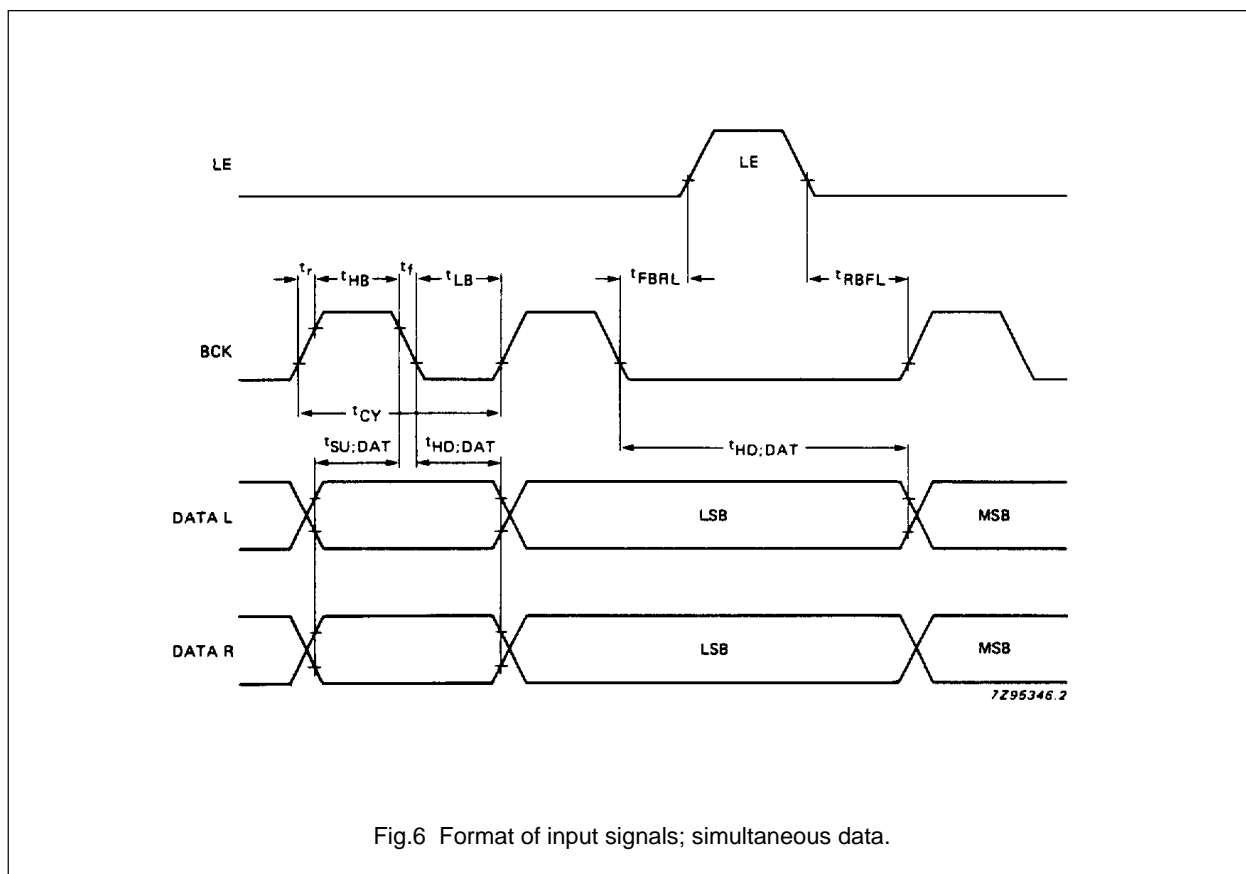


Fig.6 Format of input signals; simultaneous data.

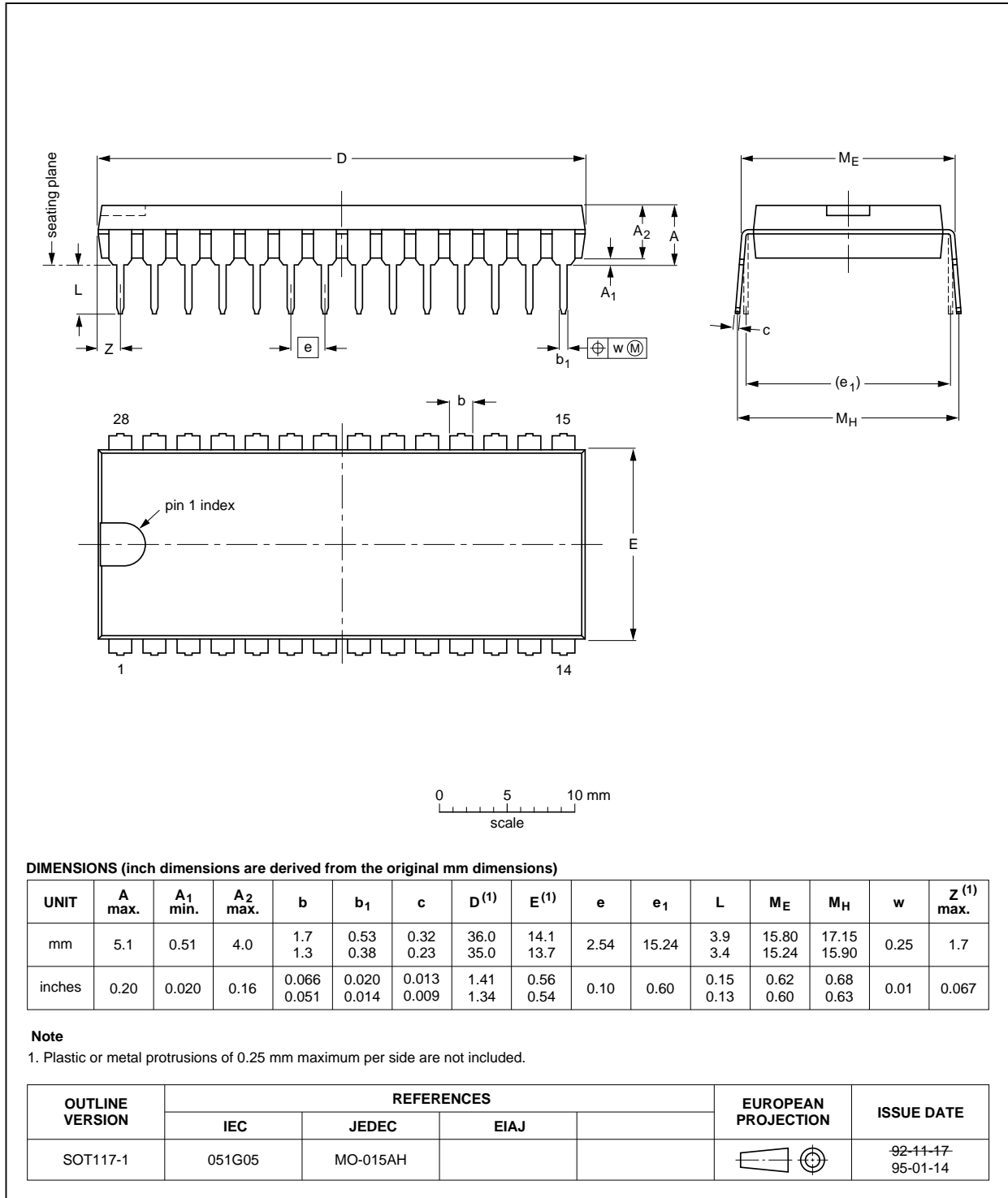
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PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



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SOLDERING**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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