



# STP130NS04ZB - STB130NS04ZB-1 STB130NS04ZB - STW130NS04ZB

N-channel clamped - 7 mΩ - 80A TO-220/I<sup>2</sup>/D<sup>2</sup>PAK/TO-247  
Fully protected mesh overlay™ MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP130NS04ZB	clamped	<9 mΩ	80A
STB130NS04ZB	clamped	<9 mΩ	80A
STW130NS04ZB	clamped	<9 mΩ	80A
STB130NS04ZB	clamped	<9 mΩ	80A

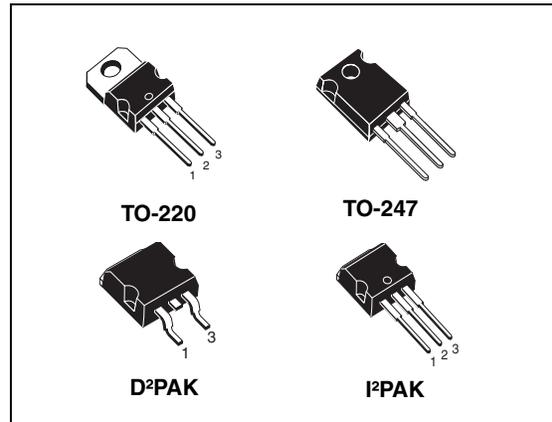
- 100% avalanche tested
- Low capacitance and gate charge
- 175°C maximum junction temperature

## Description

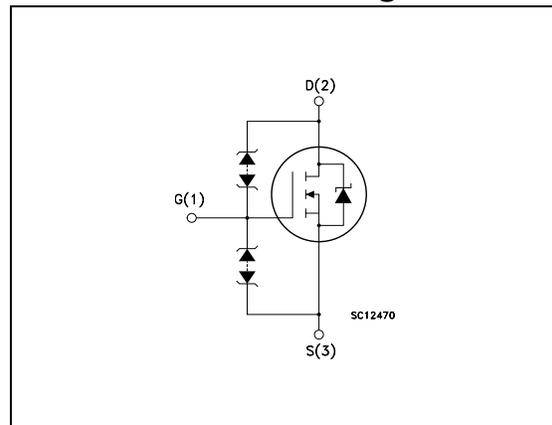
This fully clamped MOSFET is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

## Applications

- High switching current
- Linear applications



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STP130NS04ZB	P130NS04ZB	TO-220	Tube
STB130NS04ZBT4	B130NS04ZB	D <sup>2</sup> PAK	Tape & reel
STW130NS04ZB	W130NS04ZB	TO-247	Tube
STB130NS04ZB-1	B130NS04ZB	I <sup>2</sup> PAK	Tube

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuit</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Packaging mechanical data</b> .....	<b>14</b>
<b>6</b>	<b>Revision history</b> .....	<b>15</b>

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	clamped	V
$V_{GS}$	Gate-source voltage	clamped	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	60	A
$I_{DG}$	Drain gate current (continuous)	$\pm 50$	mA
$I_{GS}$	Gate source current (continuous)	$\pm 50$	mA
$I_{DM}^{(1)}$	Drain current (pulsed)	320	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	300	W
	Derating factor	2.0	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate-source ESD(HBM-C=100 pF, R=1.5 K $\Omega$ )	4	KV
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area

**Table 2. Thermal data**

		TO-220	D <sup>2</sup> PAK/I <sup>2</sup> PAK	TO-247	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.50			$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb Max		35		$^\circ\text{C}/\text{W}$
$R_{thj-a}$	Thermal resistance junction-ambient Max	62.5		50	
$T_l^{(2)}$	Maximum lead temperature for soldering purpose	300			$^\circ\text{C}$

1. When mounted on 1 inch<sup>2</sup> FR4 2oz Cu

2. (1.6 mm from case, for 10 sec)

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ Max)	80	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J=25^\circ\text{C}$ , $I_d=I_{ar}$ , $V_{dd}=30\text{V}$ )	500	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$ , $V_{GS} = 0$ $-40 < T_j < 175^{\circ}\text{C}$	33			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 16 \text{ V}$ , $T_j = 25^{\circ}\text{C}$ $V_{DS} = 16 \text{ V}$ , $T_j = 125^{\circ}\text{C}$			10 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 10 \text{ V}$ , $T_j = 25^{\circ}\text{C}$			10	nA
$V_{GSS}$	Gate-source breakdown voltage	$I_{GS} = \pm 100 \mu\text{A}$	18			V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS} = I_D = 1 \text{ mA}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 40 \text{ A}$		7	9	m $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15 \text{ V}$ , $I_D = 40 \text{ A}$		50		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$		2700 1275 285		pF pF pF
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD} = 17.5 \text{ V}$ , $I_D = 40 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see Figure 13)		40 10		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD} = 17.5 \text{ V}$ , $I_D = 40 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see Figure 13)		220 100		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 20 \text{ V}$ , $I_D = 80 \text{ A}$ $V_{GS} = 10 \text{ V}$ (see Figure 14)		80 20 27	105	nC nC nC

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=80A, V_{GS}=0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=80A,$ $di/dt = 100A/\mu s,$ $V_{DD}=25V, T_j=150^\circ C$ (see Figure 15)		90 0.18 4		ns $\mu C$ A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

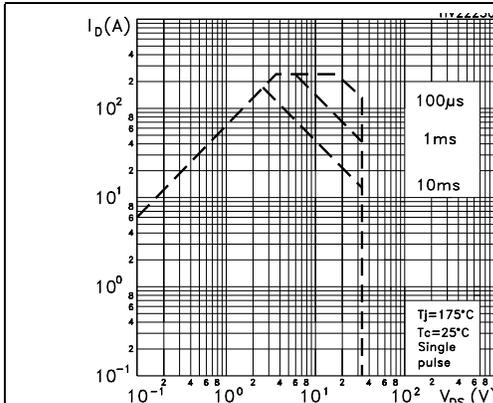


Figure 2. Thermal impedance

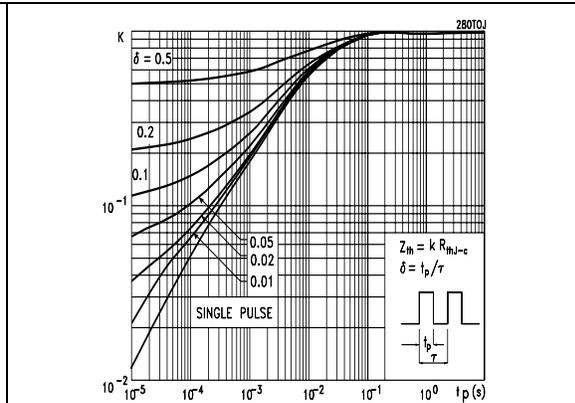


Figure 3. Output characteristics

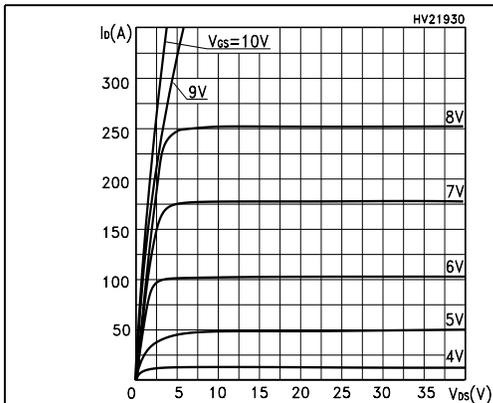


Figure 4. Transfer characteristics

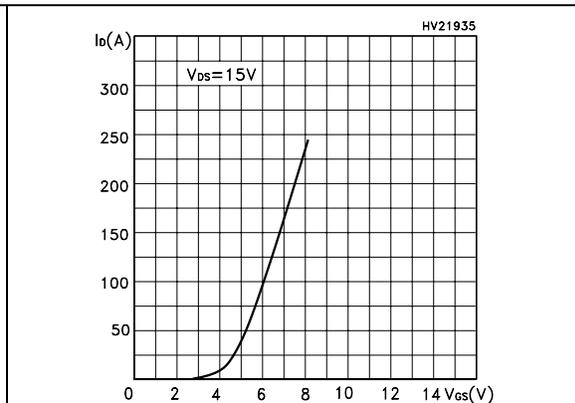


Figure 5. Transconductance

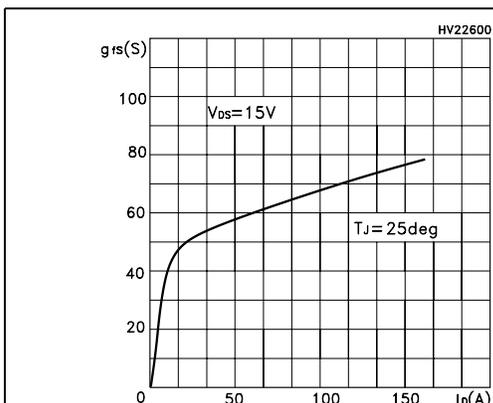


Figure 6. Static drain-source on resistance

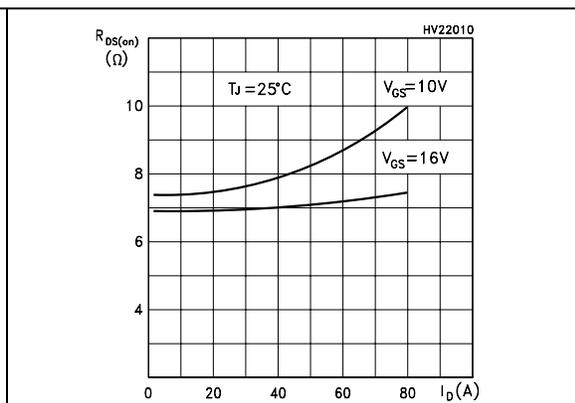


Figure 7. Gate charge vs gate-source voltage    Figure 8. Normalized on resistance vs temperature

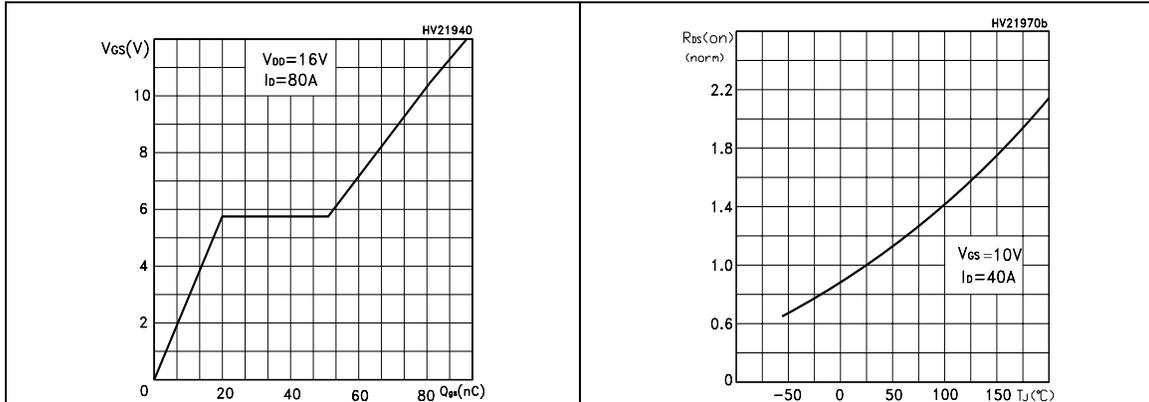


Figure 9. Normalized gate threshold voltage vs temperature    Figure 10. Source-drain diode forward characteristics

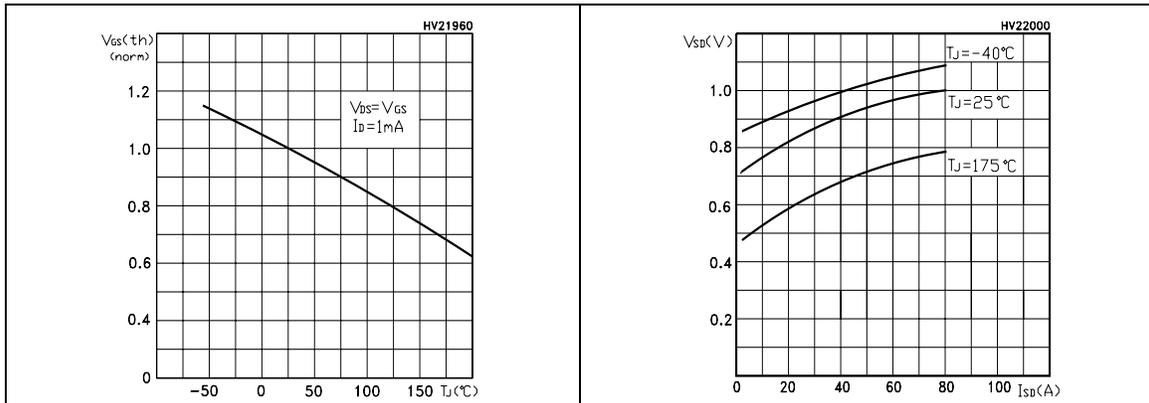


Figure 11. Capacitance variations

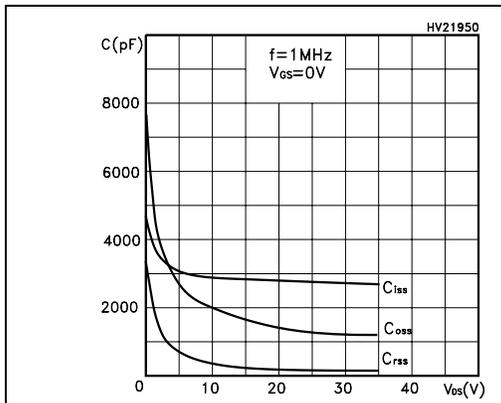
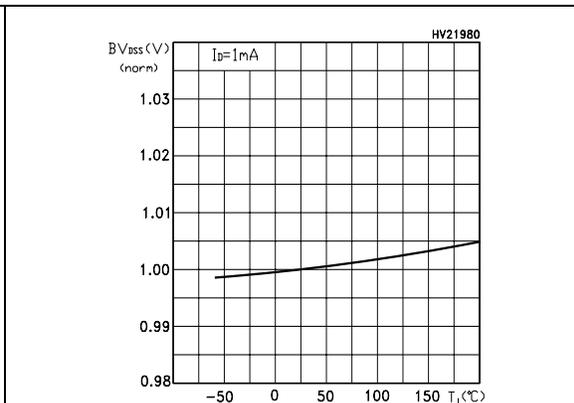


Figure 12. Normalized  $B_{VDSS}$  vs temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

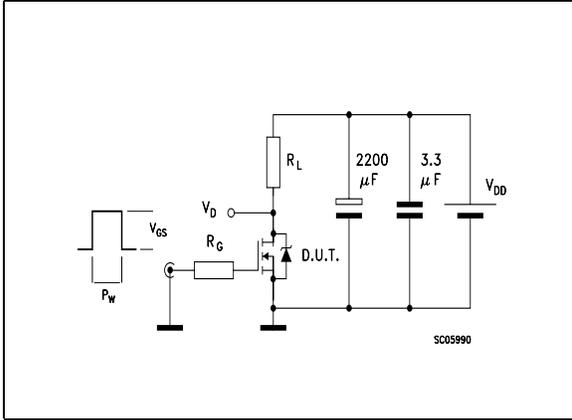


Figure 14. Gate charge test circuit

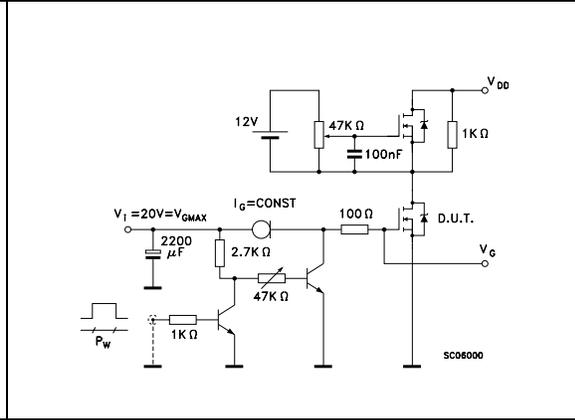


Figure 15. Test circuit for inductive load switching and diode recovery times

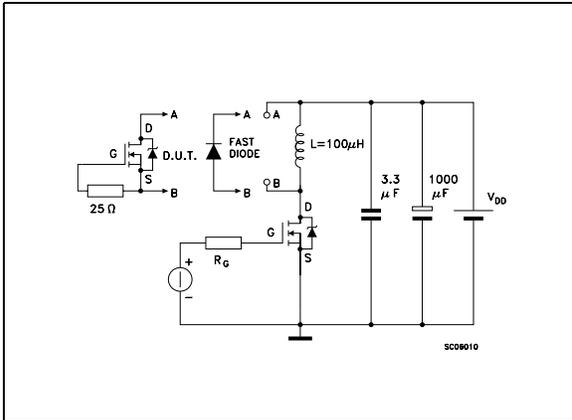


Figure 16. Unclamped Inductive load test circuit

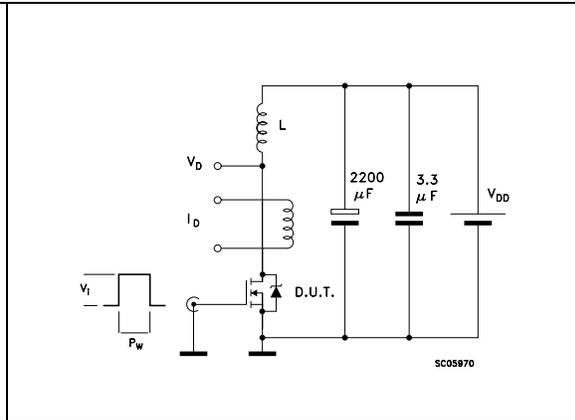


Figure 17. Unclamped inductive waveform

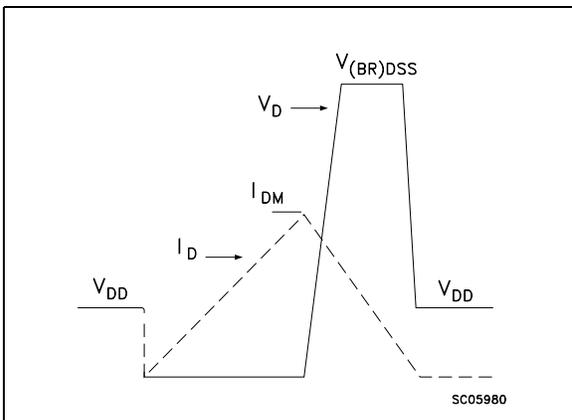
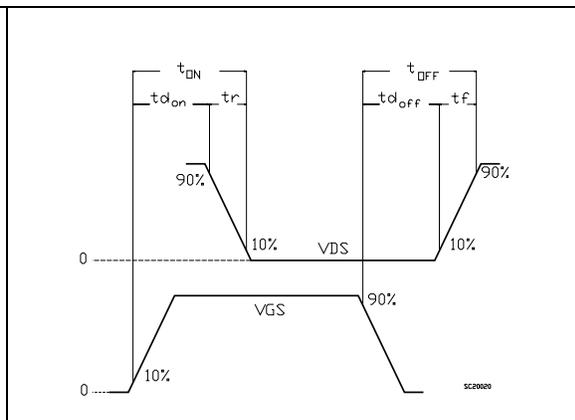


Figure 18. Switching time waveform

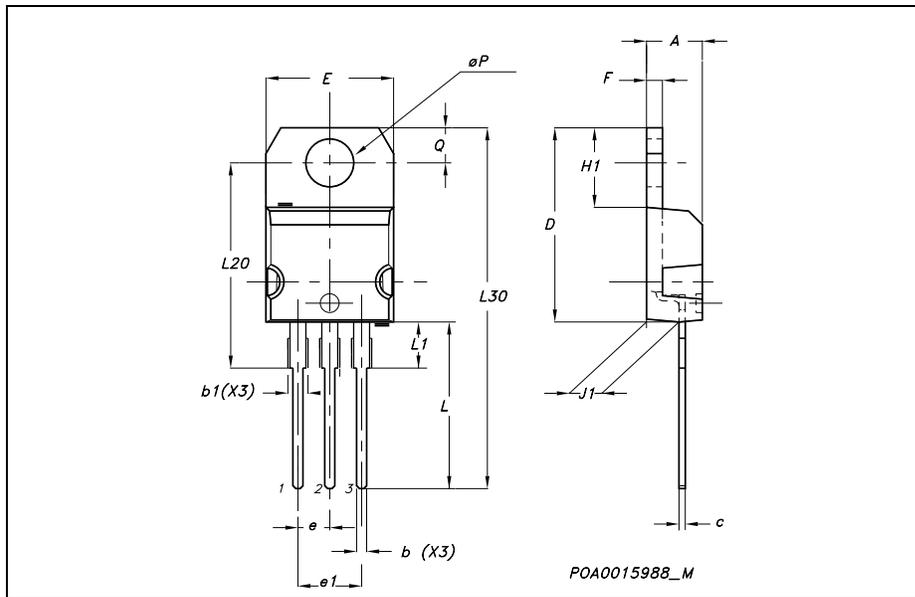


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

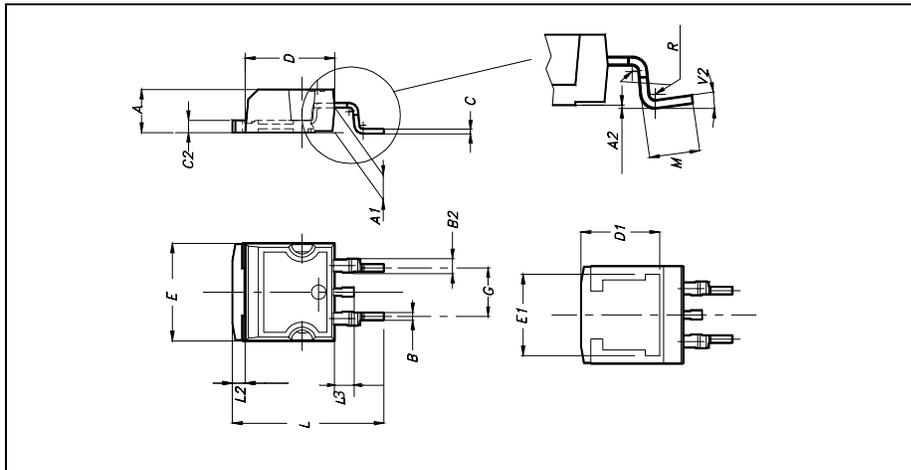
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



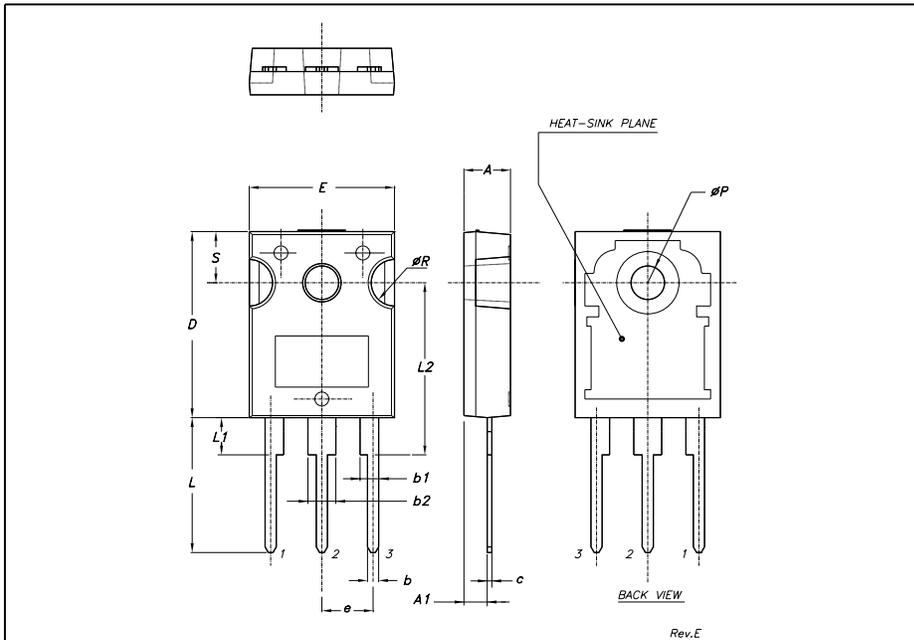
**D<sup>2</sup>PAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



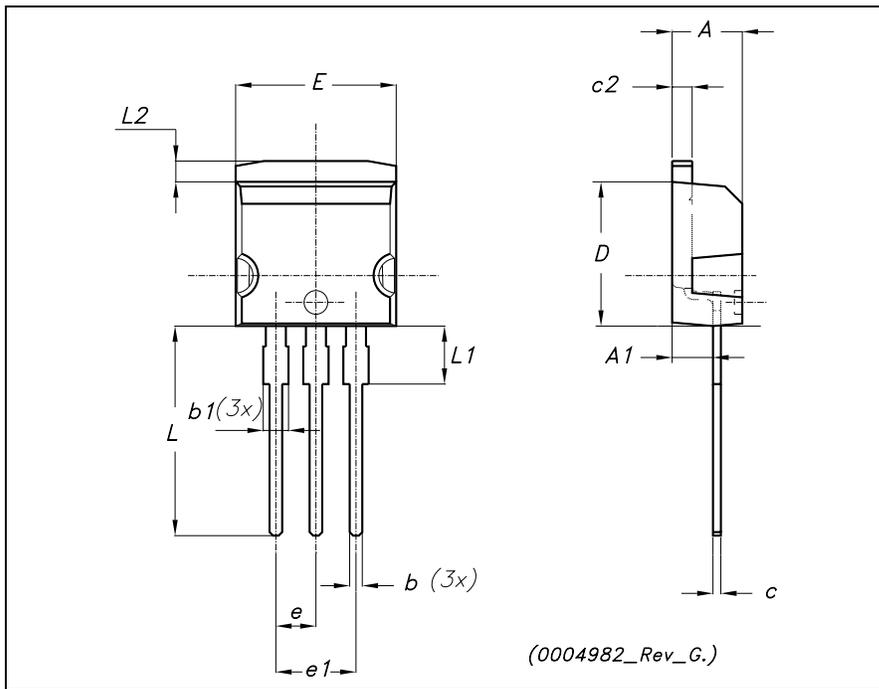
**TO-247 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



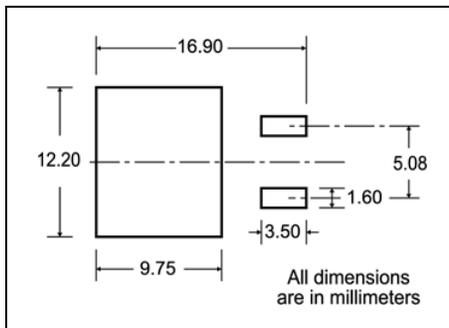
**TO-262 (I<sup>2</sup>PAK) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055

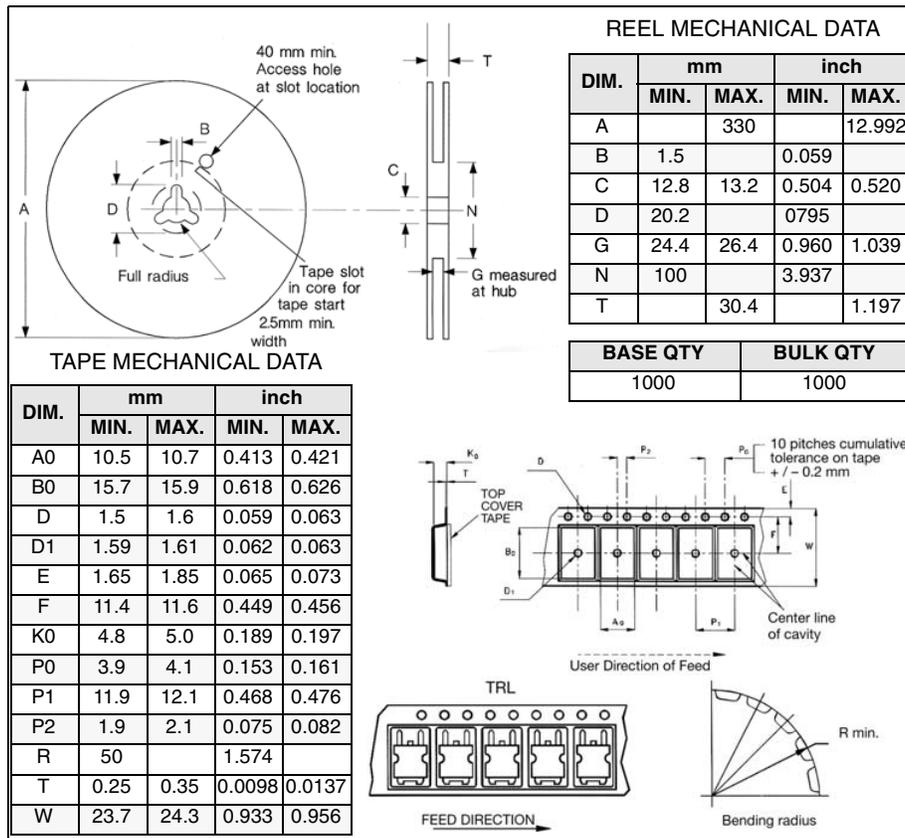


## 5 Packaging mechanical data

### D<sup>2</sup>PAK FOOTPRINT



### TAPE AND REEL SHIPMENT



## 6 Revision history

Table 7. Revision history

Date	Revision	Changes
10-Feb-2005	1	First release.
14-Jan-2006	2	Inserted D <sup>2</sup> PAK, complete version.
03-Oct-2006	3	Inserted I <sup>2</sup> PAK.

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