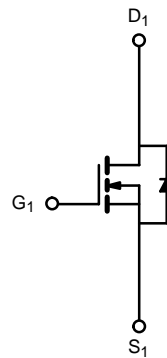
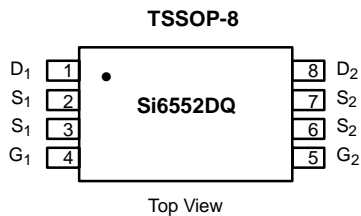
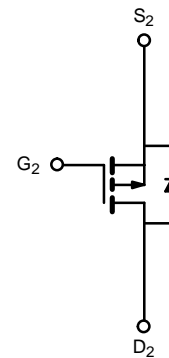


## Dual N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
	$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
N-Channel	20	0.08 @ $V_{GS} = 4.5$ V	$\pm 2.8$
		0.11 @ $V_{GS} = 2.5$ V	$\pm 2.1$
P-Channel	-12	0.1 @ $V_{GS} = -4.5$ V	$\pm 2.5$
		0.18 @ $V_{GS} = -2.5$ V	$\pm 1.9$



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	$V_{DS}$	20	-12	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	$\pm 2.8$	$\pm 2.5$
		$T_A = 70^\circ\text{C}$	$\pm 2.3$	$\pm 2.0$
Pulsed Drain Current	$I_{DM}$	$\pm 20$		A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.0	-1.0	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	1.0	
		$T_A = 70^\circ\text{C}$	0.64	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
<b>Static</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	0.6			V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-0.6			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	N-Ch			1	μA
		V <sub>DS</sub> = -12 V, V <sub>GS</sub> = 0 V	P-Ch			-1	
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	N-Ch			5	
		V <sub>DS</sub> = -12 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	P-Ch			-5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	10			A
		V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -4.5 V	P-Ch	-10			
		V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 2.5 V	N-Ch	4			
		V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -2.5 V	P-Ch	-4			
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.8 A	N-Ch			0.08	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = 2.5 A	P-Ch			0.1	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 2.1 A	N-Ch			0.11	
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = 1.9 A	P-Ch			0.18	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2.8 A	N-Ch		12		S
		V <sub>DS</sub> = -9 V, I <sub>D</sub> = -2.5 A	P-Ch		7		
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.0 A, V <sub>GS</sub> = 0 V	N-Ch			1.2	V
		I <sub>S</sub> = -1.0 A, V <sub>GS</sub> = 0 V	P-Ch			-1.2	
<b>Dynamic<sup>b</sup></b>							
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.8 A P-Channel V <sub>DS</sub> = -6 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.5 A	N-Ch		16	40	nC
Gate-Source Charge	Q <sub>gs</sub>		N-Ch		3		
Gate-Drain Charge	Q <sub>gd</sub>		P-Ch		2		
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 4.5 V, R <sub>G</sub> = 6 Ω P-Channel V <sub>DD</sub> = -6 V, R <sub>L</sub> = 6 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -4.5 V, R <sub>G</sub> = 6 Ω	N-Ch		37	60	ns
			P-Ch		21	40	
Rise Time	t <sub>r</sub>		N-Ch		66	100	
			P-Ch		35	70	
Turn-Off Delay Time	t <sub>d(off)</sub>		N-Ch		56	100	
			P-Ch		43	80	
Fall Time	t <sub>f</sub>		N-Ch		57	100	
			P-Ch		22	40	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	N-Channel—I <sub>F</sub> = 1.0 A, di/dt = 100 A/μs	N-Ch		26	70	
		P-Channel—I <sub>F</sub> = -1.0 A, di/dt = 100 A/μs	P-Ch		35	70	

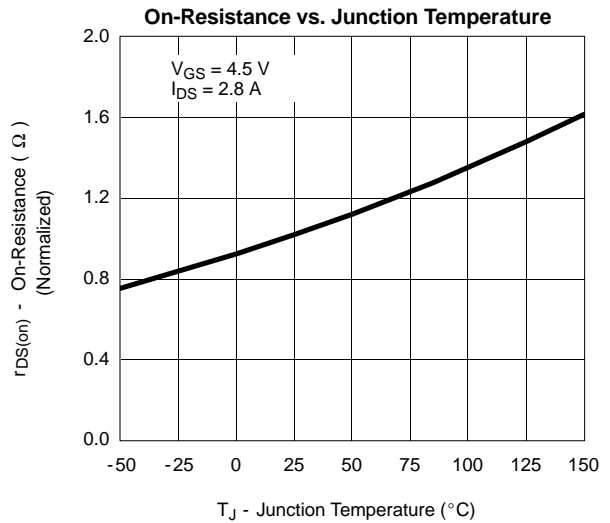
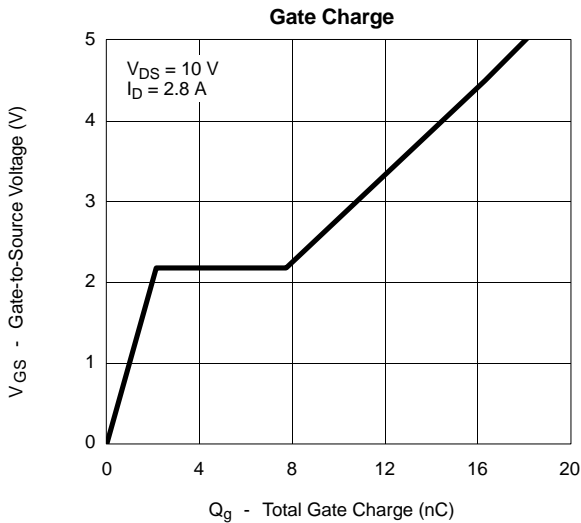
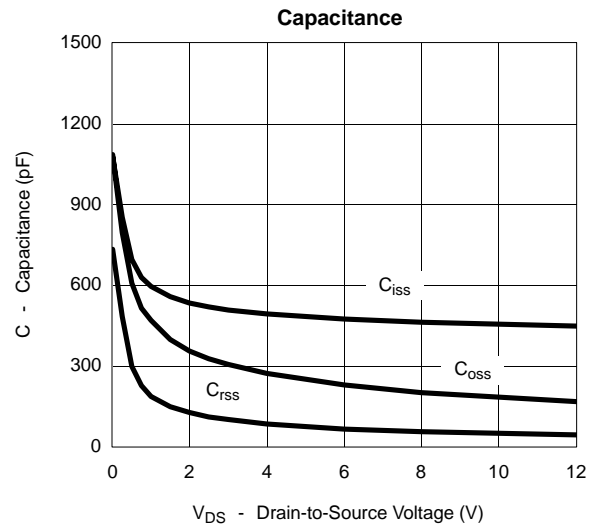
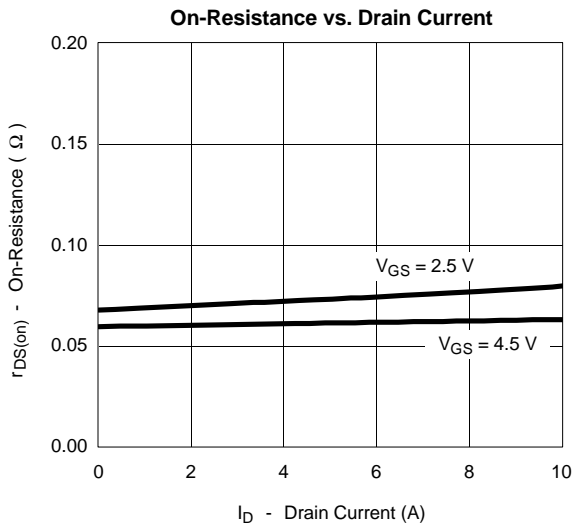
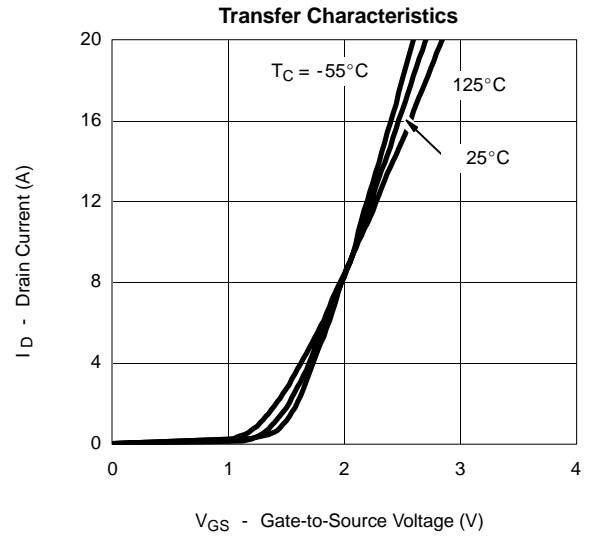
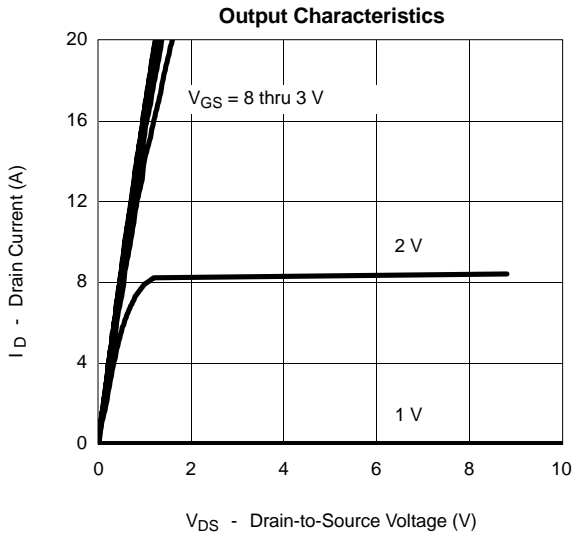
## Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.



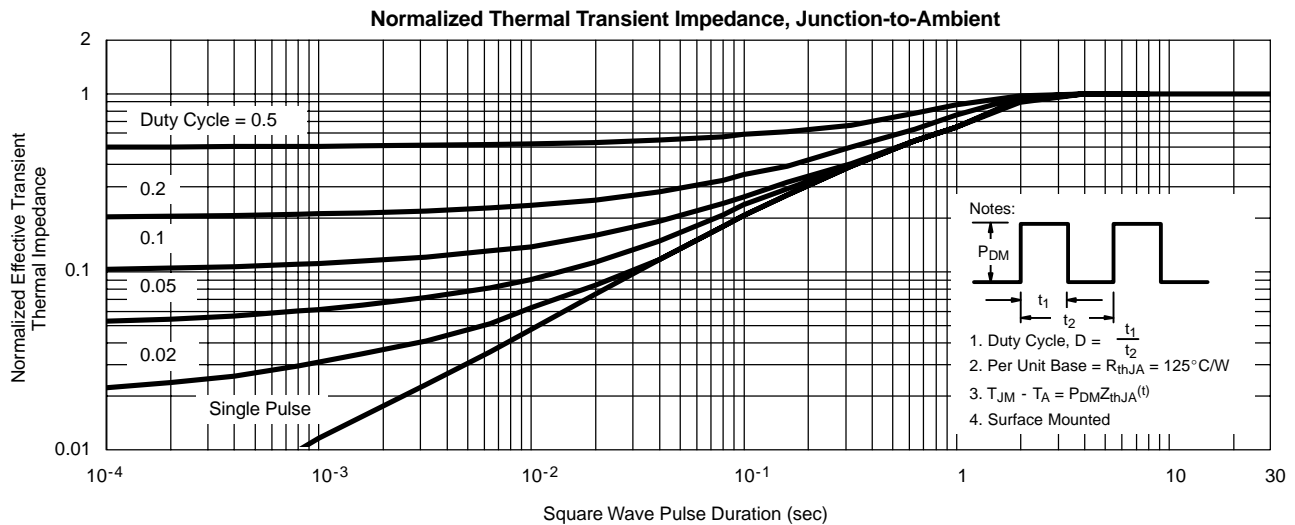
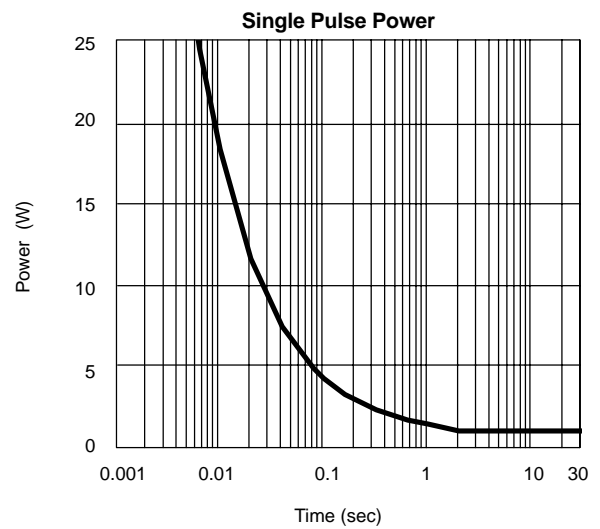
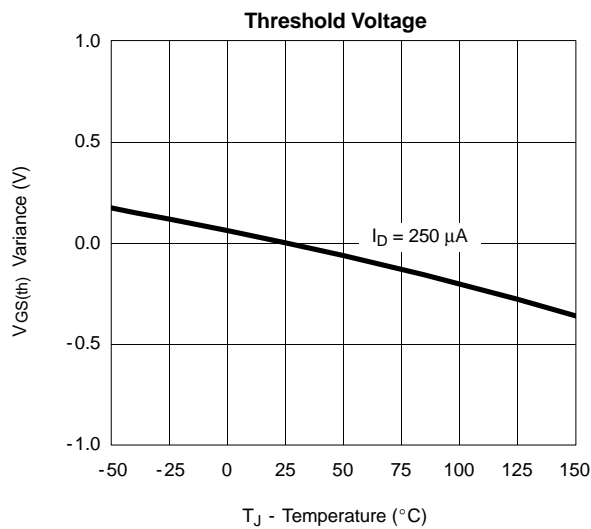
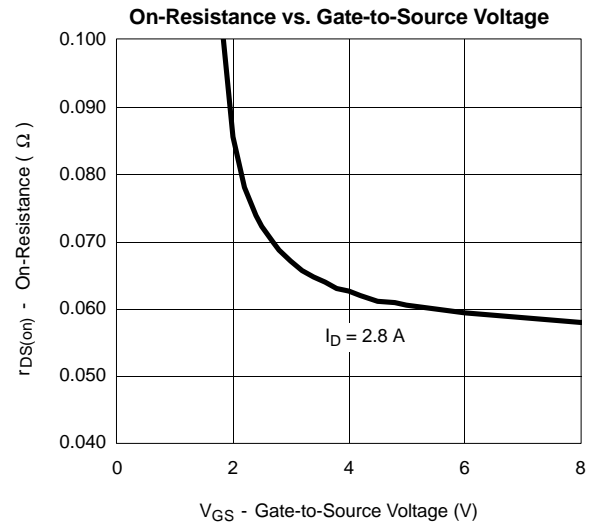
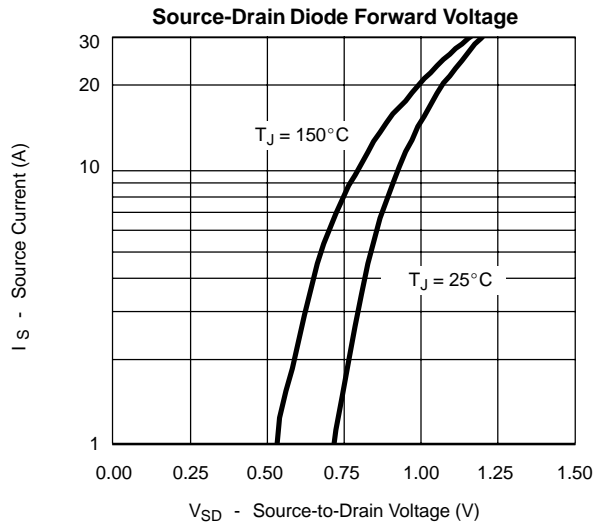
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**N-CHANNEL**



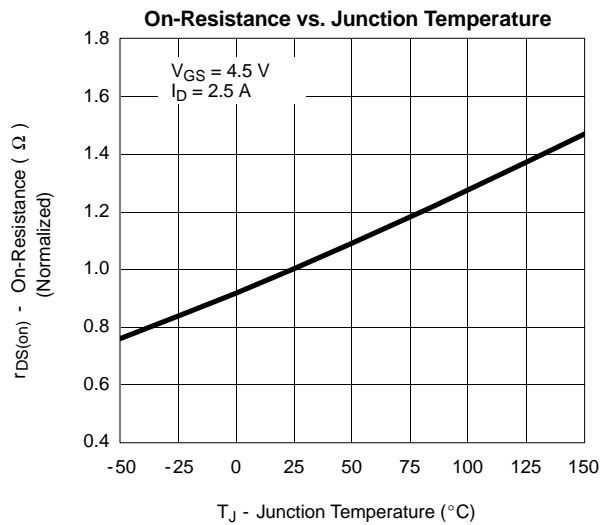
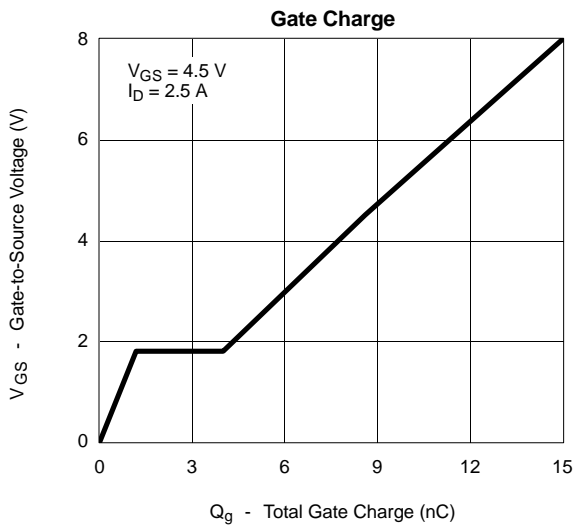
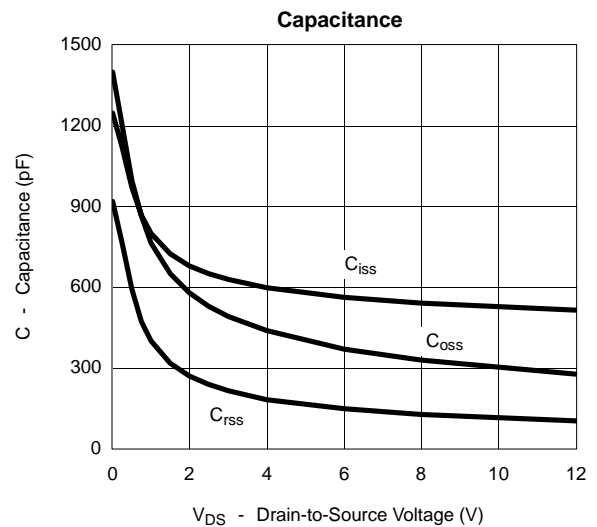
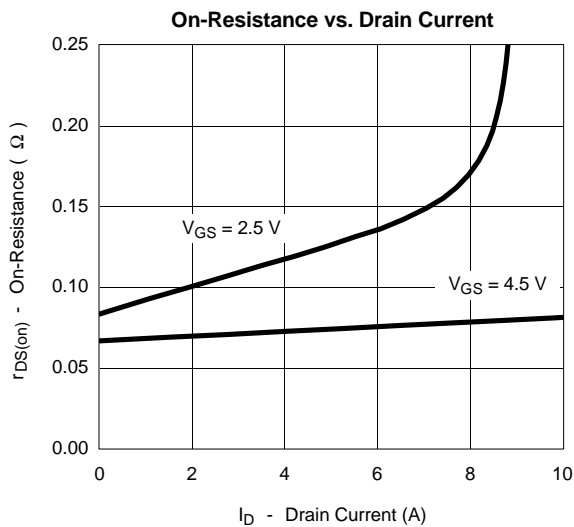
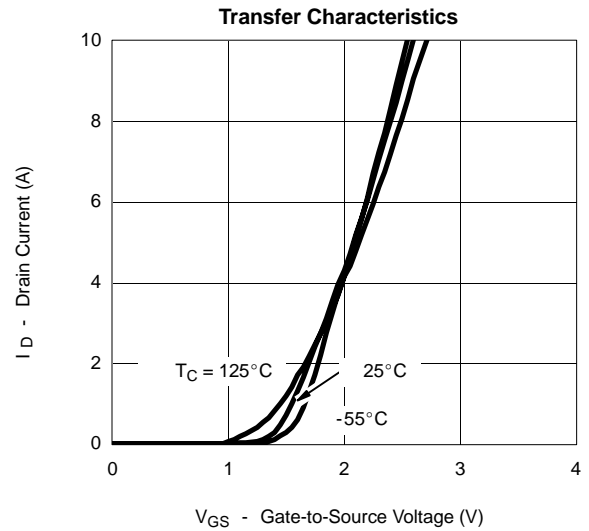
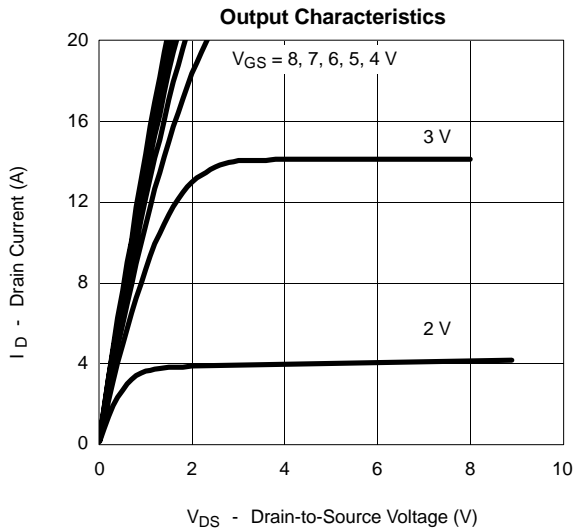
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**N-CHANNEL**



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**P-CHANNEL**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) P-CHANNEL**

