

Dual N-Channel 20-V (D-S) MOSFET

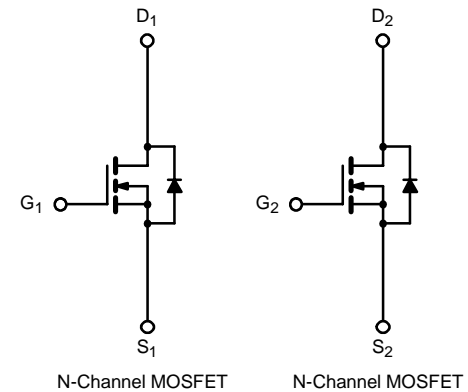
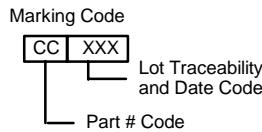
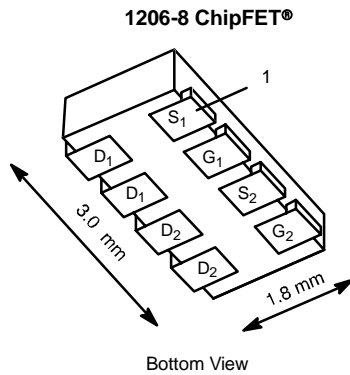
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.040 @ $V_{GS} = 4.5$ V	5.9
	0.045 @ $V_{GS} = 2.5$ V	5.6
	0.052 @ $V_{GS} = 1.8$ V	5.2

FEATURES

- TrenchFET® Power MOSFETS
- Ultra Low $r_{DS(on)}$ and Excellent Power Handling In Compact Footprint

APPLICATIONS

- Load Switch
- PA Switch
- Battery Switch



Ordering Information: Si5908DC-T1—E3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	20		V	
Gate-Source Voltage	V_{GS}	± 8			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	5.9	4.4	A
		$T_A = 85^\circ\text{C}$	4.2	3.1	
Pulsed Drain Current	I_{DM}	20			
Continuous Source Current (Diode Conduction) ^a	I_S	1.8	0.9	W	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.1		1.1
		$T_A = 85^\circ\text{C}$	1.1		0.6
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 5$ sec	50	60	$^\circ\text{C/W}$
		Steady State	90	110	
Maximum Junction-to-Foot (Drain)	R_{thJF}	30	40		

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

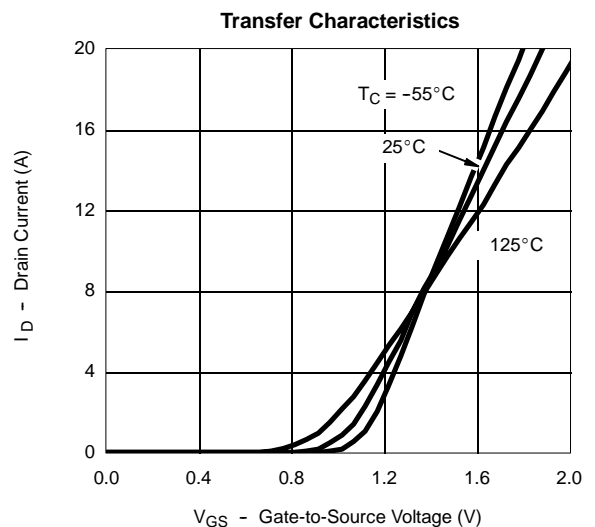
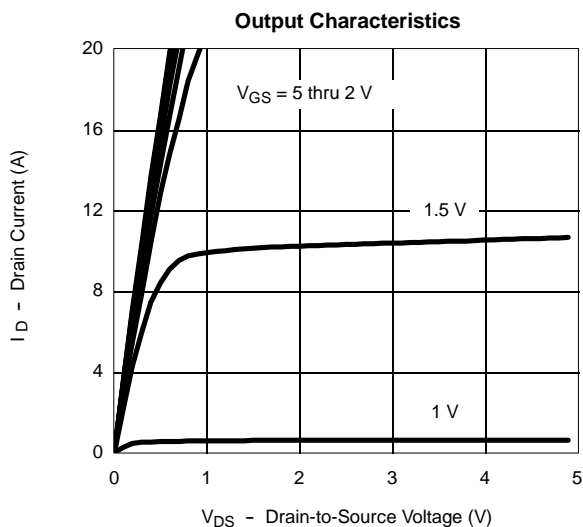


SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.4		1.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 85 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.4 A		0.032	0.040	Ω
		V _{GS} = 2.5 V, I _D = 4.1 A		0.036	0.045	
		V _{GS} = 1.8 V, I _D = 1.9 A		0.042	0.052	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 4.4 A		22		S
Diode Forward Voltage ^a	V _{SD}	I _S = 0.9 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 4.4 A		5	7.5	nC
Gate-Source Charge	Q _{gs}			0.85		
Gate-Drain Charge	Q _{gd}			1		
Gate Resistance	R _g			1.9		Ω
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 6 Ω		20	30	ns
Rise Time	t _r			36	55	
Turn-Off Delay Time	t _{d(off)}			30	45	
Fall Time	t _f			12	20	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 0.9 A, di/dt = 100 A/μs		45	90	

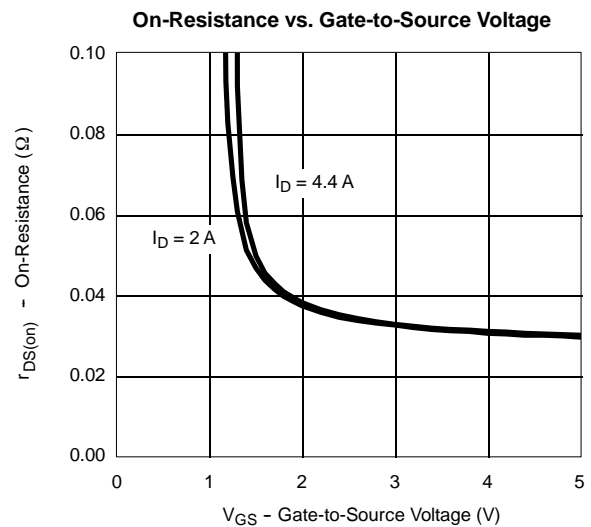
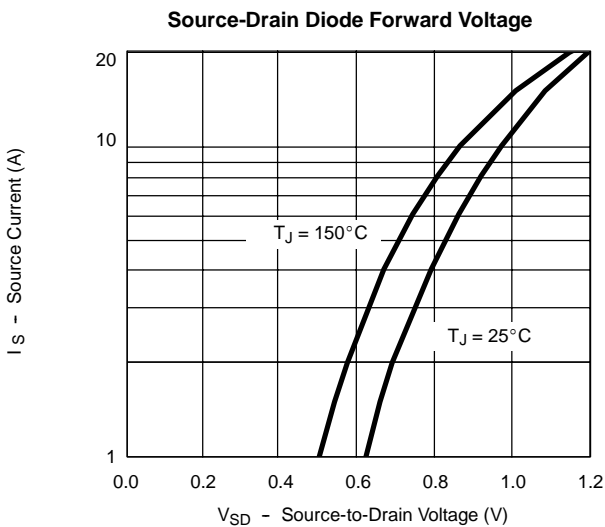
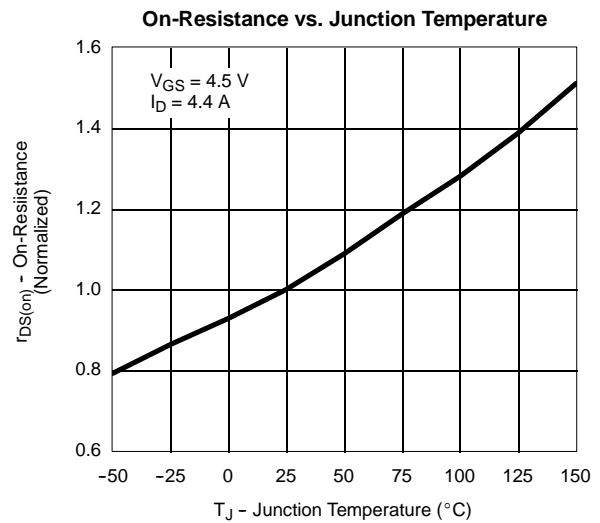
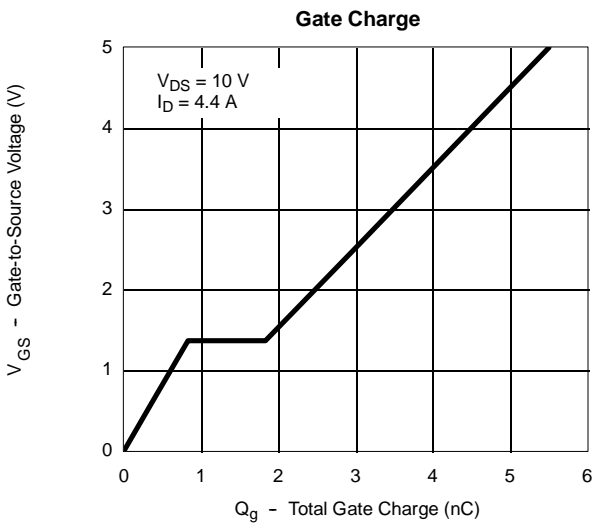
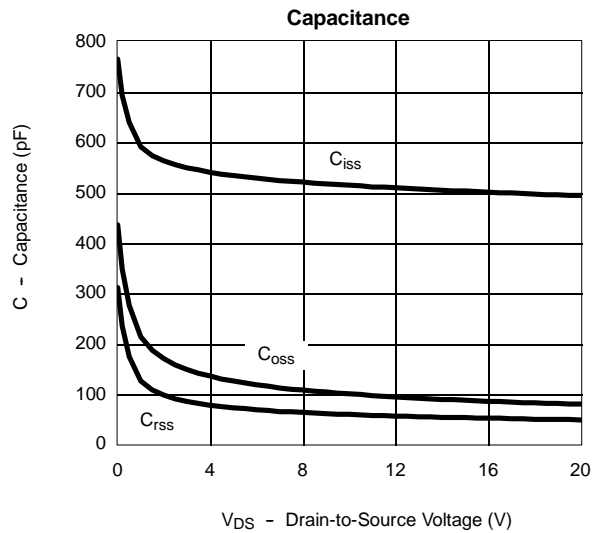
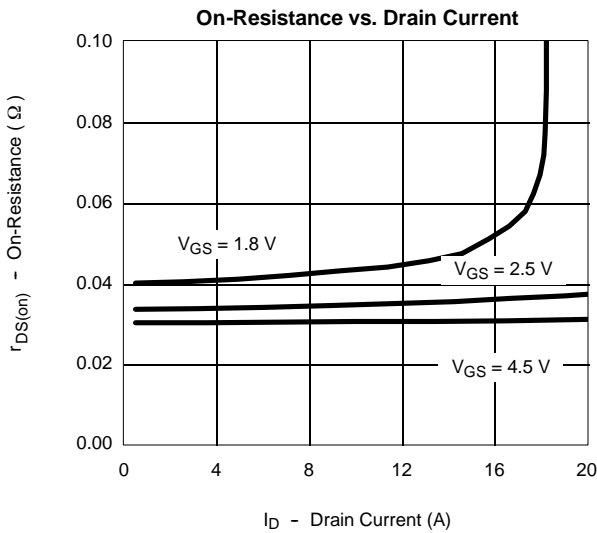
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

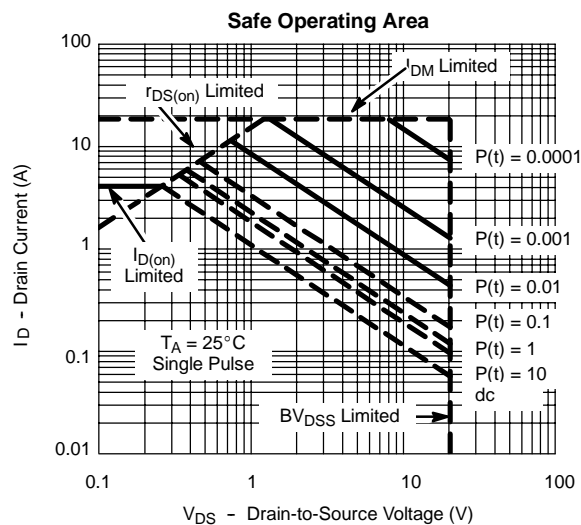
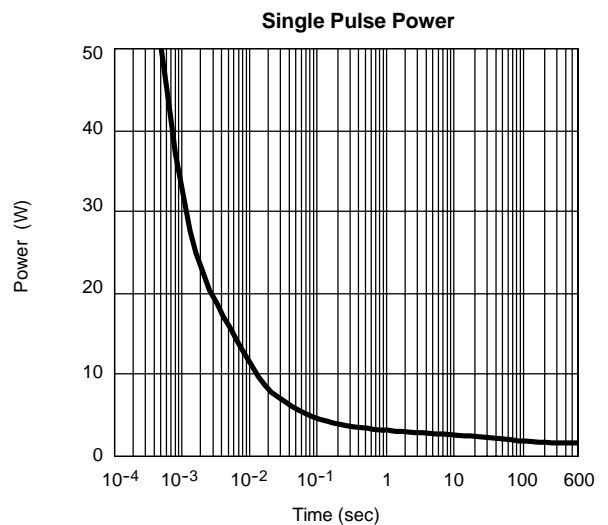
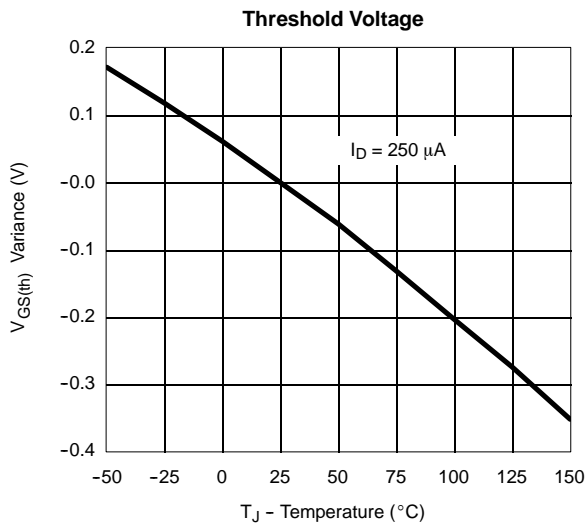


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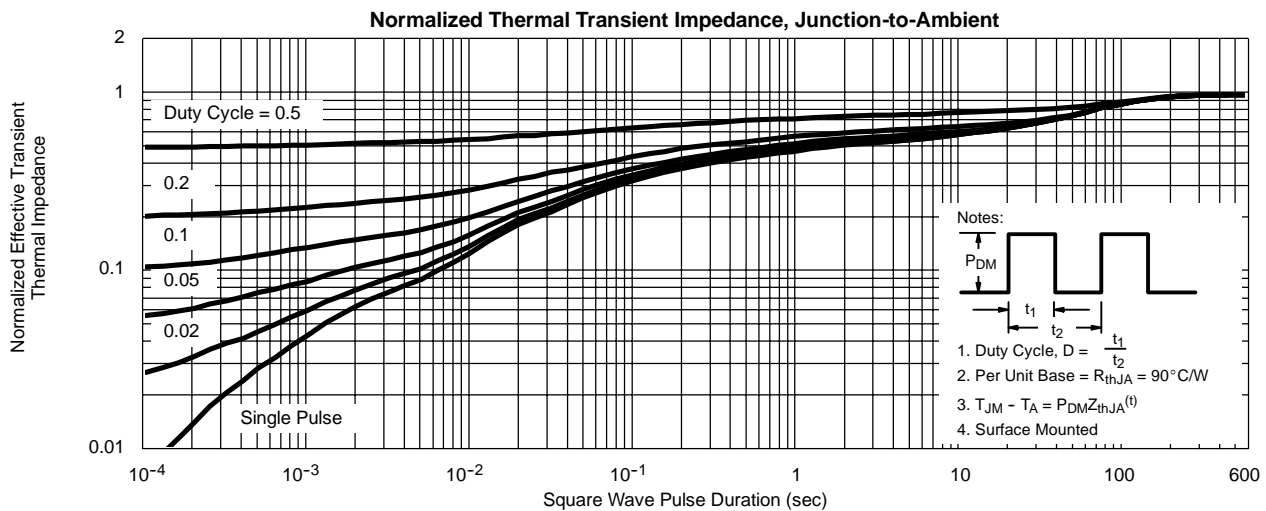




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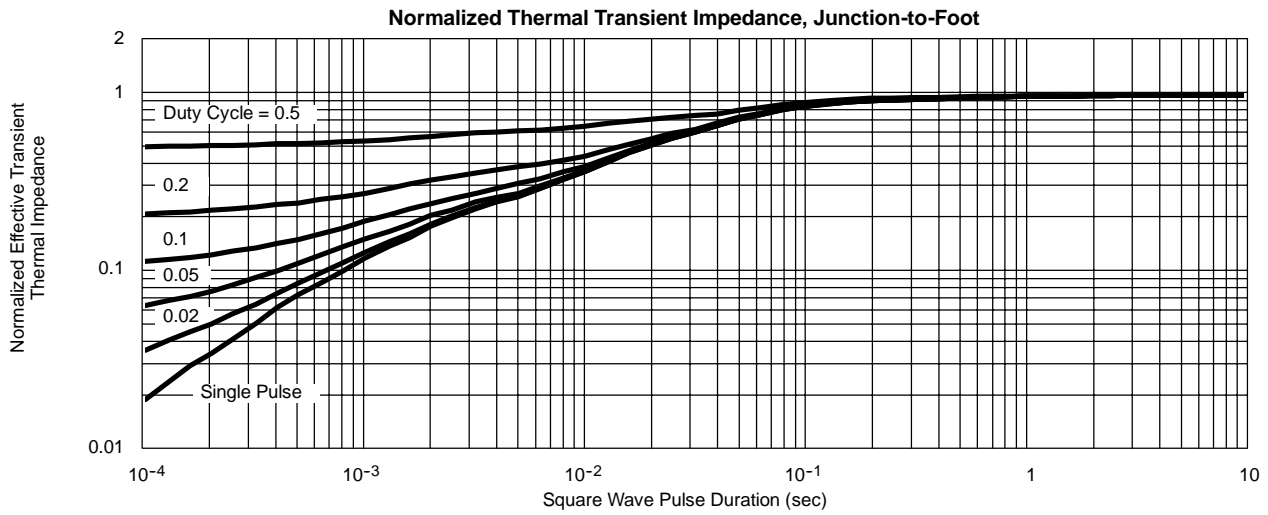


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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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