

MOSMIC[®] for TV-Tuner Prestage with 12 V Supply Voltage

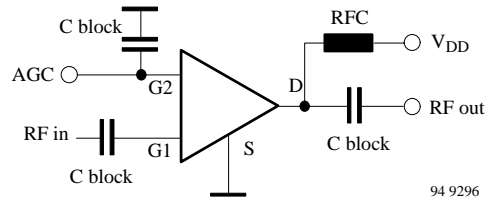
MOSMIC - MOS Monolithic Integrated Circuit

Electrostatic sensitive device.
Observe precautions for handling.



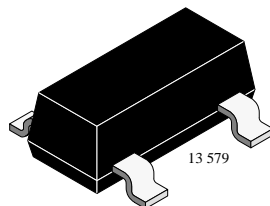
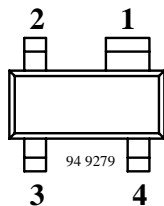
Applications

Low noise gain controlled input stages in UHF-and VHF- tuner with 12 V supply voltage.

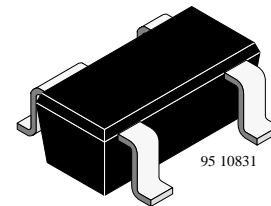
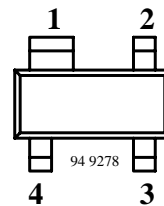


Features

- Integrated gate protection diodes
- Low noise figure
- High gain
- Biasing network on chip
- Improved cross modulation at gain reduction
- High AGC-range
- SMD package



S849T Marking: 849
Plastic case (SOT 143)
1 = Source, 2 = Drain, 3 = Gate 2, 4 = Gate 1



S849TR Marking: 49R
Plastic case (SOT 143R)
1 = Source, 2 = Drain, 3 = Gate 2, 4 = Gate 1

Absolute Maximum Ratings

$T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified

Parameter	Test Conditions	Symbol	Value	Unit
Drain - source voltage		V_{DS}	16	V
Drain current		I_D	30	mA
Gate 1/Gate 2 - source peak current		$\pm I_{G1/G2SM}$	10	mA
Gate 1/Gate 2 - source voltage		$\pm V_{G1/G2SM}$	7.5	V
Total power dissipation	$T_{amb} \leq 60^{\circ}\text{C}$	P_{tot}	200	mW
Channel temperature		T_{Ch}	150	$^{\circ}\text{C}$
Storage temperature range		T_{stg}	-55 to +150	$^{\circ}\text{C}$

Maximum Thermal Resistance

$T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified

Parameter	Test Conditions	Symbol	Value	Unit
Channel ambient	on glass fibre printed board (25 x 20 x 1.5) mm ³ plated with 35 μm Cu	R_{thChA}	450	K/W

Electrical DC Characteristics

$T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Gate 1 - source breakdown voltage	$\pm I_{G1S} = 10 \text{ mA}, V_{G2S} = V_{DS} = 0$	$\pm V_{(BR)G1SS}$	8		12	V
Gate 2 - source breakdown voltage	$\pm I_{G2S} = 10 \text{ mA}, V_{G1S} = V_{DS} = 0$	$\pm V_{(BR)G2SS}$	8		12	V
Gate 1 - source leakage current	$+V_{G1S} = 6 \text{ V}, V_{G2S} = V_{DS} = 0$	$+I_{G1SS}$			60	μA
	$-V_{G1S} = 6 \text{ V}, V_{G2S} = V_{DS} = 0$	$-I_{G1SS}$			120	μA
Gate 2 - source leakage current	$\pm V_{G2S} = 6 \text{ V}, V_{G1S} = V_{DS} = 0$	$\pm I_{G2SS}$			20	nA
Drain current	$V_{DS} = 12 \text{ V}, V_{G1S} = 0, V_{G2S} = 6 \text{ V}$	I_{DSS}	50		500	μA
Self-biased operating current	$V_{DS} = 12 \text{ V}, V_{G1S} = \text{nc}, V_{G2S} = 6 \text{ V}$	I_{DSP}	8	12	16	mA
Gate 2 - source cut-off voltage	$V_{DS} = 12 \text{ V}, V_{G1S} = \text{nc}, I_D = 200 \mu\text{A}$	$V_{G2S(\text{OFF})}$		1.0		V

Electrical AC Characteristics

$V_{DS} = 12 \text{ V}, V_{G2S} = 6 \text{ V}, f = 1 \text{ MHz}, T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Forward transadmittance		$ y_{21s} $	20	24	28	mS
Gate 1 input capacitance		C_{issg1}		2.1	2.5	pF
Feedback capacitance		C_{rss}		20		fF
Output capacitance		C_{oss}		0.9		pF
Power gain	$G_S = 2 \text{ mS}, G_L = 0.5 \text{ mS}, f = 200 \text{ MHz}$	G_{ps}		26		dB
	$G_S = 3,3 \text{ mS}, G_L = 1 \text{ mS}, f = 800 \text{ MHz}$	G_{ps}	16.5	20		dB
AGC range	$V_{DS} = 12 \text{ V}, V_{G2S} = 1 \text{ to } 6 \text{ V}, f = 800 \text{ MHz}$	ΔG_{ps}	40			dB
Noise figure	$G_S = 2 \text{ mS}, G_L = 0.5 \text{ mS}, f = 200 \text{ MHz}$	F		1		dB
	$G_S = 3,3 \text{ mS}, G_L = 1 \text{ mS}, f = 800 \text{ MHz}$	F		1.3		dB

Caution for Gate 1 switch-off mode:

No external DC-voltage on Gate 1 in active mode!

Switch-off at Gate 1 with $V_{G1S} < 0.7 \text{ V}$ is feasible.

Using open collector switching transistor (inside of PLL), insert 10 k Ω collector resistor.



Common Source S-Parameters

$V_{DS} = 12\text{ V}$, $V_{G2S} = 6\text{ V}$, $Z_0 = 50\ \Omega$, $T_{amb} = 25^\circ\text{C}$, unless otherwise specified

f/MHz	S11		S21		S12		S22	
	LOG MAG	ANG	LOG MAG	ANG	LOG MAG	ANG	LOG MAG	ANG
	dB	deg	dB	deg	dB	deg	dB	deg
50	-0.01	-3.9	7.46	175.0	-61.64	87.7	-0.17	-1.7
100	-0.04	-7.6	7.37	169.3	-55.58	85.2	-0.20	-3.3
150	-0.11	-11.5	7.30	163.4	-52.05	82.0	-0.22	-5.0
200	-0.16	-15.1	7.21	157.8	-49.78	79.5	-0.25	-6.6
250	-0.28	-19.1	7.09	151.8	-48.15	76.4	-0.26	-8.4
300	-0.39	-22.4	6.98	146.8	-46.79	75.0	-0.31	-9.8
350	-0.51	-26.0	6.79	141.2	-45.92	72.6	-0.34	-11.3
400	-0.65	-29.4	6.66	136.0	-45.15	70.9	-0.38	-12.8
450	-0.79	-32.7	6.47	131.0	-44.66	69.5	-0.44	-14.3
500	-0.95	-35.8	6.29	125.8	-44.28	67.8	-0.48	-15.9
550	-1.09	-39.0	6.13	121.0	-44.13	67.3	-0.53	-17.4
600	-1.26	-42.2	5.91	116.0	-44.04	68.0	-0.59	-18.8
650	-1.41	-45.1	5.76	111.8	-43.84	68.6	-0.63	-20.2
700	-1.56	-48.3	5.55	106.9	-43.97	69.2	-0.65	-21.6
750	-1.71	-50.9	5.40	102.6	-44.18	70.4	-0.72	-23.1
800	-1.89	-53.6	5.22	98.0	-44.54	73.2	-0.76	-24.4
850	-2.02	-56.7	5.08	93.8	-44.81	77.0	-0.80	-25.9
900	-2.15	-59.5	4.89	89.4	-45.03	83.4	-0.85	-27.6
950	-2.28	-62.3	4.75	85.2	-44.87	90.8	-0.90	-29.0
1000	-2.45	-65.1	4.55	80.9	-44.59	95.7	-0.96	-30.2
1050	-2.59	-67.8	4.38	76.2	-44.59	100.2	-1.07	-31.6
1100	-2.75	-70.5	4.20	72.2	-44.54	108.4	-1.11	-33.0
1150	-2.81	-73.3	4.14	67.9	-44.05	116.7	-1.13	-34.7
1200	-2.96	-75.7	4.02	64.3	-43.33	125.5	-1.15	-36.2
1250	-3.07	-78.7	3.90	60.1	-42.41	133.5	-1.18	-37.6
1300	-3.18	-81.4	3.73	55.6	-41.13	139.3	-1.26	-39.1

Typical Characteristics ($T_{amb} = 25^{\circ}C$ unless otherwise specified)

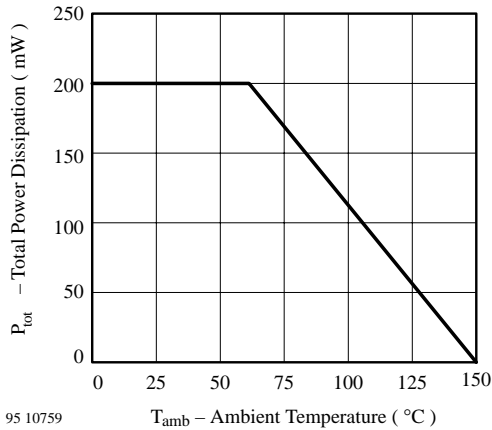


Figure 1. Total Power Dissipation vs. Ambient Temperature

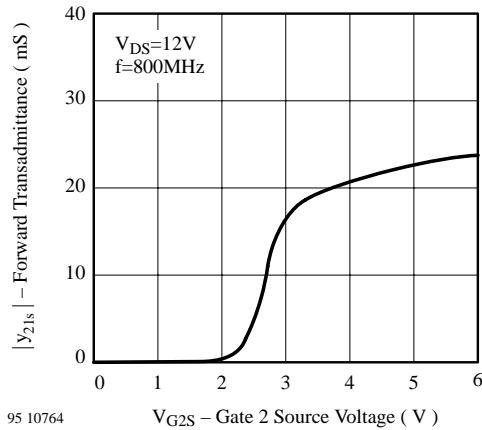


Figure 4. Forward Transadmittance vs. Gate 2 Source Voltage

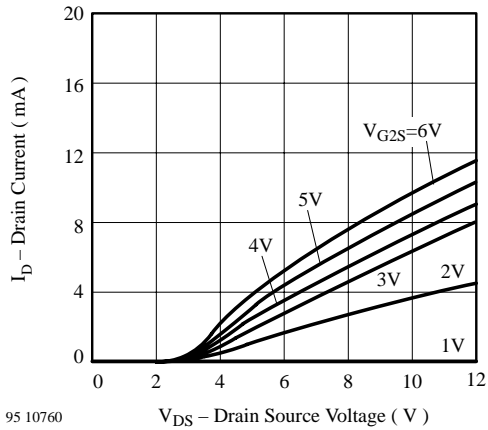


Figure 2. Drain Current vs. Drain Source Voltage

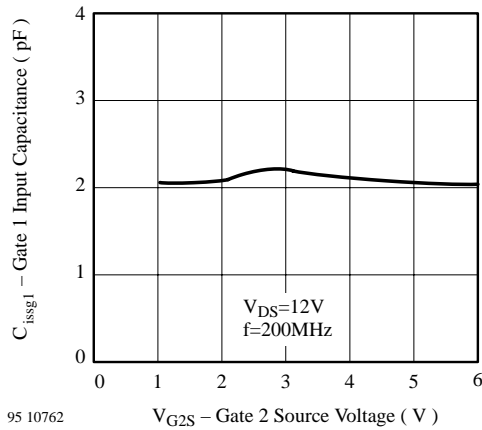


Figure 5. Gate 1 Input Capacitance vs. Gate 2 Source Voltage

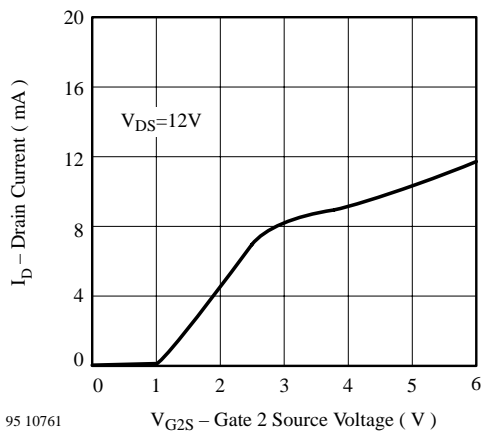


Figure 3. Drain Current vs. Gate 2 Source Voltage

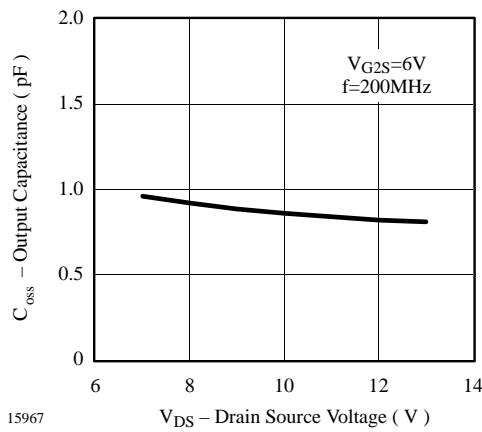


Figure 6. Output Capacitance vs. Drain Source Voltage

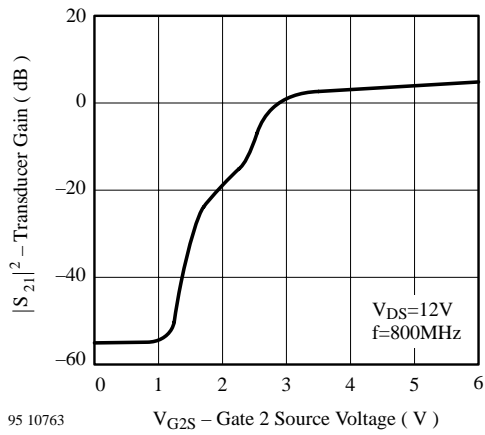


Figure 7. Transducer Gain vs. Gate 2 Source Voltage

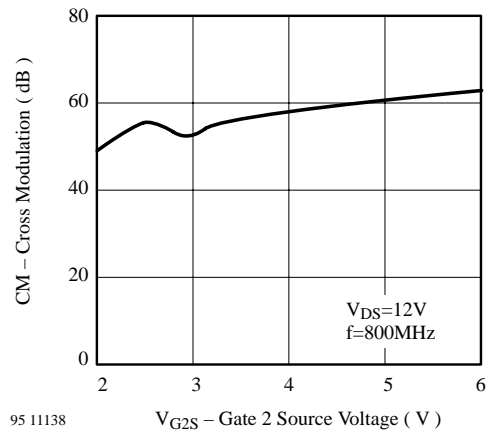


Figure 8. Cross Modulation vs. Gate 2 Source Voltage

S849T/S849TR

Vishay Semiconductors



$V_{DS} = 8 \text{ V}$, $I_D = 10 \text{ mA}$, $V_{G2S} = 4 \text{ V}$, $Z_0 = 50 \Omega$

S_{11}

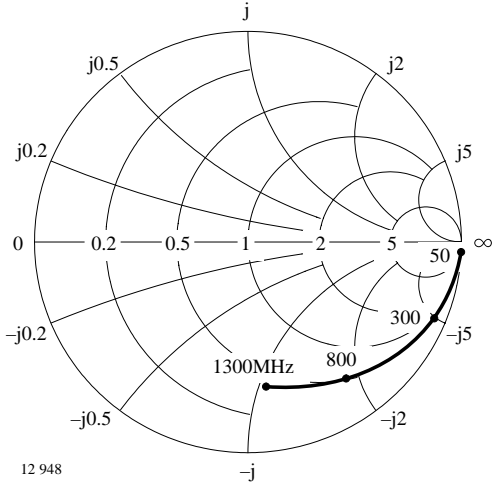


Figure 9. Input reflection coefficient

S_{12}

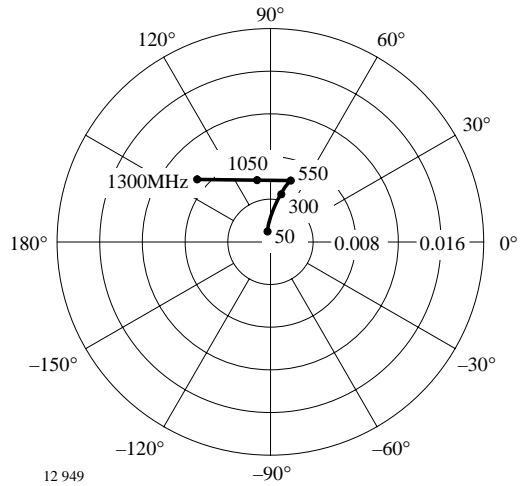


Figure 11. Reverse transmission coefficient

S_{21}

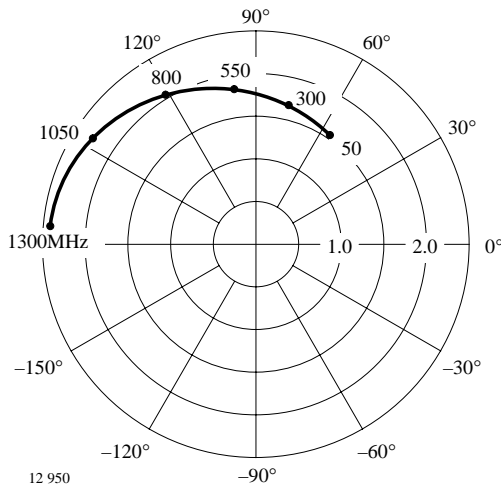


Figure 10. Forward transmission coefficient

S_{22}

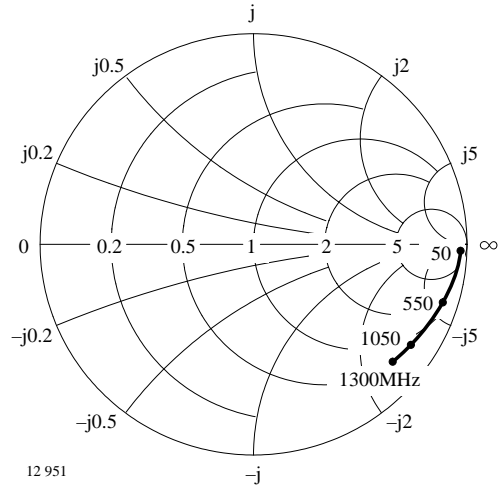
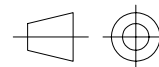
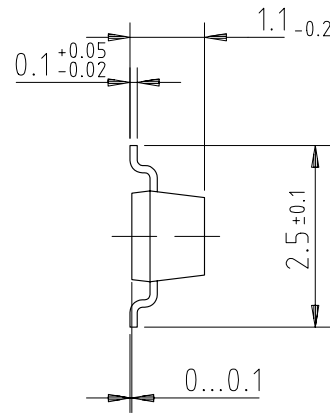
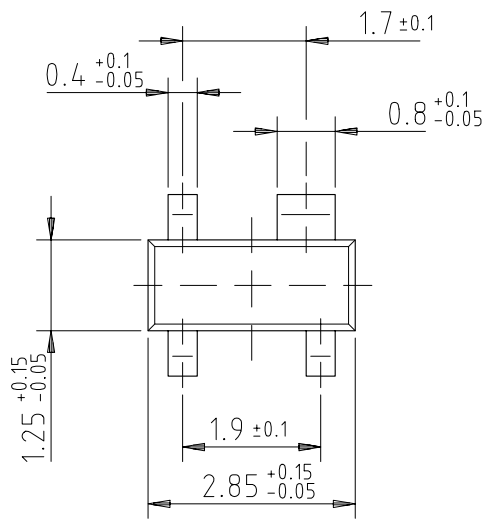


Figure 12. Output reflection coefficient

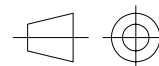
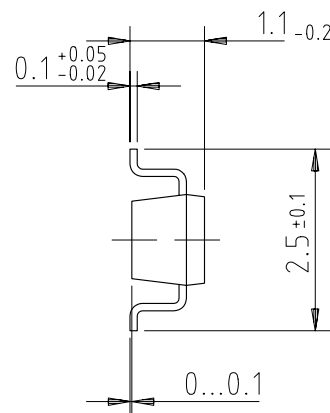
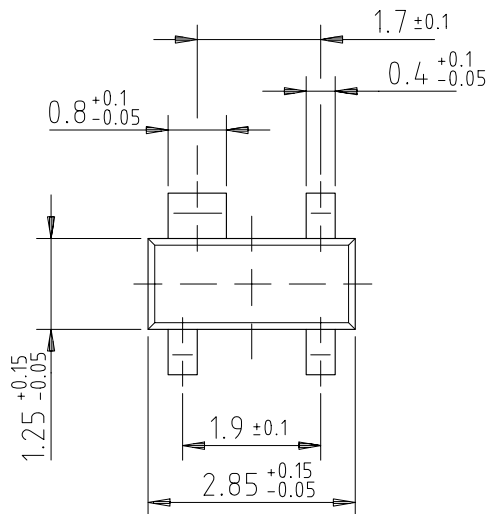
Dimensions of S849T in mm



96 12240

technical drawings
according to DIN
specifications

Dimensions of S849TR in mm



96 12239

technical drawings
according to DIN
specifications



Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Vishay-Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify Vishay-Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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