FEATURES

16M-BIT [x 1 / x 2] CMOS SERIAL FLASH
32M-BIT [x 1 / x 2] CMOS SERIAL FLASH
64M-BIT [x 1 / x 2] CMOS SERIAL FLASH

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 16M:16,777,216 x 1 bit structure or 8,388,608 x 2 bits (two I/O read mode) structure
  32M:33,554,432 x 1 bit structure or 16,772,216 x 2 bits (two I/O read mode) structure
  64M:67,108,864 x 1 bit structure or 33,554,432 x 2 bits (two I/O read mode) structure
- 512 Equal Sectors with 4K byte each (16Mb)
  1024 Equal Sectors with 4K byte each (32Mb)
  2048 Equal Sectors with 4K byte each (64Mb)
  - Any Sector can be erased individually
- 32 Equal Blocks with 64K byte each (16Mb)
  64 Equal Blocks with 64K byte each (32Mb)
  128 Equal Blocks with 64K byte each (64Mb)
  - Any Block can be erased individually
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V

PERFORMANCE

- High Performance
  - Fast access time: 86MHz serial clock (15pF + 1TTL Load) and 66MHz serial clock (30pF + 1TTL Load)
  - Serial clock of two I/O read mode : 50MHz (15pF + TTL Load), which is equivalent to 100MHz
  - Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
  - Byte program time: 9us (typical)
  - Continuously program mode (automatically increase address under word program mode)
  - Fast erase time: 60ms(typ.) /sector (4K-byte per sector) ; 0.7s(typ.) /block (64K-byte per block); 14s(typ.) /chip for 16Mb, 25s(typ.) for 32Mb, and 50s(typ.) for 64Mb
- Low Power Consumption
  - Low active read current: 25mA(max.) at 86MHz, 20mA(max.) at 66MHz and 10mA(max.) at 33MHz
  - Low active programming current: 20mA (max.)
  - Low active erase current: 20mA (max.)
  - Low standby current: 20uA (max.)
  - Deep power-down mode 1uA (typical)
- Typical 100,000 erase/program cycles

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
    The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 512-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)

- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - Both REMS and REMS2 commands for 1-byte manufacturer ID and 1-byte device ID

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI Input
  - Serial Data Input
- SO Output
  - Serial Data Output
- WP#/ACC pin
  - Hardware write protection and program/erase acceleration
- HOLD# pin
  - pause the chip without diselecting the chip
- PACKAGE
  - 16-pin SOP (300mil)
  - 8-land WSON (8x6mm or 6x5mm)
  - 8-pin SOP (200mil, 150mil)
  - 8-pin PDIP (300mil)
  - 8-land USON (4x4mm)
  - **All Pb-free devices are RoHS Compliant**

ALTERNATIVE

- Security Serial Flash (MX25L1615D/MX25L3215D/MX25L6415D) may provides additional protection features for option. The datasheet is provided under NDA.

GENERAL DESCRIPTION

The MX25L1605D are 16,777,216 bit serial Flash memory, which is configured as 2,097,152 x 8 internally. When it is in two I/O read mode, the structure becomes 8,388,608 bits x 2. The MX25L3205D are 33,554,432 bit serial Flash memory, which is configured as 4,194,304 x 8 internally. When it is in two I/O read mode, the structure becomes 16,772,216 bits x 2. The MX25L6405D are 67,108,864 bit serial Flash memory, which is configured as 8,388,608 x 8 internally. When it is in two I/O read mode, the structure becomes 33,554,432 bits x 2. (please refer to the "Two I/O Read mode" section). The MX25L1605D/3205D/6405D feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output.

The MX25L1605D/3205D/6405D provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for Continuously program mode, and erase command is executes on sector (4K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 20uA DC current.

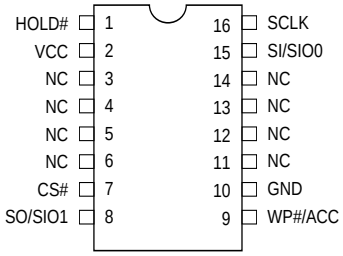
The MX25L1605D/3205D/6405D utilizes MXIC's proprietary memory cell, which reliably stores memory contents even after typical 100,000 program and erase cycles.

Table 1. Additional Feature Comparison

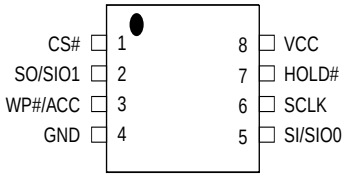
Additional Features / Part Name	Protection and Security		Read Performance	Identifier			
	Flexible Block protection (BP0-BP3)	512-bit secured OTP	2 I/O Read (50MHz)	Device ID (command : AB hex)	Device ID (command : 90 hex)	Device ID (command : EF hex)	RDID (command: 9F hex)
MX25L1605D	V	V	V	14 (hex)	C2 14 (hex) (if ADD=0)	C2 14 (hex) (if ADD=0)	C2 20 15 (hex)
MX25L3205D	V	V	V	15 (hex)	C2 15 (hex) (if ADD=0)	C2 15 (hex) (if ADD=0)	C2 20 16 (hex)
MX25L6405D	V	V	V	16 (hex)	C2 16 (hex) (if ADD=0)	C2 16 (hex) (if ADD=0)	C2 20 17 (hex)

PIN CONFIGURATIONS

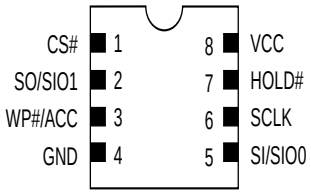
16-PIN SOP (300mil)



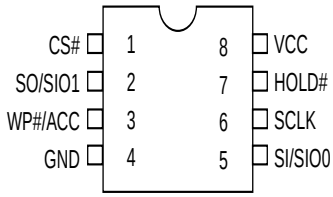
8-PIN SOP (200mil, 150mil)



8-LAND WSON (8x6mm, 6x5mm), USON (4x4mm)



8-PIN PDIP (300mil)



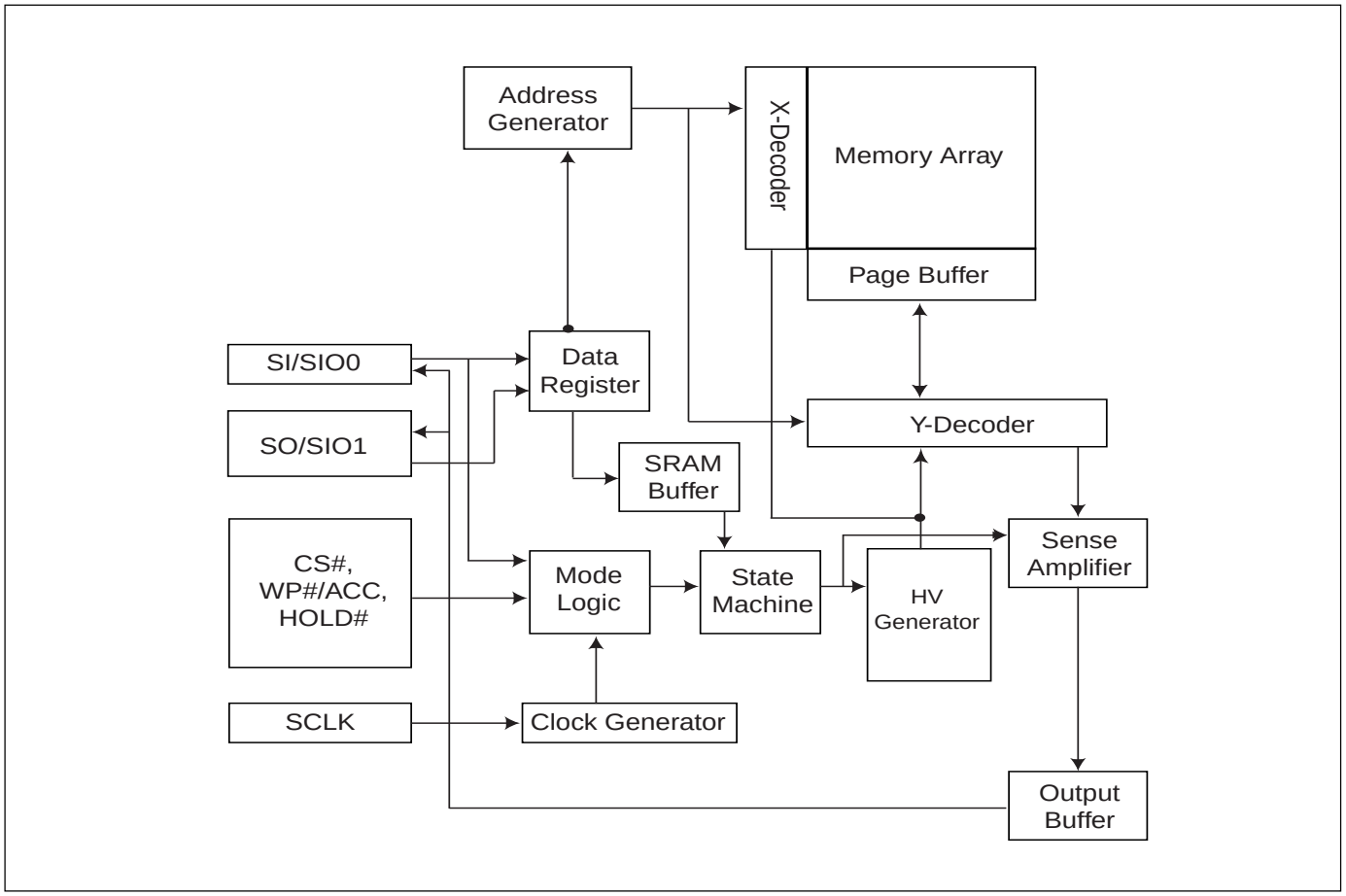
PACKAGE OPTIONS

	16M	32M	64M
150mil 8-SOP	V		
200mil 8-SOP	V	V	
300mil 16-SOP	V	V	V
300mil 8-PDIP	V	V	
6x5mm WSON	V	V	
8x6mm WSON			V
4x4mm USON	V	V	

PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O read mode)
SCLK	Clock Input
WP#/ACC	Write protection: connect to GND ; 9.5~10.5V for program/erase acceleration: connect to 9.5~10.5V
HOLD#	Hold, to pause the device without deselecting the device
VCC	+ 3.3V Power Supply
GND	Ground

BLOCK DIAGRAM



DATA PROTECTION

The MX25L1605D/3205D/6405D is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Power-on reset and tPUW: to avoid sudden power switch by system power supply transition, the power-on reset and tPUW (internal timer) may protect the Flash.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Continuously Program mode (CP) instruction completion
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion
  - Write Read-lock Bit (WRLB) instruction completion

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).

- Advanced Security Features: there are some protection and securuity features which protect content from inadvertent write and hostile access.

  I. Block lock protection

  - The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The proected area definition is shown as table of "Protected Area Sizes", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
  Please refer to table of "protected area sizes".
  - The Hardware Proteced Mode (HPM) use WP#/ACC to protect the (BP3, BP2, BP1, BP0) bits and SRWD bit.

Table 2. Protected Area Sizes

Status bit				Protect Level		
BP3	BP2	BP1	BP0	16Mb	32Mb	64Mb
0	0	0	0	0(none)	0(none)	0(none)
0	0	0	1	1(1block, block 31th)	1(1block, block 63th)	1(2blocks, block 126th-127th)
0	0	1	0	2(2blocks, block 30th-31th)	2(2blocks, block 62th-63th)	2(4blocks, block 124th-127th)
0	0	1	1	3(4blocks, block 28th-31th)	3(4blocks, block 60th-63th)	3(8blocks, block 120th-127th)
0	1	0	0	4(8blocks, block 24th-31th)	4(8blocks, block 56th-63th)	4(16blocks, block 112th-127th)
0	1	0	1	5(16blocks, block 16th-31th)	5(16blocks, block 48th-63th)	5(32blocks, block 96th-127th)
0	1	1	0	6(32blocks, all)	6(32blocks, block 32th-63th)	6(64blocks,block 64th-127th)
0	1	1	1	7(32blocks, all)	7(64blocks, all)	7(128blocks, all)
1	0	0	0	8(32blocks, all)	8(64blocks, all)	8(128blocks, all)
1	0	0	1	9(32blocks, all)	9(32blocks, block 0th-31th)	9(64blocks, block 0th-63th)
1	0	1	0	10(16blocks, block 0th-15th)	10(48blocks, block 0th-47th)	10(96blocks, block 0th-95th)
1	0	1	1	11(24blocks, block 0th-23th)	11(56blocks, block 0th-55th)	11(112blocks, block 0th-111th)
1	1	0	0	12(28blocks, block 0th-27th)	12(60blocks, block 0th-59th)	12(120blocks, block 0th-119th)
1	1	0	1	13(30blocks, block 0th-29th)	13(62blocks, block 0th-61th)	13(124blocks, block 0th-123th)
1	1	1	0	14(31blocks, block 0th-30th)	14(63blocks, block 0th-62th)	14(126blocks, block 0th-125th)
1	1	1	1	15(32blocks, all)	15(64blocks, all)	15(128blocks, all)

II. Additional 512-bit secured OTP for unique identifier: to provide 512-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to table 3. 512-bit secured OTP definition.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 512-bit secured OTP by entering 512-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 512-bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of "security register definition" for security register bit definition and table of "512-bit secured OTP definition" for address range definition.
- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 512-bit secured OTP mode, array access is not allowed.

Table 3. 512-bit Secured OTP Definition

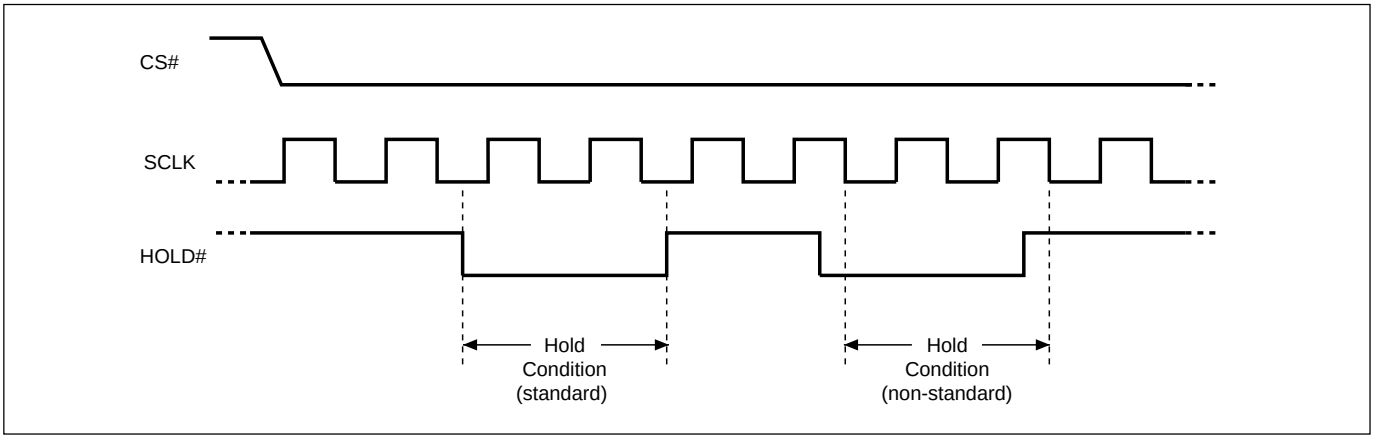
Address range	Size	Standard Factory Lock	Customer Lock
xxxx00~xxxx0F	128-bit	ESN (electrical serial number)	Determined by customer
xxxx10~xxxx3F	384-bit	N/A	

HOLD FEATURES

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select(CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low(if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), see Figure 1.

Figure 1. Hold Condition Operation



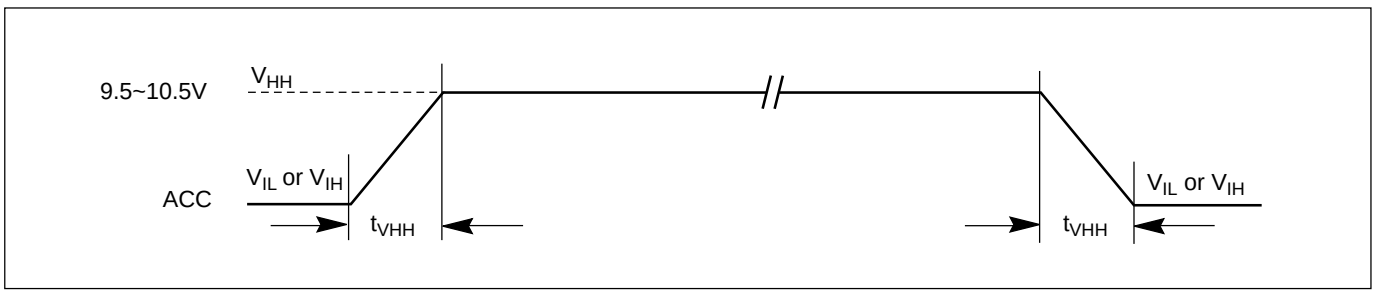
The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

PROGRAM/ERASE ACCELERATION

To activate the program/erase acceleration function requires ACC pin connecting to 9.5~10.5V voltage (see Figure 2), and then to be followed by the normal program/erase process. By utilizing the program/erase acceleration operation, the performances are improved as shown on table of "ERASE AND PROGRAM PERFORMACE".

After power-up ready, it should wait 10ms at least to apply VHH(9.5~10.5V) on the WP#/ACC pin.

Figure 2. ACCELERATED PROGRAM TIMING DIAGRAM



Note: tVHH (VHH Rise and Fall Time) min. 250ns

Table 4. COMMAND DEFINITION

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	FAST READ (fast read data)	2READ (2 x I/O read command) note1	SE (sector erase)
1st byte	06 (hex)	04 (hex)	9F (hex)	05 (hex)	01 (hex)	03 (hex)	0B (hex)	BB (hex)	20 (hex)
2nd byte						AD1	AD1	ADD(2)	AD1
3rd byte						AD2	AD2	ADD(2) & Dummy(2)	AD2
4th byte						AD3	AD3		AD3
5th byte							Dummy		
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte manufacturer ID & 2-byte device ID	to read out the values of the status register	to write new values to the status register	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	to erase the selected sector

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SI/SIO0 which is different from 1 x I/O condition

COMMAND (byte)	BE (block erase)	CE (chip erase)	PP (Page program)	CP (Continuously program mode)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	REMS2 (read ID for 2x I/O mode)
1st byte	D8 (hex)	60 or C7 (hex)	02 (hex)	AD (hex)	B9 (hex)	AB (hex)	AB (hex)	90 (hex)	EF (hex)
2nd byte	AD1		AD1	AD1			x	x	x
3rd byte	AD2		AD2	AD2			x	x	x
4th byte	AD3		AD3	AD3			x	ADD(note 2)	ADD(note 2)
5th byte									
Action	to erase the selected block	to erase whole chip	to program the selected page	continously program whole chip, the address is automatically increase	enters deep power down mode	release from deep power down mode	to read out 1-byte device ID	outout the manufacturer ID & device ID	output the manufacturer ID & device ID

Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first

COMMAND (byte)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)	ESRY (enable SO to output RY/BY#)	DSRY (disable SO to output RY/BY#)
1st byte	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)	70 (hex)	80 (hex)
2nd byte						
3rd byte						
4th byte						
5th byte						
Action	to enter the 512-bit secured OTP mode	to exit the 512-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	to enable SO to output RY/BY# during CP mode	to disable SO to output RY/BY# during CP mode

Note 3: It is not recommoded to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Table 5-1. Memory Organization (16Mb)

Block	Sector	Address Range	
31	511	1FF000h	1FFFFFh
	:	:	:
	496	1F0000h	1F0FFFh
30	495	1EF000h	1EFFFFh
	:	:	:
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	:	:	:
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	:	:	:
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	:	:	:
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	:	:	:
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	:	:	:
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	:	:	:
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	:	:	:
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	:	:	:
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	:	:	:
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	:	:	:
	320	140000h	140FFFh
19	319	13F000h	13FFFFh
	:	:	:
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	:	:	:
	288	120000h	120FFFh
17	287	11F000h	11FFFFh
	:	:	:
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	:	:	:
	256	100000h	100FFFh
15	255	0FF000h	0FFFFFh
	:	:	:
	240	0F0000h	0F0FFFh
14	239	0EF000h	0EFFFFh
	:	:	:
	224	0E0000h	0E0FFFh
13	223	0DF000h	0DFFFFh
	:	:	:
	208	0D0000h	0D0FFFh
12	207	0CF000h	0CFFFFh
	:	:	:
	192	0C0000h	0C0FFFh
11	191	0BF000h	0BFFFFh
	:	:	:
	176	0B0000h	0B0FFFh
10	175	0AF000h	0AFFFFh
	:	:	:
	160	0A0000h	0A0FFFh
9	159	09F000h	09FFFFh
	:	:	:
	144	090000h	090FFFh
8	143	08F000h	08FFFFh
	:	:	:
	128	080000h	080FFFh
7	127	07F000h	07FFFFh
	:	:	:
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	:	:	:
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	:	:	:
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	:	:	:
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	:	:	:
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	:	:	:
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	:	:	:
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	:	:	:
	4	004000h	004FFFh
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

Table 5-2. Memory Organization (32Mb)

Block	Sector	Address Range	
63	1023	3FF000h	3FFFFFh
	:	:	:
	1008	3F0000h	3F0FFFh
62	1007	3EF000h	3EFFFFh
	:	:	:
	992	3E0000h	3E0FFFh
61	991	3DF000h	3DFFFFh
	:	:	:
	976	3D0000h	3D0FFFh
60	975	3CF000h	3CFFFFh
	:	:	:
	960	3C0000h	3C0FFFh
59	959	3BF000h	3BFFFFh
	:	:	:
	944	3B0000h	3B0FFFh
58	943	3AF000h	3AFFFFh
	:	:	:
	928	3A0000h	3A0FFFh
57	927	39F000h	39FFFFh
	:	:	:
	912	390000h	390FFFh
56	911	38F000h	38FFFFh
	:	:	:
	896	380000h	380FFFh
55	895	37F000h	37FFFFh
	:	:	:
	880	370000h	370FFFh
54	879	36F000h	36FFFFh
	:	:	:
	864	360000h	360FFFh
53	863	35F000h	35FFFFh
	:	:	:
	848	350000h	350FFFh
52	847	34F000h	34FFFFh
	:	:	:
	832	340000h	340FFFh
51	831	33F000h	33FFFFh
	:	:	:
	816	330000h	330FFFh
50	815	32F000h	32FFFFh
	:	:	:
	800	320000h	320FFFh
49	799	31F000h	31FFFFh
	:	:	:
	784	310000h	310FFFh
48	783	30F000h	30FFFFh
	:	:	:
	768	300000h	300FFFh
47	767	2FF000h	2FFFFFh
	:	:	:
	752	2F0000h	2F0FFFh
46	751	2EF000h	2EFFFFh
	:	:	:
	736	2E0000h	2E0FFFh
45	735	2DF000h	2DFFFFh
	:	:	:
	720	2D0000h	2D0FFFh
44	719	2CF000h	2CFFFFh
	:	:	:
	704	2C0000h	2C0FFFh
43	703	2BF000h	2BFFFFh
	:	:	:
	688	2B0000h	2B0FFFh
42	687	2AF000h	2AFFFFh
	:	:	:
	672	2A0000h	2A0FFFh
41	671	29F000h	29FFFFh
	:	:	:
	656	290000h	290FFFh
40	655	28F000h	28FFFFh
	:	:	:
	640	280000h	280FFFh
39	639	27F000h	27FFFFh
	:	:	:
	624	270000h	270FFFh
38	623	26F000h	26FFFFh
	:	:	:
	608	260000h	260FFFh
37	607	25F000h	25FFFFh
	:	:	:
	592	250000h	250FFFh
36	591	24F000h	24FFFFh
	:	:	:
	576	240000h	240FFFh
35	575	23F000h	23FFFFh
	:	:	:
	560	230000h	230FFFh
34	559	22F000h	22FFFFh
	:	:	:
	544	220000h	220FFFh
33	543	21F000h	21FFFFh
	:	:	:
	528	210000h	210FFFh
32	527	20F000h	20FFFFh
	:	:	:
	512	200000h	200FFFh

Block	Sector	Address Range	
31	511	1FF000h	1FFFFFh
	:	:	:
	496	1F0000h	1F0FFFh
30	495	1EF000h	1EFFFFh
	:	:	:
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	:	:	:
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	:	:	:
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	:	:	:
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	:	:	:
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	:	:	:
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	:	:	:
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	:	:	:
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	:	:	:
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	:	:	:
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	:	:	:
	320	140000h	140FFFh
19	319	13F000h	13FFFFh
	:	:	:
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	:	:	:
	288	120000h	120FFFh
17	287	11F000h	11FFFFh
	:	:	:
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	:	:	:
	256	100000h	100FFFh

Block	Sector	Address Range	
15	255	0FF000h	0FFFFFh
	:	:	:
	240	0F0000h	0F0FFFh
14	239	0EF000h	0EFFFFh
	:	:	:
	224	0E0000h	0E0FFFh
13	223	0DF000h	0DFFFFh
	:	:	:
	208	0D0000h	0D0FFFh
12	207	0CF000h	0CFFFFh
	:	:	:
	192	0C0000h	0C0FFFh
11	191	0BF000h	0BFFFFh
	:	:	:
	176	0B0000h	0B0FFFh
10	175	0AF000h	0AFFFFh
	:	:	:
	160	0A0000h	0A0FFFh
9	159	09F000h	09FFFFh
	:	:	:
	144	090000h	090FFFh
8	143	08F000h	08FFFFh
	:	:	:
	128	080000h	080FFFh
7	127	07F000h	07FFFFh
	:	:	:
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	:	:	:
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	:	:	:
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	:	:	:
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	:	:	:
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	:	:	:
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	:	:	:
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	:	:	:
	4	004000h	004FFFh
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

Table 5-3. Memory Organization (64Mb)

Block	Sector	Address Range	
127	2047	7FF000h	7FFFFFh
	⋮	⋮	⋮
	2032	7F0000h	7F0FFFh
126	2031	7EF000h	7EFFFFh
	⋮	⋮	⋮
	2016	7E0000h	7E0FFFh
125	2015	7DF000h	7DFFFFh
	⋮	⋮	⋮
	2000	7D0000h	7D0FFFh
124	1999	7CF000h	7CFFFFh
	⋮	⋮	⋮
	1984	7C0000h	7C0FFFh
123	1983	7BF000h	7BFFFFh
	⋮	⋮	⋮
	1968	7B0000h	7B0FFFh
122	1967	7AF000h	7AFFFFh
	⋮	⋮	⋮
	1952	7A0000h	7A0FFFh
121	1951	79F000h	79FFFFh
	⋮	⋮	⋮
	1936	790000h	790FFFh
120	1935	78F000h	78FFFFh
	⋮	⋮	⋮
	1920	780000h	780FFFh
119	1919	77F000h	77FFFFh
	⋮	⋮	⋮
	1904	770000h	770FFFh
118	1903	76F000h	76FFFFh
	⋮	⋮	⋮
	1888	760000h	760FFFh
117	1887	75F000h	75FFFFh
	⋮	⋮	⋮
	1872	750000h	750FFFh
116	1871	74F000h	74FFFFh
	⋮	⋮	⋮
	1856	740000h	740FFFh
115	1855	73F000h	73FFFFh
	⋮	⋮	⋮
	1840	730000h	730FFFh
114	1839	72F000h	72FFFFh
	⋮	⋮	⋮
	1824	720000h	720FFFh
113	1823	71F000h	71FFFFh
	⋮	⋮	⋮
	1808	710000h	710FFFh
112	1807	70F000h	70FFFFh
	⋮	⋮	⋮
	1792	700000h	700FFFh
111	1791	6FF000h	6FFFFFh
	⋮	⋮	⋮
	1776	6F0000h	6F0FFFh
110	1775	6EF000h	6EFFFFh
	⋮	⋮	⋮
	1760	6E0000h	6E0FFFh
109	1759	6DF000h	6DFFFFh
	⋮	⋮	⋮
	1744	6D0000h	6D0FFFh
108	1743	6CF000h	6CFFFFh
	⋮	⋮	⋮
	1728	6C0000h	6C0FFFh
107	1727	6BF000h	6BFFFFh
	⋮	⋮	⋮
	1712	6B0000h	6B0FFFh
106	1711	6AF000h	6AFFFFh
	⋮	⋮	⋮
	1696	6A0000h	6A0FFFh
105	1695	69F000h	69FFFFh
	⋮	⋮	⋮
	1680	690000h	690FFFh
104	1679	68F000h	68FFFFh
	⋮	⋮	⋮
	1664	680000h	680FFFh
103	1663	67F000h	67FFFFh
	⋮	⋮	⋮
	1648	670000h	670FFFh
102	1647	66F000h	66FFFFh
	⋮	⋮	⋮
	1632	660000h	660FFFh
101	1631	65F000h	65FFFFh
	⋮	⋮	⋮
	1616	650000h	650FFFh
100	1615	64F000h	64FFFFh
	⋮	⋮	⋮
	1600	640000h	640FFFh
99	1599	63F000h	63FFFFh
	⋮	⋮	⋮
	1584	630000h	630FFFh
98	1583	62F000h	62FFFFh
	⋮	⋮	⋮
	1568	620000h	620FFFh
97	1567	61F000h	61FFFFh
	⋮	⋮	⋮
	1552	610000h	610FFFh
96	1551	60F000h	60FFFFh
	⋮	⋮	⋮
	1536	600000h	600FFFh

Block	Sector	Address Range	
95	1535	5FF000h	5FFFFFh
	⋮	⋮	⋮
	1520	5F0000h	5F0FFFh
94	1519	5EF000h	5EFFFFh
	⋮	⋮	⋮
	1504	5E0000h	5E0FFFh
93	1503	5DF000h	5DFFFFh
	⋮	⋮	⋮
	1488	5D0000h	5D0FFFh
92	1487	5CF000h	5CFFFFh
	⋮	⋮	⋮
	1472	5C0000h	5C0FFFh
91	1471	5BF000h	5BFFFFh
	⋮	⋮	⋮
	1456	5B0000h	5B0FFFh
90	1455	5AF000h	5AFFFFh
	⋮	⋮	⋮
	1440	5A0000h	5A0FFFh
89	1439	59F000h	59FFFFh
	⋮	⋮	⋮
	1424	590000h	590FFFh
88	1423	58F000h	58FFFFh
	⋮	⋮	⋮
	1408	580000h	580FFFh
87	1407	57F000h	57FFFFh
	⋮	⋮	⋮
	1392	570000h	570FFFh
86	1391	56F000h	56FFFFh
	⋮	⋮	⋮
	1376	560000h	560FFFh
85	1375	55F000h	55FFFFh
	⋮	⋮	⋮
	1360	550000h	550FFFh
84	1359	54F000h	54FFFFh
	⋮	⋮	⋮
	1344	540000h	540FFFh
83	1343	53F000h	53FFFFh
	⋮	⋮	⋮
	1328	530000h	530FFFh
82	1327	52F000h	52FFFFh
	⋮	⋮	⋮
	1312	520000h	520FFFh
81	1311	51F000h	51FFFFh
	⋮	⋮	⋮
	1296	510000h	510FFFh
80	1295	50F000h	50FFFFh
	⋮	⋮	⋮
	1280	500000h	500FFFh

Block	Sector	Address Range	
79	1279	4FF000h	4FFFFFh
	⋮	⋮	⋮
	1264	4F0000h	4F0FFFh
78	1263	4EF000h	4EFFFFh
	⋮	⋮	⋮
	1248	4E0000h	4E0FFFh
77	1247	4DF000h	4DFFFFh
	⋮	⋮	⋮
	1232	4D0000h	4D0FFFh
76	1231	4CF000h	4CFFFFh
	⋮	⋮	⋮
	1216	4C0000h	4C0FFFh
75	1215	4BF000h	4BFFFFh
	⋮	⋮	⋮
	1200	4B0000h	4B0FFFh
74	1119	4AF000h	4AFFFFh
	⋮	⋮	⋮
	1184	4A0000h	4A0FFFh
73	1183	49F000h	49FFFFh
	⋮	⋮	⋮
	1168	490000h	490FFFh
72	1167	48F000h	48FFFFh
	⋮	⋮	⋮
	1152	480000h	480FFFh
71	1151	47F000h	47FFFFh
	⋮	⋮	⋮
	1136	470000h	470FFFh
70	1135	46F000h	46FFFFh
	⋮	⋮	⋮
	1120	460000h	460FFFh
69	1119	45F000h	45FFFFh
	⋮	⋮	⋮
	1104	450000h	450FFFh
68	1103	44F000h	44FFFFh
	⋮	⋮	⋮
	1088	440000h	440FFFh
67	1087	43F000h	43FFFFh
	⋮	⋮	⋮
	1072	430000h	430FFFh
66	1071	42F000h	42FFFFh
	⋮	⋮	⋮
	1056	420000h	420FFFh
65	1055	41F000h	41FFFFh
	⋮	⋮	⋮
	1040	410000h	410FFFh
64	1039	40F000h	40FFFFh
	⋮	⋮	⋮
	1024	400000h	400FFFh

Block	Sector	Address Range	
63	1023	3FF000h	3FFFFFh
	⋮	⋮	⋮
	1008	3F0000h	3F0FFFh
62	1007	3EF000h	3EFFFFh
	⋮	⋮	⋮
	992	3E0000h	3E0FFFh
61	991	3DF000h	3DFFFFh
	⋮	⋮	⋮
	976	3D0000h	3D0FFFh
60	975	3CF000h	3CFFFFh
	⋮	⋮	⋮
	960	3C0000h	3C0FFFh
59	959	3BF000h	3BFFFFh
	⋮	⋮	⋮
	944	3B0000h	3B0FFFh
58	943	3AF000h	3AFFFFh
	⋮	⋮	⋮
	928	3A0000h	3A0FFFh
57	927	39F000h	39FFFFh
	⋮	⋮	⋮
	912	390000h	390FFFh
56	911	38F000h	38FFFFh
	⋮	⋮	⋮
	896	380000h	380FFFh
55	895	37F000h	37FFFFh
	⋮	⋮	⋮
	880	370000h	370FFFh
54	879	36F000h	36FFFFh
	⋮	⋮	⋮
	864	360000h	360FFFh
53	863	35F000h	35FFFFh
	⋮	⋮	⋮
	848	350000h	350FFFh
52	847	34F000h	34FFFFh
	⋮	⋮	⋮
	832	340000h	340FFFh
51	831	33F000h	33FFFFh
	⋮	⋮	⋮
	816	330000h	330FFFh
50	815	32F000h	32FFFFh
	⋮	⋮	⋮
	800	320000h	320FFFh
49	799	31F000h	31FFFFh
	⋮	⋮	⋮
	784	310000h	310FFFh
48	783	30F000h	30FFFFh
	⋮	⋮	⋮
	768	300000h	300FFFh

Block	Sector	Address Range	
47	767	2FF000h	2FFFFFh
	⋮	⋮	⋮
	752	2F0000h	2F0FFFh
46	751	2EF000h	2EFFFFh
	⋮	⋮	⋮
	736	2E0000h	2E0FFFh
45	735	2DF000h	2DFFFFh
	⋮	⋮	⋮
	720	2D0000h	2D0FFFh
44	719	2CF000h	2CFFFFh
	⋮	⋮	⋮
	704	2C0000h	2C0FFFh
43	703	2BF000h	2BFFFFh
	⋮	⋮	⋮
	688	2B0000h	2B0FFFh
42	687	2AF000h	2AFFFFh
	⋮	⋮	⋮
	672	2A0000h	2A0FFFh
41	671	29F000h	29FFFFh
	⋮	⋮	⋮
	656	290000h	290FFFh
40	655	28F000h	28FFFFh
	⋮	⋮	⋮
	640	280000h	280FFFh
39	639	27F000h	27FFFFh
	⋮	⋮	⋮
	624	270000h	270FFFh
38	623	26F000h	26FFFFh
	⋮	⋮	⋮
	608	260000h	260FFFh
37	607	25F000h	25FFFFh
	⋮	⋮	⋮
	592	250000h	250FFFh
36	591	24F000h	24FFFFh
	⋮	⋮	⋮
	576	240000h	240FFFh
35	575	23F000h	23FFFFh
	⋮	⋮	⋮
	560	230000h	230FFFh
34	559	22F000h	22FFFFh
	⋮	⋮	⋮
	544	220000h	220FFFh
33	543	21F000h	21FFFFh
	⋮	⋮	⋮
	528	210000h	210FFFh
32	527	20F000h	20FFFFh
	⋮	⋮	⋮
	512	200000h	200FFFh

Block	Sector	Address Range	
31	511	1FF000h	1FFFFFh
	:	:	:
	496	1F0000h	1F0FFFh
30	495	1EF000h	1EFFFFh
	:	:	:
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	:	:	:
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	:	:	:
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	:	:	:
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	:	:	:
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	:	:	:
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	:	:	:
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	:	:	:
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	:	:	:
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	:	:	:
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	:	:	:
	320	140000h	140FFFh
19	319	13F000h	13FFFFh
	:	:	:
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	:	:	:
	288	120000h	120FFFh
17	287	11F000h	11FFFFh
	:	:	:
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	:	:	:
	256	100000h	100FFFh

Block	Sector	Address Range	
15	255	0FF000h	0FFFFFh
	:	:	:
	240	0F0000h	0F0FFFh
14	239	0EF000h	0EFFFFh
	:	:	:
	224	0E0000h	0E0FFFh
13	223	0DF000h	0DFFFFh
	:	:	:
	208	0D0000h	0D0FFFh
12	207	0CF000h	0CFFFFh
	:	:	:
	192	0C0000h	0C0FFFh
11	191	0BF000h	0BFFFFh
	:	:	:
	176	0B0000h	0B0FFFh
10	175	0AF000h	0AFFFFh
	:	:	:
	160	0A0000h	0A0FFFh
9	159	09F000h	09FFFFh
	:	:	:
	144	090000h	090FFFh
8	143	08F000h	08FFFFh
	:	:	:
	128	080000h	080FFFh
7	127	07F000h	07FFFFh
	:	:	:
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	:	:	:
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	:	:	:
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	:	:	:
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	:	:	:
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	:	:	:
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	:	:	:
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	:	:	:
	4	004000h	004FFFh
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.

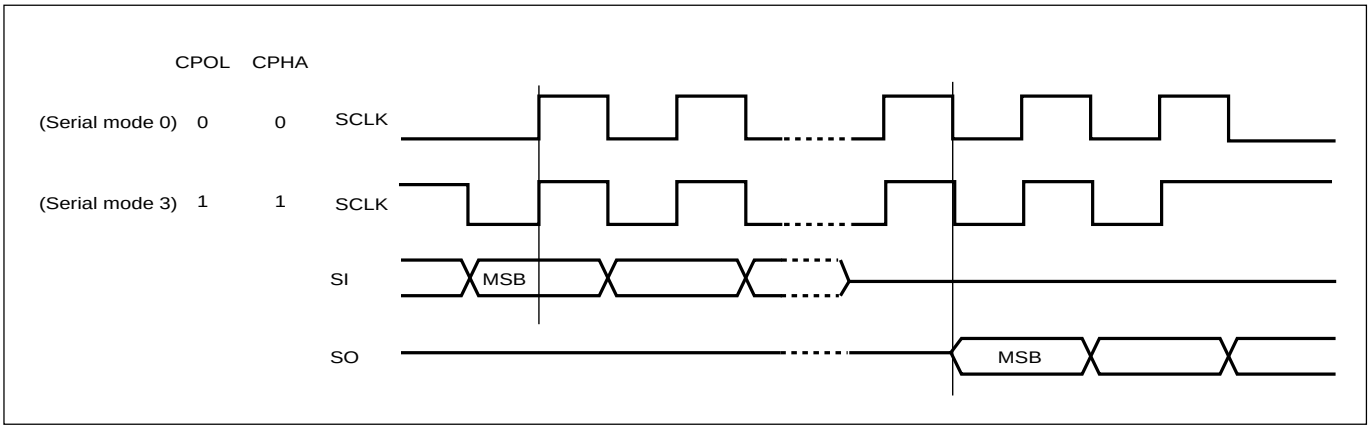
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as Figure 3.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, 2READ, RES, REMS and REMS2 the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, CP, RDP, DP, ENSO, EXSO,and WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 3. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

COMMAND DESCRIPTION

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, CP, SE, BE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low-> sending WREN instruction code-> CS# goes high. (see Figure 12)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low-> sending WRDI instruction code-> CS# goes high. (see Figure 13)

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion
- Continuously program mode (CP) instruction completion

(3) Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte device ID, and the individual device ID of second-byte ID are listed as table of "ID Definitions".

The sequence of issuing RDID instruction is: CS# goes low-> sending RDID instruction code -> 24-bits ID data out on SO -> to end RDID operation can use CS# to high at any time during data out. (see Figure. 14)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low-> sending RDSR instruction code-> Status Register data out on SO (see Figure. 15)

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and not affect value of WEL bit if it is applied to a protected memory area.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area(as defined in table 1) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase(CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed).

Continuously Program Mode(CP mode) bit. The Continuously Program Mode bit indicates the status of CP mode, "0" indicates not in CP mode; "1" indicates in CP mode.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/ACC) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/ACC pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only.

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	Continuously program mode (CP mode)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1= status register write disable	0 = normal program mode 1 = CP mode(default 0)	(note1)	(note1)	(note1)	(note1)	1= write enable 0= not write enable	1= write operation 0= not in write operation
Non- volatile bit	volatile bit	Non- volatile bit	Non- volatile bit	Non- volatile bit	Non- volatile bit	volatile bit	volatile bit

note1: see the table "Protected Area Sizes"

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in table 1). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/ACC) pin signal. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low-> sending WRSR instruction code-> Status Register data on SI-> CS# goes high. (see Figure 16)

The WRSR instruction has no effect on b6, b1, b0 of the status register.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 6. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode(SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:
1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in Table 1.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):
- When SRWD bit=0, no matter WP#/ACC is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/ACC is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Note: If SRWD bit=1 but WP#/ACC is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/ACC is low (or WP#/ACC is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/ACC to against data modification.

Note: to exit the hardware protected mode requires WP#/ACC driving high once the hardware protected mode is entered. If the WP#/ACC pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

(6) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low-> sending READ instruction code-> 3-byte address on SI -> data out on SO-> to end READ operation can use CS# to high at any time during data out. (see Figure. 17)

(7) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low-> sending FAST_READ instruction code-> 3-byte address on SI-> 1-dummy byte address on SI->data out on SO-> to end FAST_READ operation can use CS# to high at any time during data out. (see Figure. 18)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(8) 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits(interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→sending 2READ instruction→24-bit address interleave on SIO1 & SIO0→ 8-bit dummy interleave on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out (see Figure of 2 x I/O Read Mode Timing Waveform)

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

The 2 I/O only perform read operation. Program/Erase /Read ID/Read status/Read ID....operation do not support 2 I/O throughputs.

(9) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see table 3) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low -> sending SE instruction code-> 3-byte address on SI -> CS# goes high. (see Figure 22)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the page.

(10) Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte sector erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see table 3) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low -> sending BE instruction code-> 3-byte address on SI -> CS# goes high. (see Figure 23)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the page.

(11) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). Any address of the sector (see table 3) is a valid address for Chip Erase (CE) instruction. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low-> sending CE instruction code-> CS# goes high. (see Figure 24)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

(12) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If the eight least significant address bits (A7-A0) are not all 0, all transmitted data which goes beyond the end of the current page are programmed from the start address if the same page (from the address whose 8 least significant address bits (A7-A0) are all 0). The CS# must keep during the whole Page Program cycle. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed. If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the request address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: CS# goes low-> sending PP instruction code-> 3-byte address on SI-> at least 1-byte on data on SI-> CS# goes high. (see Figure 20)

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

(13) Continuously program mode (CP mode)

The CP mode may enhance program performance by automatically increasing address to the next higher address after each byte data has been programmed.

The Continuously program (CP) instruction is for multiple byte program to Flash. A write Enable (WREN) instruction must execute to set the Write Enable Latch(WEL) bit before sending the Continuously program (CP) instruction. CS# requires to go high before CP instruction is executing. After CP instruction and address input, two bytes of data is input sequentially from MSB(bit7) to LSB(bit0). The first byte data will be programmed to the initial address range with A0=0 and second byte data with A0=1. If only one byte data is input, the CP mode will not process. If more than two bytes data are input, the additional data will be ignored and only two byte data are valid. The CP program instruction will be ignored and not affect the WEL bit if it is applied to a protected memory area. Any byte to be programmed should be in the erase state (FF) first. It will not roll over during the CP mode, once the last unprotected address has been reached, the chip will exit CP mode and reset write Enable Latch bit (WEL) as "0" and CP mode bit as "0". Please check the WIP bit status if it is not in write progress before entering next valid instruction. During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), RDPR command (A1 hex), and RDSCUR command (2B hex). And the WRDI command is valid after completion of a CP programming cycle, which means the WIP bit=0.

The sequence of issuing CP instruction is : CS# high to low-> sending CP instruction code-> 3-byte address on SI-> Data Byte on SI->CS# goes high to low-> sending CP instruction.....-> last desired byte programmed or sending Write Disable (WRDI) instruction to end CP mode-> sending RDSR instruction to verify if CP mode is ended. (see Figure of CP mode timing waveform)

Three methods to detect the completion of a program cycle during CP mode:
1) Software method-I: by checking WIP bit of Status Register to detect the completion of CP mode.

2) Software method-II: by waiting for a tBP time out to determine if it may load next valid command or not.
3) Hardware method: by writing ESRY (enable SO to output RY/BY#) instruction to detect the completion of a program cycle during CP mode. The ESRY instruction must be executed before CP mode execution. Once it is enable in CP mode, the CS# goes low will drive out the RY/BY# status on SO, "0" indicates busy stage, "1" indicates ready stage, SO pin outputs tri-state if CS# goes high. DSRY (disable SO to output RY/BY#) instruction to disable the SO to output RY/BY# and return to status register data output during CP mode. Please note that the ESRY/DSRY command are not accepted unless the completion of CP mode.

(14) Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low-> sending DP instruction code-> CS# goes high. (see Figure 25)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (those instructions allow the ID being reading out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

(15) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in Table 6. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The sequence is shown as Figure 26,27.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power Down Mode.

(16) Read Electronic Manufacturer ID & Device ID (REMS), (REMS2)

The REMS & REMS2 instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS & REMS2 instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" or "EFh" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for MXIC (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in figure 25. The Device ID values are listed in Table of ID Definitions. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table 7. ID Definitions

Command Type	MX25L1605D			MX25L3205D			MX25L6405D		
RDID (JEDEC ID)	Manufacturer ID	Memory type	Memory Density	Manufacturer ID	Memory type	Memory Density	Manufacturer ID	Memory type	Memory Density
	C2	20	15	C2	20	16	C2	20	17
RES	Electronic ID			Electronic ID			Electronic ID		
	14			15			16		
REMS/REMS2	Manufacturer ID	Device ID		Manufacturer ID	Device ID		Manufacturer ID	Device ID	
	C2	14		C2	15		C2	16	

(17) Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 512-bit secured OTP mode. The additional 512-bit secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low-> sending ENSO instruction to enter Secured OTP mode -> CS# goes high.

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

(18) Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 512-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low-> sending EXSO instruction to exit Secured OTP mode-> CS# goes high.

(19) Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low-> send ing RDSCUR instruction -> Security Register data out on SO-> CS# goes high.

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex- factory or not. When it is "0", it indicates non- factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 512-bit Secured OTP area cannot be update any more. While it is in 512-bit secured OTP mode, array access is not allowed.

Table 8. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	x	x	x	LDSO (indicate if lock-down	Secrured OTP indicator bit
reserved	reserved	reserved	reserved	reserved	reserved	0 = not lock-down 1 = lock-down (cannot program/erase OTP)	0 = non-factory lock 1 = factory lock
volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit

(20) Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. Unlike write status register, the WREN instruction is not required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 512-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low-> sending WRSCUR instruction -> CS# goes high.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

POWER-ON STATE

The device is at below states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, after VCC reaching the VWI level, a tPUW time delay is required before the device is fully accessible for commands like write enable(WREN), page program (PP), Continuously Program (CP), sector erase(SE), chip erase(CE), WRSCUR and write status register(WRSR). If the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tPUW after VCC reached VWI level
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL, even time of tPUW has not passed.
Please refer to the figure of "power-up timing".

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended.(generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40° C to 85° C for Industrial grade
Storage Temperature	-55° C to 125° C
Applied Input Voltage	-0.5V to 4.6V
Applied Output Voltage	-0.5V to 4.6V
VCC to Ground Potential	-0.5V to 4.6V

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see Figure 4, 5.

Figure 4. Maximum Negative Overshoot Waveform

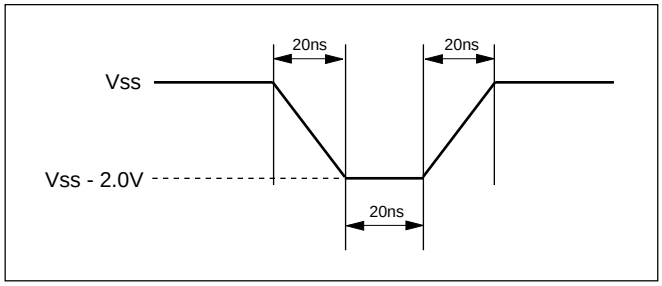
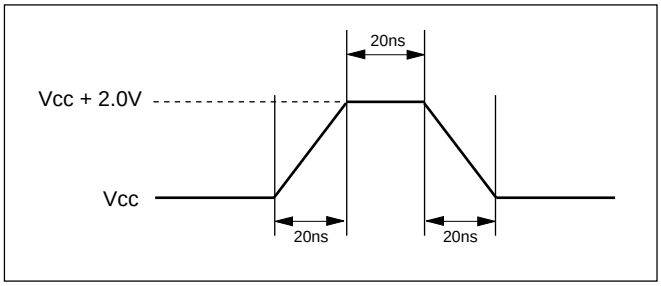


Figure 5. Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25° C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 6. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

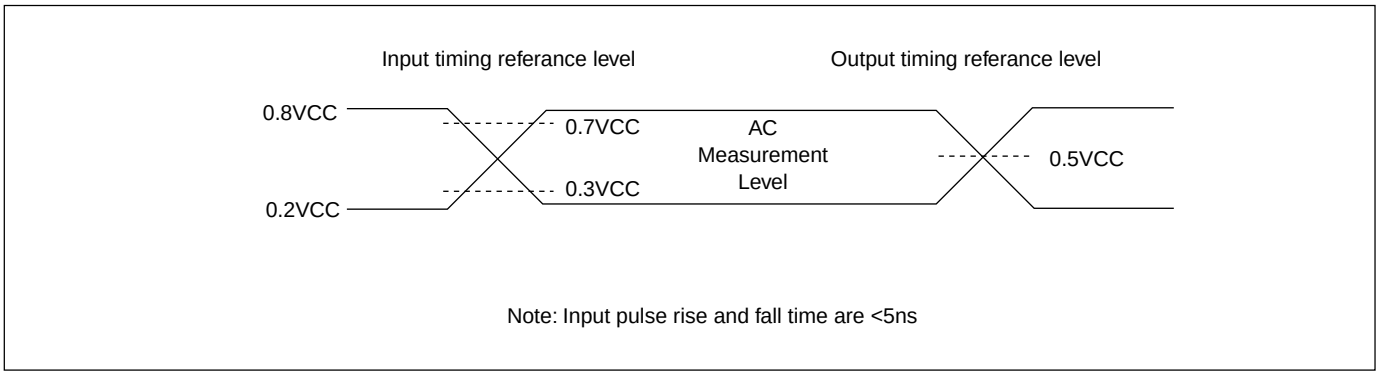


Figure 7. OUTPUT LOADING

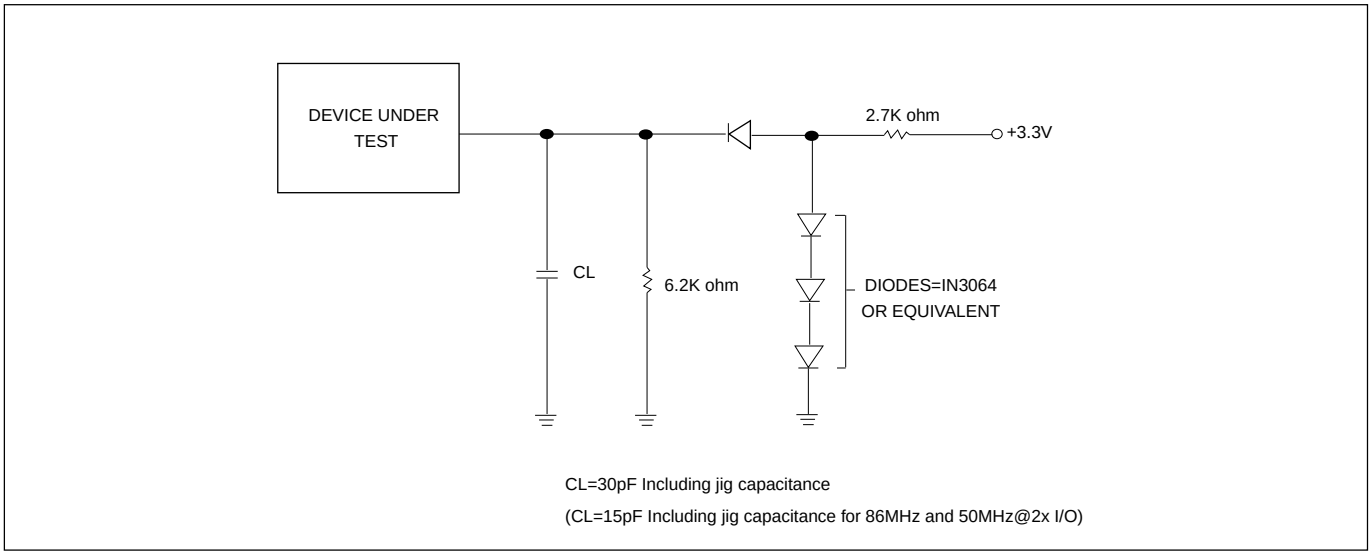


Table 9. DC CHARACTERISTICS
(Temperature = -40° C to 85° C for Industrial grade, VCC = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
ILI	Input Load Current	1			± 2	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			± 2	uA	VCC = VCC Max VIN = VCC or GND
ILIHV	HV pin input Leakage Current				35	uA	WP#/ACC=10.5V
ISB1	VCC Standby Current	1			20	uA	VIN = VCC or GND CS# = VCC
ISB2	Deep Power-down Current				20	uA	VIN = VCC or GND CS# = VCC
ICC1	VCC Read	1			25	mA	f=86MHz fT=50MHz (2 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
					20	mA	f=66MHz SCLK=0.1VCC/0.9VCC, SO=Open
					10	mA	f=33MHz SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1			20	mA	Program in Progress CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current				20	mA	Program status register in progress CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1			20	mA	Erase in Progress CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1			20	mA	Erase in Progress CS#=VCC
VHH	Voltage for ACC Program/ Erase Acceleration		9.5		10.5	V	VCC=2.7V~3.6V
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Table 10. AC CHARACTERISTICS
(Temperature = -40° C to 85° C for Industrial grade, VCC = 2.7V ~ 3.6V)

Symbol	Alt.	Parameter			Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions:			10KHz		86	MHz
		FAST_READ, PP, SE, BE, CE, DP, RES,RDP					(Condition:15pF)	
		WREN, WRDI, RDID, RDSR, WRSR					66	MHz
							(Condition:30pF)	
fRSCLK	fR	Clock Frequency for READ instructions			10KHz		33	MHz
fTSCLK	fT	Clock Frequency for 2READ instructions			10KHz		50	MHz
							(Condition:15pF)	
tCH(1)	tCLH	Clock High Time			7			ns
tCL(1)	tCLL	Clock Low Time			7			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)			0.1			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)			0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)			5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)			5			ns
tDVCH	tDSU	Data In Setup Time			2			ns
tCHDX	tDH	Data In Hold Time			5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)			5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)			5			ns
tSHSL	tCSH	CS# Deselect Time			100			ns
tSHQZ(2)	tDIS	Output Disable Time	64Mb/	2.7V-3.6V			10	ns
			32Mb/	3.0V-3.6V			8	ns
			16Mb					
tCLQV	tV	Clock Low to Output Valid	64Mb/	2.7V-3.6V			10	ns
			32Mb/	3.0V-3.6V			8	ns
			16Mb					
tCLQX	tHO	Output Hold Time			0			ns
tHLCH		HOLD# Setup Time (relative to SCLK)			5			ns
tCHHH		HOLD# Hold Time (relative to SCLK)			5			ns
tHHCH		HOLD Setup Time (relative to SCLK)			5			ns
tCHHL		HOLD Hold Time (relative to SCLK)			5			ns
tHHQX(2)	tLZ	HOLD to Output Low-Z	64Mb/	2.7V-3.6V			10	ns
			32Mb/	3.0V-3.6V			8	ns
			16Mb					
tHLQZ(2)	tHZ	HOLD# to Output High-Z	64Mb/	2.7V-3.6V			10	ns
			32Mb/	3.0V-3.6V			8	ns
			16Mb					
tWHSL(4)		Write Protect Setup Time			20			ns
tSHWL(4)		Write Protect Hold Time			100			ns
tDP(2)		CS# High to Deep Power-down Mode					10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read					8.8	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read					8.8	us

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
tW		Write Status Register Cycle Time			40	100	ms
tBP		Byte-Program			9	300	us
tPP		Page Program Cycle Time			1.4	5	ms
tSE		Sector Erase Cycle Time			60	300	ms
tBE		Block Erase Cycle Time			0.7	2	s
tCE		Chip Erase Cycle Time	64Mb		50	80	s
			32Mb		25	50	s
			16Mb		14	30	s

Notes:
1. tCH + tCL must be greater than or equal to 1/ fC. For Fast Read, tCL/tCH=5.5/5.5.
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
5. Test condition is shown as Figure 6.

Table 11. Power-Up Timing and VWI Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to CS# low	200		us
tPUW(1)	Time delay to Write instruction	1	10	ms
VWI(1)	Write Inhibit Voltage	1.5	2.5	V

Note: 1. These parameters are characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Figure 8. Serial Input Timing

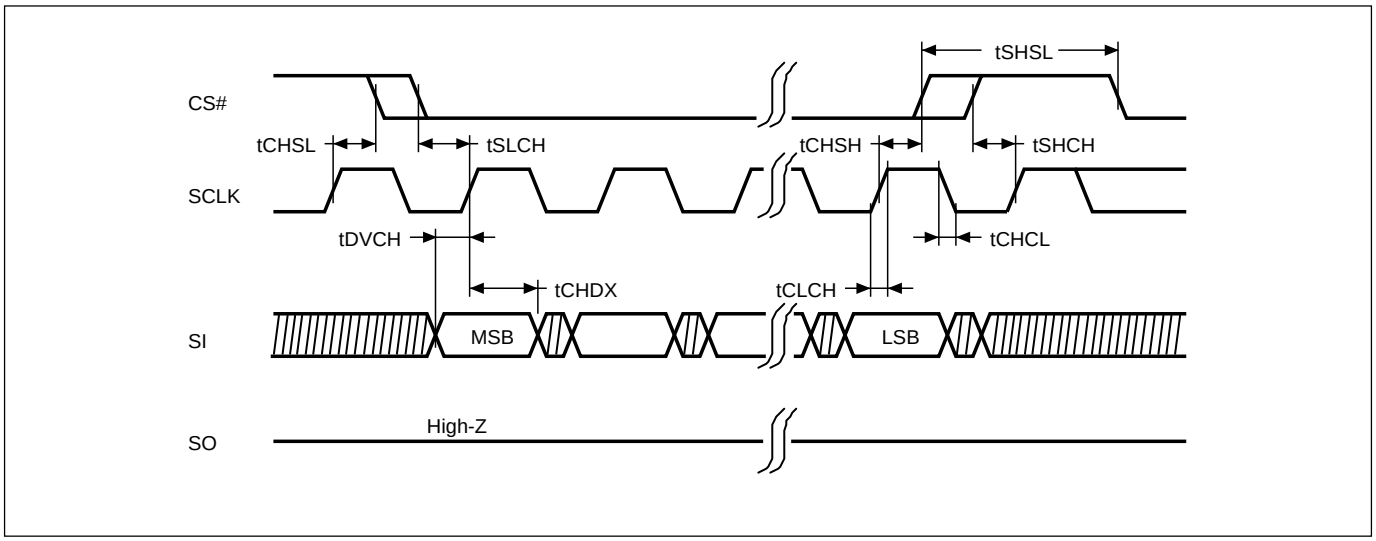


Figure 9. Output Timing

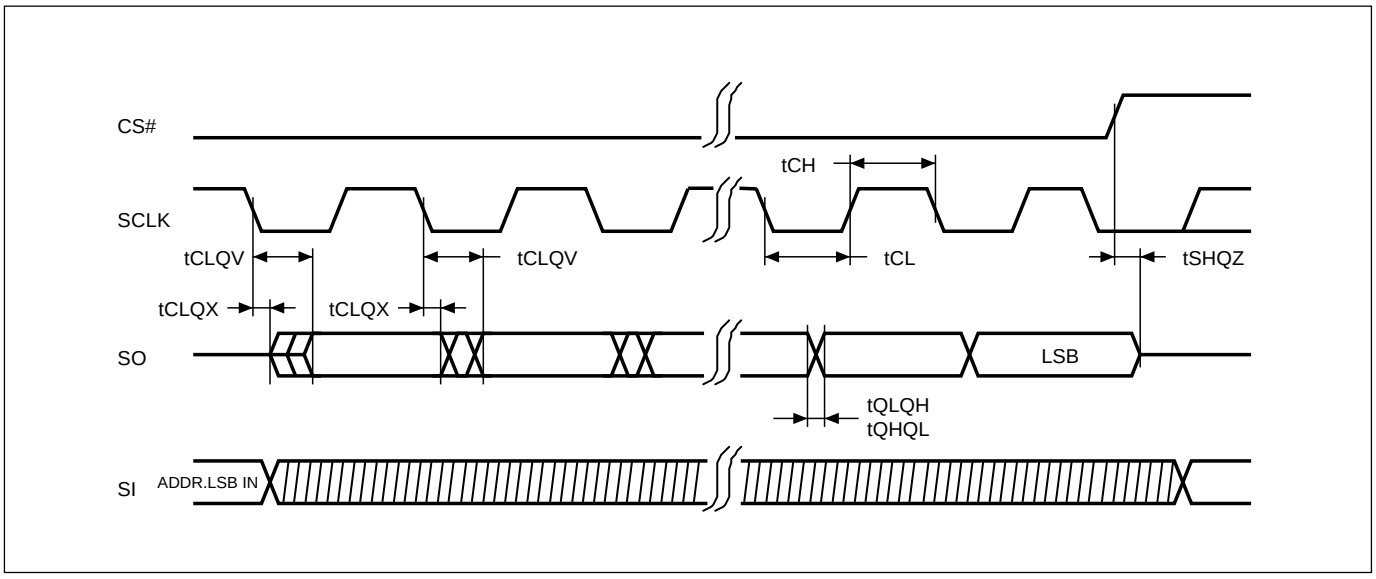
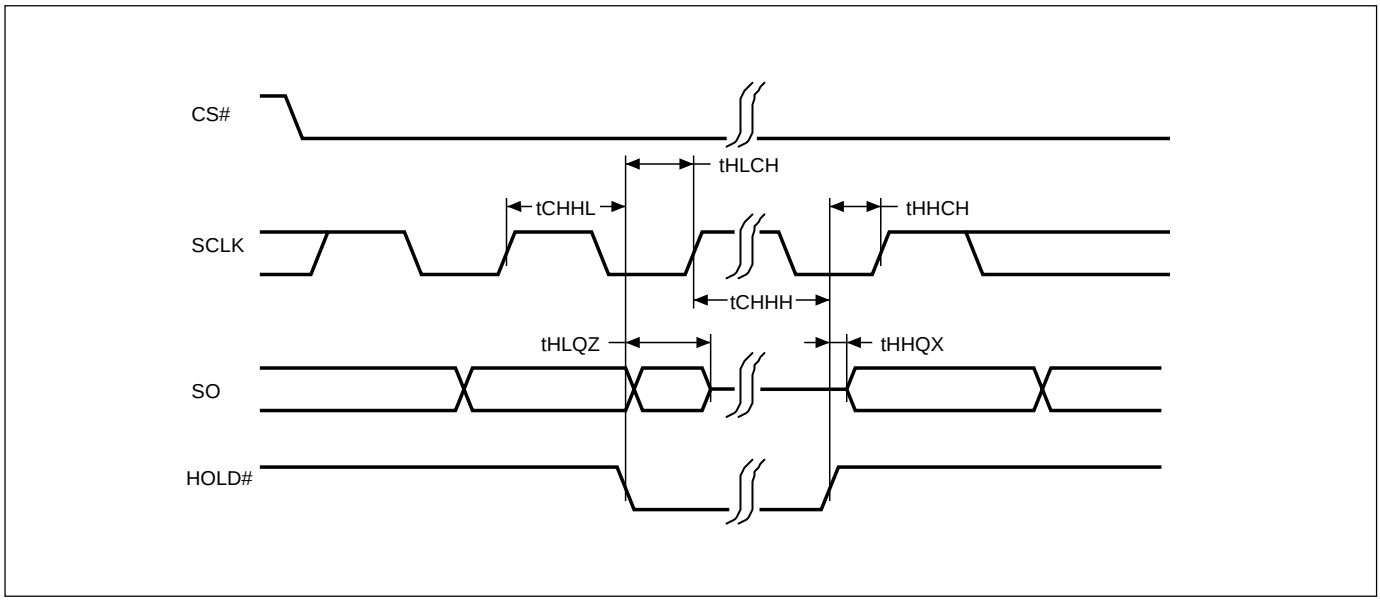


Figure 10. Hold Timing



* SI is "don't care" during HOLD operation.

Figure 11. WP# Disable Setup and Hold Timing during WRSR when SRWD=1

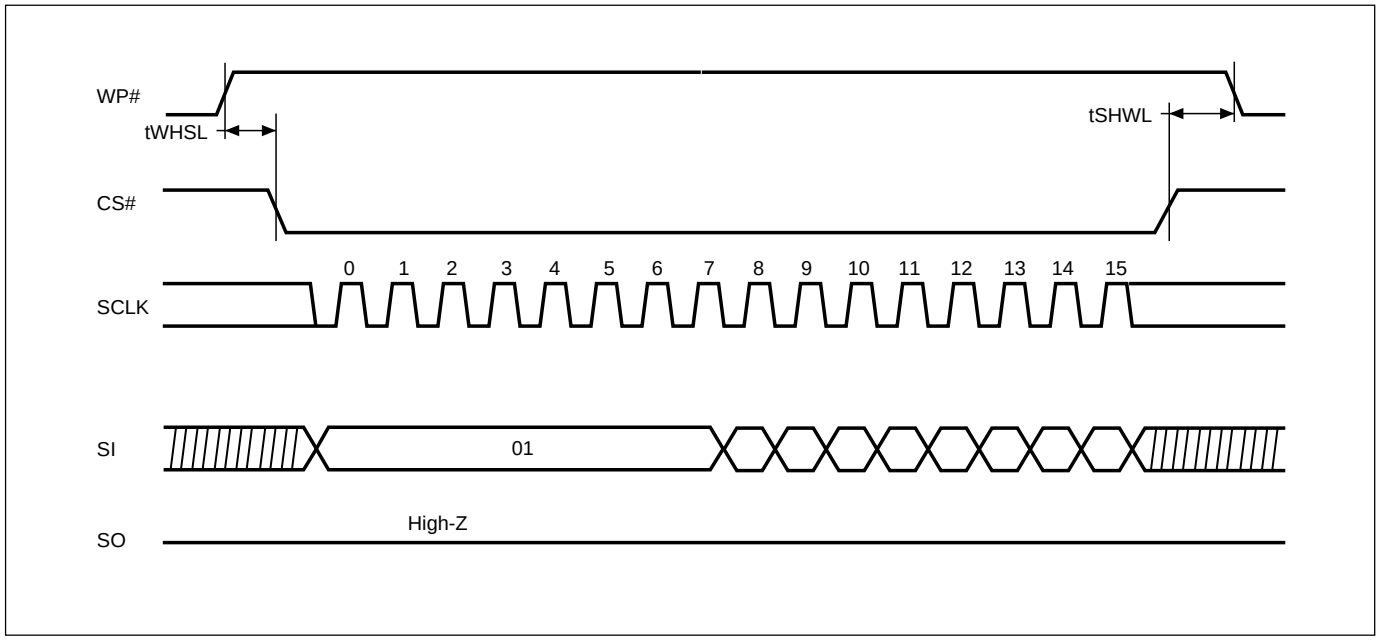


Figure 12. Write Enable (WREN) Sequence (Command 06)

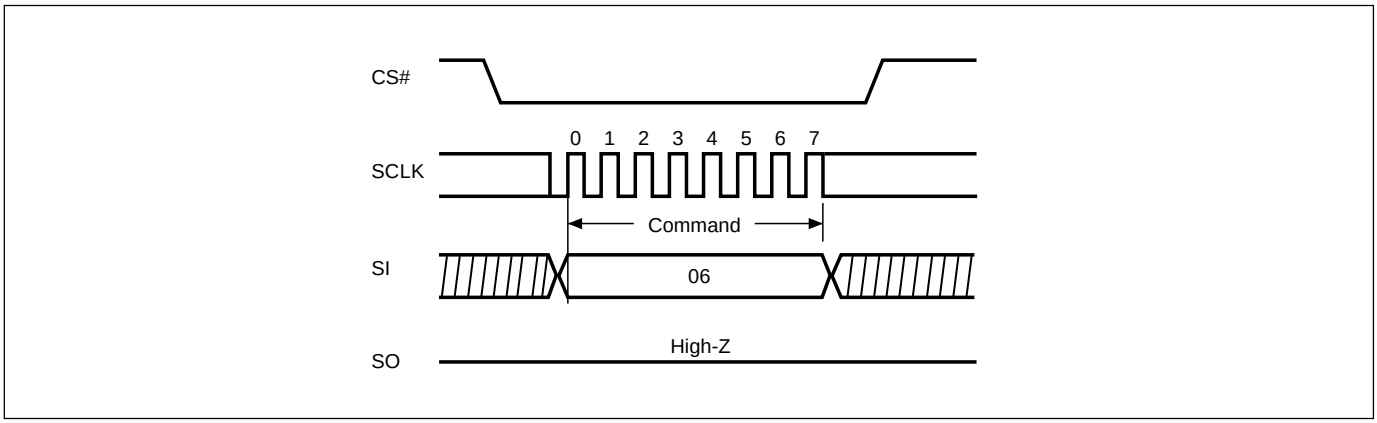


Figure 13. Write Disable (WRDI) Sequence (Command 04)

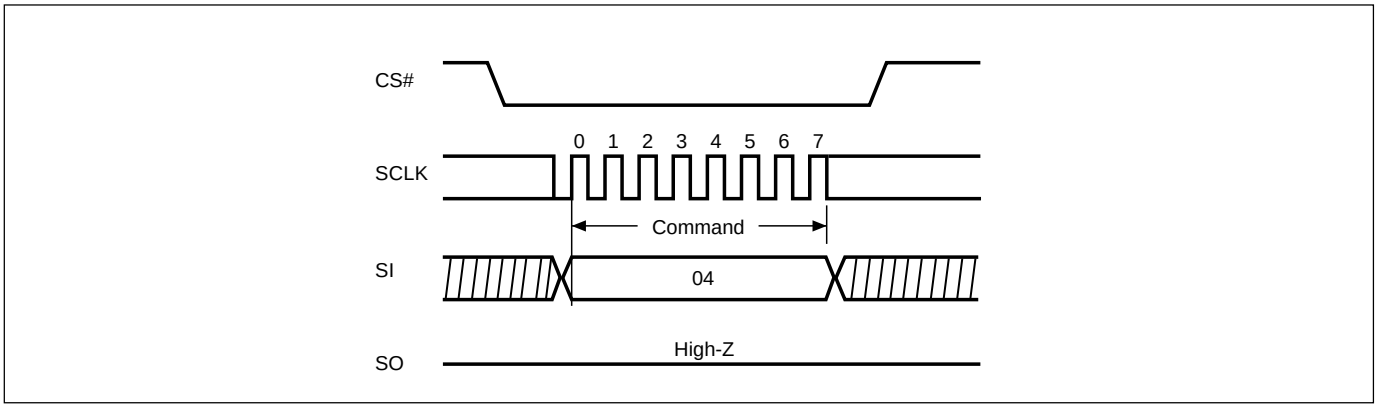


Figure 14. Read Identification (RDID) Sequence (Command 9F)

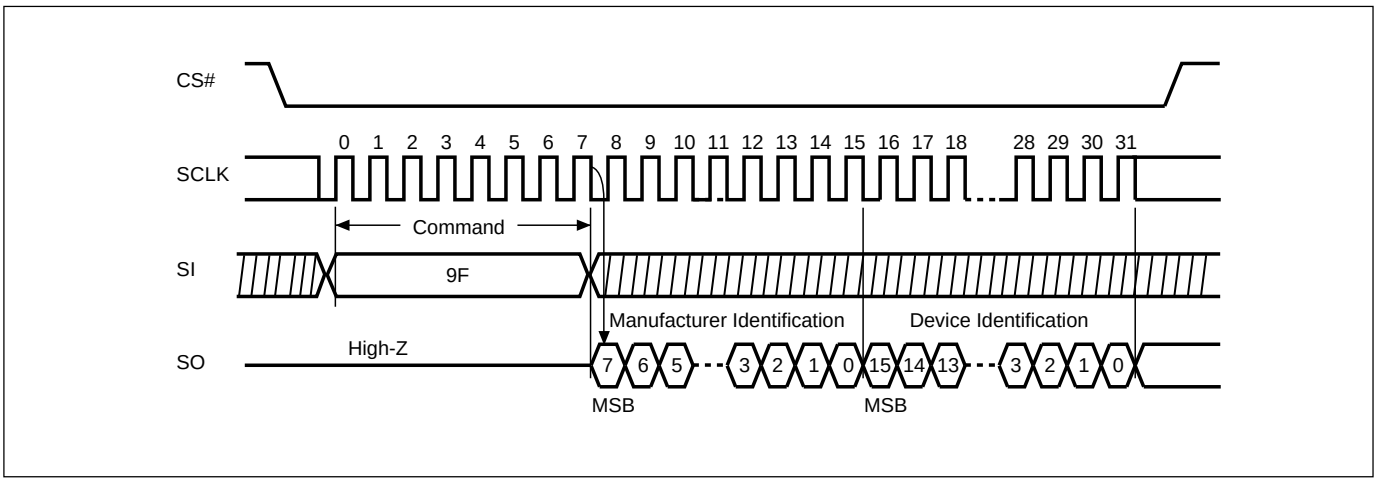


Figure 15. Read Status Register (RDSR) Sequence (Command 05)

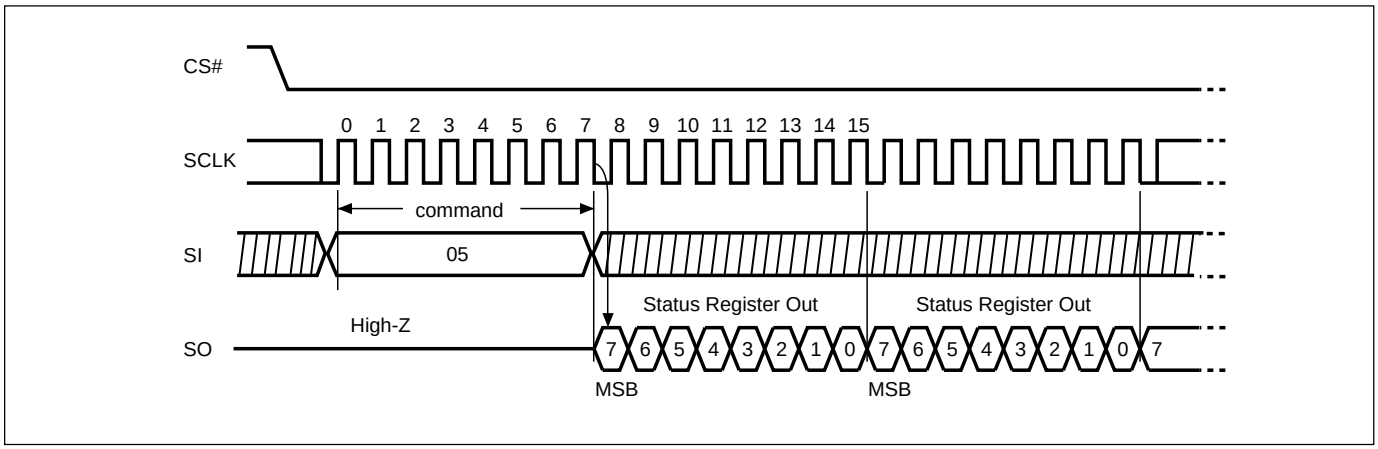


Figure 16. Write Status Register (WRSR) Sequence (Command 01)

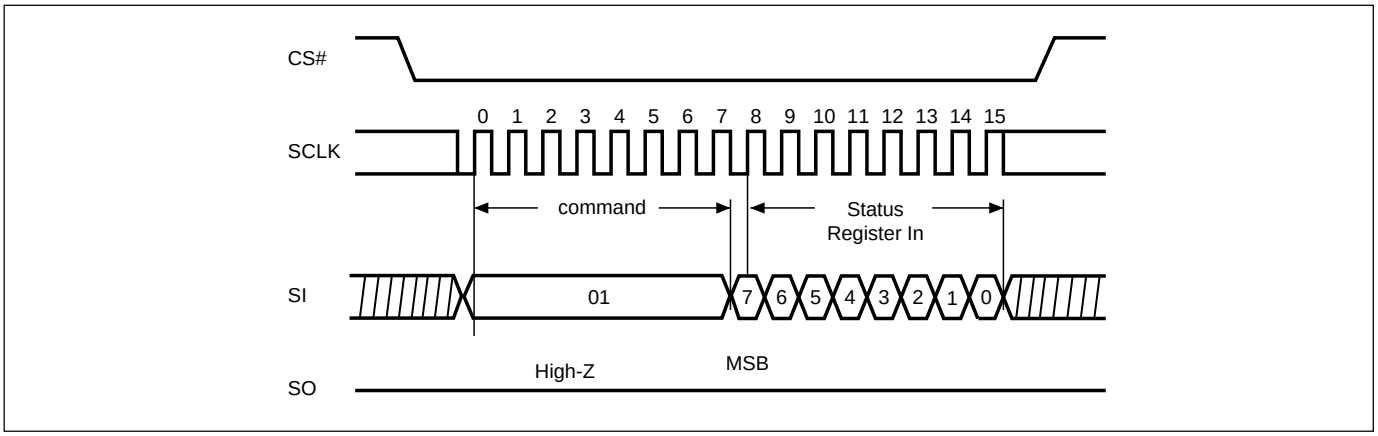


Figure 17. Read Data Bytes (READ) Sequence (Command 03)

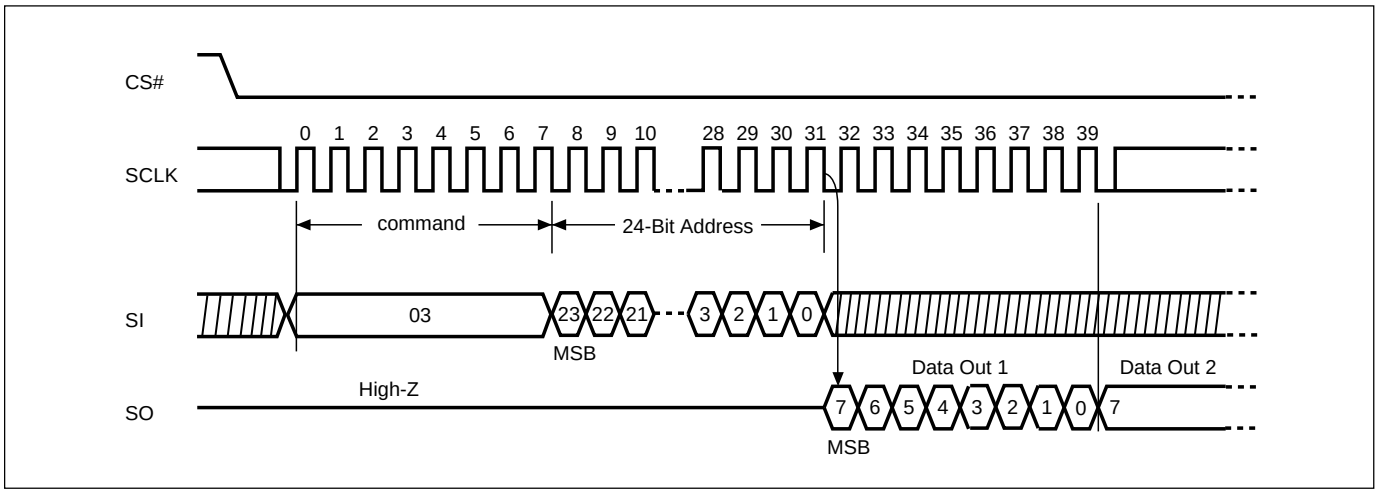


Figure 18. Read at Higher Speed (FAST_READ) Sequence (Command 0B)

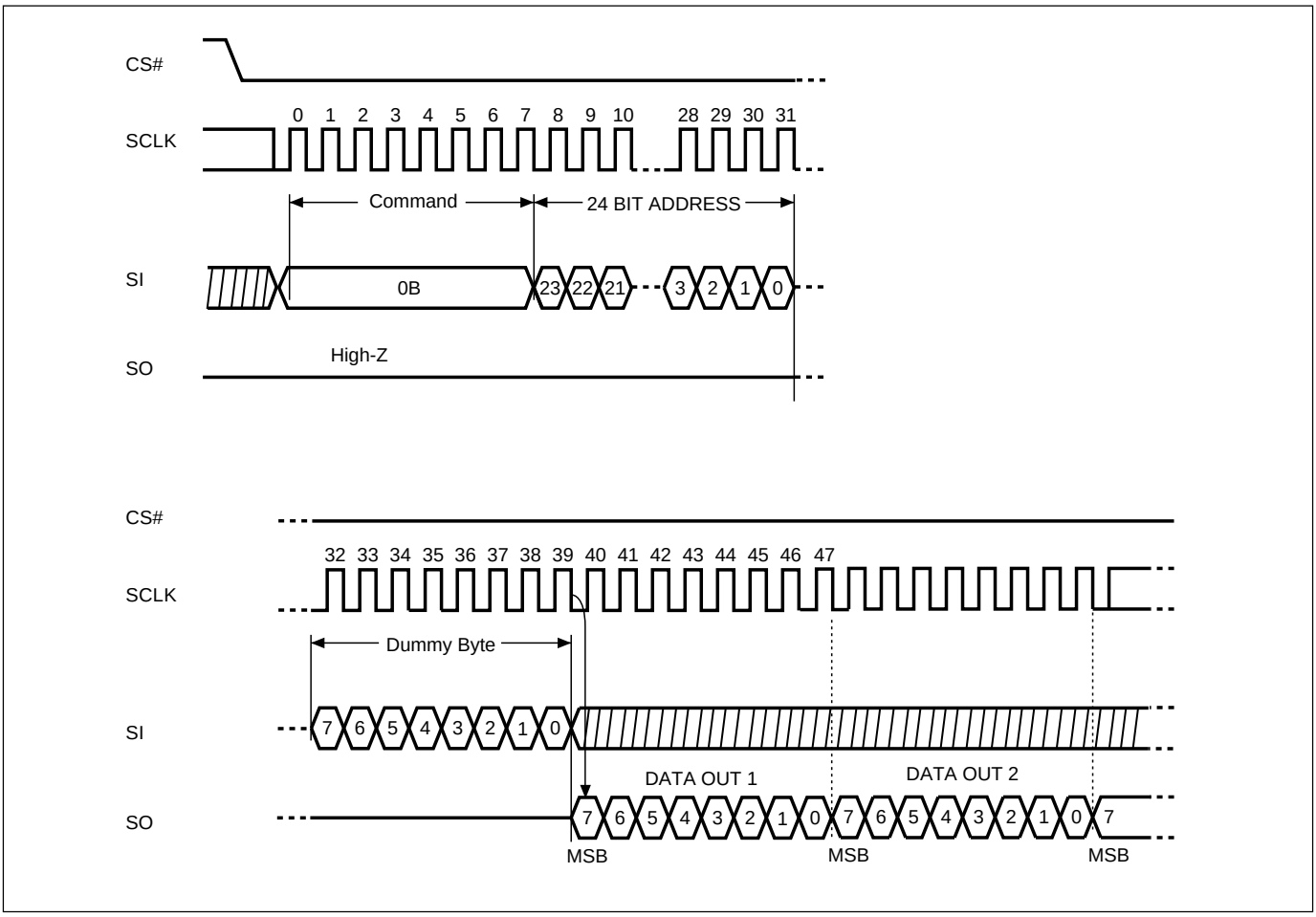


Figure 19. 2 x I/O Read Mode Sequence (Command BB)

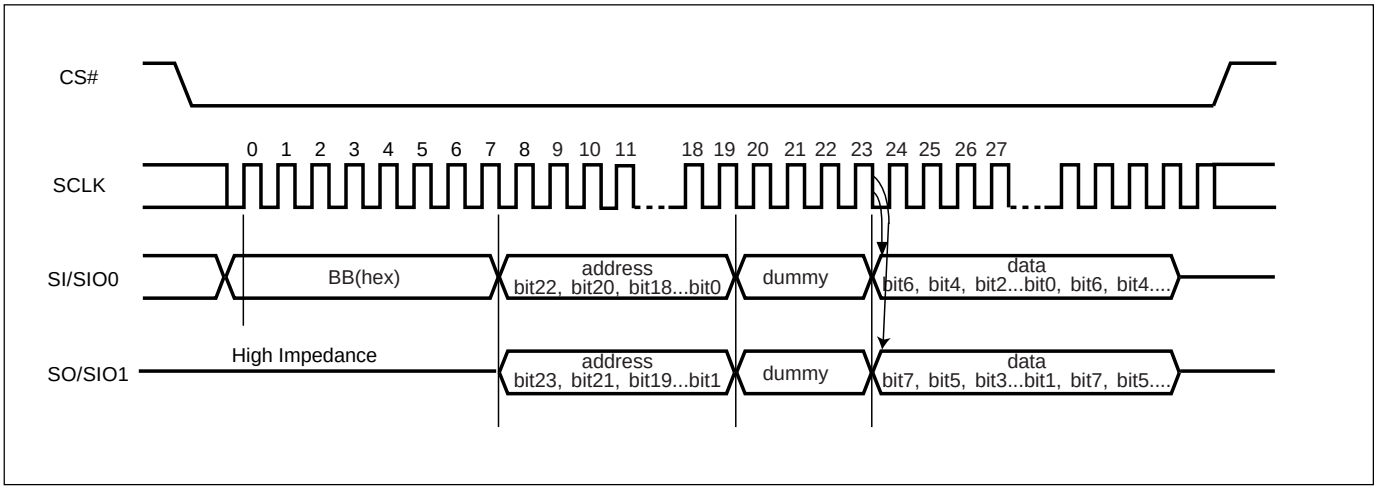


Figure 20. Page Program (PP) Sequence (Command 02)

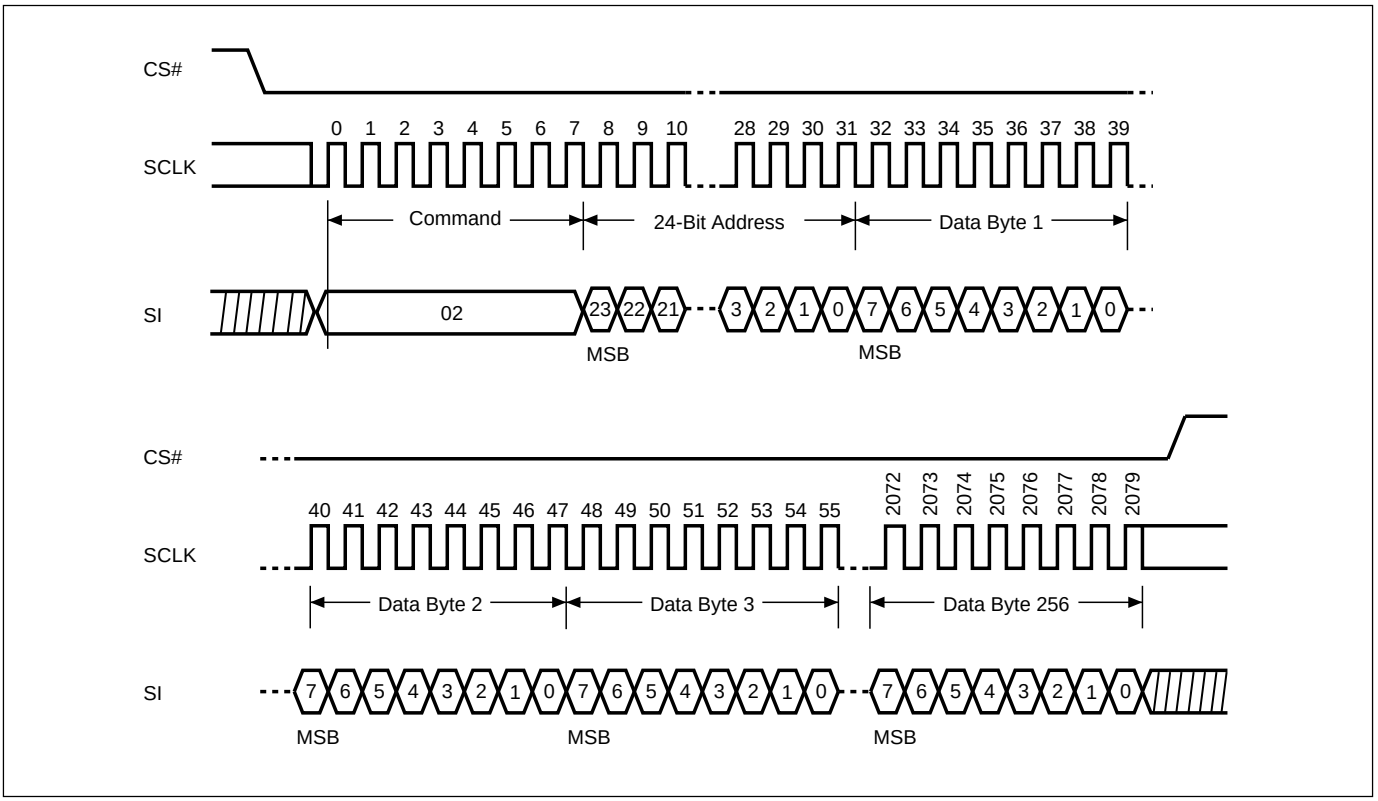
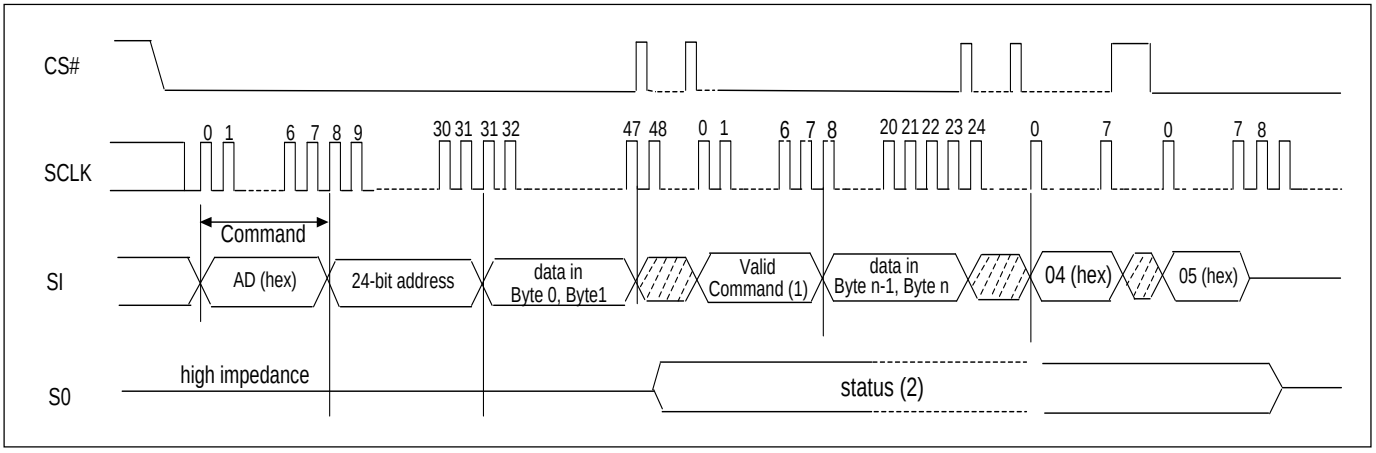
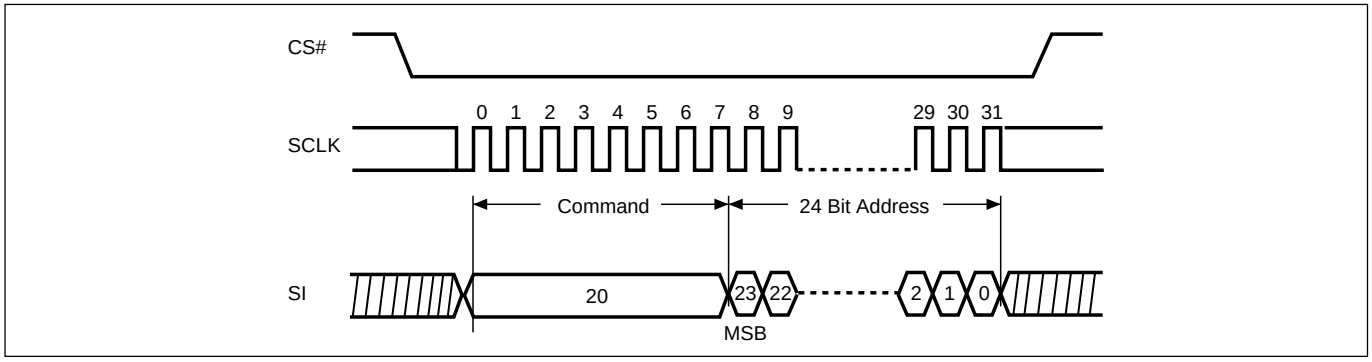


Figure 21. Continously Program (CP) Mode Sequence with Hardware Detection (Command AD)



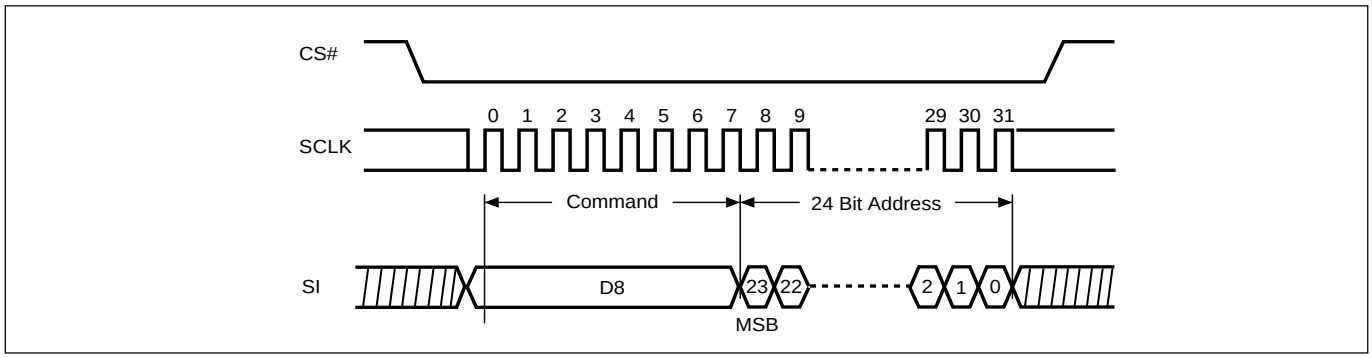
Note: (1) During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), RDPR command (A1 hex), and RDSCUR command (2B hex).
(2) Once an internal programming operation begins, CS# goes low will drive the status on the SO pin and CS# goes high will return the SO pin to tri-state.
(3) To end the CP mode, either reaching the highest unprotected address or sending Write Disable (WRDI) command (04 hex) may achieve it and then it is recommended to send RDSR command (05 hex) to verify if CP mode is ended

Figure 22. Sector Erase (SE) Sequence (Command 20)



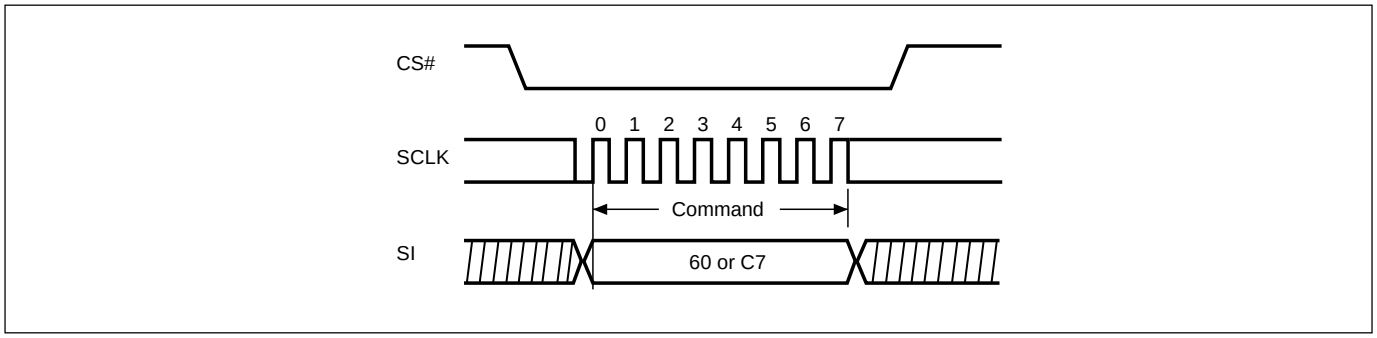
Note: SE command is 20(hex).

Figure 23. Block Erase (BE) Sequence (Command D8)



Note: BE command is D8(hex).

Figure 24. Chip Erase (CE) Sequence (Command 60 or C7)



Note: CE command is 60(hex) or C7(hex).

Figure 25. Deep Power-down (DP) Sequence (Command B9)

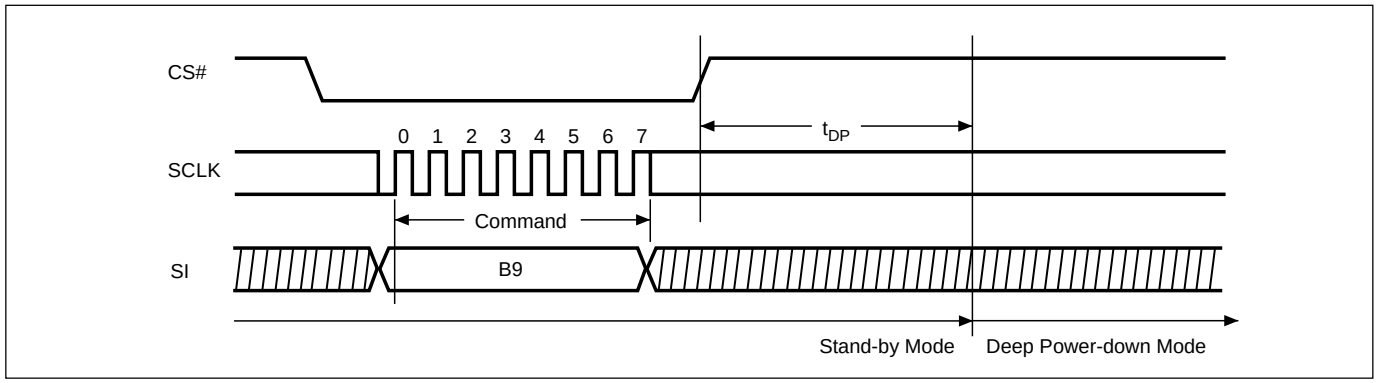


Figure 26. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)

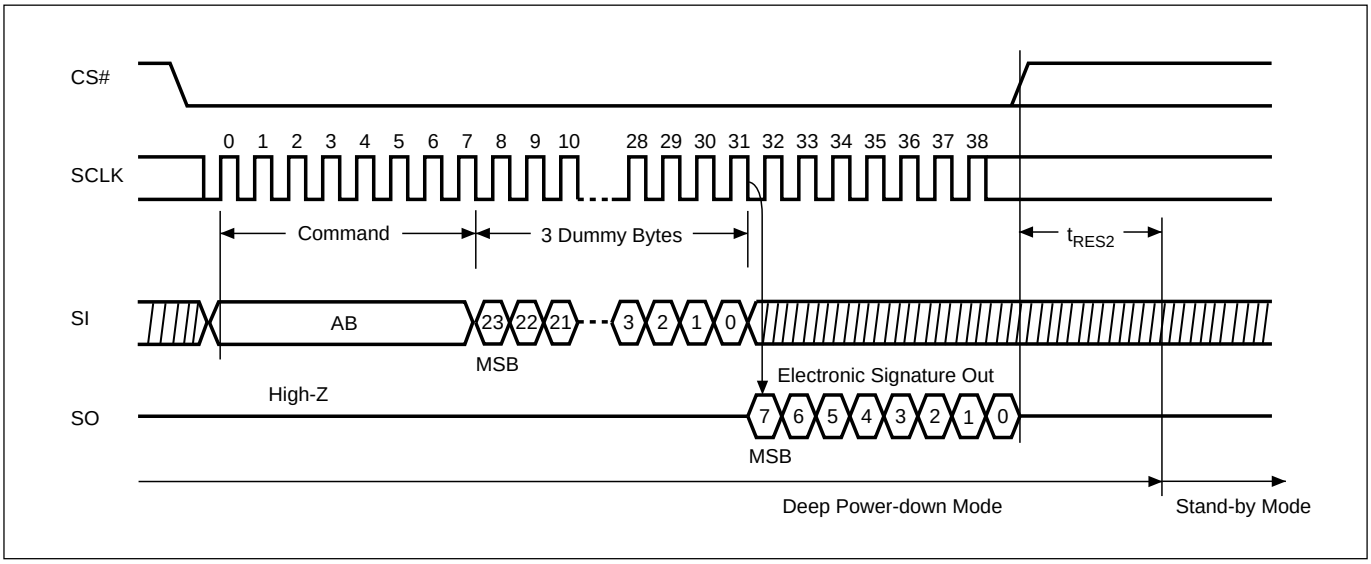


Figure 27. Release from Deep Power-down (RDP) Sequence (Command AB)

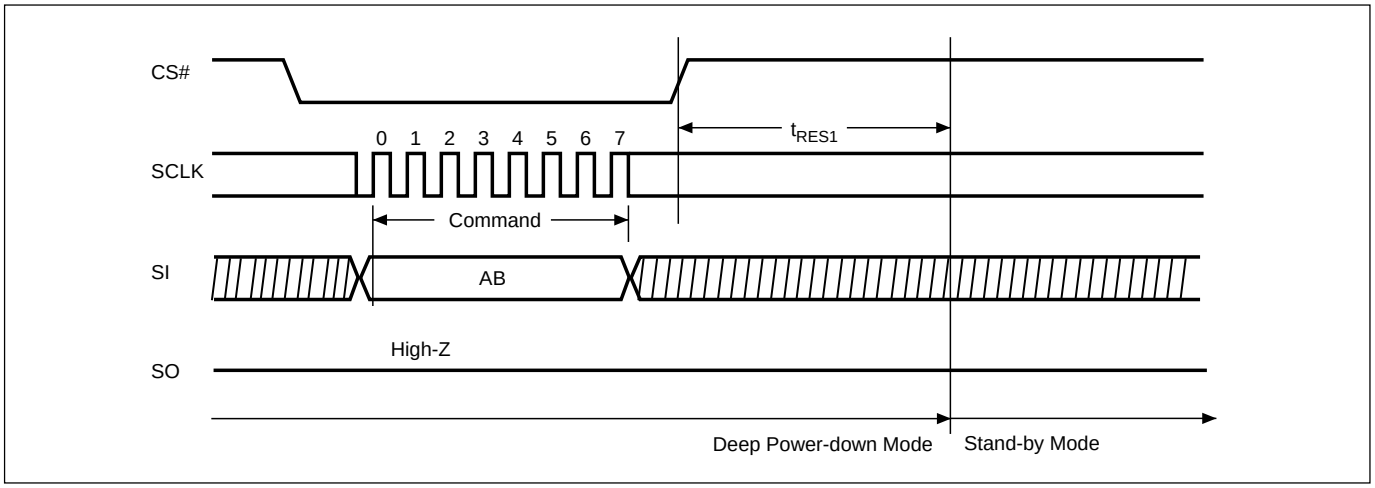
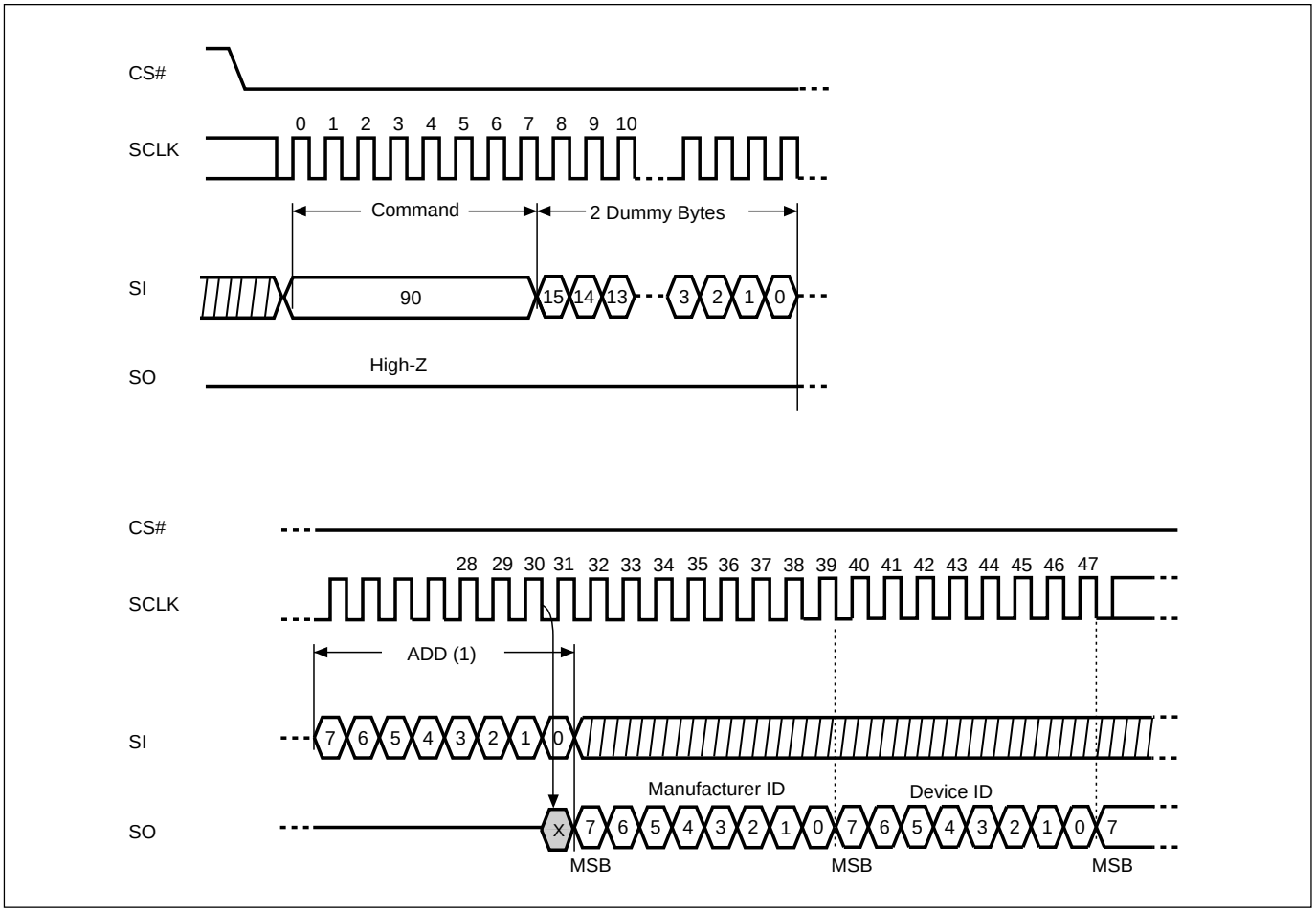


Figure 28. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90 or EF)

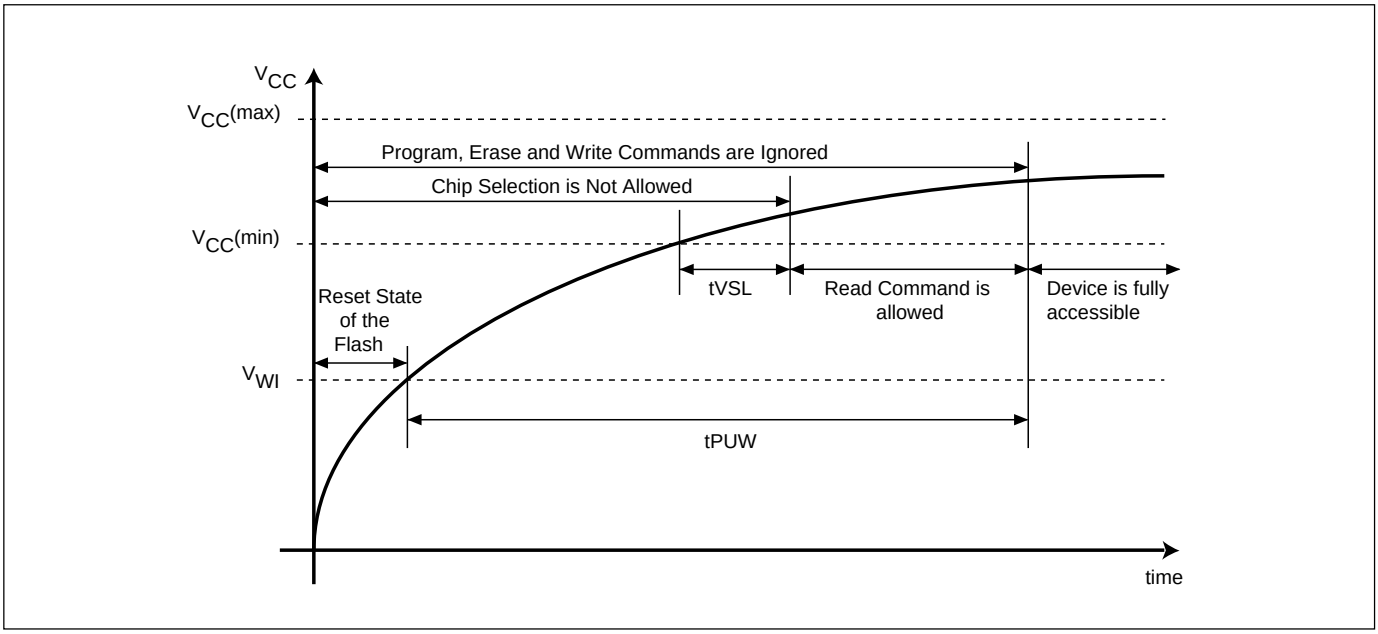


Notes:

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first

(2) Instruction is either 90(hex) or EF(hex).

Figure 29. Power-up Timing



Note: VCC (max.) is 3.6V and VCC (min.) is 2.7V.

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

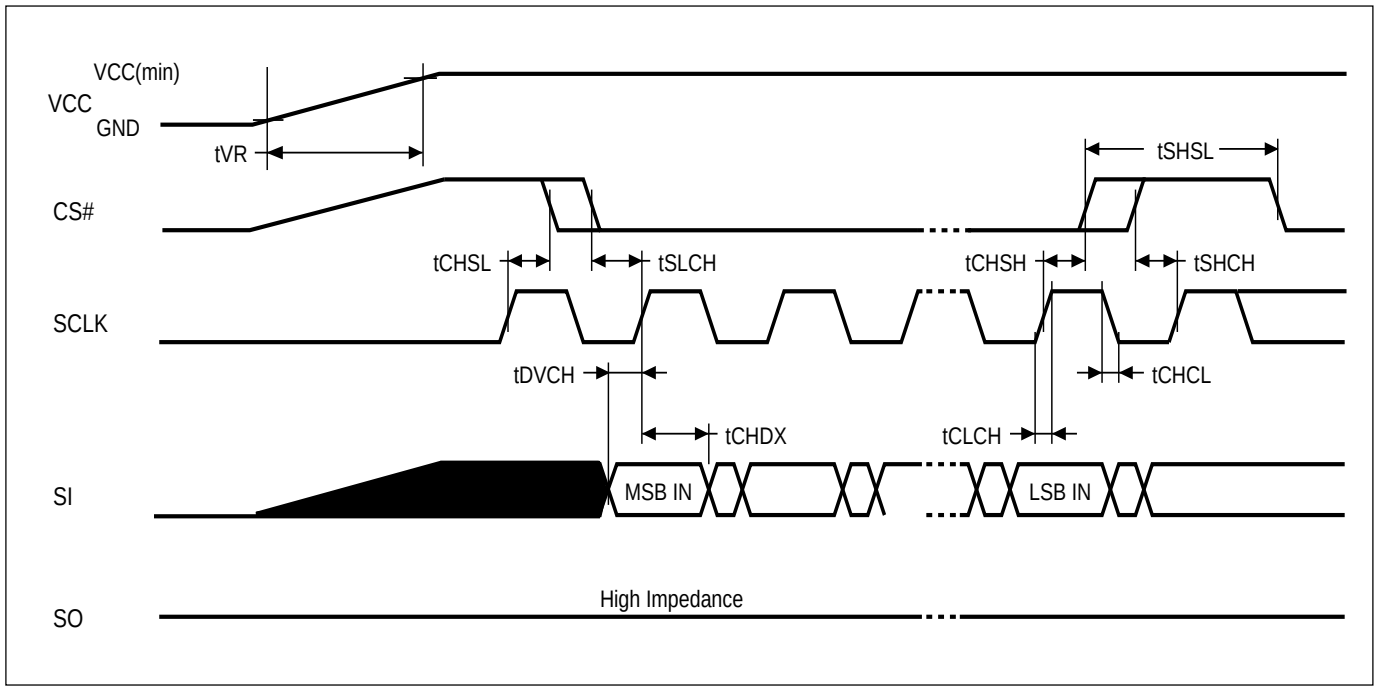


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "AC CHARACTERISTICS" table.

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		Min.	TYP. (1)	Max. (2)	UNIT
Write Status Register Cycle Time			40	100	ms
Sector Erase Time			60	300	ms
Block Erase Time			0.7	2	s
Chip Erase Time	64Mb		50	80	s
	32Mb		25	50	s
	16Mb		14	30	s
Chip Erase Time (at ACC mode)	64Mb		30	48	s
	32Mb		15	30	s
	16Mb		8	18	s
Byte Program Time (via page program command)			9	300	us
Page Program Time			1.4	5	ms
Page Program Time (at ACC mode)			1.4	5	ms
Erase/Program Cycle			100,000		cycles

Note:
1. Typical program and erase time assumes the following conditions: 25° C, 3.3V, and checker board pattern.
2. Under worst conditions of 85° C and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. Erase/Program cycles comply with JEDEC JESD-47E & A117A standard.

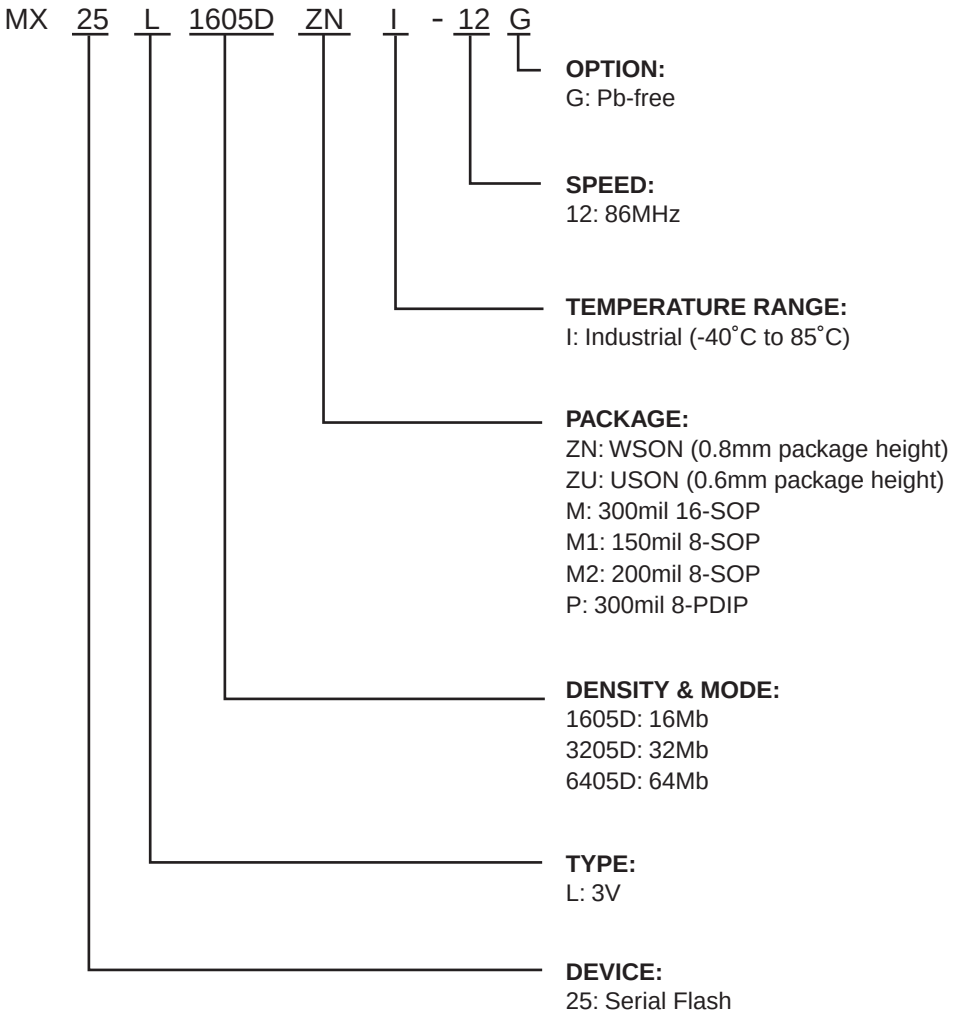
LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on ACC	-1.0V	10.5V
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

ORDERING INFORMATION

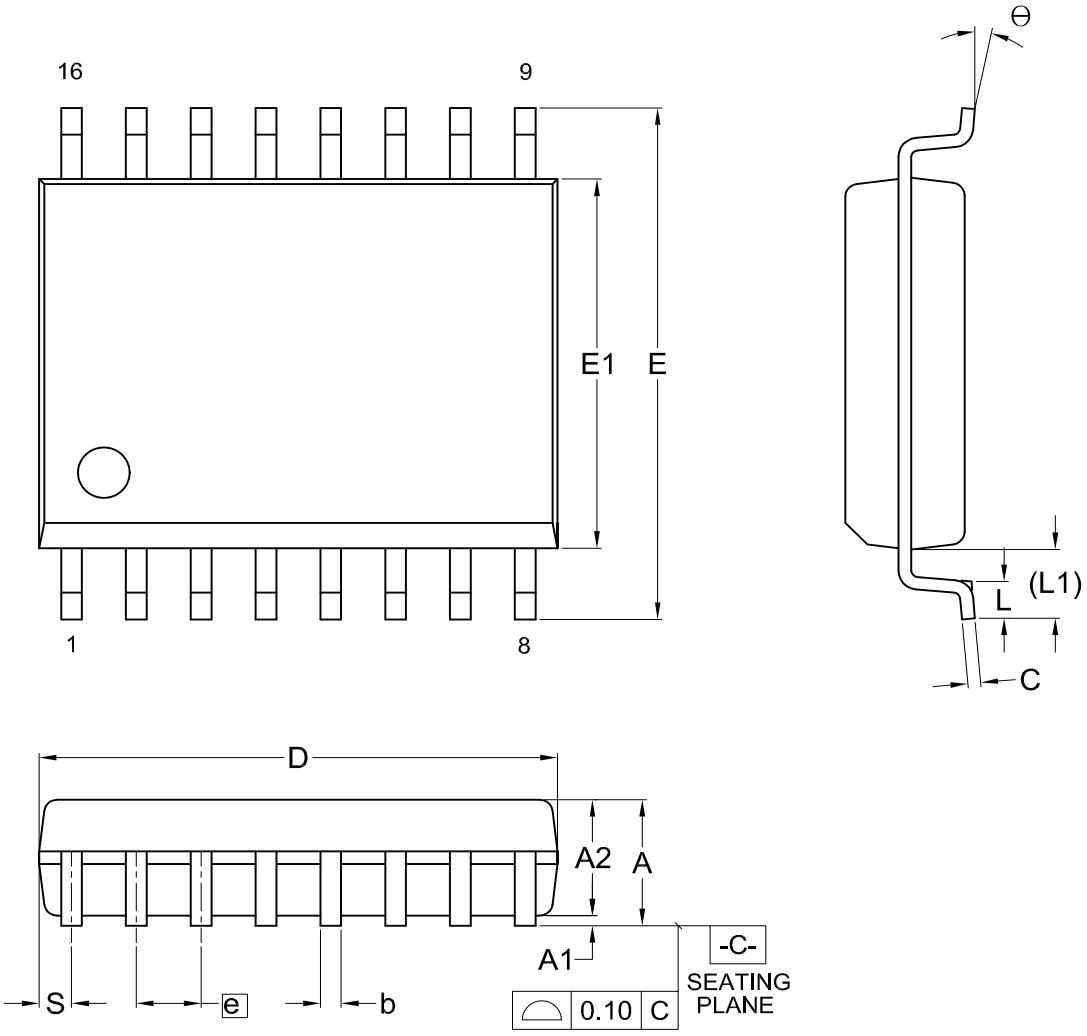
PART NO.	CLOCK (MHz)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (uA)	Temperature	PACKAGE	Remark
MX25L1605DM2I-12G	86	25	20	-40° C~85° C	8-SOP (200mil)	Pb-free
MX25L1605DMI-12G	86	25	20	-40° C~85° C	16-SOP	Pb-free
MX25L1605DM1I-12G	86	25	20	-40° C~85° C	8-SOP (150mil)	Pb-free
MX25L1605DPI-12G	86	25	20	-40° C~85° C	8-PDIP (300mil)	Pb-free
MX25L1605DZNI-12G	86	25	20	-40° C~85° C	8-WSON (6x5mm)	Pb-free
MX25L1605DZUI-12G	86	25	20	-40° C~85° C	8-USON (4x4mm)	Pb-free
MX25L3205DZNI-12G	86	25	20	-40° C~85° C	8-WSON (6x5mm)	Pb-free
MX25L3205DM2I-12G	86	25	20	-40° C~85° C	8-SOP (200mil)	Pb-free
MX25L3205DMI-12G	86	25	20	-40° C~85° C	16-SOP	Pb-free
MX25L3205DPI-12G	86	25	20	-40° C~85° C	8-PDIP (300mil)	Pb-free
MX25L3205DZUI-12G	86	25	20	-40° C~85° C	8-USON (4x4mm)	Pb-free
MX25L6405DZNI-12G	86	25	20	-40° C~85° C	8-WSON (8x6mm)	Pb-free
MX25L6405DMI-12G	86	25	20	-40° C~85° C	16-SOP	Pb-free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for SOP 16L (300MIL)

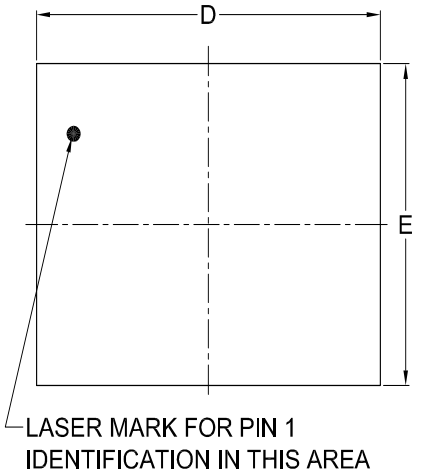


Dimensions (inch dimensions are derived from the original mm dimensions)

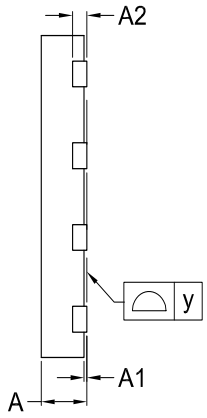
SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	Min.	---	0.10	2.25	0.36	0.20	10.10	10.10	7.42	---	0.40	1.31	0.51	0
	Nom.	---	0.20	2.31	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5
	Max.	2.65	0.30	2.40	0.51	0.30	10.50	10.50	7.60	---	1.27	1.57	0.77	8
Inch	Min.	---	0.004	0.089	0.014	0.008	0.397	0.397	0.292	---	0.016	0.052	0.020	0
	Nom.	---	0.008	0.091	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5
	Max.	0.104	0.012	0.094	0.020	0.012	0.413	0.413	0.299	---	0.050	0.062	0.030	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1402	8	MS-013			03-07-'06

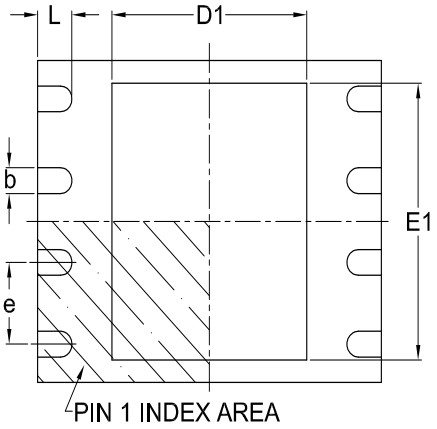
Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)



TOP VIEW



SIDE VIEW



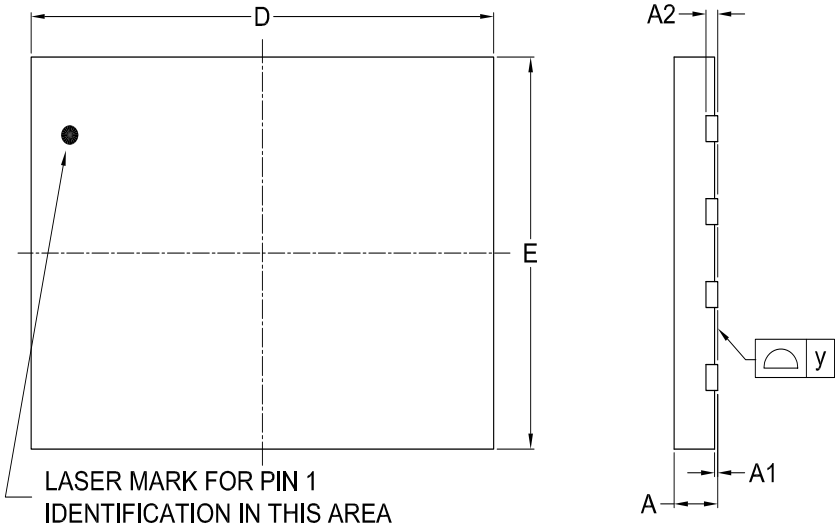
BOTTOM VIEW

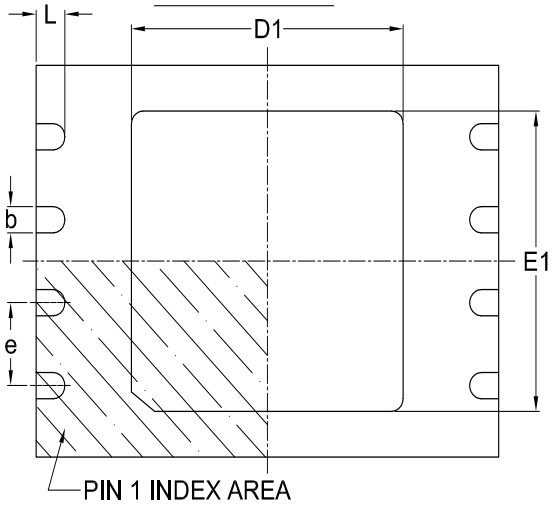
Dimensions (inch dimensions are derived from the original mm dimensions)
*1 : This package has exposed metal pad underneath the package , it can't contact to metal trace or pad on board.
*2 : The exposed pad size must not violate the min. metal separtion requirement, 0.2mm with terminals.

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	5.90	3.30	4.90	3.90	0.50	—	0.00
	Nom.	—	---	0.20	0.40	6.00	3.40	5.00	4.00	0.60	1.27	—
	Max.	0.80	0.05	---	0.48	6.10	3.50	5.10	4.10	0.75	—	0.08
Inch	Min.	0.028	---	---	0.014	0.232	0.129	0.193	0.154	0.020	—	0.00
	Nom.	—	---	0.008	0.016	0.236	0.134	0.197	0.157	0.024	0.05	—
	Max.	0.032	0.002	---	0.019	0.240	0.138	0.201	0.161	0.030	—	0.003

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-3401	4	MO-220			2007/09/20

Doc. Title: Package Outline for WSON 8L (8x6x0.8MM, LEAD PITCH 1.27MM)





Dimensions (inch dimensions are derived from the original mm dimensions)

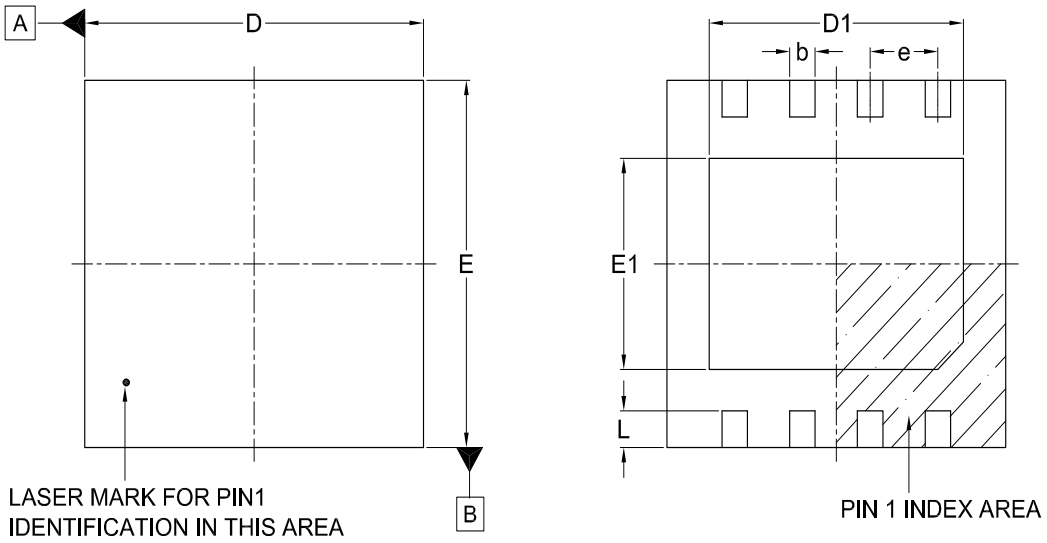
*1 : This package has exposed metal pad underneath the package , it can't contact to metal trace or pad on board.

*2 : The exposed pad size must not violate the min. metal separtion requirement, 0.2mm with terminals.

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	—	0.35	7.90	4.65	5.90	4.55	0.40	—	0.00
	Nom.	—	---	0.20	0.40	8.00	4.70	6.00	4.60	0.50	1.27	—
	Max.	0.80	0.05	—	0.48	8.10	4.75	6.10	4.65	0.60	—	0.08
Inch	Min.	0.028	---	—	0.014	0.311	0.183	0.232	0.179	0.016	—	0.00
	Nom.	—	---	0.008	0.016	0.315	0.185	0.236	0.181	0.020	0.05	—
	Max.	0.032	0.002	—	0.019	0.319	0.187	0.240	0.183	0.024	—	0.003

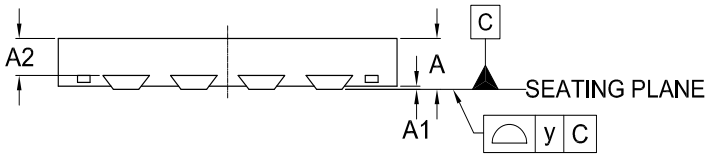
Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-3402	5	MO-220			

Title: Package Outline for USON 8L (4x4x0.6MM, LEAD PITCH 0.8MM)



TOP VIEW

BOTTOM VIEW



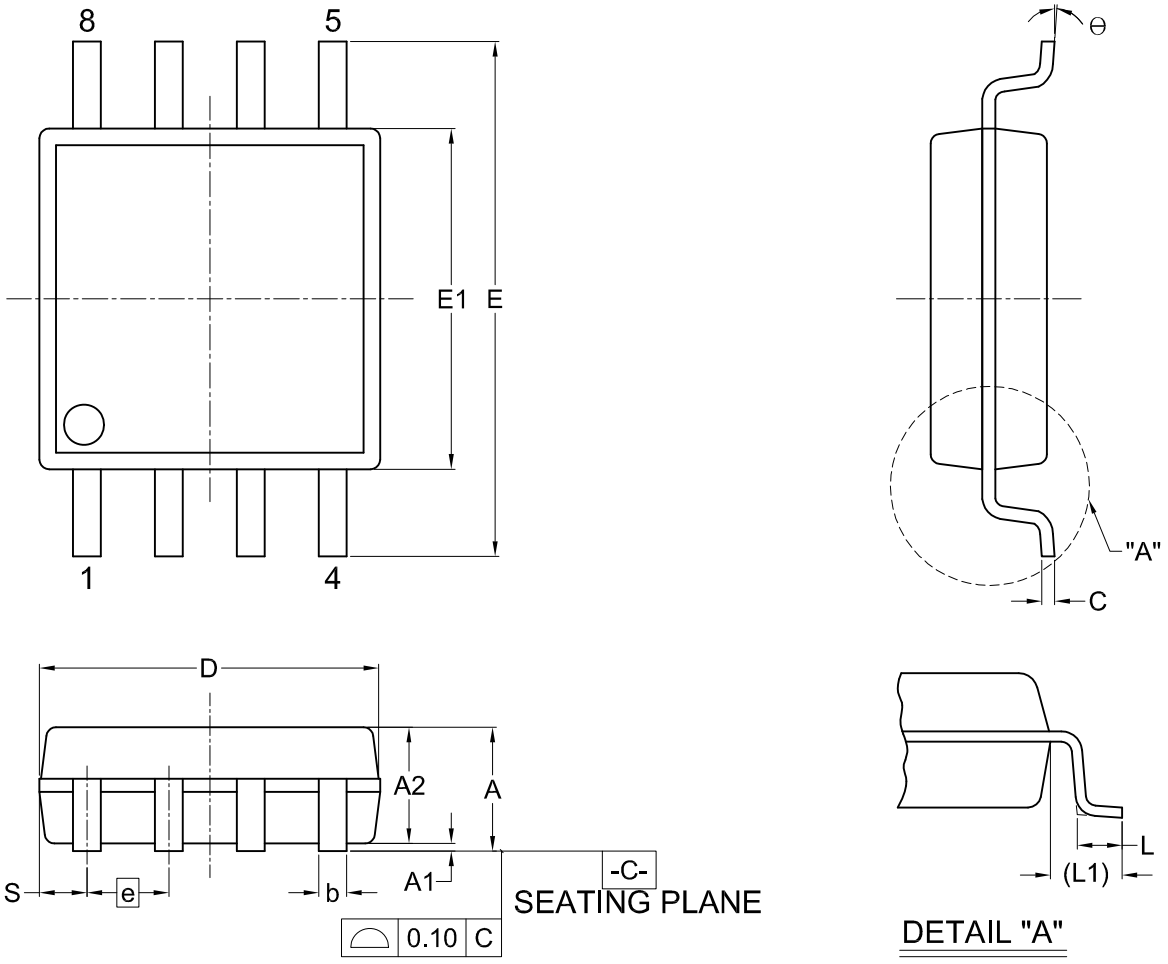
SIDE VIEW

Dimensions (inch dimensions are derived from the original mm dimensions)
*1 : This package has exposed metal pad underneath the package , it can't contact to metal trace or pad on board.
*2 : The exposed pad size must not violate the min. metal separtion requirement, 0.2mm with terminals.

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.50	---	—	0.25	3.90	2.90	3.90	2.20	0.35	—	0.00
	Nom.	0.55	0.04	0.40	0.30	4.00	3.00	4.00	2.30	0.40	0.80	—
	Max.	0.60	0.05	0.43	0.35	4.10	3.10	4.10	2.40	0.45	—	0.08
Inch	Min.	0.020	---	—	0.010	0.154	0.114	0.154	0.087	0.014	—	0.00
	Nom.	0.022	0.002	0.016	0.011	0.157	0.118	0.157	0.091	0.016	0.031	—
	Max.	0.024	0.002	0.017	0.014	0.161	0.122	0.161	0.094	0.018	—	0.003

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-3601	3	MO-252			2008/03/12

Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)

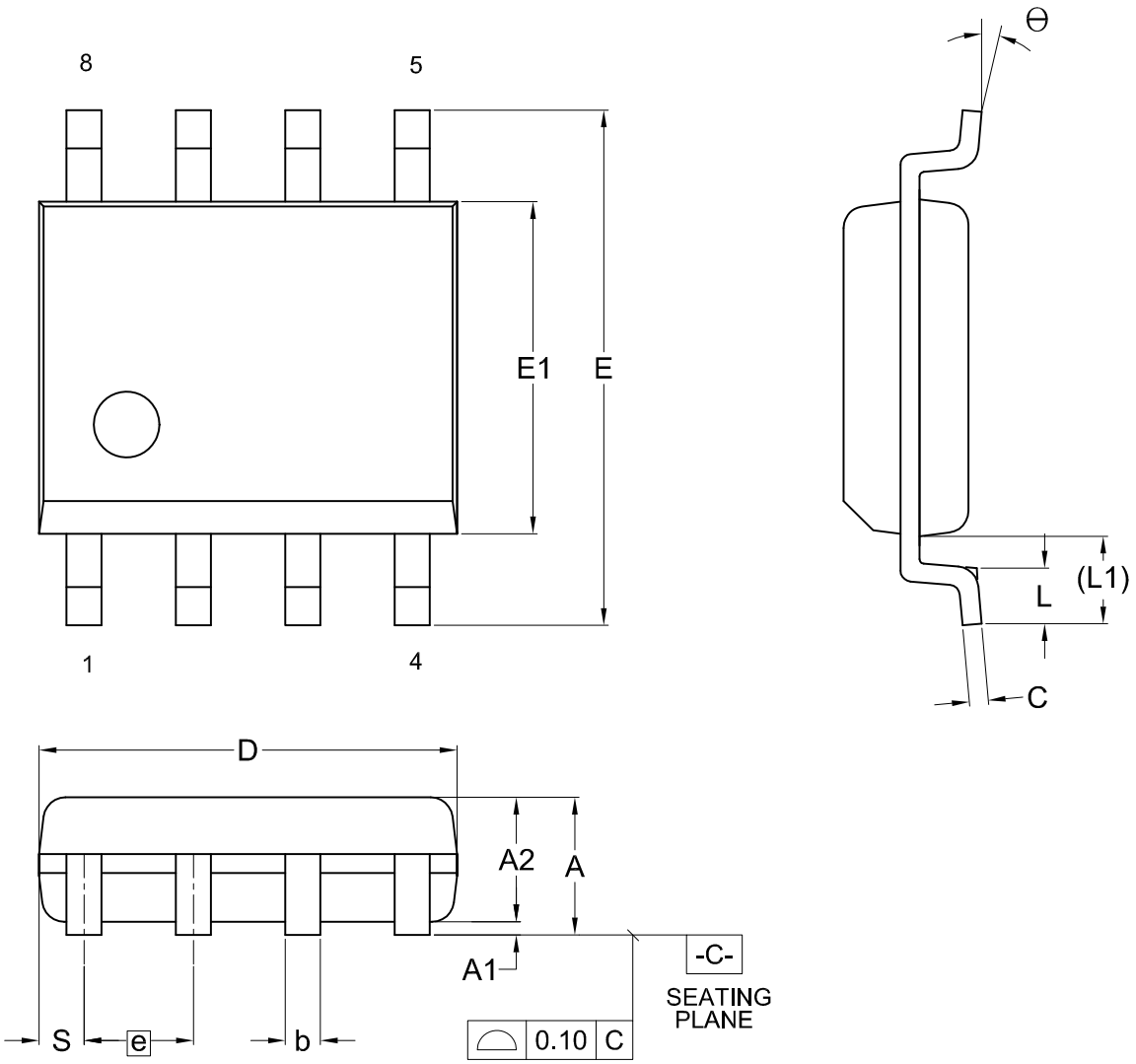


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	—	0.05	1.70	0.36	0.19	5.13	7.70	5.18		0.50	1.21	0.62	0
	Nom.	---	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5
	Max.	2.16	0.25	1.91	0.51	0.25	5.33	8.10	5.38		0.80	1.41	0.88	8
Inch	Min.	---	0.002	0.067	0.014	0.007	0.202	0.303	0.204		0.020	0.048	0.024	0
	Nom.	---	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5
	Max.	0.009	0.010	0.075	0.020	0.010	0.210	0.319	0.212		0.031	0.056	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1406	1				05-06-'05

Title: Package Outline for SOP 8L (150MIL)

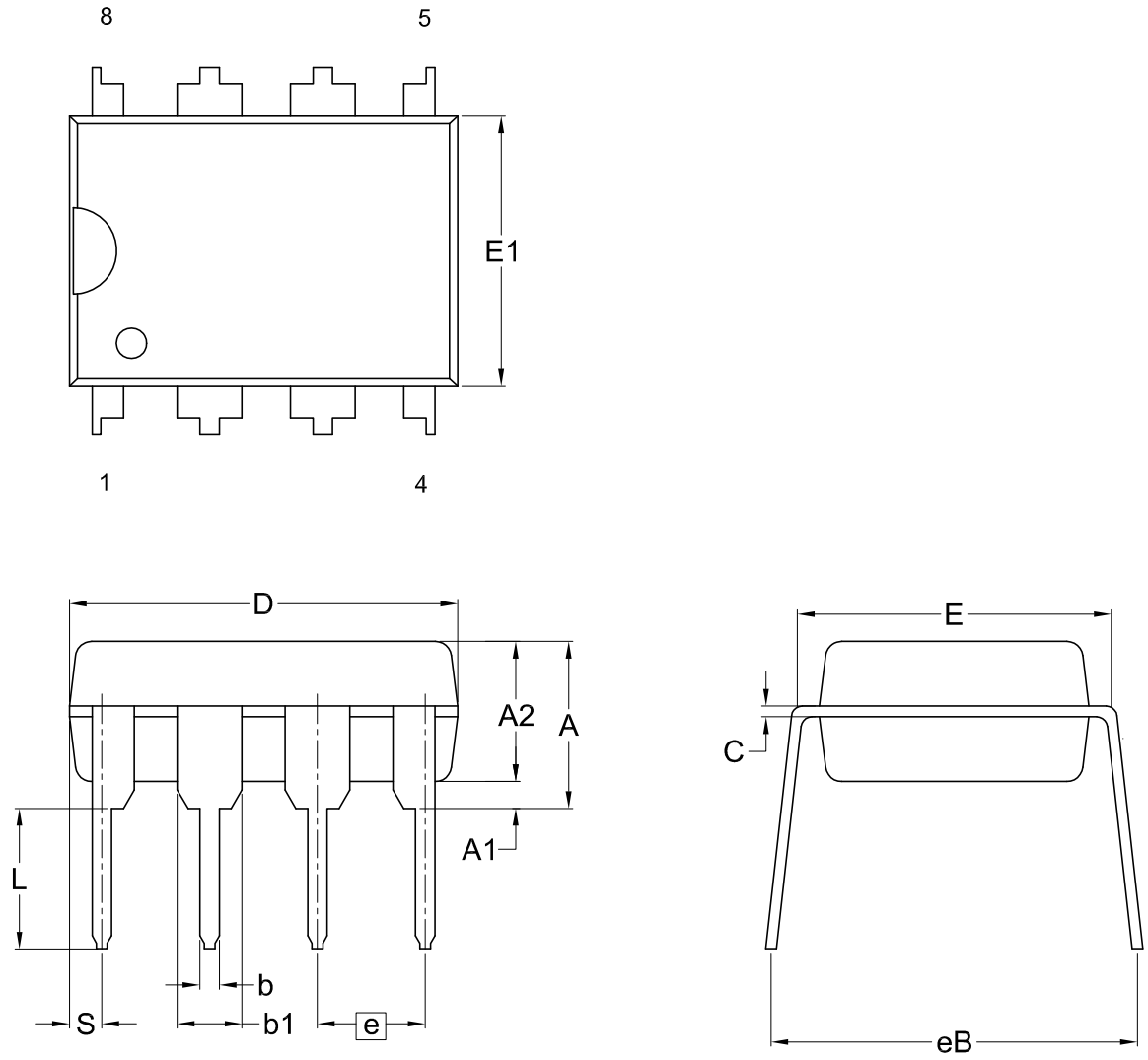


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	Min.	---	0.10	1.35	0.36	0.15	4.77	5.80	3.80		0.46	0.85	0.41	0
	Nom.	---	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5
	Max.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00		0.86	1.25	0.67	8
Inch	Min.	---	0.004	0.053	0.014	0.006	0.188	0.228	0.150		0.018	0.033	0.016	0
	Nom.	---	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.050	0.026	0.041	0.021	5
	Max.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158		0.034	0.049	0.026	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1401	6	MS-012			11-26-'03

Title: Package Outline for PDIP 8L (300MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	---	0.38	3.18	0.36	1.14	0.20	9.02	7.62	6.22	—	7.87	2.92	0.76
	Nom.	---	---	3.30	0.46	1.52	0.25	9.27	7.87	6.35	2.54	8.89	3.30	1.14
	Max.	5.33	---	3.43	0.56	1.78	0.36	10.16	8.13	6.48	—	9.53	3.81	1.52
Inch	Min.	---	0.015	0.125	0.014	0.045	0.008	0.355	0.300	0.245	—	0.310	0.115	0.030
	Nom.	---	---	0.130	0.018	0.060	0.010	0.365	0.310	0.250	0.100	0.350	0.130	0.045
	Max.	0.210	---	0.135	0.022	0.070	0.014	0.400	0.320	0.255	—	0.375	0.150	0.060

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0201	6	MS-001			09-01-'06

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Preliminary"	P1	MAR/07/2008
1.1	1. Dual I/O Pre-released	P1,3,21,31	MAY/12/2008
1.2	1. Added 8-land USON package information	P2,4,46,47,50	JUL/08/2008
1.3	1. Modified figure 4 & 5 waveform	P28	AUG/15/2008
	2. Revised VHH spec from 11.0V(typ.)~11.5V(max.) to 9.5V(min.)~10.5V(max.)	P4,8,30,45	
1.4	1. Revised sector erase time spec from 90ms(typ.) to 60ms(typ.)	P32,45	OCT/01/2008
	2. Removed "Advanced Information" for MX25L3205DZUI-12G	P46	

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