The RF MOSFET Line

RF Power Field Effect Transistor

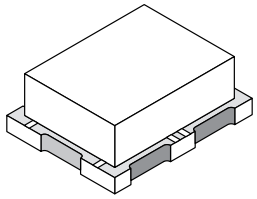
N–Channel Enhancement–Mode

MRF5003

3.0 W, 7.5 V, 512 MHz
N–CHANNEL
BROADBAND
RF POWER FET

The MRF5003 is designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 7.5 Volt and 12.5 Volt mobile, portable, and base station FM equipment.

- Guaranteed Performance at 512 MHz, 7.5 Volts
  Output Power = 3.0 Watts
  Power Gain = 9.5 dB
  Efficiency = 45%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 512 MHz, 2.0 dB Overdrive
- Suitable for 12.5 Volt Applications
- True Surface Mount Package
- Available in Tape and Reel by Adding R1 Suffix to Part Number.
  R1 Suffix = 500 Units per 16 mm, 7 inch Reel.
- Circuit board photomaster available upon request by contacting
  RF Tactical Marketing in Phoenix, AZ.



CASE 430–01, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	36	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 Meg Ohm)	V_{DGR}	36	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	1.7	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.07	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

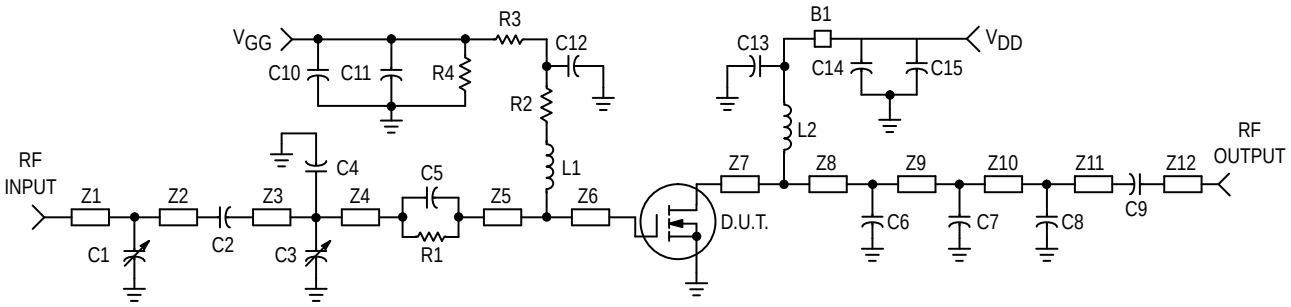
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	14	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 2.5 mAdc)		$V_{(BR)DSS}$	36	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)		I_{DSS}	—	—	1.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 5.0 mAdc)		$V_{GS(th)}$	1.25	2.25	3.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$V_{DS(on)}$	—	—	0.375	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 0.5 Adc)		g_{fs}	0.6	—	—	mho
DYNAMIC CHARACTERISTICS						
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	16.5	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	—	37	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	3.5	4.4	5.4	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)						
Common–Source Amplifier Power Gain (V_{DD} = 7.5 Vdc, P_{out} = 3.0 W, I_{DQ} = 50 mA)	f = 512 MHz f = 175 MHz	G_{ps}	 9.5 —	 10.5 15	 — —	dB
Drain Efficiency (V_{DD} = 7.5 Vdc, P_{out} = 3.0 W, I_{DQ} = 50 mA)	f = 512 MHz f = 175 MHz	h	 45 —	 50 55	 — —	%



C1, C3, C7, C8	0 to 20 pF Johanson
C2, C9	56 pF, 100 mil Chip
C4	10 pF, 100 mil Chip
C5	47 pF, Miniature Clamped Mica Capacitor
C6	22 pF, 100 mil Chip
C10, C15	10 µF, 50 V, Electrolytic
C11, C14	0.1 µF, Capacitor
C12	1000 pF, 100 mil Chip
C13	160 pF, 100 mil Chip
R1	35 Ω, 1/4 W Carbon
R2	30 Ω, 0.1 W Chip
R3	1.0 kΩ, 0.1 W Chip
R4	1.0 MΩ, 1/4 W Carbon
B1	Fair Rite Products Short Ferrite Bead (2743021446)
Board — Glass Teflon®, 31 mils	
Note: Plated ceramic part locators (0.1″ x 0.15″) soldered onto Z6 and Z7.	

Z1	0.350″ x 0.08″ Microstrip
Z2	0.190″ x 0.08″ Microstrip
Z3	0.800″ x 0.08″ Microstrip
Z4	0.380″ x 0.08″ Microstrip
Z5	0.150″ x 0.08″ Microstrip
Z6	0.285″ x 0.08″ Microstrip
Z7	0.340″ x 0.08″ Microstrip
Z8	0.070″ x 0.08″ Microstrip
Z9	0.280″ x 0.08″ Microstrip
Z10	0.840″ x 0.08″ Microstrip
Z11	0.180″ x 0.08″ Microstrip
Z12	0.600″ x 0.08″ Microstrip
L1	7 Turns, 0.076″ ID, #24 AWG Enamel
L2	5 Turns, 0.126″ ID, #20 AWG Enamel
Input/Output Connectors — Type N	

Figure 1. 512 MHz Narrowband Test Circuit

TYPICAL CHARACTERISTICS

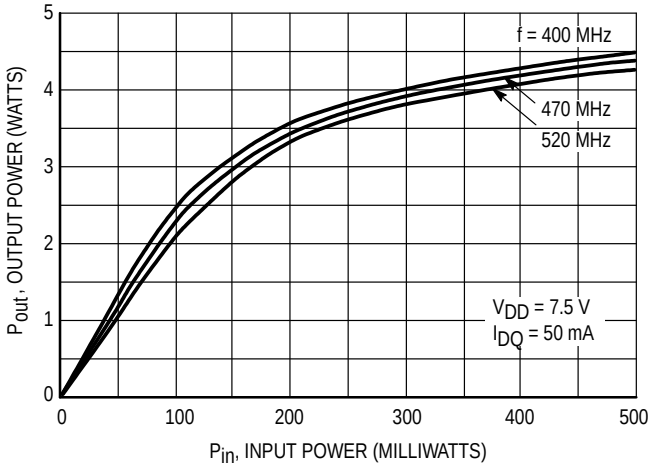


Figure 2. Output Power versus Input Power

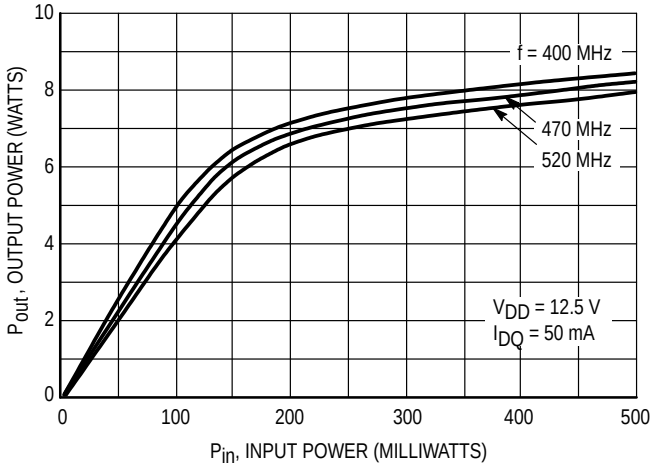


Figure 3. Output Power versus Input Power

TYPICAL CHARACTERISTICS

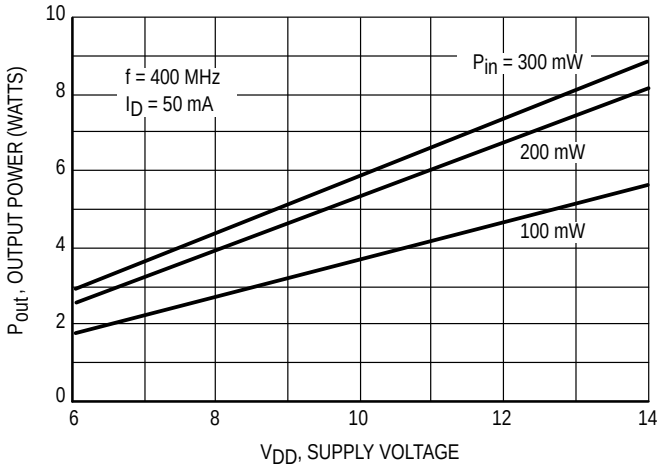


Figure 4. Output Power versus Supply Voltage

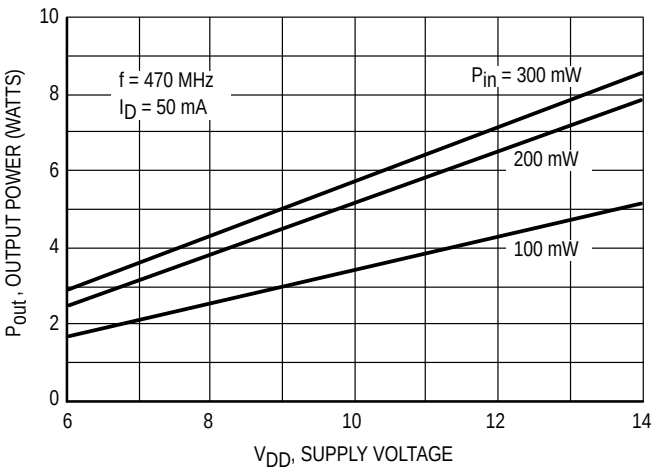


Figure 5. Output Power versus Supply Voltage

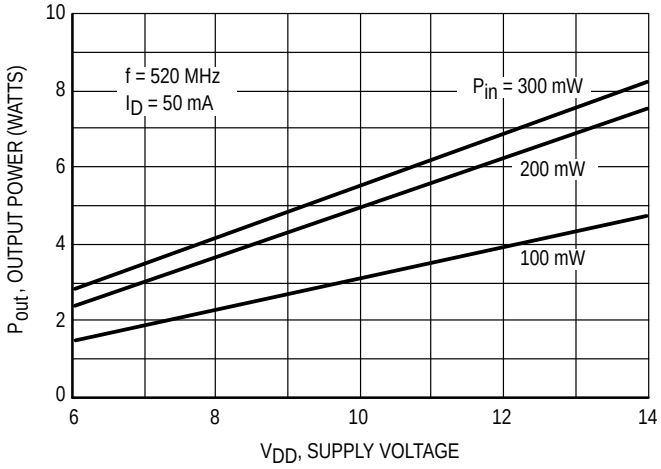


Figure 6. Output Power versus Supply Voltage

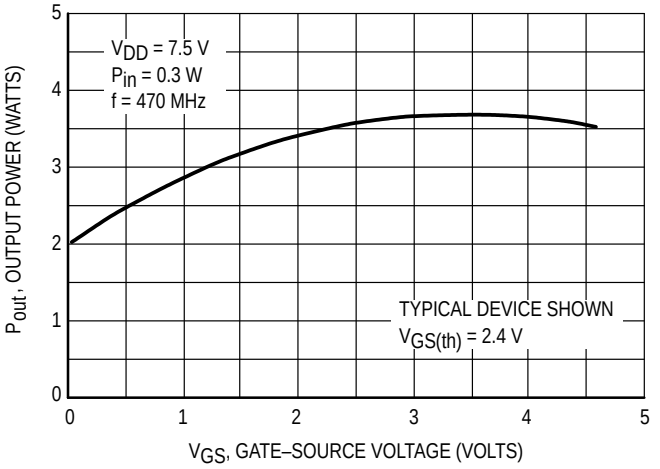


Figure 7. Output Power versus Gate Voltage

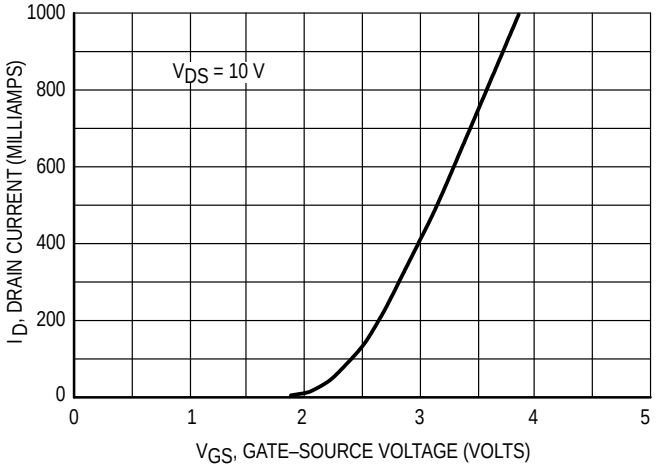


Figure 8. Drain Current versus Gate Voltage (Typical Device Shown)

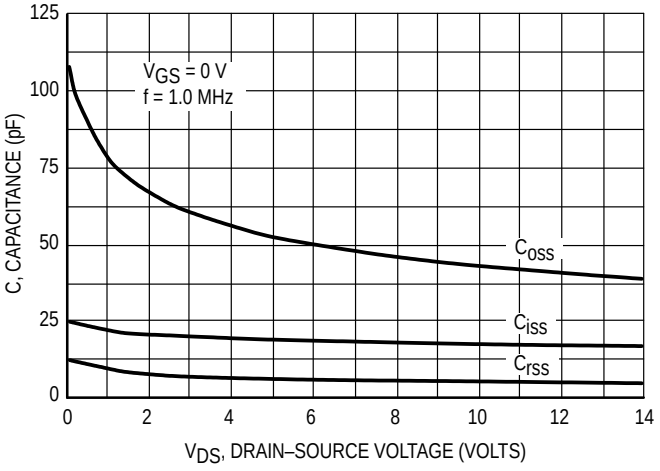


Figure 9. Capacitance versus Voltage

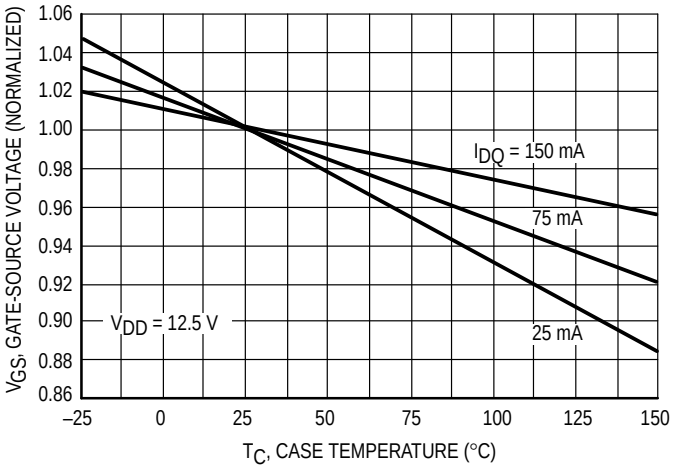


Figure 10. Gate–Source Voltage versus Case Temperature

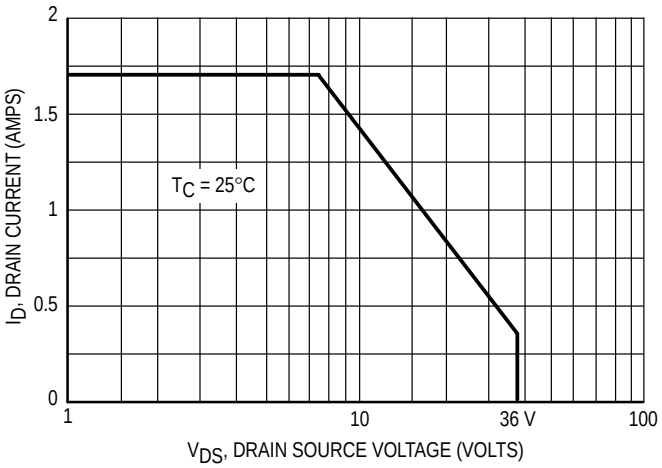
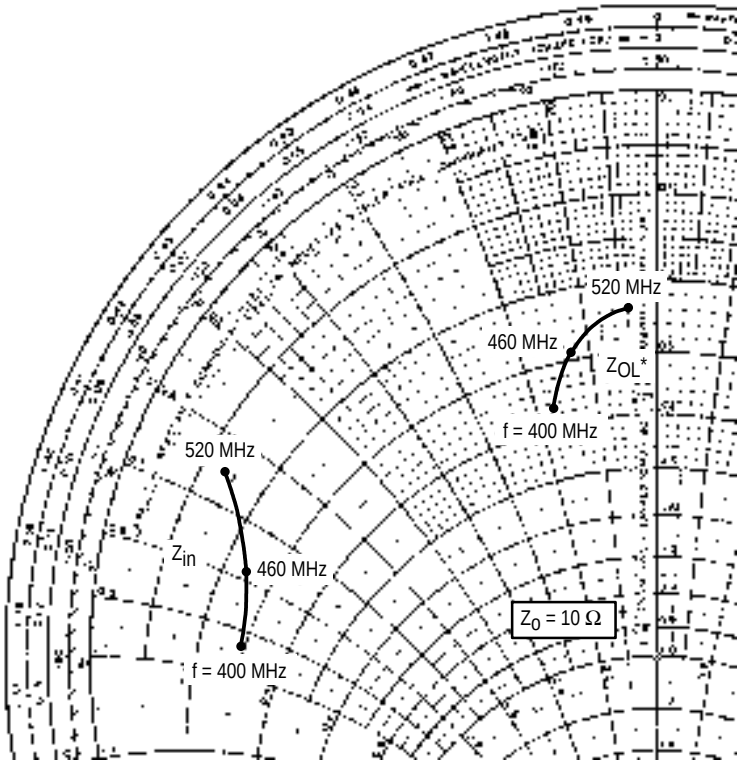


Figure 11. Maximum Rated Forward Biased Safe Operating Area



V_{DD} = 7.5 V, I_{DQ} = 50 mA, P_{out} = 3.0 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	2.8 – j9.2	3.6 – j1.7
430	2.7 – j8.5	3.3 – j1.5
460	2.5 – j7.8	2.7 – j1.1
490	2.0 – j7.2	2.5 – j0.8
520	1.3 – j6.5	2.4 – j0.5

Z_{in} = Conjugate of source impedance with parallel 35 Ω resistor and 47 pF capacitor in series with gate.

Z_{OL}* = Conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50%.

Note: Z_{ol}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

Figure 12. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DS} = 10 V)

I_D = 50 mA

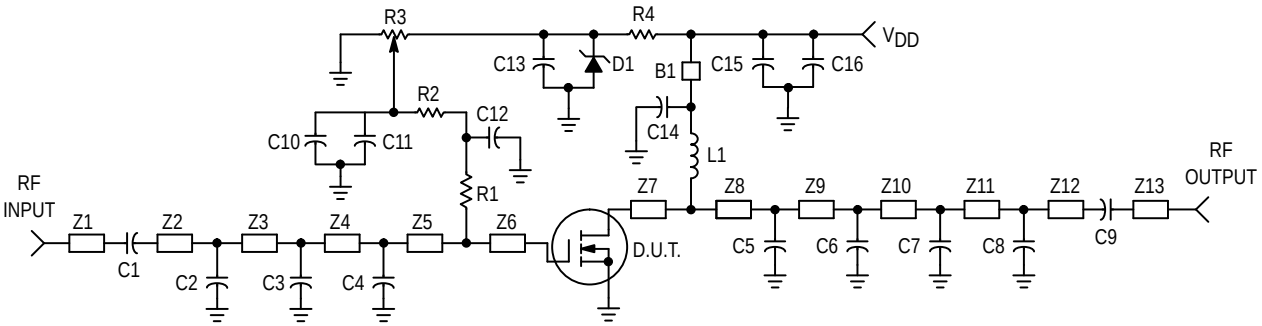
f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
50	0.69	−90	10.8	117	0.07	29	0.74	−119
100	0.58	−120	6.0	96	0.08	10	0.78	−146
200	0.58	−139	3.0	75	0.08	−7	0.81	−161
300	0.64	−147	1.9	61	0.07	−16	0.84	−166
400	0.70	−152	1.3	50	0.06	−21	0.86	−169
500	0.75	−157	0.99	41	0.05	−24	0.88	−172
700	0.82	−165	0.61	28	0.03	−15	0.92	−176
850	0.86	−171	0.45	21	0.02	13	0.94	−179
1000	0.89	−176	0.34	16	0.02	47	0.95	178

I_D = 500 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
50	0.76	−124	15.0	109	0.04	23	0.76	−151
100	0.72	−150	7.9	94	0.04	12	0.81	−165
200	0.72	−163	4.0	80	0.04	6	0.83	−172
300	0.73	−168	2.6	71	0.04	5	0.84	−175
400	0.75	−171	1.9	62	0.04	7	0.85	−176
500	0.77	−173	1.5	55	0.03	12	0.86	−178
700	0.81	−177	0.97	42	0.03	29	0.89	−180
850	0.84	−180	0.75	35	0.03	44	0.90	178
1000	0.86	177	0.60	29	0.04	55	0.92	176

I_D = 1.0 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
50	0.80	−125	14.6	110	0.04	23	0.75	−155
100	0.76	−150	7.8	95	0.04	10	0.81	−167
200	0.76	−164	3.9	81	0.04	1	0.83	−173
300	0.77	−169	2.6	71	0.04	−3	0.84	−175
400	0.79	−172	1.9	63	0.03	−5	0.85	−176
500	0.80	−174	1.4	56	0.03	−5	0.86	−177
700	0.83	−178	0.95	43	0.03	−1	0.88	−179
850	0.85	179	0.73	35	0.02	9	0.90	179
1000	0.87	177	0.58	28	0.02	22	0.91	178



C1, C9	100 pF 100 mil Chip
C2	16 pF, 100 mil Chip
C3	24 pF, 100 mil Chip
C4	68 pF, 100 mil Chip
C5	51 pF, 100 mil Chip
C6	39 pF, 100 mil Chip
C7	6.2 pF, 100 mil Chip
C8	9.1 pF, 100 mil Chip
C10, C15	39000 pF, 100 mil Chip
C11, C16	10 μF, 50 V Electrolytic
C12	10000 pF, 100 mil Chip
B1	Fair Rite Products Short Ferrite Bead (2743021446)
C13	0.1 μF, 100 mil Chip
C14	160 pF, 100 mil Chip
R1	43 Ω, 0.1 W Chip Resistor
R2	1000 Ω, 0.1 W Chip Resistor
R3	10 kΩ Potentiometer
R4	3000 Ω, 0.1 W Chip Resistor
L1	5 Turns, 0.126″ ID, #20 AWG Enamel
Z1 to Z13	See Photomaster
D1	1N4734 Motorola Zener
Board — G10, 1/32″	
Input/Output Connectors — SMA	

Figure 13. Schematic of Broadband Demonstration Amplifier

PERFORMANCE CHARACTERISTICS OF BROADBAND DEMONSTRATION AMPLIFIER

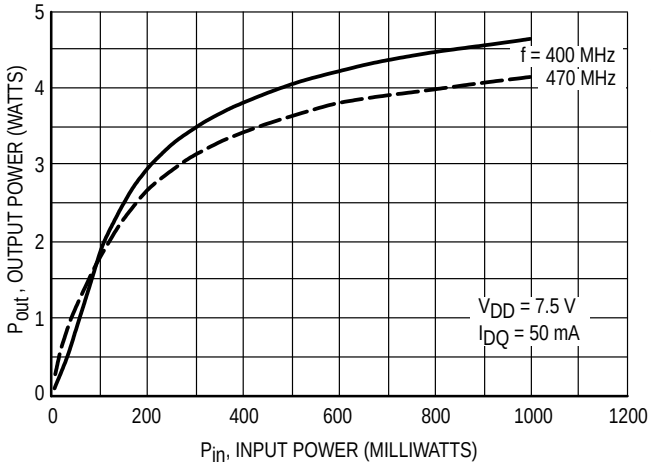


Figure 14. Output Power versus Input Power

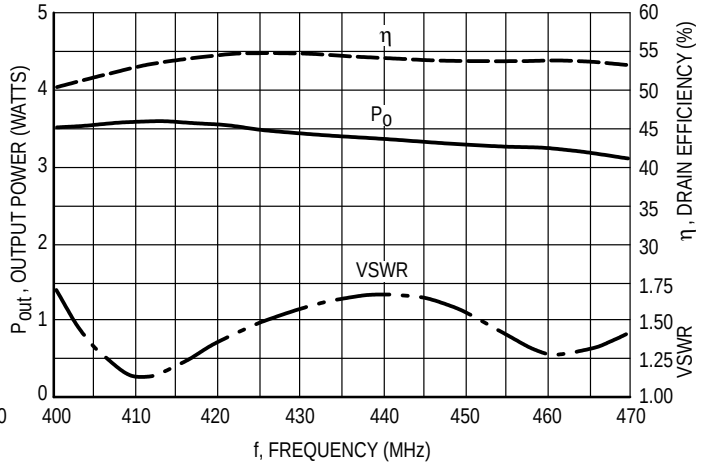


Figure 15. Output Power, Drain Efficiency and VSWR versus Frequency

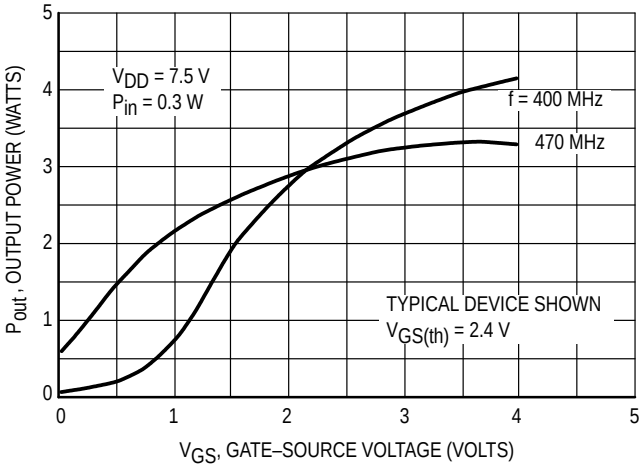


Figure 16. Output Power versus Gate Voltage

DESIGN CONSIDERATIONS

The MRF5003 is a common–source, RF power, N–Channel enhancement mode, Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design. Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts.

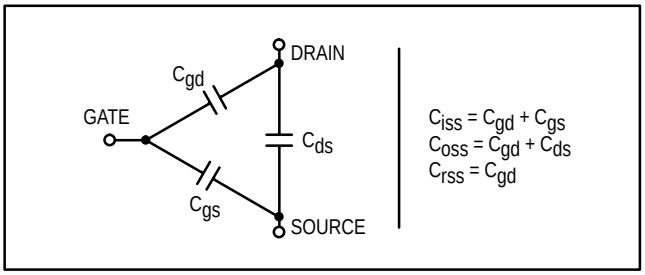
The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling.

Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since the MRF5003 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 8 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. The MRF5003 was characterized at I_{DQ} = 50 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF5003 may be controlled from its rated value down to zero (negative gain) with a low power dc control signal, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 16 is an example of output power variation with gate–source bias voltage. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 14°C/W assumes a majority of the 0.100″ x 0.200″ source contact on the back side of the package is in good contact with an appropriate heat sink. In the test fixture shown in Figure 1, the device is clamped directly to a copper pedestal. In the demonstration amplifier, the device was mounted on top of the G10 circuit board and heat removal was accomplished through several solder filled plated through holes. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package.

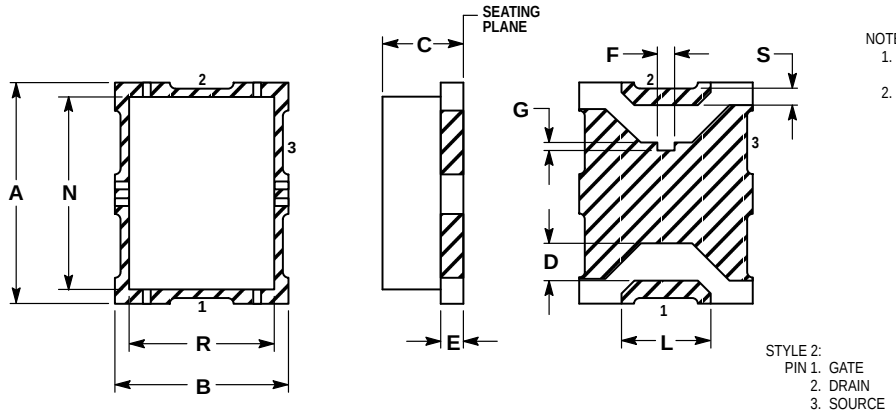
AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5003. For examples see Motorola Application Note AN721, “Impedance Matching Networks Applied to RF Power Transistors”. Both small–signal S–parameters and large–signal impedances are provided. While the S–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of the MRF5003 yield a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Different stabilizing techniques were applied to the test fixture and demonstration amplifiers. The RF test fixture implements a parallel resistor and capacitor in series with the gate while the demonstration amplifier utilizes a 43 Ω shunt resistor from gate to ground. Both circuits have a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two port stability analysis with the MRF5003 S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, “RF Small–Signal Design Using Two–Port Parameters”, for a discussion of two port network theory and stability.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.260	0.270	6.60	6.86
B	0.200	0.210	5.08	5.33
C	0.090	0.104	2.29	2.64
D	0.040	0.050	1.02	1.27
E	0.022	0.028	0.56	0.71
F	0.015	0.025	0.38	0.64
G	0.005	0.015	0.13	0.38
L	0.100	0.110	2.54	2.79
N	0.226	0.236	5.74	5.99
R	0.166	0.176	4.22	4.47
S	0.025	0.035	0.64	0.89

STYLE 2:
PIN 1. GATE
2. DRAIN
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